DIGITAL INDUSTRIES SOFTWARE

Deliver 3D IC innovations faster

Are you ready to deliver more than Moore?

3D IC breaks through process limitations

Heterogeneous semiconductor integration is an inflection point that's not only bringing new architectures into the market but also disrupting the engineering process.

Low latency, high-bandwidth data movement 3D IC enables companies to partition a design and integrate silicon IP at the most appropriate process node and process, providing lower manufacturing costs, higher wafer yields, lower power consumption and overall lower costs.

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To lead the way in 3D IC design, teams must adopt four enabling approaches

1 Transition from design-based to systems-based optimization

From early planning through design sign-off and manufacturing hand-off. This requires consistent system representation throughout the design process and the aggregation, visibility and interoperability of cross-domain content.

Enabling digital transformation can be achieved through a holistic system level design approach

2 Expand the supply chain and tool ecosystem

Changes in the supply chain and ecosystem for heterogeneous systems demand a new level of tool interoperability and openness than previously seen. Sharing and updating design content in a multi-vendor and/or multi-tool environment is a must.

It places a greater demand on assembly-level verification throughout the design process to ensure that individual components work together as expected.

Innovative technology requires innovative methodology

3 Balancing design resources across competing multi-domain requirements

System co-optimization entails balancing requirements and resources across multiple domains. This balancing act requires visibility into downstream effects earlier in the design process to gain an early perspective on power, performance and area (PPA).

An early perspective enables better engineering decisions on resource allocation—resulting in higher performing, more cost-effective products

Much tighter integration with the system, RTL and ASIC design processes

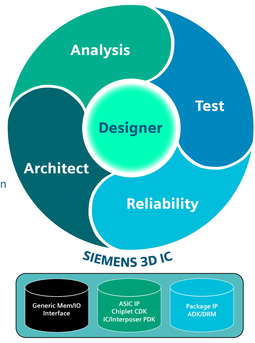
4 Globalization

A full system focus demands greater cohesiveness across engineering teams (silicon, packaging, and PCB) around the world, breaking away from traditional engineering silos.

The benefits achieved through this game-changing heterogeneous integration come with a new set of design and verification challenges.

Built on a leading technology foundation

- RTL driven architectural planning through manufacturing flow
- Leverages broad technology portfolio of Siemens DISW
- Incorporating test, thermal and mechanical stress support
- Enabled as five integrated and optimized workflows
- Designed specifically to address 2.5D/3D IC challenges
- Multi-domain co-design with in-process analysis and optimization
- Modular architecture to support 3rd party point tools
- Ecosystem and 3D IC design service support



Now it's your turn to engineer a smarter future

Accelerate your semiconductor development to become more agile and efficient with Siemens 3D IC workflows and technology portfolios.

- Digital Transformation
- Validation and Verification
- Resource Utilization

The Siemens 3D IC heterogeneous semiconductor packaging workflows catapult you into the future of IC design today.

For more information on 3D IC design solutions, go to **siemens.com/3dic**

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