Computer Systems

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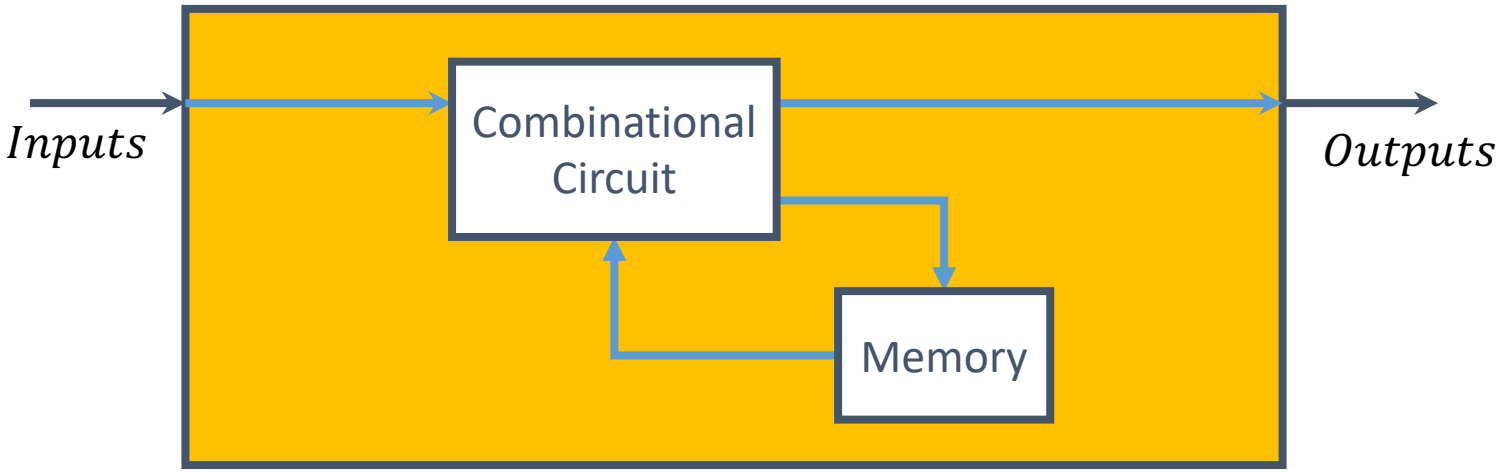
Sequential Logic Circuits

Combinational / Sequential

- **Combinational Circuits:** Outputs only depend on immediate inputs.
- **Sequential Circuits:** Outputs depend not only on immediate inputs, but also previous outputs.



Sequence

- Memory element's transition among states.
- The next state of the memory element is determined by its inputs and the present state.
- A circuit can be seen as a time sequence of inputs, outputs, and internal states.

Sequential Circuits

- Asynchronous – State changes immediately after inputs are changed.

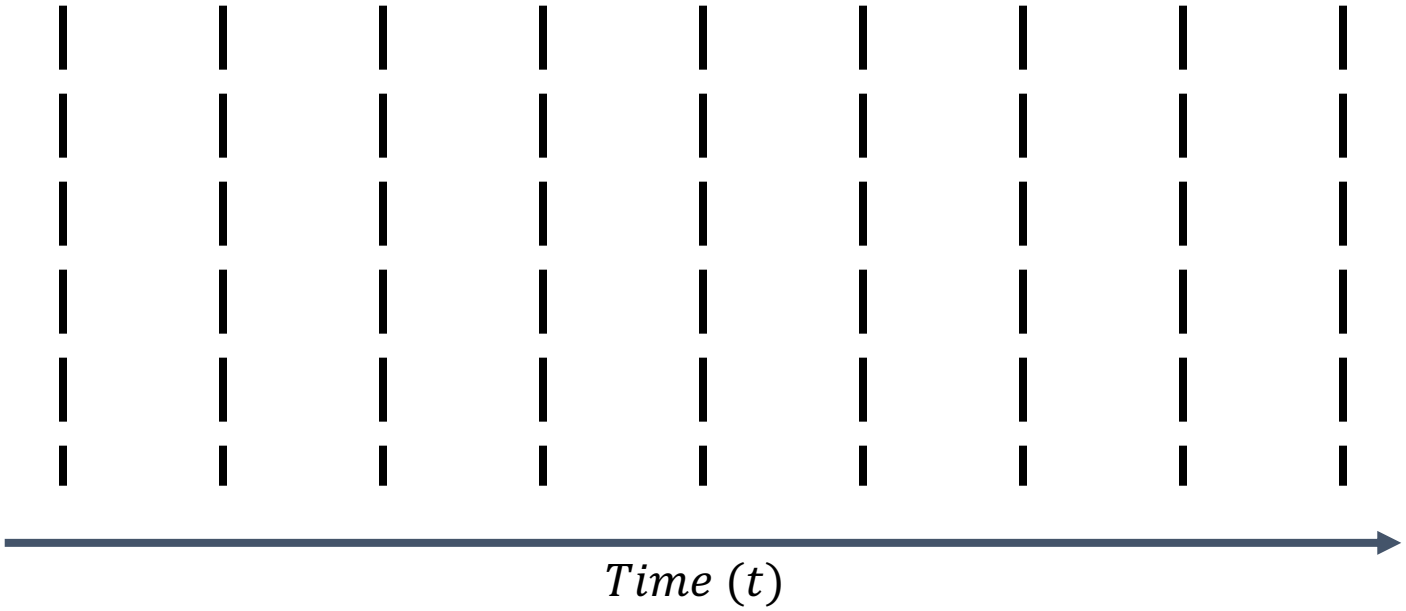
- Synchronous – State changes only within discrete time intervals.

Asynchronus Sequential Circuits

- The state of a circuit changes as soon as the inputs change.
- Faster due to immediate state changes.
  - Only propagation delays affects the speed.
- A combinational circuit with feedback.
- Due to this nature, circuit may become unstable.
- Difficult to design circuits with Asynchronus Sequential circuits.

Synchronus Sequential Circuits

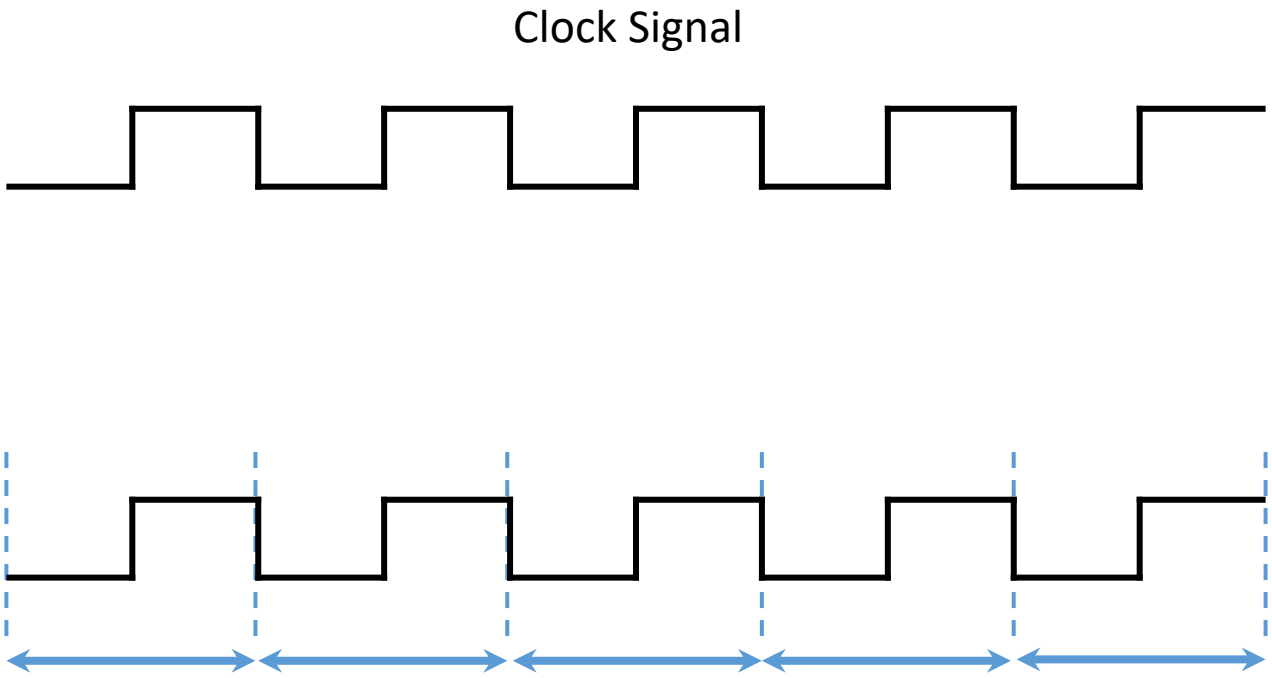
- Synchronization is achieved by making the circuit changes its state at discrete intervals of time.



Clocked Synchronus Seq. Circuits

- Separate controller signal for the synchronization.
- A clock can be used to generate signals (pulses).
- Storage elements' states are changed with clock pulses.
- Clock signal is connected to all the storage elements in the circuit.
- Pulses determine **when** the state changes occur.
- Other inputs determine **what** changes will be made.

Clock Signal

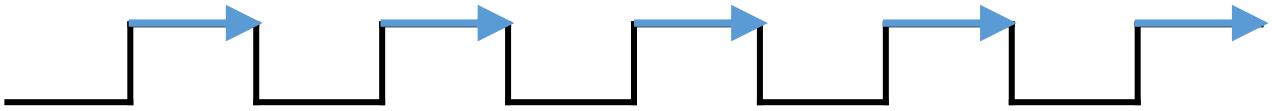


Flip - Flop

- A storage elements used in **C**locked **S**ynchronus **S**equential **C**ircuits (C.S.S.C) are called **Flip-Flops**.
- It can store one bit of information.
- A C.S.S.C may contain many flip-flops.
- Propagation delays and Clock interval are critical.
- State changes are triggered by the clock pulse transition (Edge sensitive).

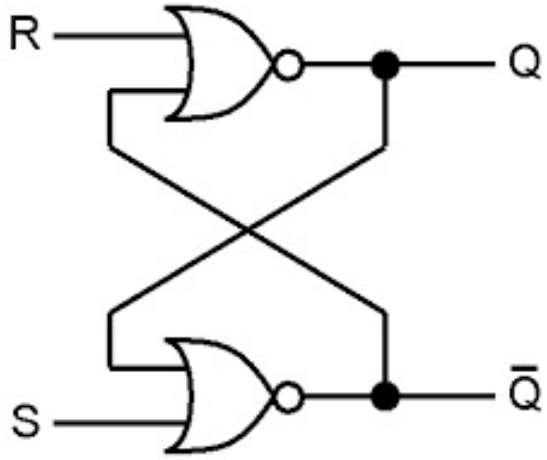
Latch

- A storage element that operates on signal levels rather than signal transition (level sensitive), is called a latch.
- Not operates on clock edges.
- Asynchronus device (Not synchronus).
- Latches are the building blocks for Flip-Flops.



S-R Latch

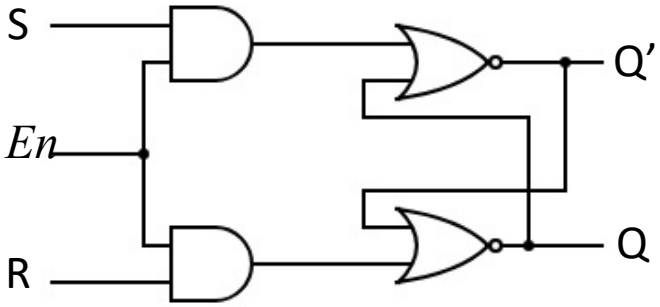
- **S** – Set, **R** – Reset
- Two cross coupled NAND gates can also be used.
- Two outputs; One is the complement of the other.
- When Q=1 -> Set State
- Otherwise Reset State

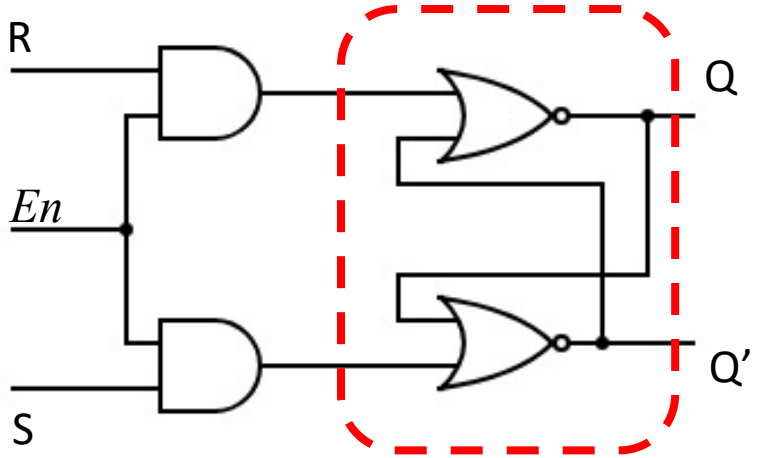


S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Forbidden

S-R Latch with Control Signal

- *En* – Enable
- When *En* = 0 circuit is a SR Latch with S=0 and R=0
- *En* should be triggered to make the S-R Latch operational.

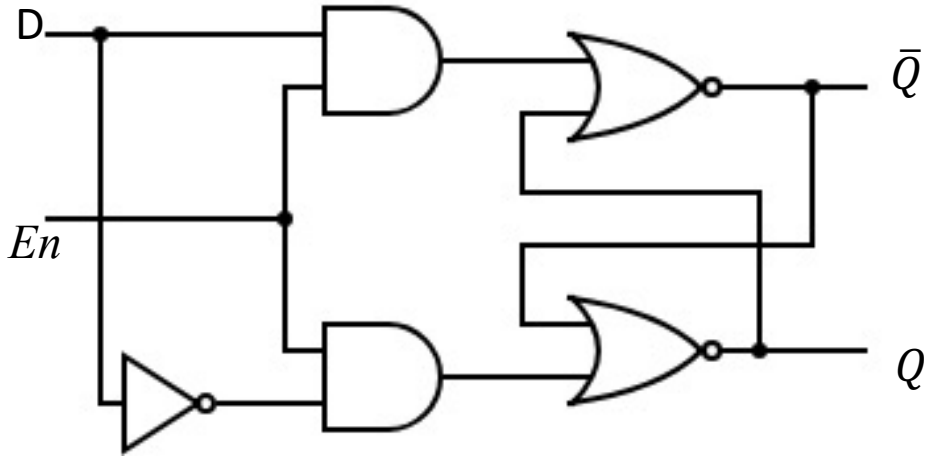




En	S	R	Q(t+1)
0	X	X	Q(t)
1	0	0	Q(t)
1	0	1	0
1	1	0	1
1	1	1	Forbidden

D Latch

- Eliminate undesireable condition of S-R Latch



En	D	Q(t+1)
0	X	Q(t)
1	0	0
1	1	1

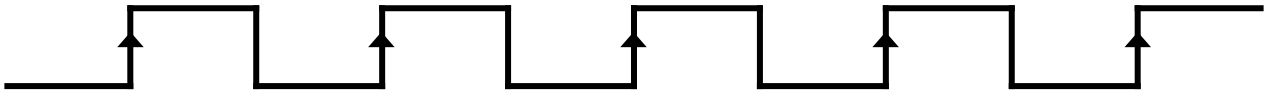
- Value in goes to out (Q) when the circuit is enabled.
- When disabled value Q remains unchanged.

Latches with Clock

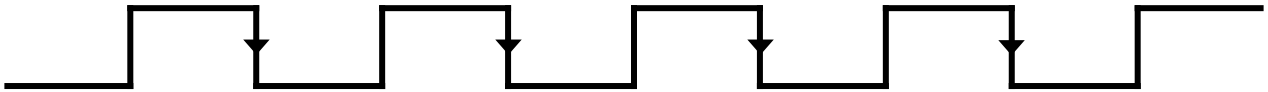
- A clock can be used as a control signal in latches.
- When control signal is active latches make transitions.
- If inputs are changed during clock pulse active period, then within a single clock pulse the latch generates two outputs.
- Latches have the problem of level sensitivity.
- Flip-Flops solves this problem by being edge sensitive.

Edge Sensitive

- Positive Edge (Rising Edge)

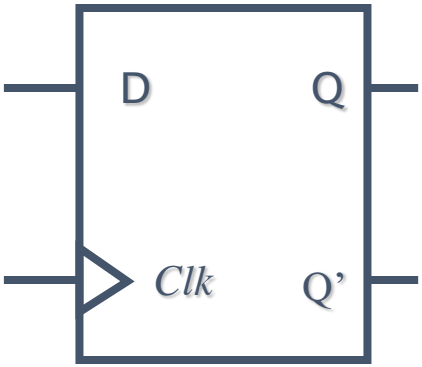


- Negative Edge (Falling Edge)



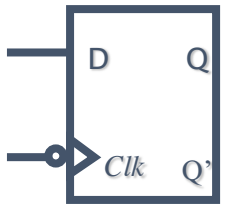
D Flip-Flop

- Edge triggered storage device.
- Store only one bit.



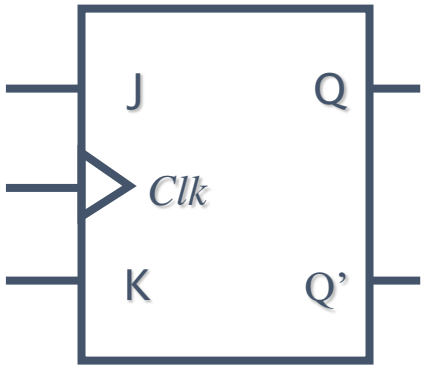
D	Clk	Q(t+1)
0	0	Q(t)
0	1	0
1	0	Q(t)
1	1	1

D	Q(t+1)
0	0
1	1



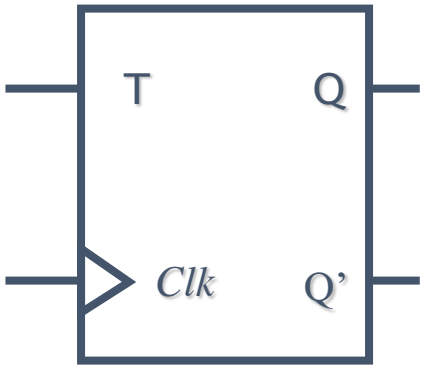
Negative Edge Sensitive
D Flip-Flop

J-K Flip-Flop and T Flip-Flop



J-K Flip-Flop

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)



T Flip-Flop

T	Q(t+1)
0	Q(t)
1	Q'(t)

Next...

Common Applications of Flip-Flops

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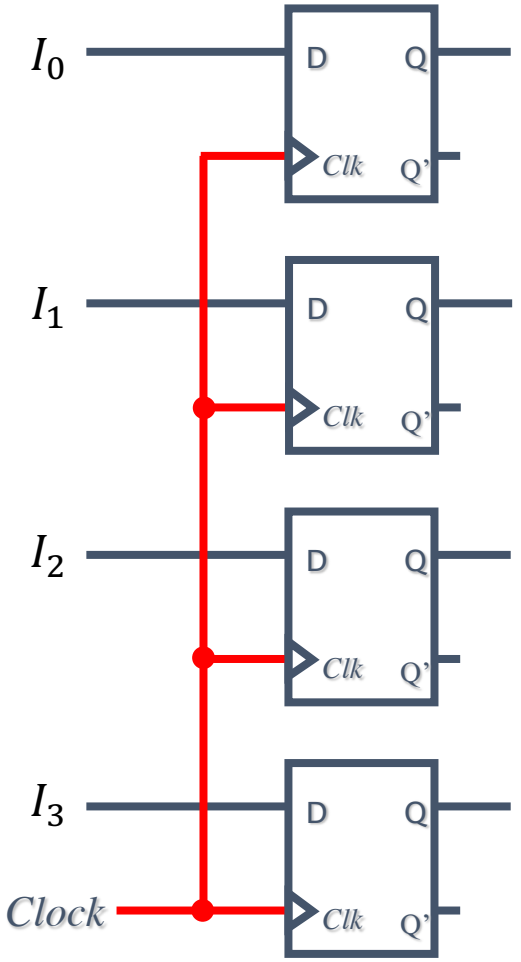
Common Applications of Flip-Flops

Registers

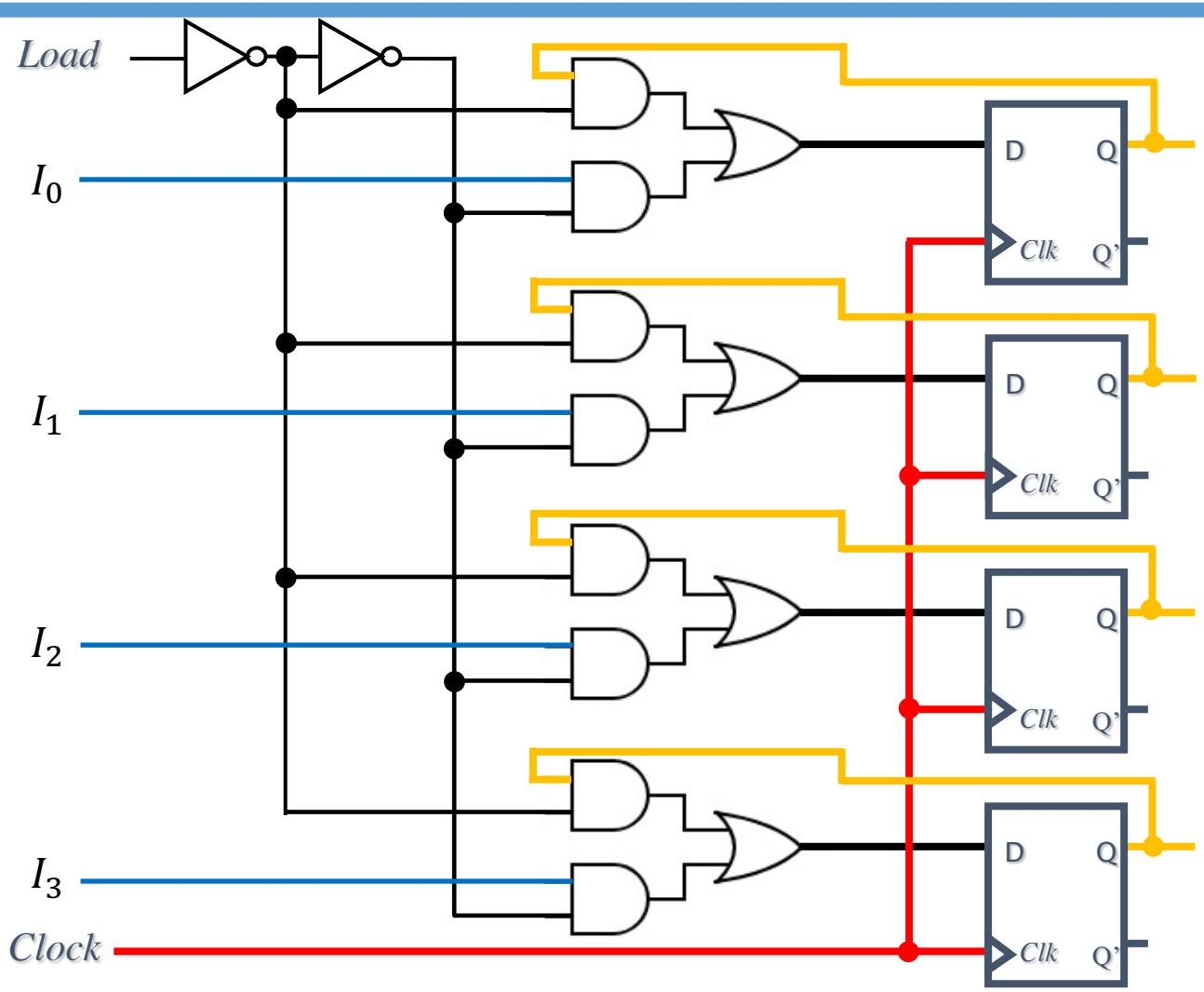
- A series of flip-flops with a common clock input is considered as a Register.
  - Ex. A 32 bit register consists of 32 flip-flops.
- A combinational circuit may combine with a register to aid additional operatioons.
  - Flip-flops to hold the information
  - Combinational circuit to process/ transfer the information

Storage Register

- Simplest Register
- A group of D Flip-Flops
- Binary inputs will be stored at the flip-flops with a clock signal.
- Stored information can be read at anytime.
- Can have separate asynchronus input signal to clear all flip-flops.



4 bit Register with Parallel Load



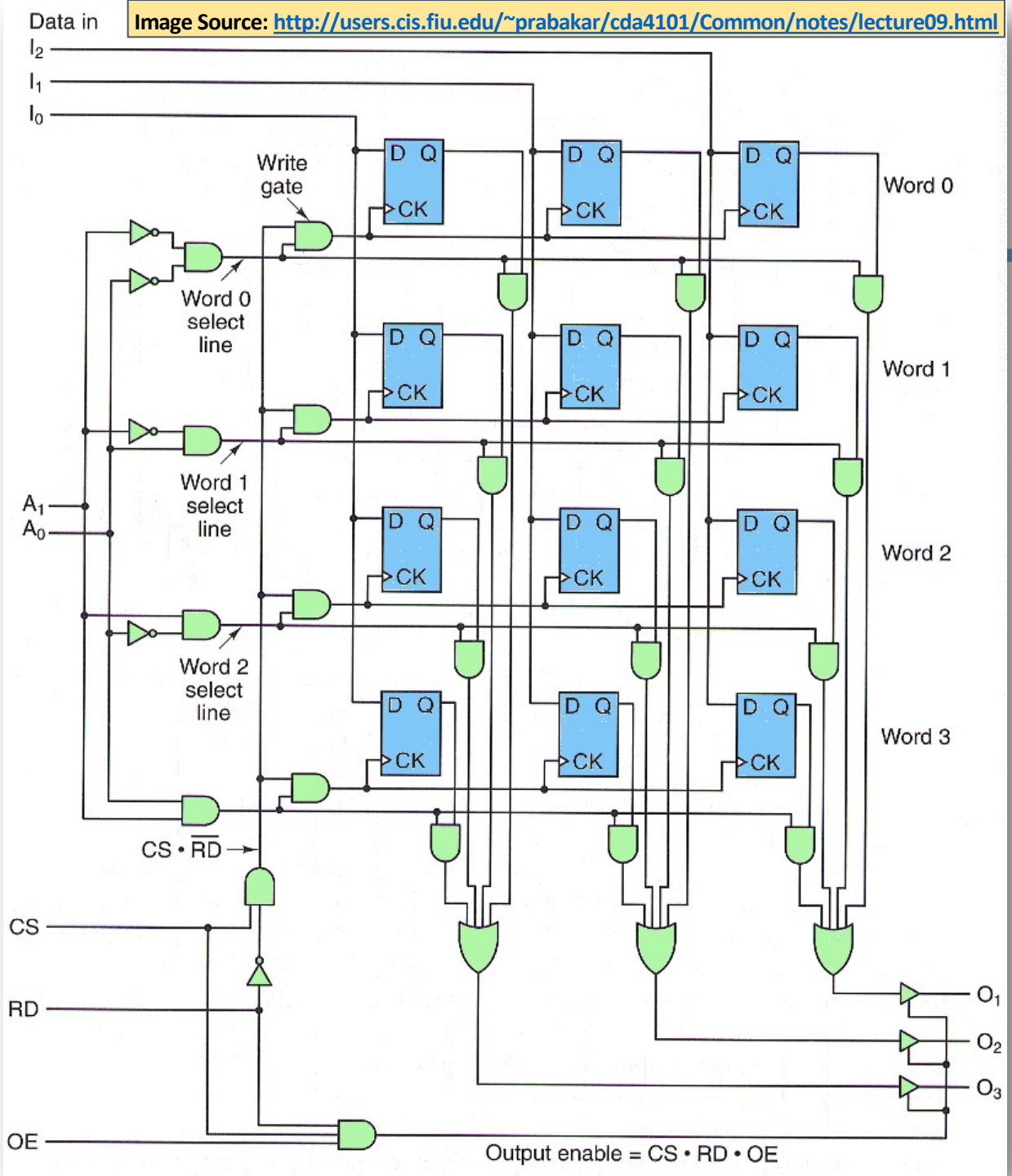
Shift Registers

Explore about "*Shift Registers*"

Start from

- https://en.wikipedia.org/wiki/Shift_register

RAM



4 words
Word Size = 3 bits

Data bus: I_2 - I_0

Address bus = A_1 - A_0

CS: Internal Activation
RD: Read Enable
OE: Output Enable

Recognize the Decoder, Multiplexers here...

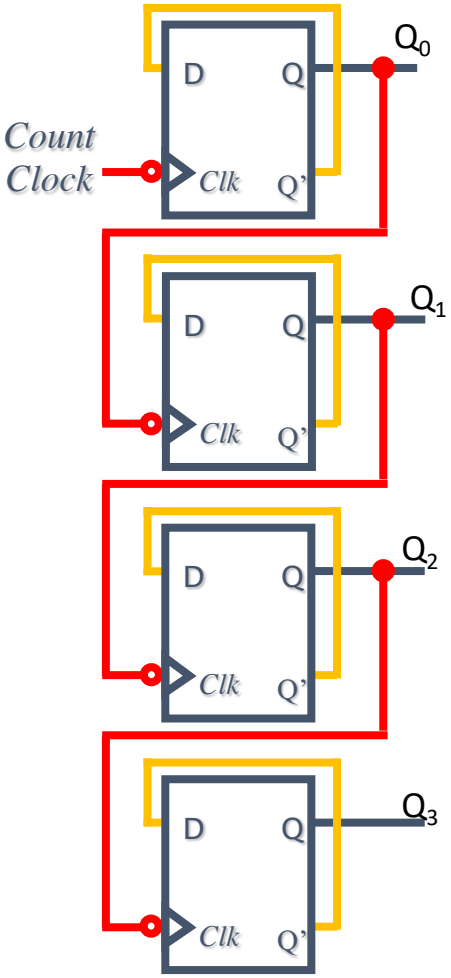
Counters

An ordered set of Flip-Flops can produce a defined sequence of states upon a series of triggers.

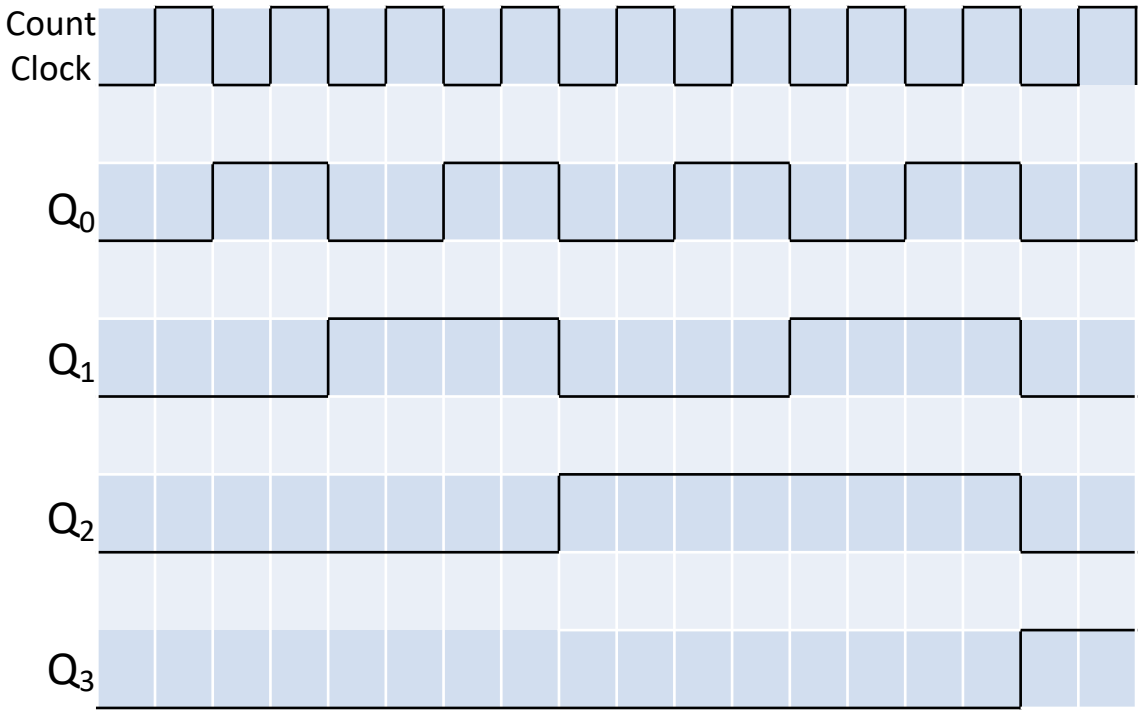
- **Ripple Counters**: Each Flip-Flop is triggered not by a clock, but by the another flip-flop output transition.

- **Synchronus Counters**: Flip-Flops are triggered by a common clock.

Binary Ripple Counter

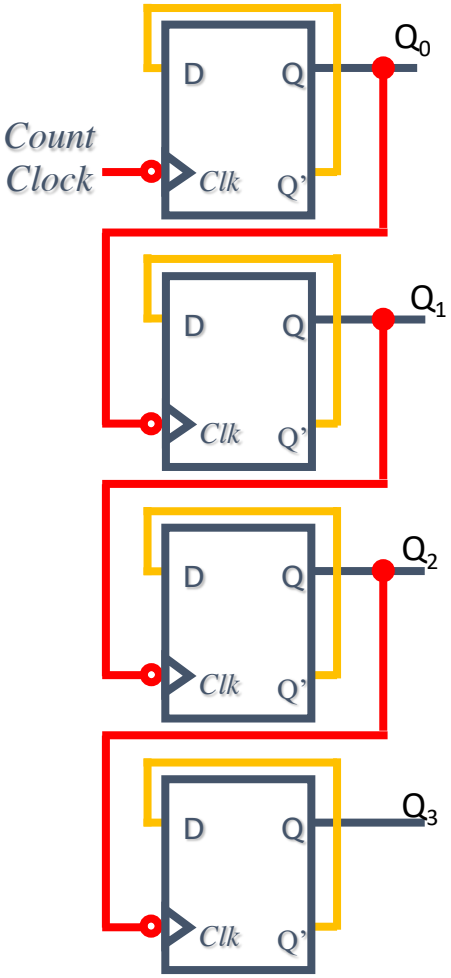


Timing Diagram

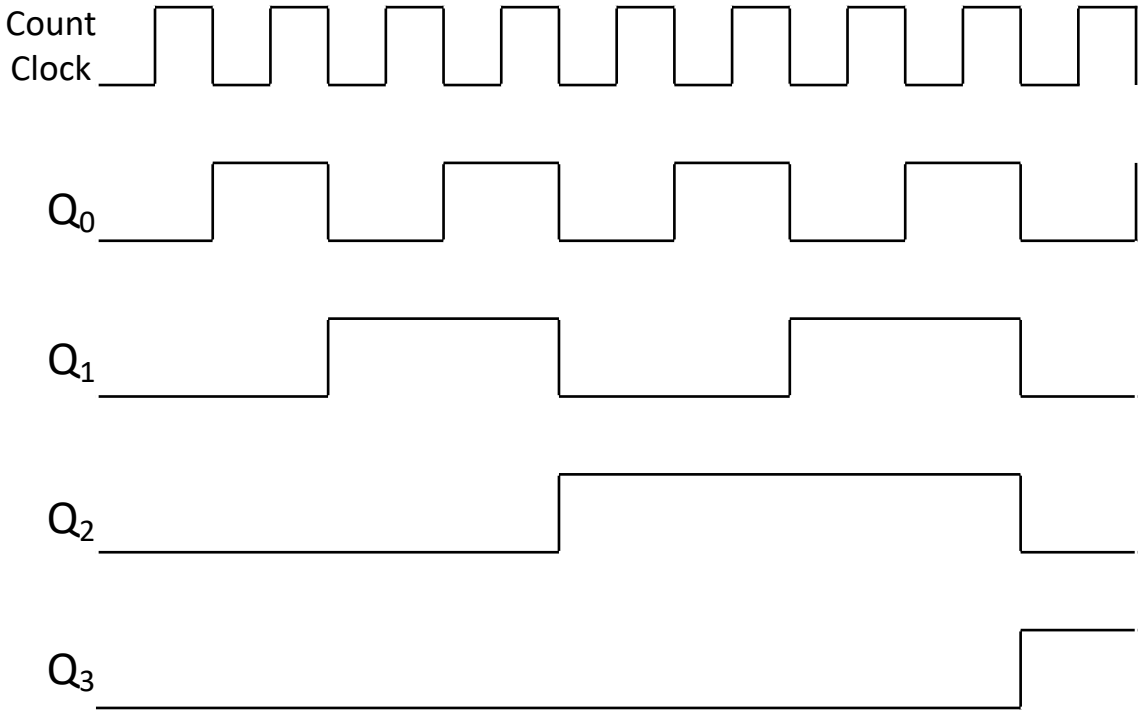


Note: Negative edge sensitive D Flip-Flops

Binary Ripple Counter (Cont.)

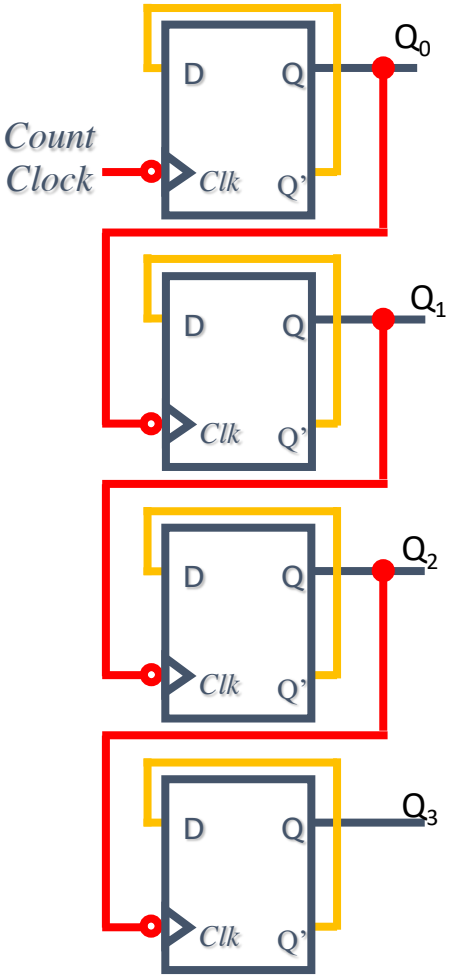


Timing Diagram

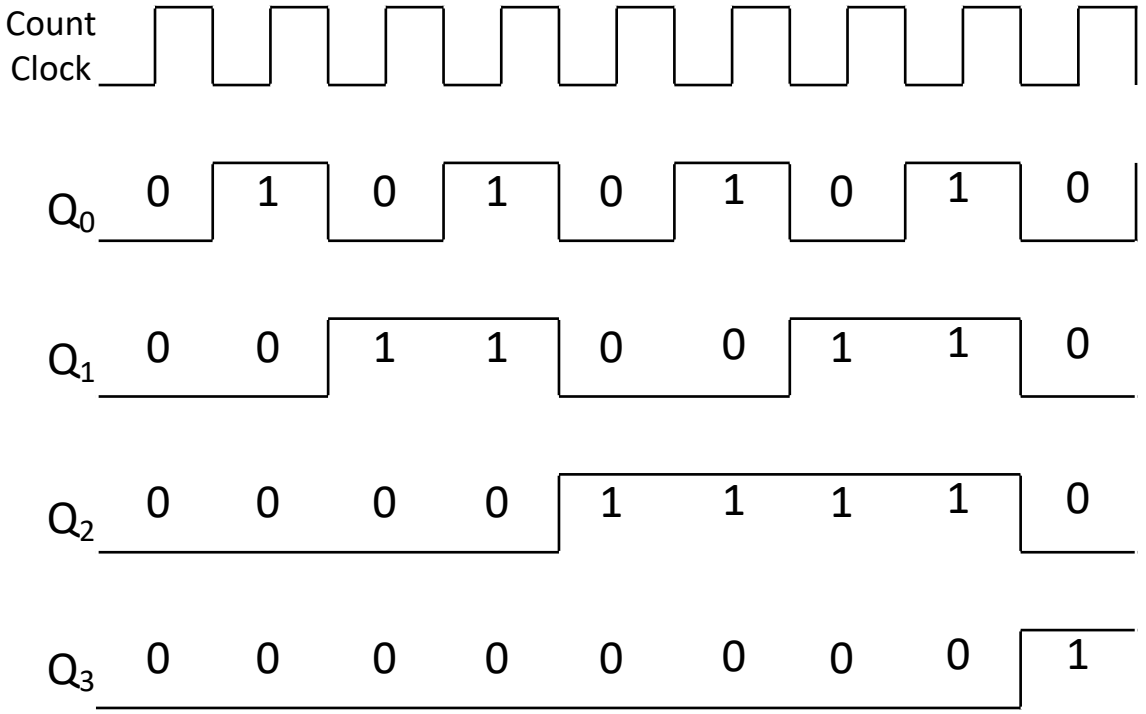


Note: Negative edge sensitive D Flip-Flops

Binary Ripple Counter (Cont.)



Timing Diagram



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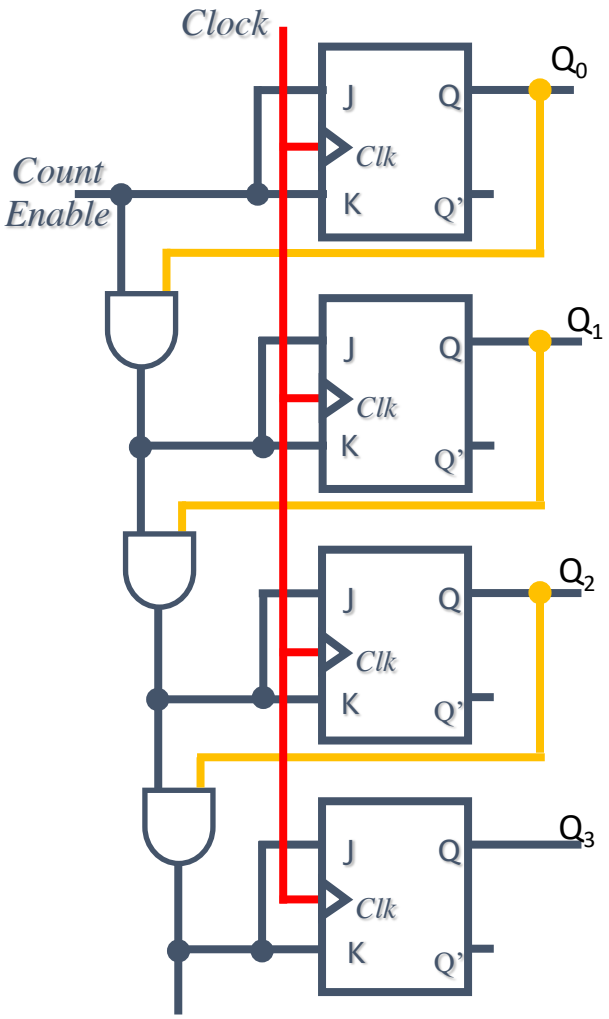
Synchronus Binary Counter



Set Up

- Q_0, Q_1, Q_2, Q_3 are zeros at the beginning
- Positive Edge triggered J-K Flip-Flops
- *Count Enable* is set 1
- Common Clock is connected to all Flip-Flops

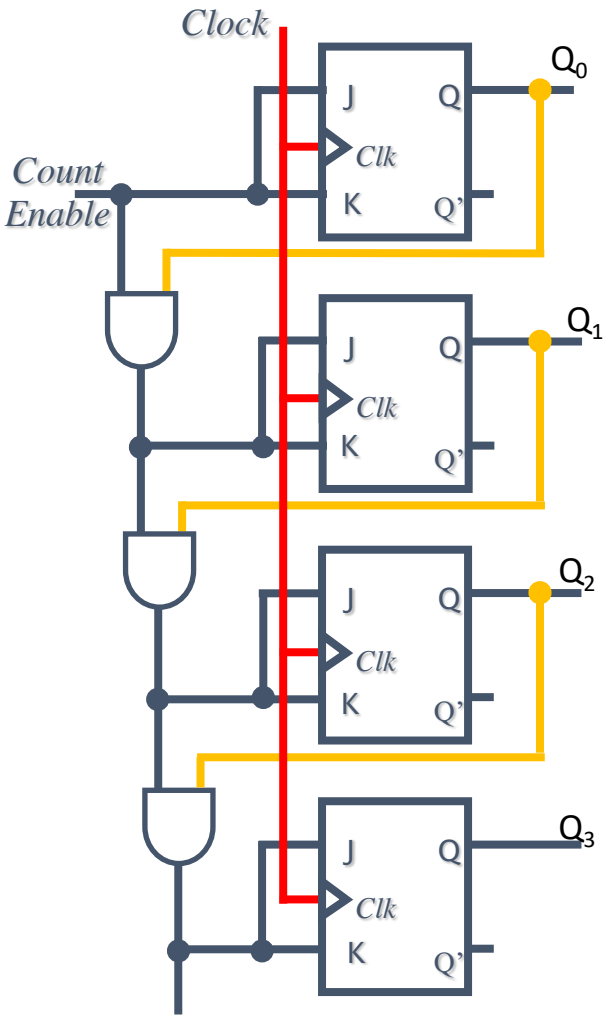
At the very first positive edge of the clock pulse

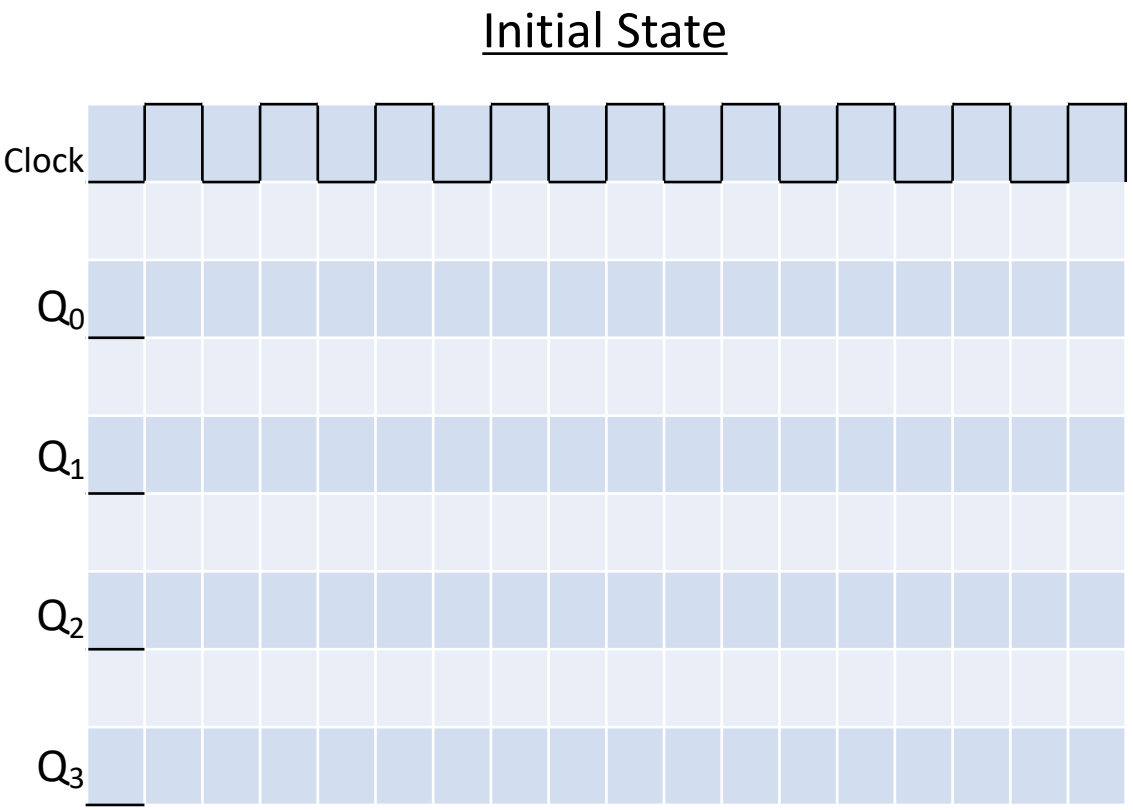
- First Flip-Flop's **J** and **K** inputs are at logical 1
- Second Flip-Flop's **J** and **K** inputs are at logical 0
- Third Flip-Flop's **J** and **K** inputs are at logical 0
- Fourth Flip-Flop's **J** and **K** inputs are at logical 0

Effect

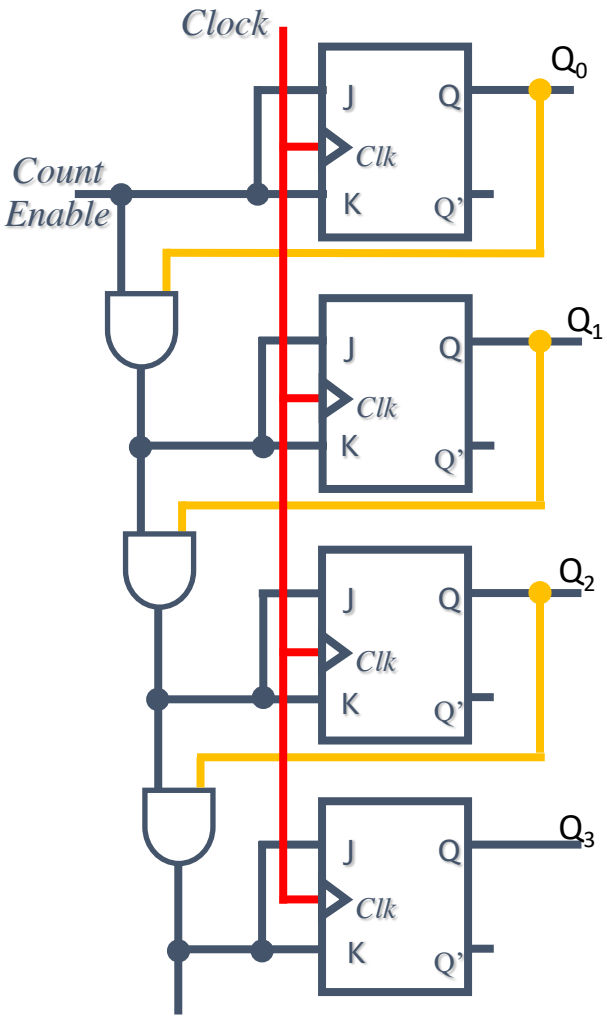
- Only the first Flip-Flop changes it's value
- All the other Flip-Flops remain unchanged
- States are unchanged until it sees the next positive edge clock signal

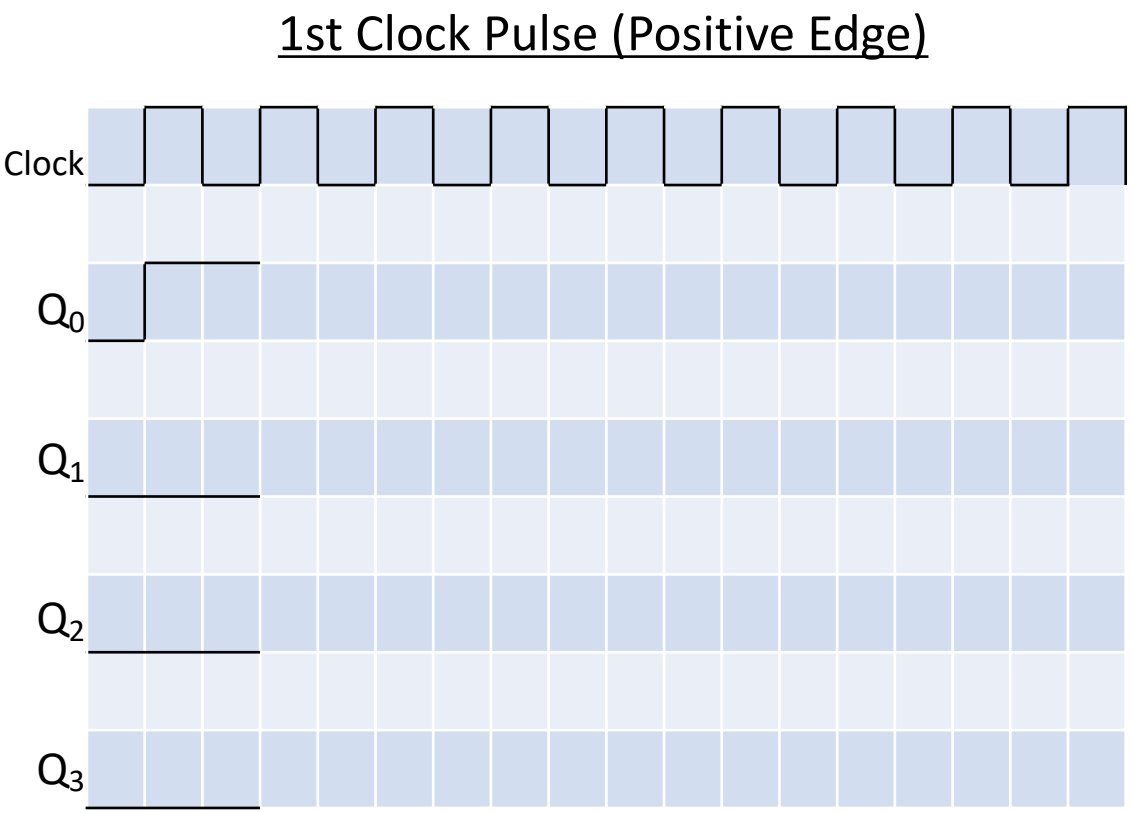
Synchronus Binary Counter (Cont.)



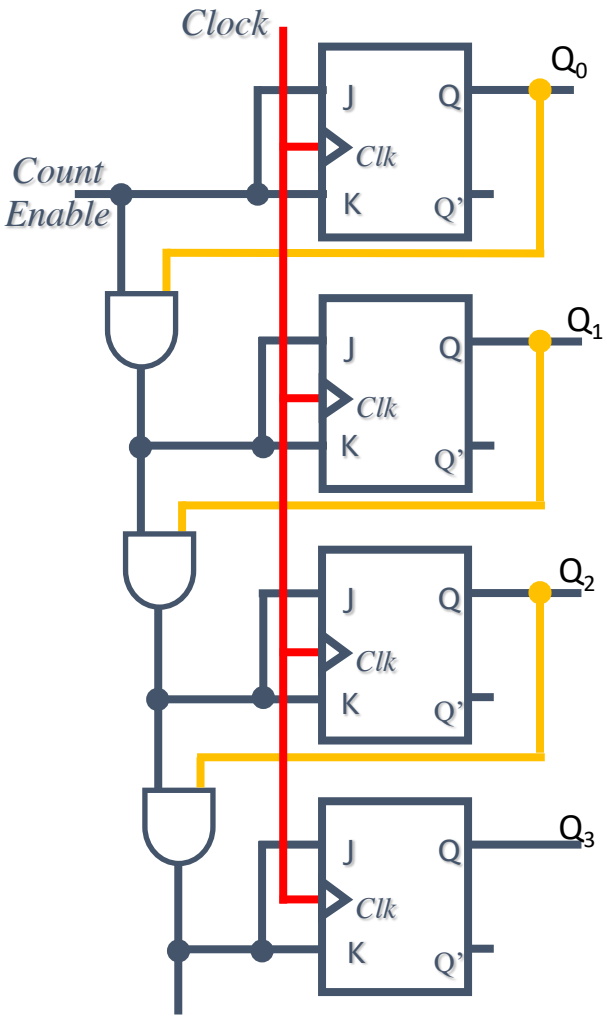


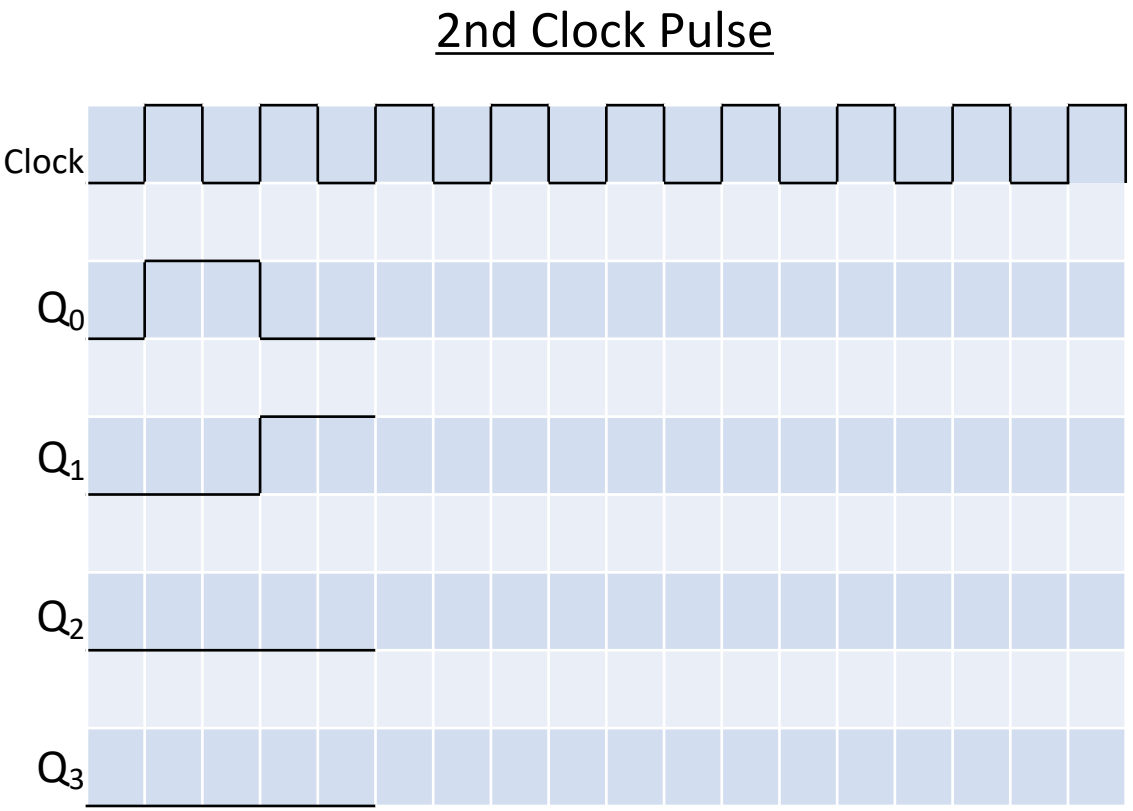
Synchronus Binary Counter (Cont.)





Synchronus Binary Counter (Cont.)





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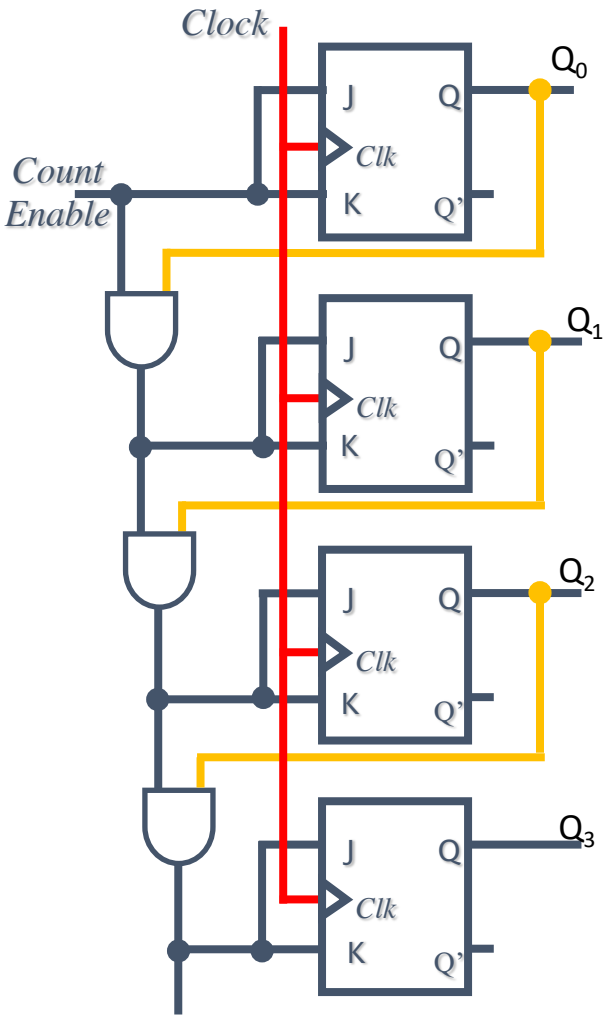
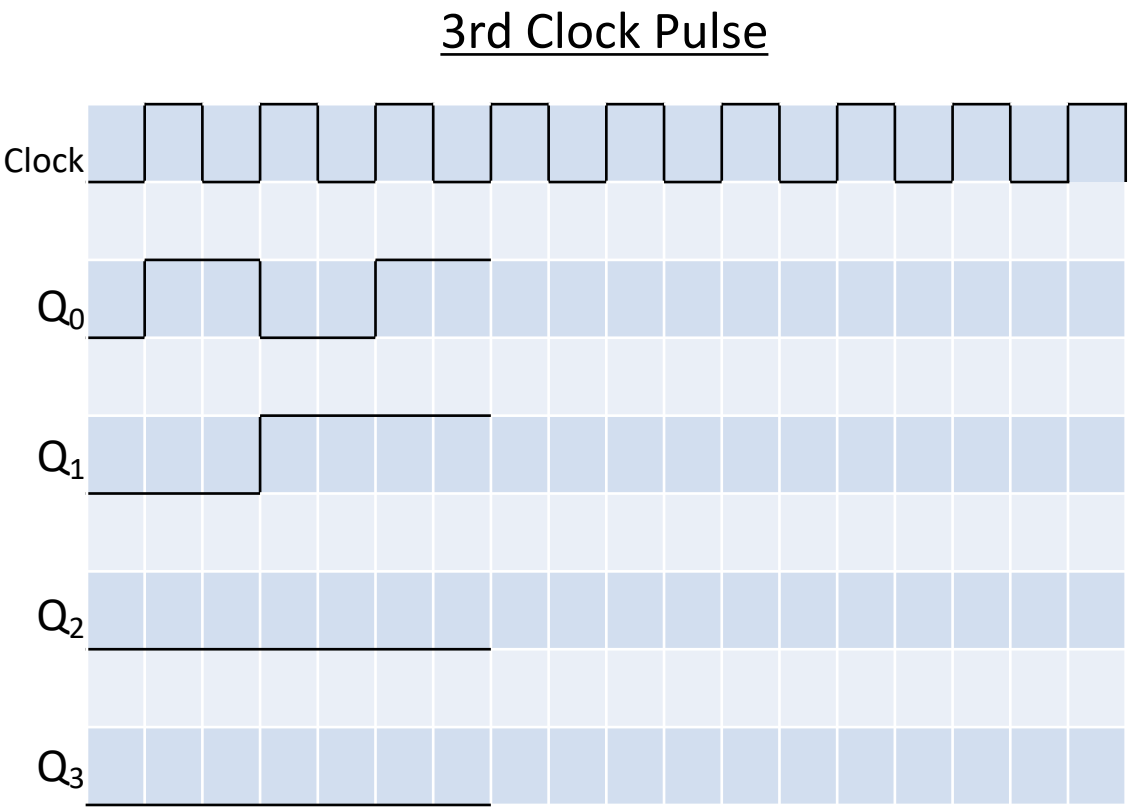
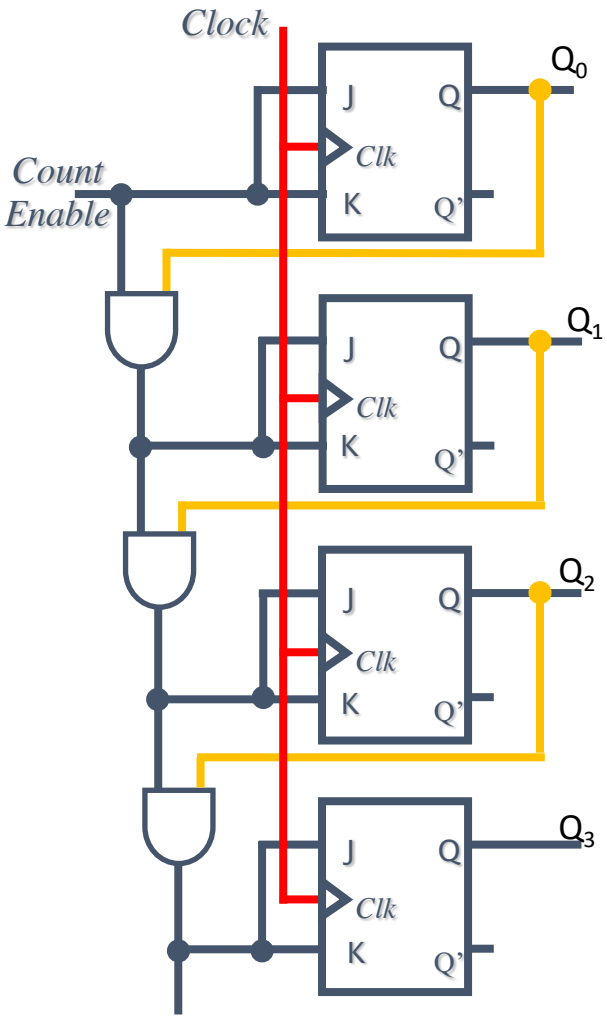
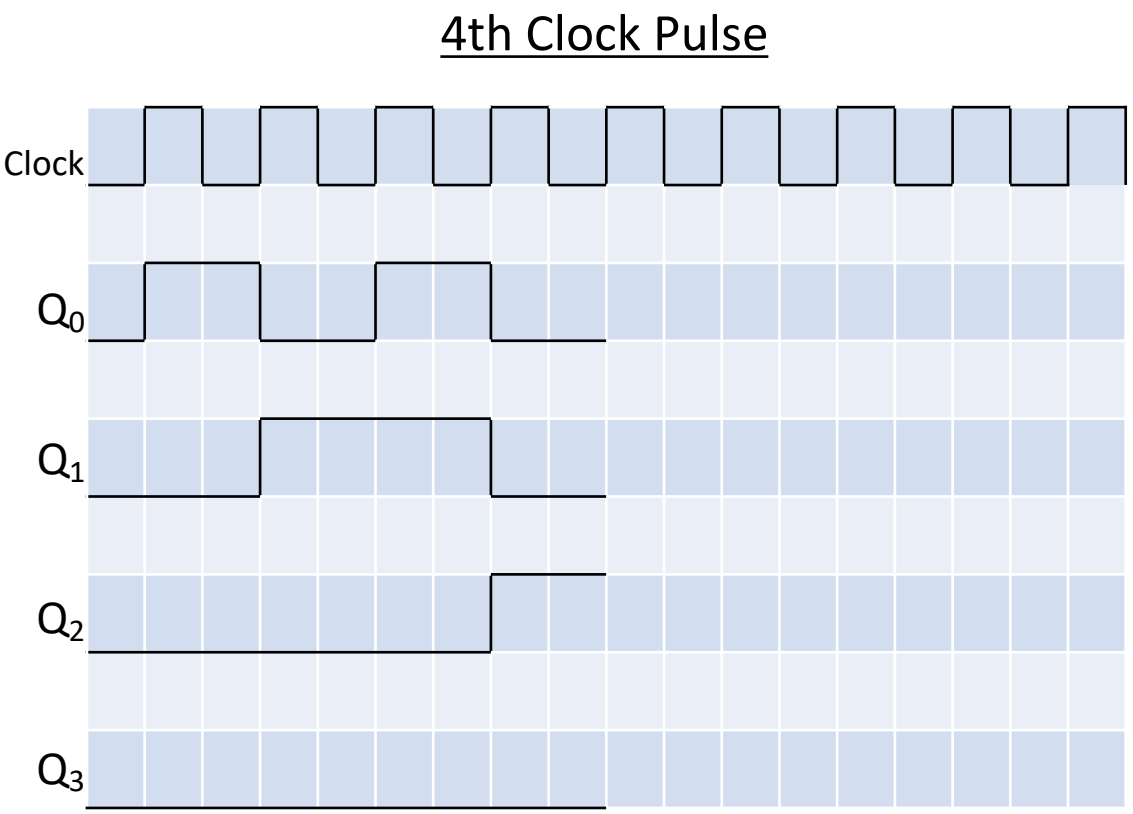


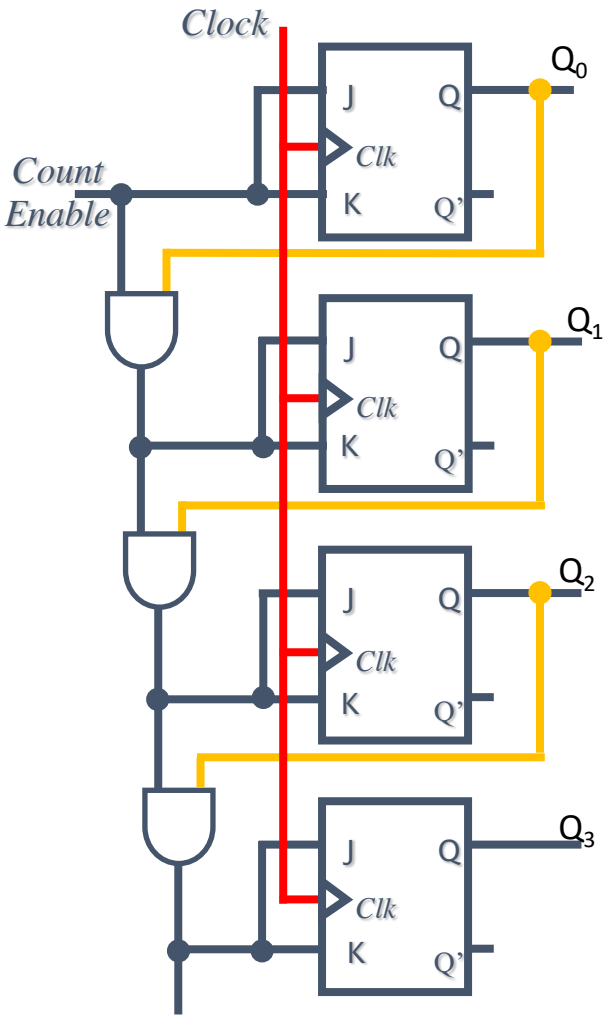


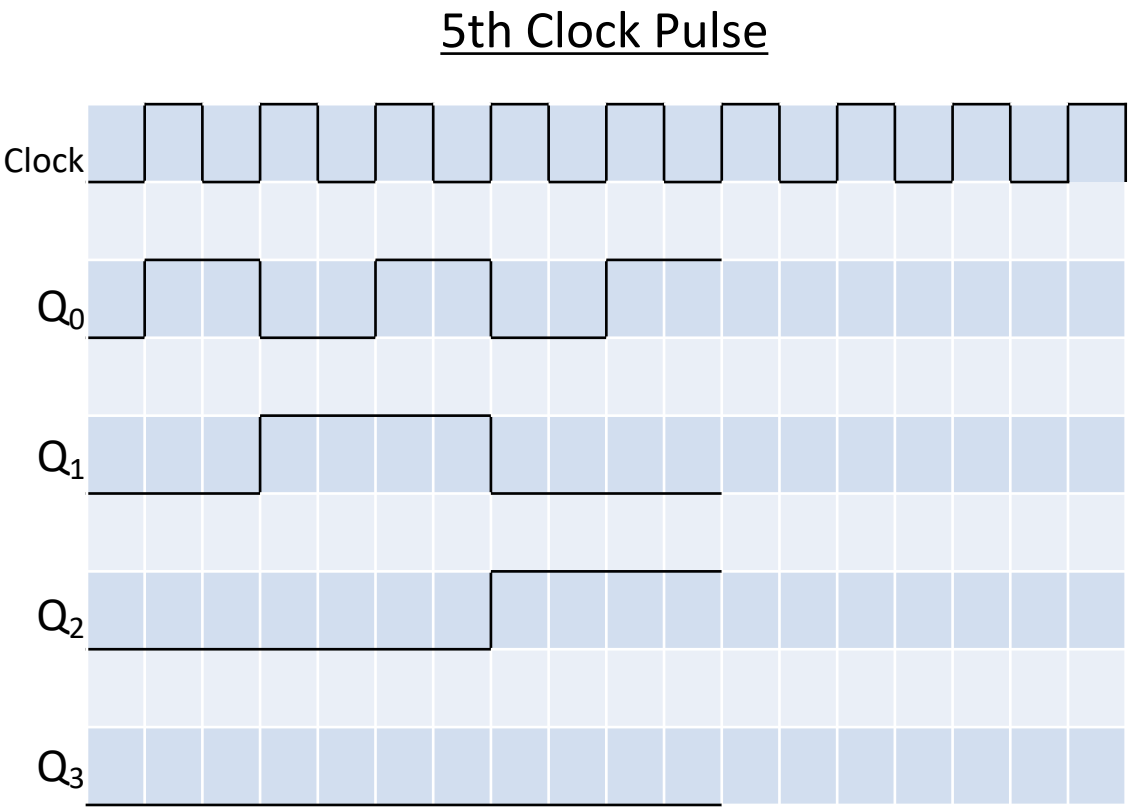
Synchronus Binary Counter (Cont.)





Synchronus Binary Counter (Cont.)





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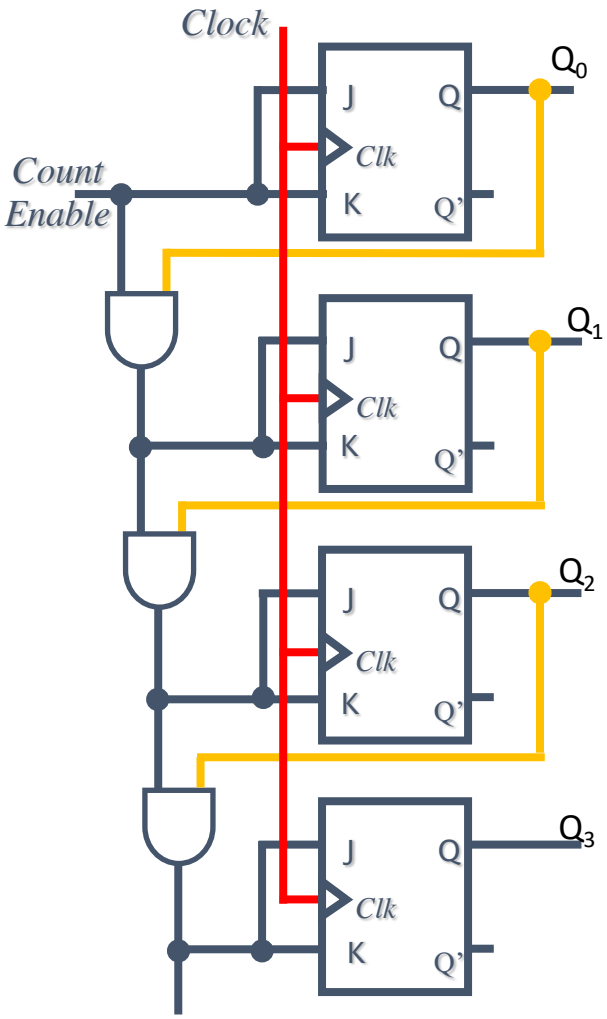

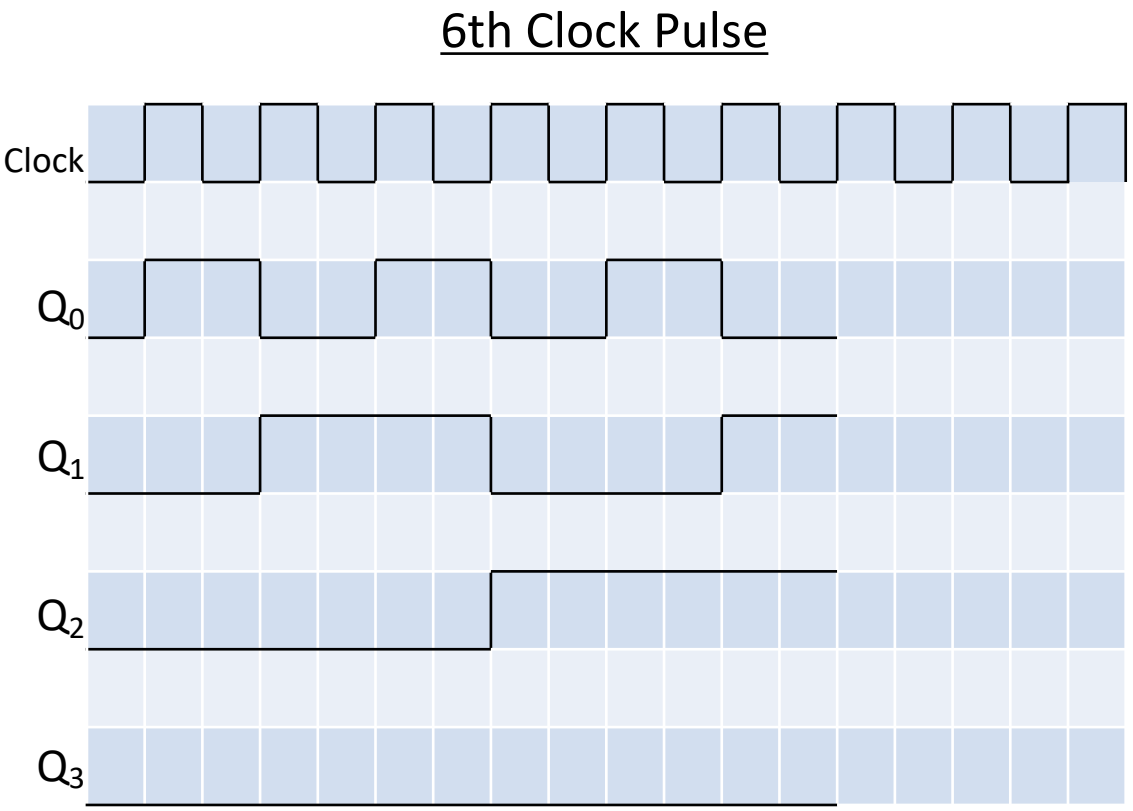

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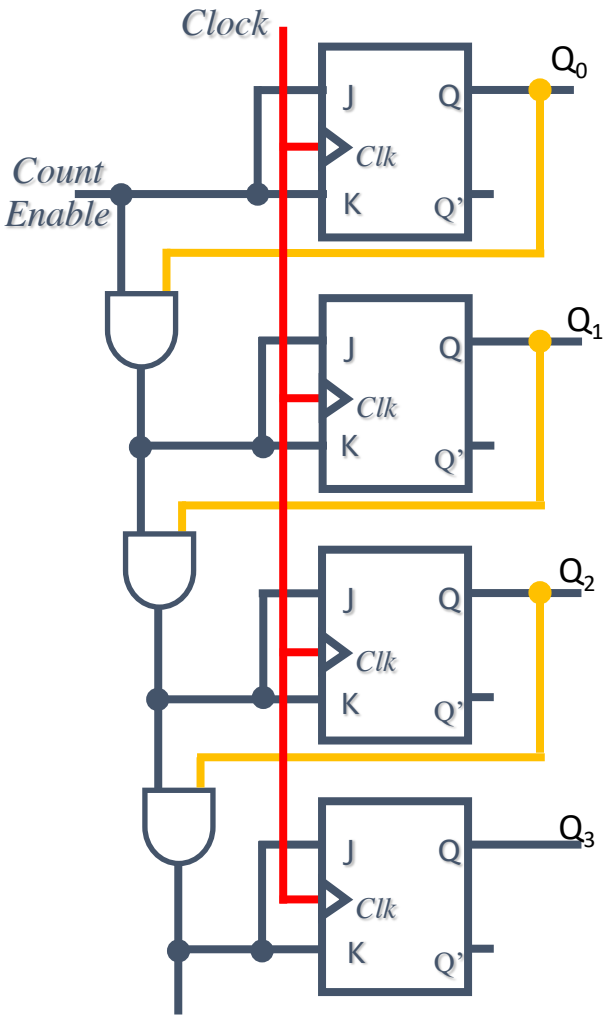

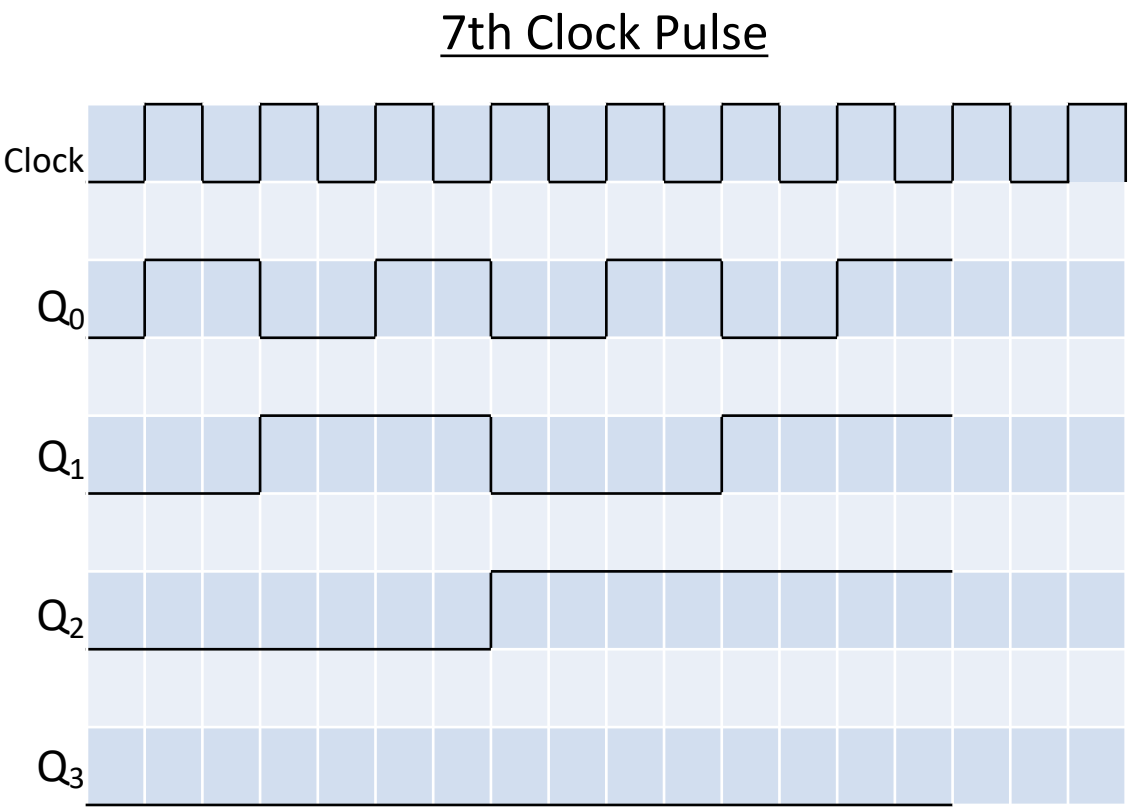

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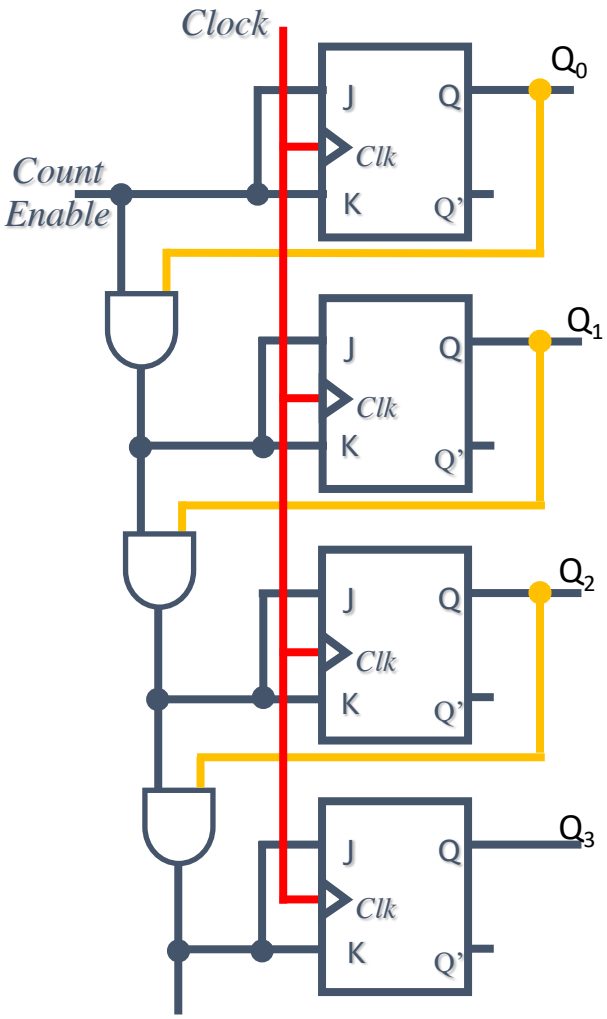

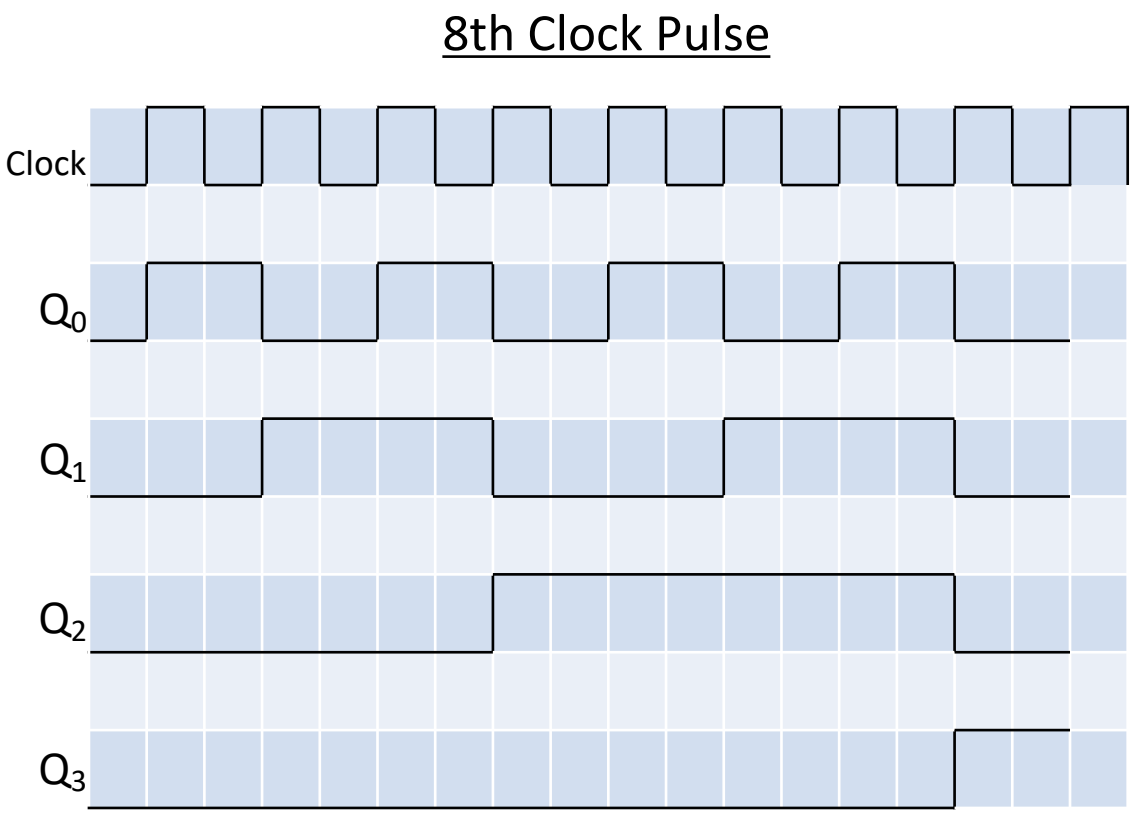

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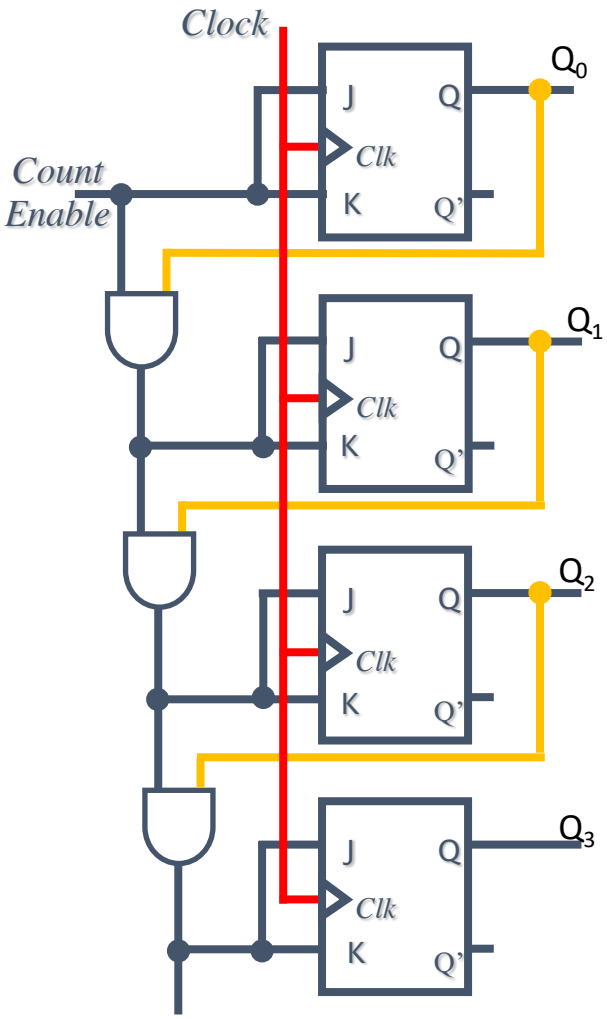

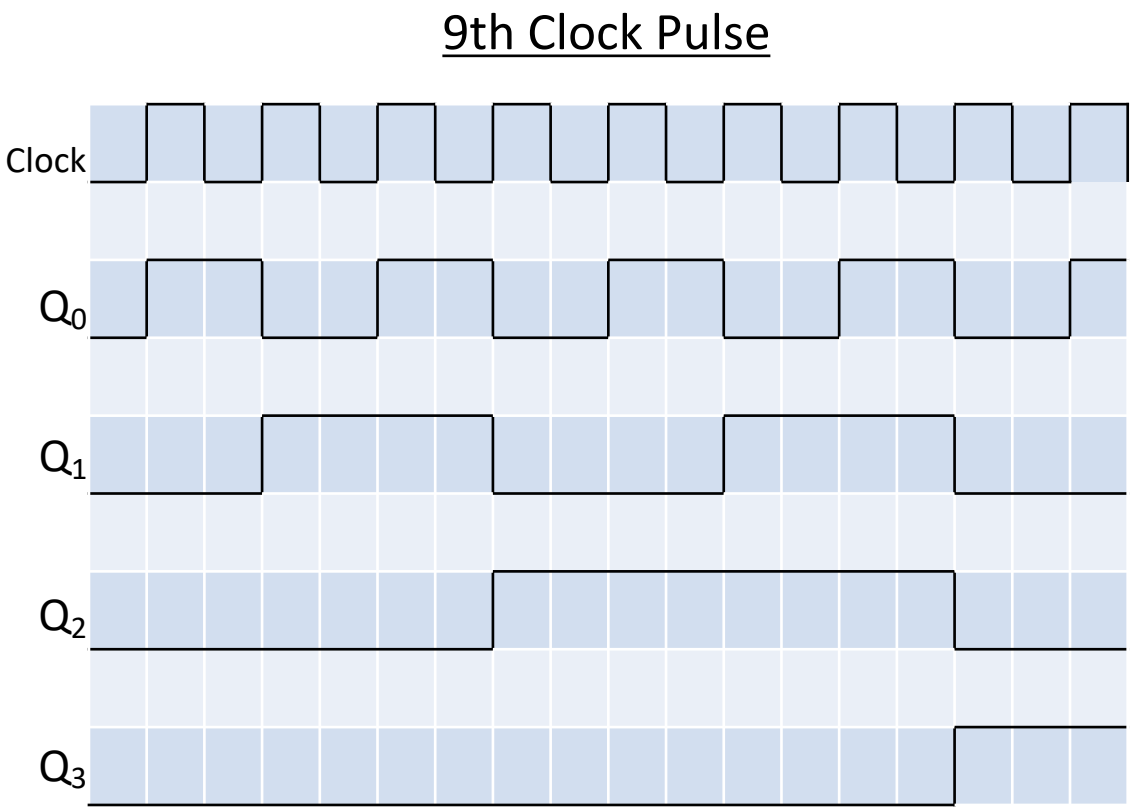

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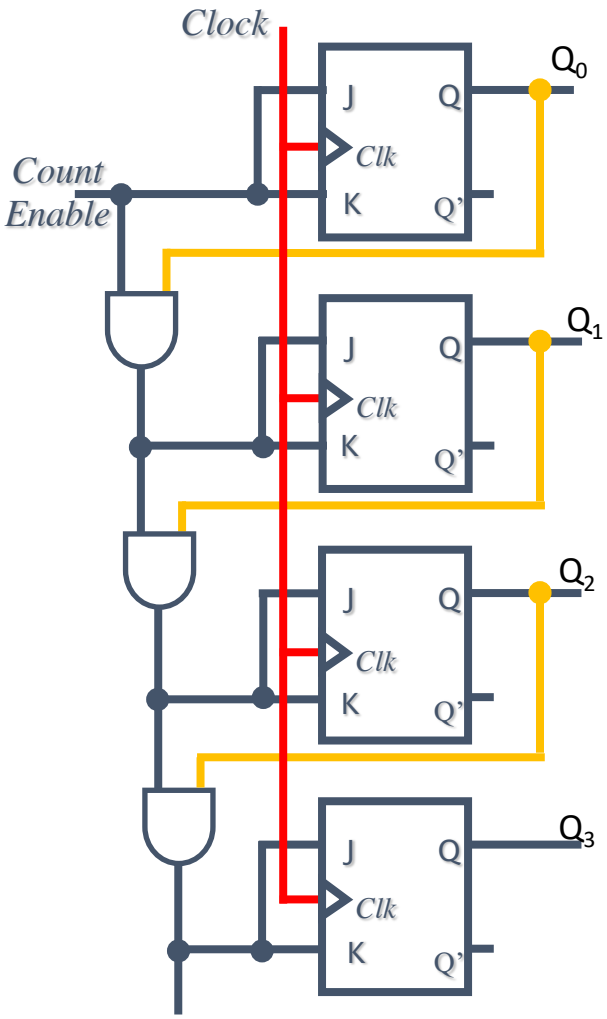

9th Clock Pulse

Clock										
Q_0	0	1	0	1	0	1	0	1	0	1
Q_1	0	0	1	1	0	0	1	1	0	0
Q_2	0	0	0	0	1	1	1	1	0	0
Q_3	0	0	0	0	0	0	0	0	1	1

External References

- http://users.cis.fiu.edu/~prabakar/cda4101/Common/notes/lecture09.html

Thank You..!