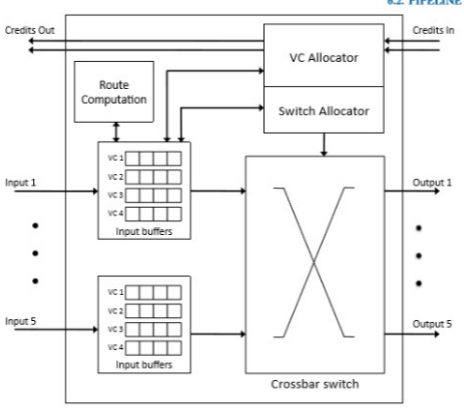
The below figure is the microarchitecture of a state-of –the-art credit based virtual channel(VC) router to explain how typical routers work. The router has five input and output ports .The major components which constitute the router are the input buffers,route computation logic, virtual channel allocator(VC allocator) , switch allocator and the crossbar switch.Most on-chip network routers are input-buffered, in which packets are stored in buffers only at the input ports, input buffered as input buffering permits the use of single-ported memories.Here, we assumed four VCs at each input port,each with its own buffer queue that is four flits deep.



Micro Architecture for Virtual Channel Router

Explanation of the steps inside the architecture:

A head ﬂit,up on arriving at an input port,is ﬁrst decoded and buffered according to its input VC in the buffer write (BW) pipeline stage. In the next stage, the routing logic performs route buffer write computation (RC) to determine the output port for the packet.The header then arbitrates for a VC corresponding to its output in the vc allocation(VA) stage.Upon successful allocation of a VC the header flit proceeds to the switch allocation(SA) stage where it arbitrates for the switch input and output ports.On winning the output port, the flit is then read from the buffer and proceeds to the switch traversal(ST)stage,where it traverses the crossbar.Finally,the flit is passed through the output port.

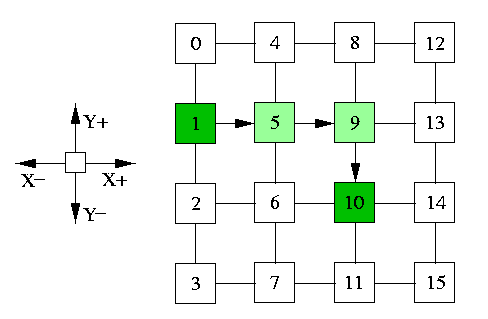
Routing algorithm in NoC:

Network on Chip is another version of System on Chip which is implemented in the form of Network, so called as NoC , The On Chip communication in NoC will take place through packet switching. Routing Algorithm determines in which path the packet can be transmitted from source to destination, for this function routers are used between nodes in the network, this routers will direct the packets depending upon the routing algorithm implemented in the design of NoC .so, it is in the hands of the designer to select a suitable network topology and routing algorithm to achieve best performance of the system that overcomes scalability and performance limitations. The routing algorithm of the designed NoC results in the performance of the system. Latency, throughput and load distribution are very important parameters to be considered while designing.

XY Routing algorithm:

In network on chip (NoC), routing is done to interface distinctive components together in the most effective way. For instance selecting a short way might be imperative in one circumstance, while making a proper activity load adjusting may be of more prominent significance in other circumstance. A limitless number of routing algorithm have been proposed and every one of them have a few advantages and disadvantages contrasted with each other. One routing may be beneficial in one NoC while the same may not suit for the other NoC.

The XY routing algorithm is one of the distributed deterministic routing algorithm . Deadlock or live lock never occurs in XY routing. XY routing algorithm is most suitable for networks implemented using mesh topology. The packets which occurs at the nodes are first routed in X-direction and then in the Y-direction. X-direction indicates movement of packets in horizontal direction and Y- direction indicates movement of packets in vertical direction to the receiver. Routers address are placed in XY coordinates.



XY routing algorithm