# Design and Implementation of 8 - Bit ALU using Verilog

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**Abstract:**

The goal of the Research work is to create an autonomous output validation system by integrating the clock system in an 8-bit arithmetic logic unit (ALU) using Verilog. This ALU has an 8-bit data width and uses a clock mechanism that synchronises with positive edges so that it can review outputs after each operation without needing to be manually modified for certain line inputs. The ALU automatically evaluates outputs at the positive edge of each clock cycle, ensuring correctness and dependability. This is accomplished by integrating a clock-driven output validation mechanism. By doing away with the necessity for manual intervention, this simplifies the verification procedure and boosts overall operational effectiveness. The design's code execution verified its functioning in a real-time setting by utilising FPGA implementation, guaranteeing smooth integration and dependable performance. Furthermore, thorough analysis with Xilinx tools revealed information on route delays and device utilisation, which was crucial for optimising the design for real-world use.

**Keywords:** ALU, Verilog.

## 1. Introduction

Arithmetic Logic Units (ALUs) are essential to digital electronics and computers because of their effectiveness and utility. One of the most important developments in the effort to improve computing power is the idea of an 8-Bit ALU strengthened with an integrated clock mechanism. This research combines the accuracy of clock-driven assessments with the simplicity of ALU operations, removing the need for human involvement when choosing operating modes. The particular feature of this work is the addition of a clock that integrates the examination of output results presented by different Operations. The ALU's output is examined at the positive edge of every clock cycle, providing an exacting assessment of each operation's outcome without the need for human interaction. This automatic validation guarantees accuracy and consistency in the calculation result while also speeding up the evaluation process.

Most importantly, this work heavily relies on the use of Xilinx tools. Using Xilinx's capabilities, Synthesis and simulation of Verilog Module, device utilisation and route delays were carefully tracked and examined. The code for the work was run on a Field-Programmable Gate Array (FPGA), demonstrating its real-time applicability and practical viability. Through the integration of an 8-Bit ALU's capabilities with a clock-based evaluation system, this work represents an innovative approach for evaluation in digital computing. Its importance in accelerating computing operations without reducing accuracy and efficiency is demonstrated by the easy integration of hardware and software as well as the automation of output validation.

### 1.1 Literature Survey

In the literature, there are several studies related to the design and implementation of ALUs using Verilog and FPGAs. Some of these studies are discussed below:

In the paper authored by Sanju et al. [2] , the full-swing gate diffusion input (GDI) technique is used to optimize a 4-bit Arithmetic Logic Unit (ALU) by delay-time improvement. Through the use of 130nm technology and HSPICE simulation, the altered ALU exhibits better power, delay, and energy efficiency performance metrics. This improved ALU architecture indicates that it can be used in low-power and high-speed applications, which means that it can be used to a variety of digital processing scenarios, such as microprocessors and digital signal processors (DSPs).

The design and analysis of a 32-bit Arithmetic Logic Unit (ALU) using reversible gates on FPGA is the primary focus of the paper by Swamynathan et al. [3]. The potential of reversible gates in low-power computation and information processing has drawn attention. The work presumably contributes to the field of reversible logic and its use in hardware design by examining the efficiency, advantages, and implementation of these gates in the ALU design inside the FPGA architecture.

The 18th International Conference based on Intelligent Systems Design and Applications (ISDA 2018) featured a paper by Shirol et al. [5], that presents a novel design and implementation strategy for an 8-bit and 16-bit Hybrid Arithmetic Logic Unit (ALU). It is possible that the hybrid ALU incorporates components or features from several ALU designs in order to improve usefulness or performance. The work presumably contributes to the advancement of ALU design paradigms by describing the design methodology, implementation specifics, and possible benefits of this unique hybrid ALU architecture.

Chandralekha et al. research [6], which was presented at the IEEE 5th International Conference (ICCCA) in 2020, focuses on designing Reversible Arithmetic Logic Units (ALUs) with a bit count of 8 and 16 that are intended for low-power applications. It probably goes over the design principles and practical applications of these reversible ALUs, highlighting how they can significantly cut down on power use in digital circuits. By assessing the effectiveness and applicability of the reversible ALUs that were built for low-power computing, the study most likely advances the field of energy-efficient hardware design.

## 2. Proposed Method

An organised and methodical approach provides a proposed approach for creating an 8-Bit Arithmetic Logic Unit (ALU) with Verilog HDL. First, the basic functions that include logic and arithmetic are carefully designed and implemented in Verilog HDL to guarantee an easy and effortless integration into the 8-bit architecture. Simultaneously, an essential part of the design is the addition of a clock module which is designed to evaluate the validity of the output at the positive edge of every clock cycle. With the help of this unique feature, selecting operational modes can now be done automatically, simplifying the validation process and ensuring correctness and efficiency.

The approach also includes a thorough use of Xilinx tools for performing in-depth analysis of route delays and device utilisation. With careful resource allocation and the identification of any delays, this essential phase helps optimise the performance of the ALU and improves the architecture for increased efficiency. Furthermore, an FPGA platform is utilised to develop and simulate the Verilog HDL code. As a validation phase, this real-world deployment verifies the ALU's operation and performance metrics in actual hardware setting. By the use of this comprehensive methodology, the study provides a comprehensive knowledge of the architecture of the ALU, its interaction with the clock module, and its performance characteristics, providing insights into the practical application of the designed system.

### 2.1 Block Diagram

The functional components and interconnections of the 8-Bit ALU utilising Verilog HDL are shown in the block diagram. The logical and arithmetic operation modules for addition, subtraction, AND, OR, XOR, NAND,

NOR, and XNOR operations are clearly shown. It also has a clock and reset mechanism, which are essential for automating the assessment procedure. The input ports A and B, which each get 8-bit binary values, are shown in the diagram along with the ALU_Sel 3-bit select line, which indicates the operation to be performed.

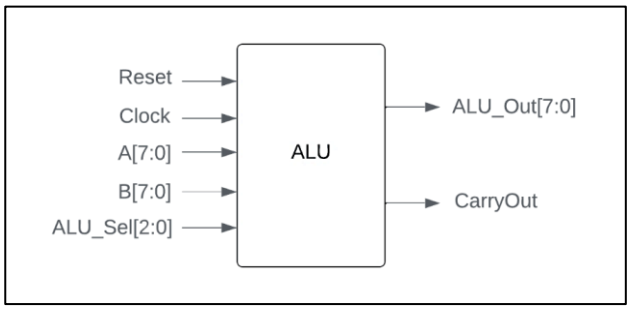


**Fig.1** Block diagram of 8-Bit ALU

The 8-bit result is displayed on the output port, ALU_Out, and carry or borrow during operations is indicated on another port. The diagram illustrates which data and control signals go through the ALU, summarising its modes of operation without focusing on structural details.

### 2.2 Detailed Structure

The RTL (Register-Transfer Level) schematic of an 8-bit ALU using Verilog provides a detailed blueprint of the functional behavior of the ALU. This schematic is fundamental in describing how the ALU operates using a combination of digital logic gates, flip-flops, and interconnecting data paths. Each component in the RTL schematic plays a crucial role in the overall operation of the ALU, ensuring that it can perform a variety of arithmetic and logical operations efficiently.

The RTL schematic for an 8-bit ALU consists of a series of interconnected modules, each designed to perform a specific function. These modules include the Arithmetic Logic Unit (ALU) itself, a Control Unit, Input Registers, an Output Register, and a Carry Flag. Below is an expanded description of each module and its role within the ALU:

1. Arithmetic Logic Unit (ALU): The ALU is the main module that performs various arithmetic and logical operations like addition, subtraction, and bitwise manipulations on 8-bit inputs, producing an 8-bit output. It uses combinational logic and Verilog case statements for operation selection, ensuring high-speed single-cycle execution.
2. Control Unit: The Control Unit generates control signals that determine the ALU's operations based on input instructions. It uses a finite state machine (FSM) in Verilog to manage operation sequencing and data flow, ensuring the ALU performs the correct functions at the right time.
3. Input Registers: Input Registers temporarily hold 8-bit operands for the ALU, ensuring stable data transfer. Defined using reg or always blocks in Verilog, they are loaded with data on clock edges, facilitating seamless operation timing for the ALU.
4. Output Register: The Output Register stores the ALU's 8-bit results after each operation. Updated each clock cycle in Verilog, it holds the most recent computation results, making them available for further processing or output, ensuring data synchronization within the system.
5. Carry Flag: The Carry Flag indicates carry-out from arithmetic operations, crucial for detecting overflow. Implemented in Verilog with a logic statement, it updates alongside the Output Register to reflect the latest operation status, aiding in multi-byte arithmetic management.

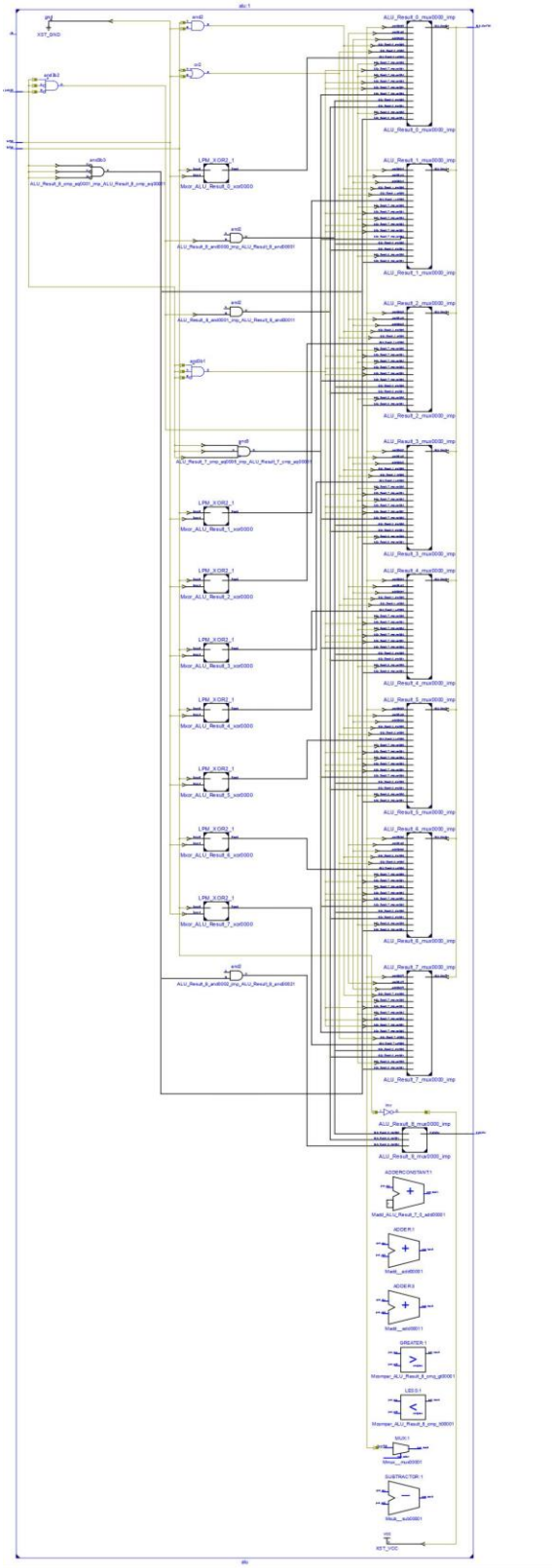

**Fig. 2** RTL Schematic

## 3. Algorithm and Flowchart

### Algorithm for ALU Module:

1. Start
2. Initialize Inputs and Outputs
   - Inputs: A, B, ALU_Sel, clk
   - Outputs: ALU_Out, CarryOut
3. ALU Operation (always block)
   - Check ALU_Sel value
   - Perform corresponding operation
     000: Addition
     001: Subtraction
     010: AND
     011: OR
     100: XOR
     101: XNOR
     110: NAND
     111: NOR
   - Set ALU_Result
   - Set CarryOut
4. Carry and Borrow Logic
   - Check ALU_Sel for 000 and 001
   - Set CarryOut or ALU_Result[8] accordingly
5. Clock Edge (posedge clk)
   - Increment count
6. Assign ALU_Result to ALU_Out
7. End

### Algorithm for Test Bench Code:

1. Start
2. Initialize Inputs
   - A, B, ALU_Sel, clk
3. Simulation Loop
   - Repeat 8 times
   - For each ALU_Sel value (000 to 111)
   - Wait for 10 time units
4. End Simulation
5. Finish

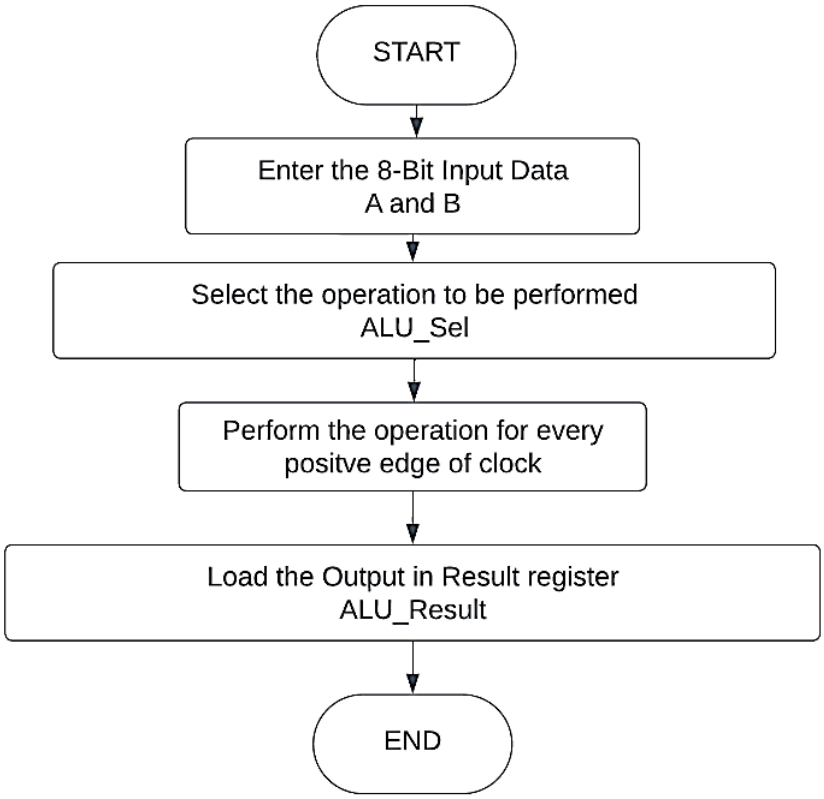


**Fig. 3** Flowchart of 8-Bit ALU

## 4. Testing and Debugging

The testing was conducted on the FPGA Board - Spartan-3E XC3S250E. The UCF file was generated, in which the FPGA pins were allotted to input and output. After generating the bit file, the FPGA kit was connected to the laptop through a downloading cable with one end as a USB connector and the other as a JTAG connector. To dump the code, the Windows FPGA batch file was edited and run. Once the FPGA was loaded with the code, the LED next to the IC started blinking, indicating the status of the chip as programmed. The output was observed on the FPGA Board. Input was provided through the DIP switches, and the clock was varied using a trim pot available on the kit. The output was observed through the LEDs interfaced with the DIP switches.

During the testing of the ALU module, several troubleshooting operations were performed whenever the output was not as expected or errors were encountered. The main issue faced was during the implementation of the carry and borrow/signed logic, denoted by CarryOut. The addition of two numbers was not producing the CarryOut signal as expected due to logical errors in the implemented equation.

While implementing the borrow logic, the output did not match the calculations made on paper. These errors were resolved by cross-checking the logic of the equations and ensuring the output remained correct by implementing various test cases with different input values.

A counter was also implemented in the code. The results observed were as expected in the simulation waveforms, but due to some warnings generated in the code, the counter's operation on the FPGA kit was not functioning correctly.

The select lines were not incrementing on every clock edge pulse. As a result, the input for the ALU select lines had to be provided manually through the DIP switches available on the FPGA kit.

## 5. Results and Discussion

The findings from experimentation and thorough analysis that resulted from the Verilog HDL implementation of an 8-Bit ALU are discussed in the following section. It includes the assessment of the integrated clock mechanism's ability to independently confirm operating outputs, eliminating the need for manual selection of operations. Furthermore, in order to optimise the performance of the ALU, this part explores the insights obtained from Xilinx tools, specifically looking at device utilisation and route delays.

An additional fundamental component is the FPGA-based Verilog HDL code execution, which demonstrates the planned ALU's real-world applicability and practical validation according to hardware constraints.

### 5.1 Simulation Result

The synthesis and simulation of 8-Bit ALU Verilog module was executed on Xillinx Software.

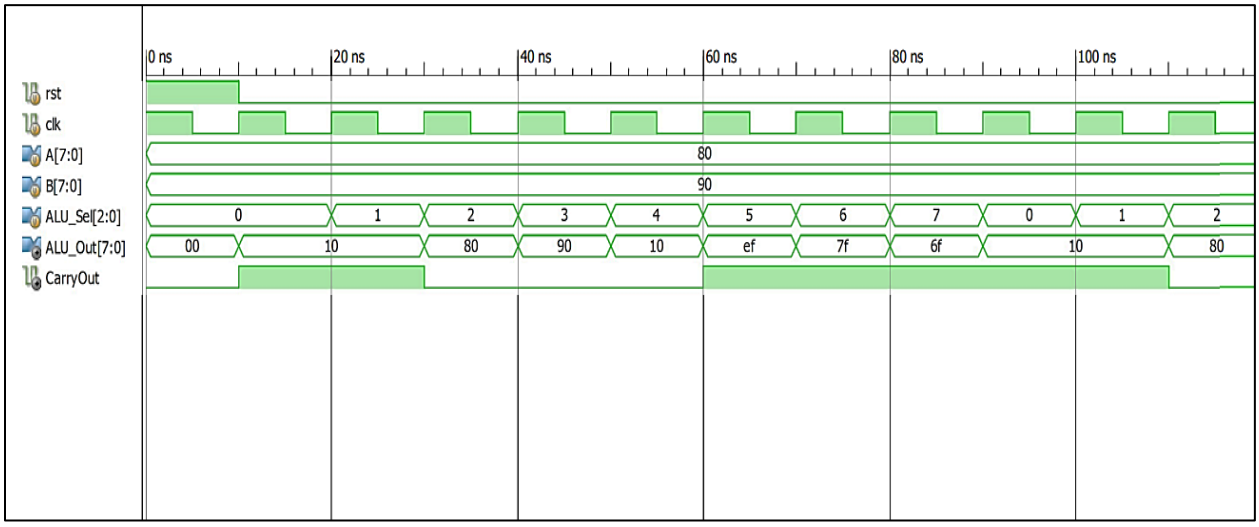


**Fig. 4** Simulation result on Xillinx ISE

- The above simulation results are obtained through the execution of testbench code.
- A and B are the two inputs given to the ALU to check the output of the system.
- A is given value 80H and B is given the value 90H. (H denotes hexadecimal)
- The selection of inputs is made in such a way that the output will generate CarryOut signal in both addition and subtraction operation.
- The ALU select line is incremented every positive edge of clock cycle in order to display all the 8 operations of ALU.
- The outputs can be cross checked with the observation table.
- The carry out which is being generated during addition operation, is denoted by CarryOut signal as observed in waveform.
- The output of subtraction operation is a negative output and it is denoted by the high value of CarryOut signal.

### 5.2 Timing Summary

- Minimum period: 7.755ns (Maximum Frequency: 128.955MHz)
- Minimum input arrival time before clock: 11.271ns
- Maximum output required time after clock: 4.040ns

### 5.3 Observation Table

**Table 1** Observation table

| OBSERVATION TABLE | | | | |
|---|---|---|---|---|
| Operands: A= 80H B=90H | | | | |
| Sr. No. | ALU_Sel | Operation | ALU_Out | CarryOut |
| 1) | 000 | Addition | 10 | 1 |
| 2) | 001 | Subtraction | F0 | 1 |
| 3) | 010 | AND | 80 | 0 |
| 4) | 011 | OR | 90 | 0 |
| 5) | 100 | XOR | 10 | 0 |
| 6) | 101 | XNOR | EF | 0 |
| 7) | 110 | NAND | 7F | 0 |
| 8) | 111 | NOR | 6F | 0 |

### 5.4 Design Summary

**Table 2** Device Utilization Summary

| Parameters | Result |
|---|---|
| No. of Slices | 49 (2%) |
| No. of Slice Flip Flops | 14 (0%) |
| No. of 4 i/p LUTs | 91(1%) |

| | |
|---|---|
| No. of I/Os | 30 |
| No. of bonded IOBs | 30 (18%) |
| No. of GCLKs | 1 (4%) |

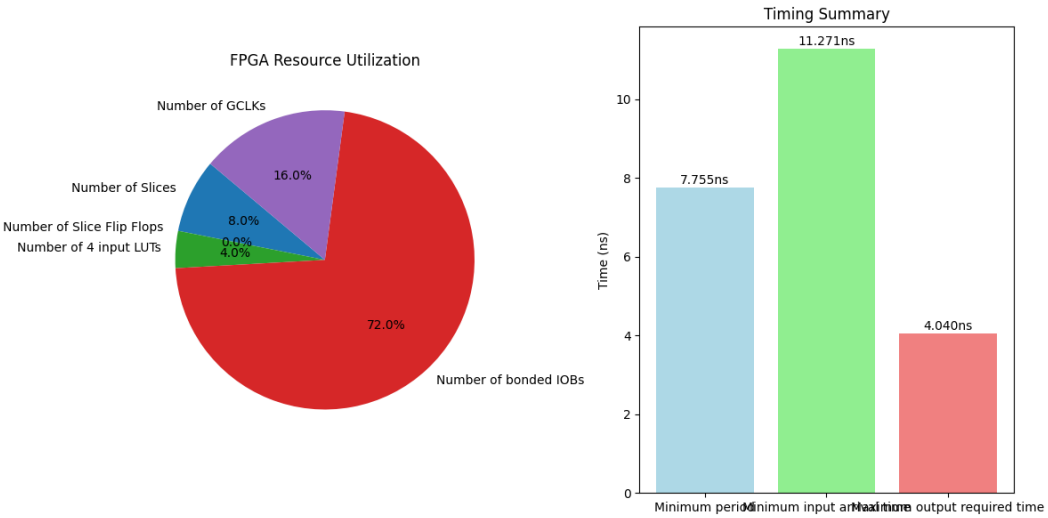


**Fig. 5** - Evaluation Parameters

## 6. Conclusion

In conclusion, Verilog HDL's development and analysis of the 8-Bit Arithmetic Logic Unit (ALU), along with a synchronised clock mechanism for automatic output validation, represent an innovative approach in digital circuit design. The clock module's integration has been essential in eliminating the need for human interaction in choosing operating modes, which has streamlined the validation procedure and guaranteed accuracy at the positive edge of each clock cycle. Furthermore, an in-depth examination of device utilisation and route delays was made possible by the careful application of Xilinx tools, which improved the efficiency and resource allocation of the ALU. The robustness and practical application of the developed ALU are confirmed by the successful implementation and execution of the Verilog HDL code on an FPGA, confirming its operation in a hardware environment.

The use of Xilinx tools allowed for an in-depth analysis of the ALU's device utilization and route delays, resulting in optimized efficiency and resource management. Specifically, the timing summary reveals:

- A minimum period of 7.755ns, corresponding to a maximum operational frequency of 128.955MHz. This indicates that the ALU can handle high-speed operations efficiently.
- A minimum input arrival time before the clock of 11.271ns, ensuring that input signals are adequately prepared before the clock edge.
- A maximum output required time after the clock of 4.040ns, demonstrating that the outputs are stable and available within a short time frame after the clock edge.

The device utilization summary provides further insights into the ALU's efficiency:

- The ALU uses 49 slices, which is just 2% of the available slices, indicating a very low resource consumption.
- It utilizes 14 slice flip-flops, amounting to 0% of the available flip-flops, highlighting minimal usage of these components.
- The ALU employs 91 four-input LUTs, which is 1% of the total available, showcasing efficient use of logic resources.
- It requires 30 I/Os and 30 bonded IOBs, which is 18% of the available bonded IOBs, reflecting moderate usage of input/output pins.
- The ALU uses 1 GCLK, accounting for 4% of the available global clock resources, indicating efficient clock resource utilization.

The successful implementation and execution of the Verilog HDL code on an FPGA validate the ALU's operational robustness and practical applicability in a hardware environment. These calculated numerical parameters demonstrate that the ALU operates reliably and effectively within the specified constraints, confirming its capability to perform high-speed arithmetic and logic operations with minimal resource consumption.

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