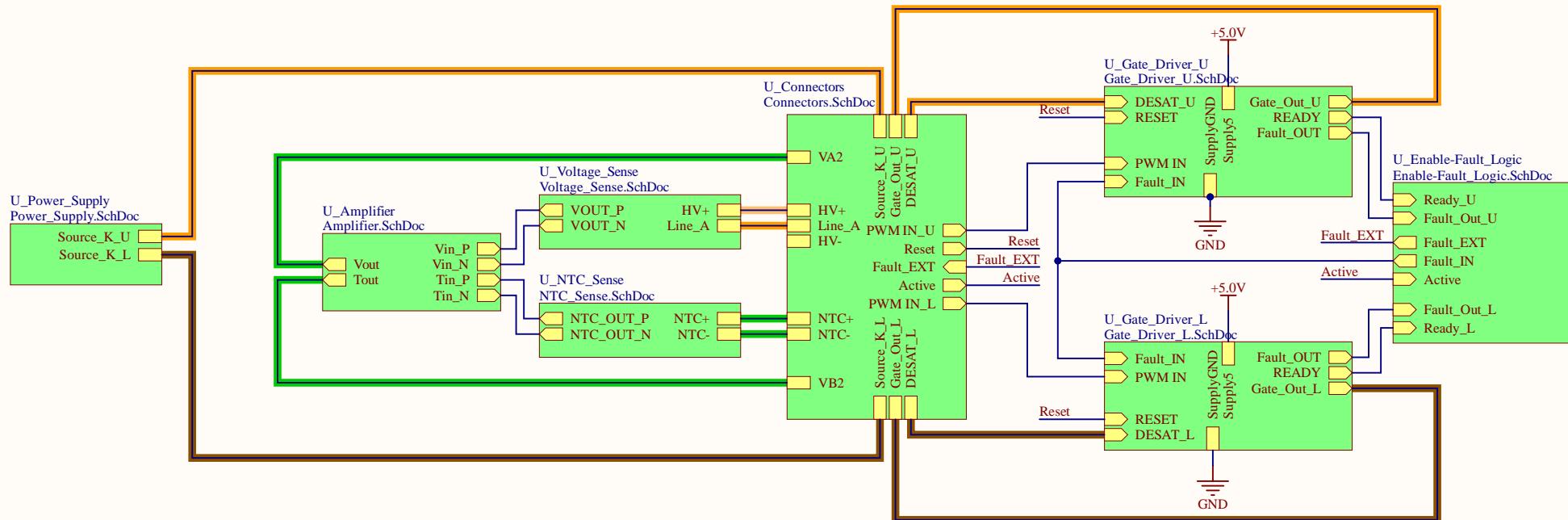
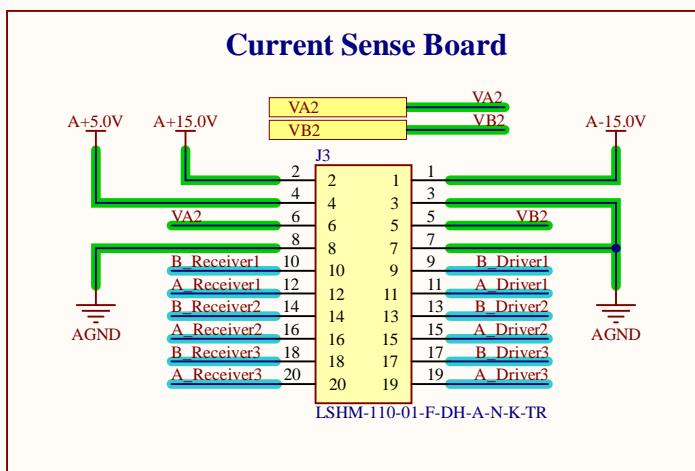
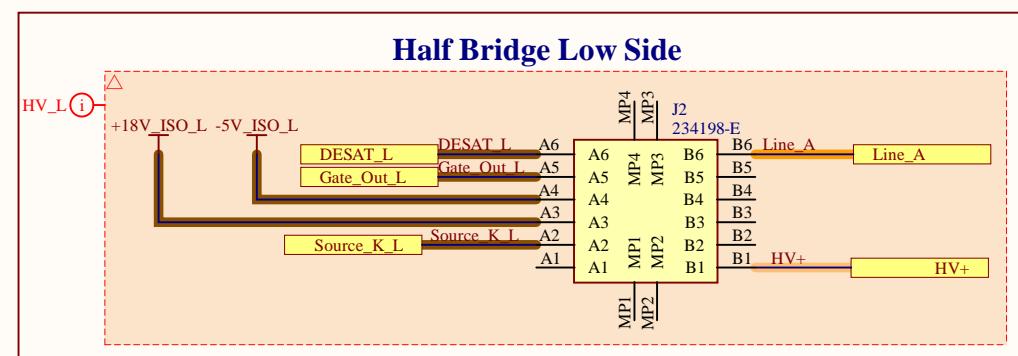
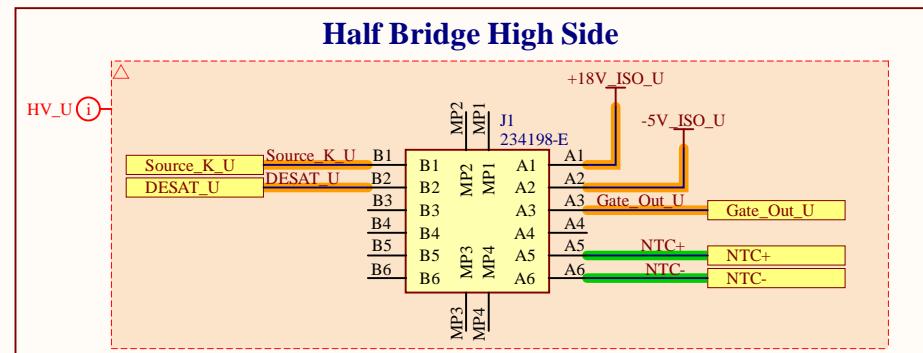
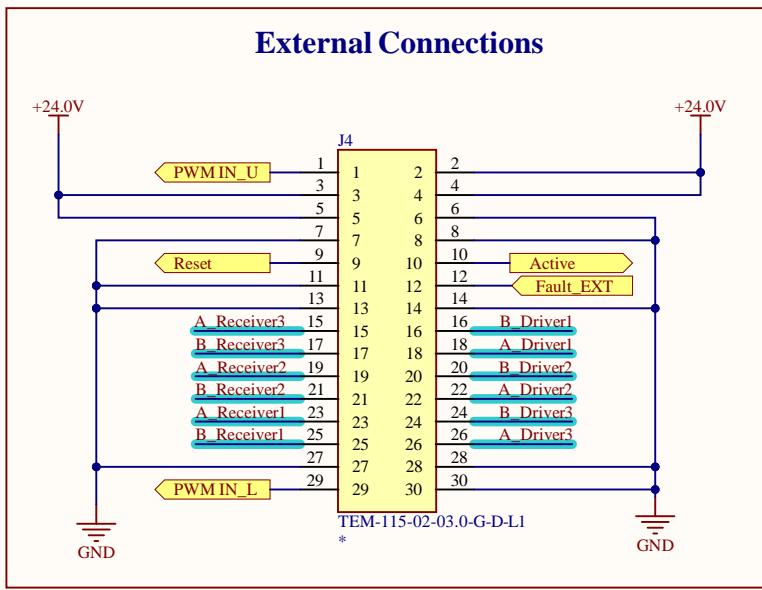


Driver Board



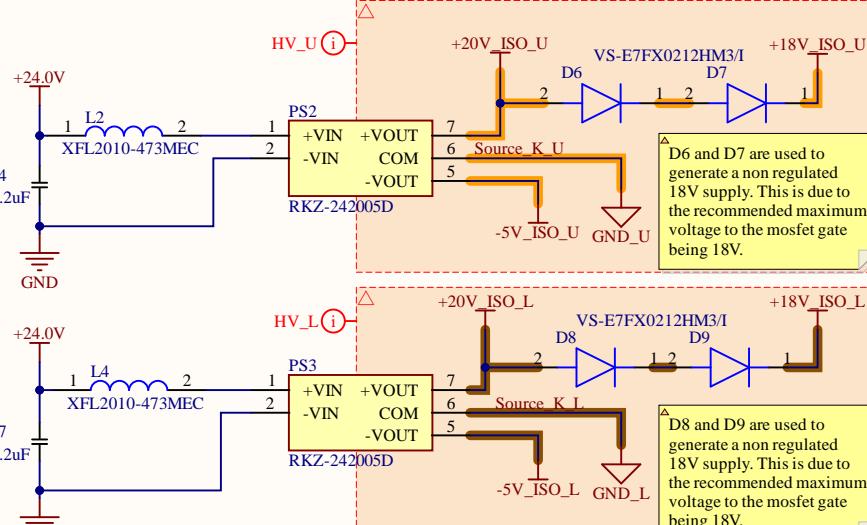
Connectors



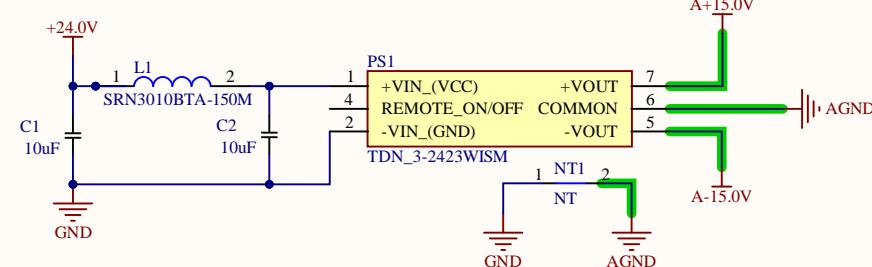
Power Supply

Source_K_U
Source_K_L

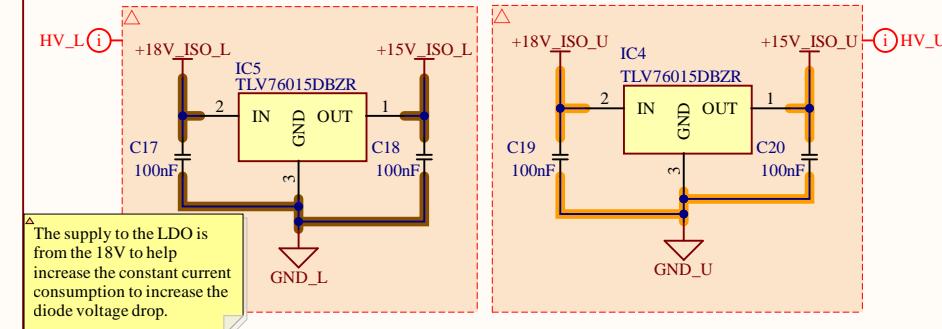
Gate Drivers DC/DC



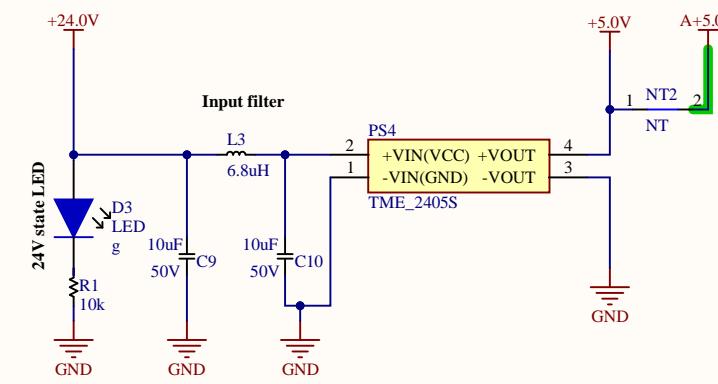
24V to +15V DC/DC



Isolation Amplifier LDOs



24V to 5V DC/DC



Gate Driver Low Side

A Inputs and Outputs

PWM_IN - Input of the PWM signal for the SiC Driving
 Supply5 - 5 Volt Supply for the Insulated DC/DC's
 SupplyGND - Ground Reference for 24 Volt and 5 Volt Supplies
 FAULT_IN - Fault Signal that results from the OR of all fault signals
 FAULT_OUT - Fault signal generated by this gate driver
 RESET - Input signal to reset the gate driver after a desaturation error
 RDY - Output signal that states the gate driver is ready to operate
 Gate_Out_L - Gate control output (Lower)
 DESAT_L - Desaturation sense, from the mosfet source (after the voltage protection diode)



The protection diode against the source voltage is placed on the half bridge PCB. It has a forward voltage drop of 1V@25°C and 0.87V@125°C.

The module maximum continuous current is 90A@175°C V_J, with a repetitive peak of 200A.

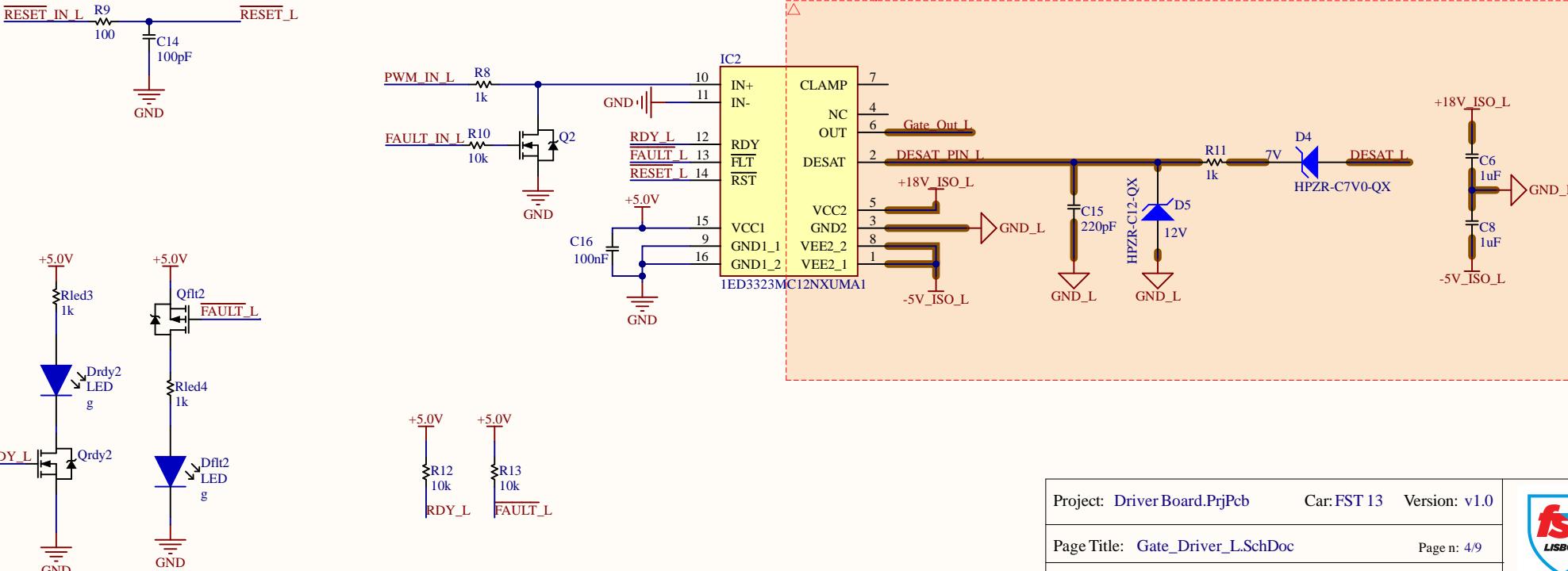
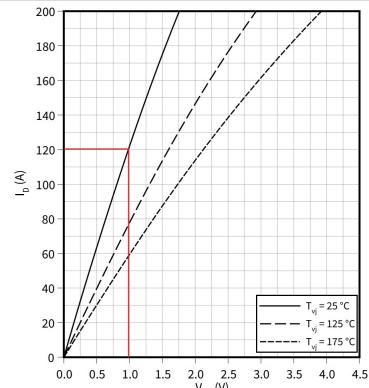
The gate driver desat threshold voltage is 9V. The zener diode D1 is set to 7V so that a safety margin is present for the initial tests, this should probably be reduced to 6V later if the desaturation protection triggers under full torque.

The blanking capacitor and resistor are set according to the datasheet.

D2 is only a pin protection against overvoltage, it can be replaced by other 12V zeners.

B Output characteristic (typical), MOSFET

$I_D = f(V_{DS})$
 $V_{GS} = 18\text{ V}$



Gate Driver High Side

Inputs and Outputs

PWM_IN - Input of the PWM signal for the SiC Driving

Supply5 - 5 Volt Supply for the Insulated DC/DC's

SupplyGND - Ground Reference for 24 Volt and 5 Volt Supplys

FAULT_IN - Fault Signal that results from the OR of all f

FAULT_OUT - Fault signal generated by this gate driver

RESET - Input signal to reset the gate driver

RDY - Output signal that states the gate driver is ready to operate



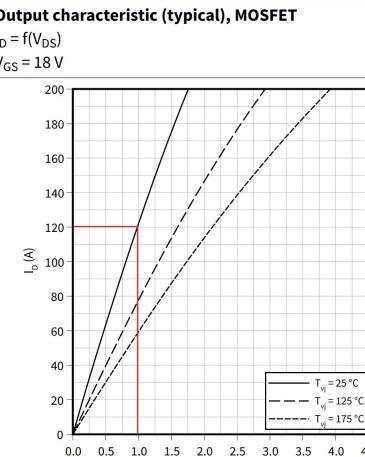
The protection diode against the source voltage is placed on the half bridge PCB. It has a forward voltage drop of $1V@25^{\circ}\text{C}$ and $0.87V@125^{\circ}\text{C}$.

The module maximum continuous current is 90A@175°C V_j, with a repetitive peak of 200A.

The gate driver desat threshold voltage is 9V. The zener diode D1 is set to 7V so that a safety margin is present for the initial tests, this should probably be reduced to 6V later if the desaturation protection triggers under full torque.

The blanking capacitor and resistor are set according to the datasheet.

D2 is only a pin protection against overvoltage, it can be replaced by other 12V zeners.



The diagram illustrates the circuitry for the Gate Driver Unit. It features a central integrated circuit (IC1) labeled **IED3323MC12NXUMA1**, which is highlighted by a dashed orange box. The IC has several pins connected to external components:

- Pin 10:** PWM_IN_U connected to R2 (1k) and GND.
- Pin 11:** GND.
- Pin 12:** RDY_U connected to Q1 (NPN transistor).
- Pin 13:** FAULT_U connected to R4 (10k) and GND.
- Pin 14:** RESET_U connected to C11 (100pF) and GND.
- Pin 15:** +5.0V connected to C13 (100nF) and GND.
- Pin 16:** GND.
- Pin 7:** CLAMP connected to HV_U (indicated by a red circle with 'i').
- Pin 4:** IN+ connected to GND.
- Pin 6:** Gate_Out_U connected to D1 (7V, 1k) and GND_U.
- Pin 2:** DESAT_PIN_U connected to D2 (12V, 220pF) and GND_U.
- Pin 5:** VCC2 connected to +18V_ISO_U.
- Pin 3:** GND2 connected to GND_U.
- Pin 8:** VEE2_2 connected to -5V_ISO_U.
- Pin 1:** VEE2_1 connected to GND_U.

Other components include a diode D1 (7V, 1k), a diode D2 (12V, 220pF), and capacitors C11 (100pF), C12 (220pF), C3 (1uF), and C5 (1uF). The circuit also includes logic gates Q1, Q2, and Q3, and LEDs Dled1, Dled2, Dfault1, and Dfault2. Power supplies +5.0V, +18V_ISO_U, and -5V_ISO_U are shown along with ground connections.

Project: Driver Board PriBob

Car-FST 1.3 Version: v1.0

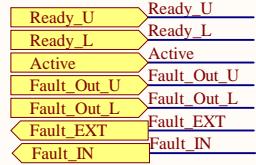


Page Title: Gate Driver U.SchDoc

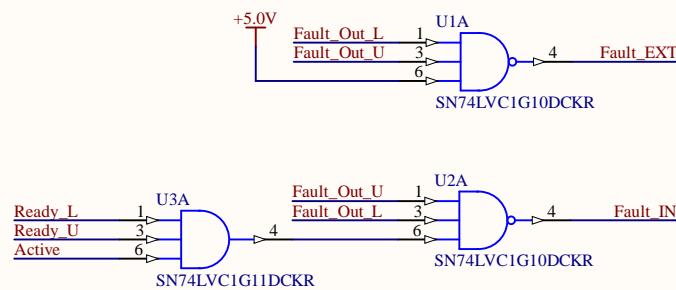
Page n: 5

Author: Israel Sother

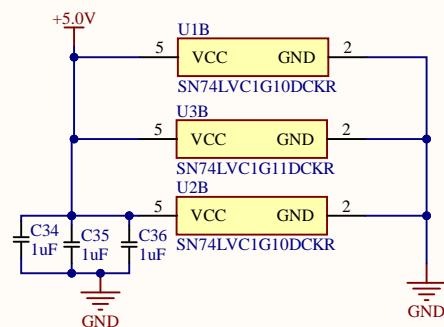
Date: 5/20/2024



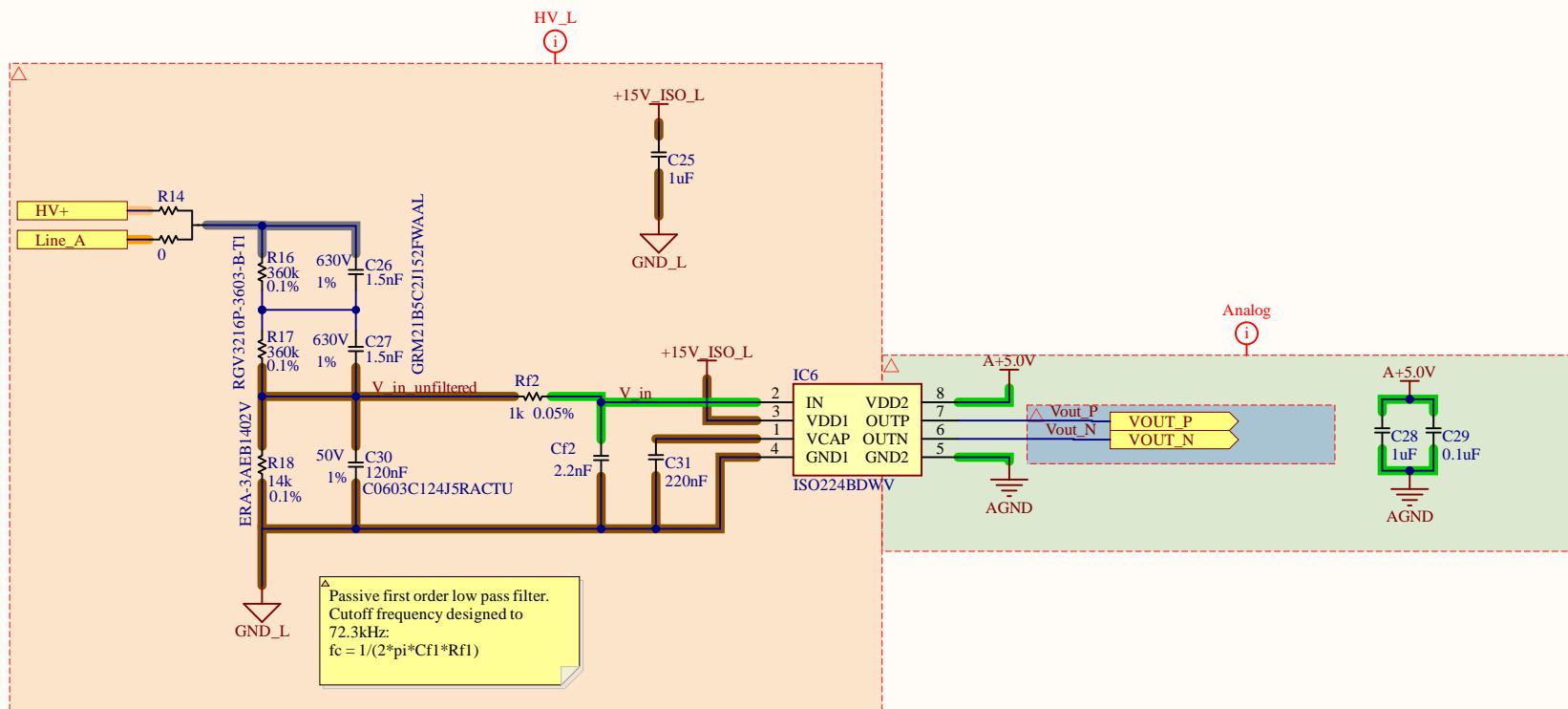
Enable Logic



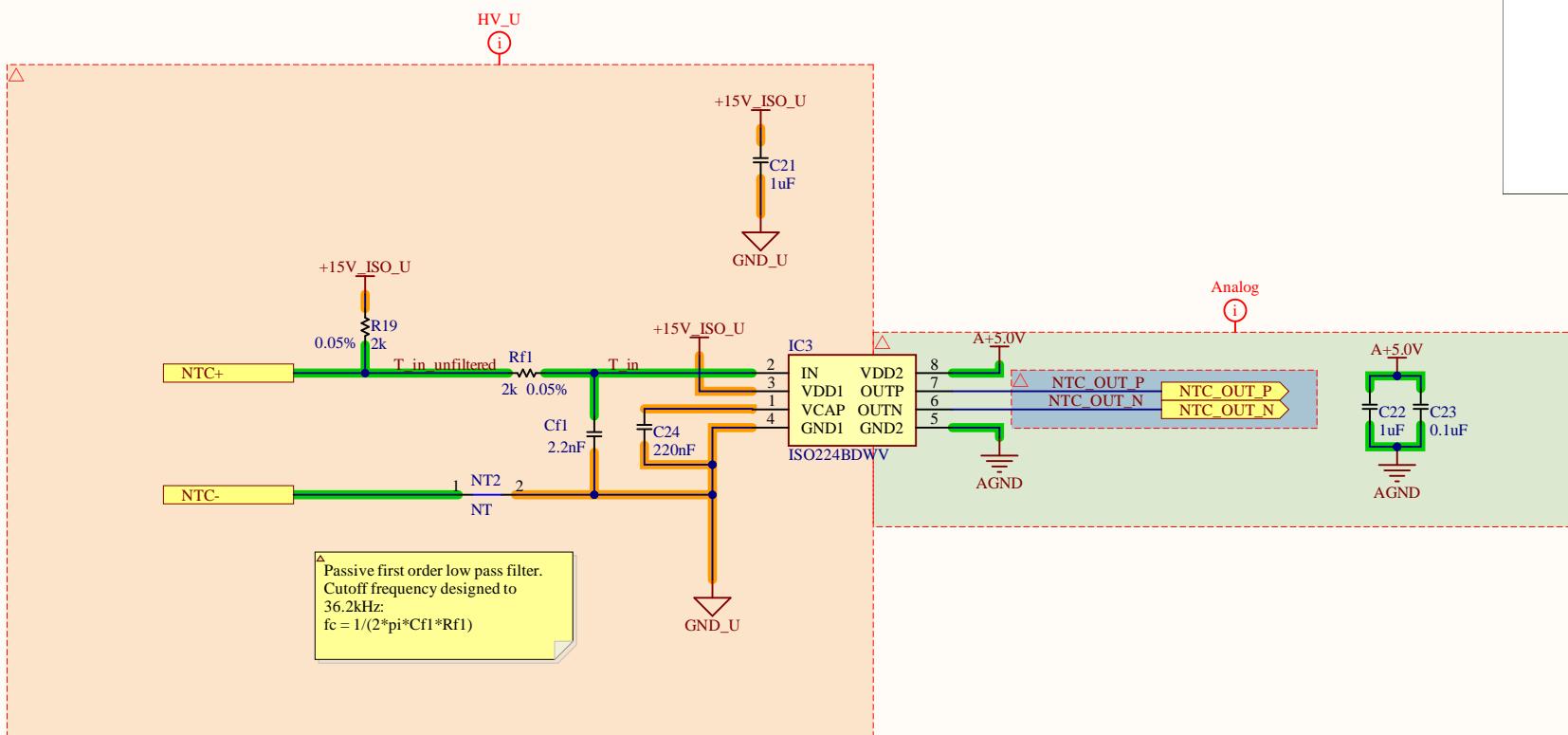
△ **Fault_EXT** signals the controller if the module is at fault or not, while the **Active** enables or disables the module by the **Fault_IN** signal.



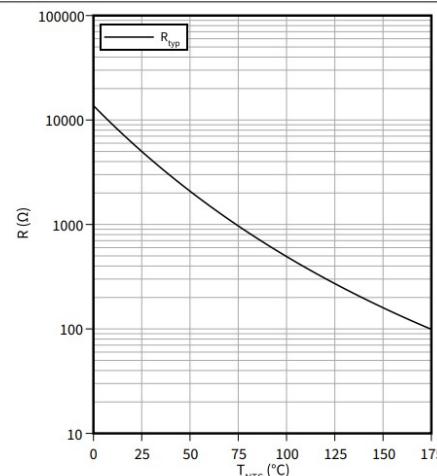
Voltage Sense



NTC Sense



Temperature characteristic (typical), NTC-Thermistor
 $R = f(T_{NTC})$



Signal Amplifier

