JOINT INSTITUTE
交大密西根学院

Ve270 Introduction to Logic Design

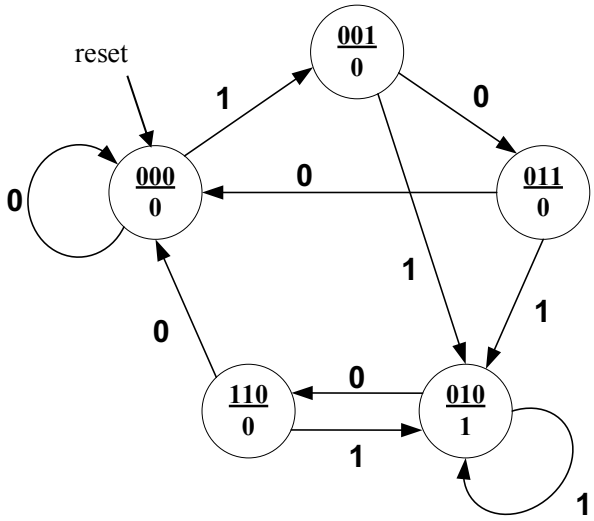
Homework 8

Assigned: July 11, 2019

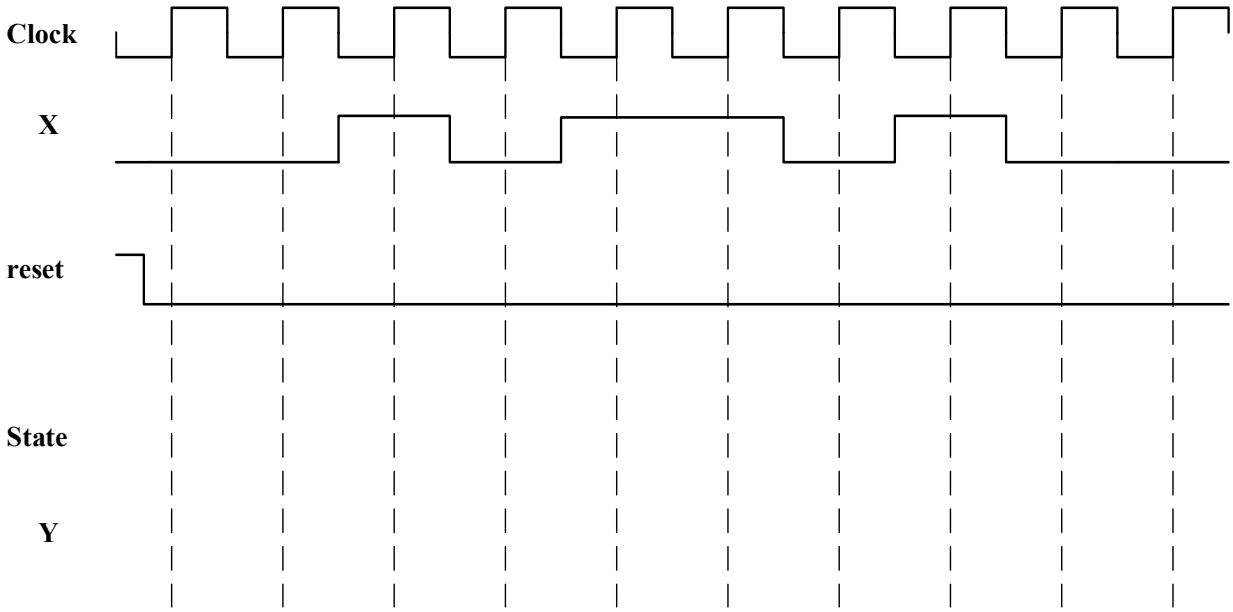
Due: July 18, 2019, 2:00pm.

The homework should be submitted in hard copies.

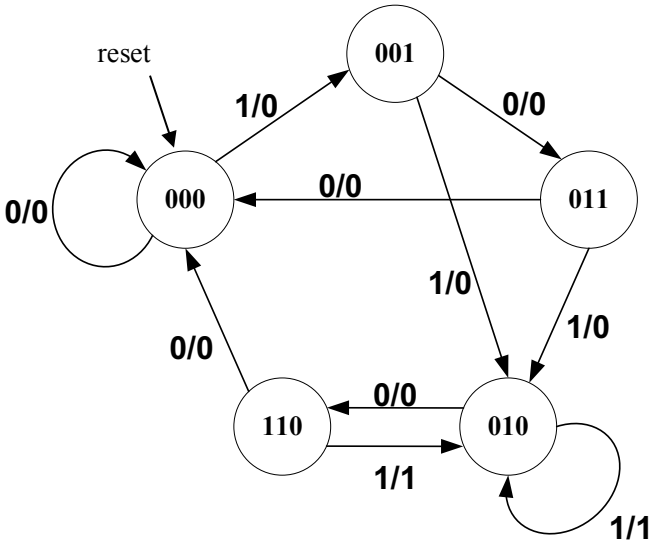
1. Design a finite state machine described by the following state diagram using D type flip flops. The state machine has one input X and one output Y. (30 Points)

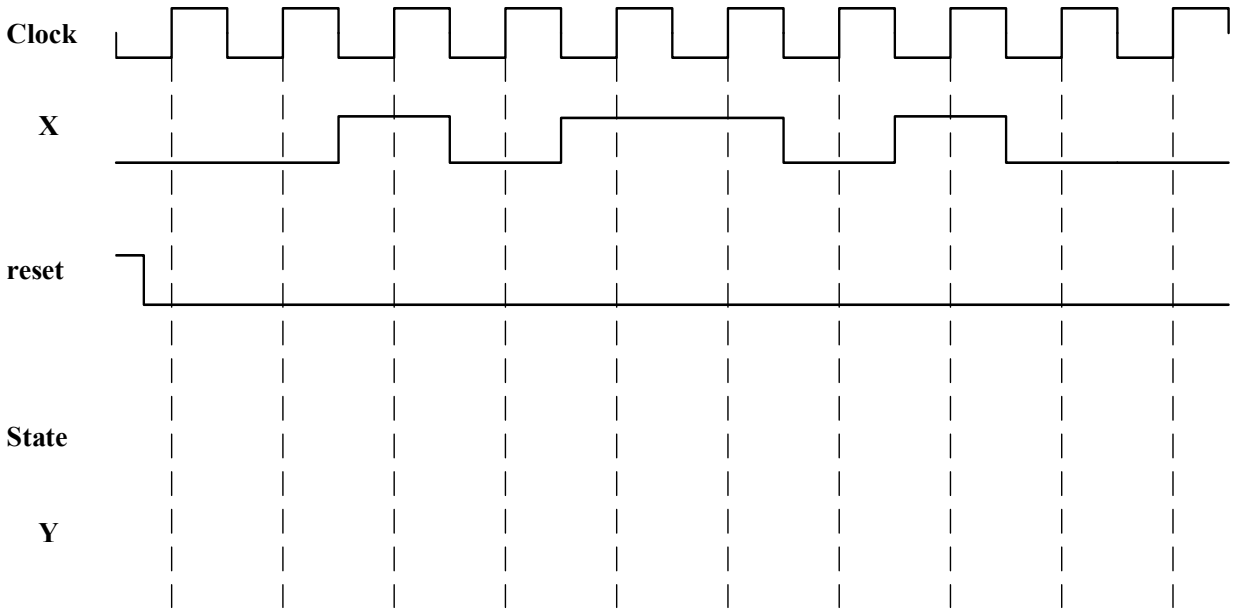


(a). Create a state table and find equations for the next state and FSM outputs.
(b). Complete the timing diagrams of states and output **Y** according to the given inputs.
(c). Is the FSM self-starting? If not, make it a self-starting FSM.



2. Repeat the same questions as Problem 1 on the following state diagram. (30 Points)





3. Problem 6.17, using implication table method (20 Points)

6.17 Reduce the number of states for the FSM in Figure 6.90

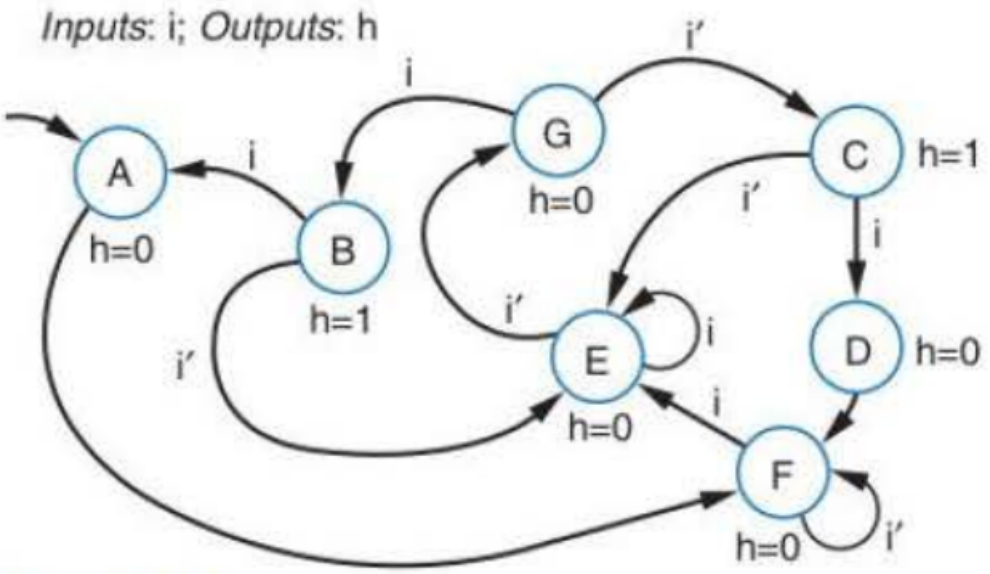


Figure 6.90 FSM example.

4. Problem 6.18 (assuming the next state of S3 is S0) (20 Points)

6.18 Compare the logic size (number of gate inputs) and the delay (number of gate-delays) of a straightforward 2-bit binary encoding of the FSM in Figure 6.91 using a 3-bit output encoding versus using a one-hot encoding.

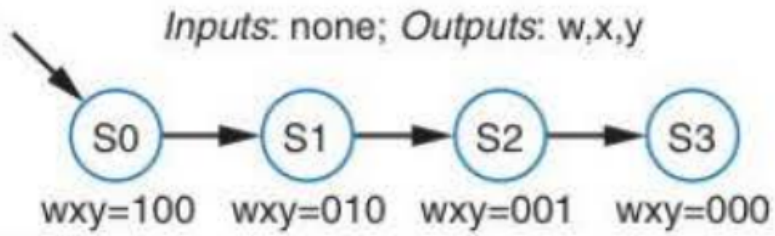


Figure 6.91 FSM example.