JOINT INSTITUTE
交大密西根学院

Ve270 Introduction to Logic Design

Homework 4

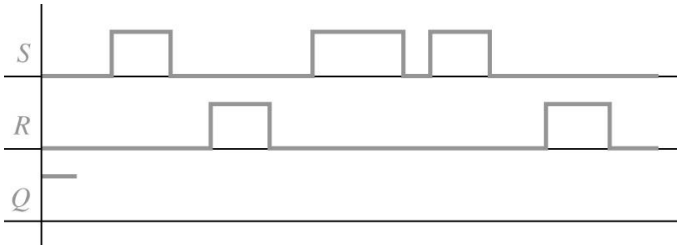
Assigned: June 6, 2019

Due: June 13, 2019, 2:00pm.

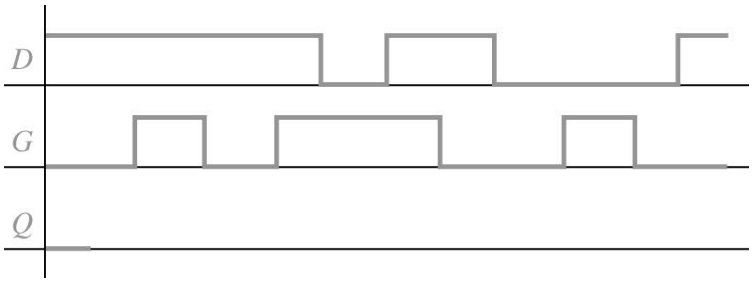
The homework should be submitted in hard copies.

***Note**: you may ignore the gate delay when drawing a timing diagram unless required differently.*

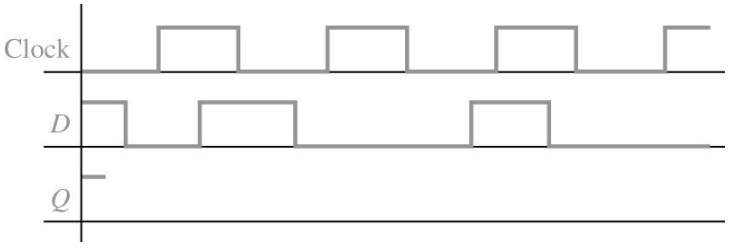
1. (10 points) Complete the following timing diagram for an SR latch. Assume Q begins at 1.



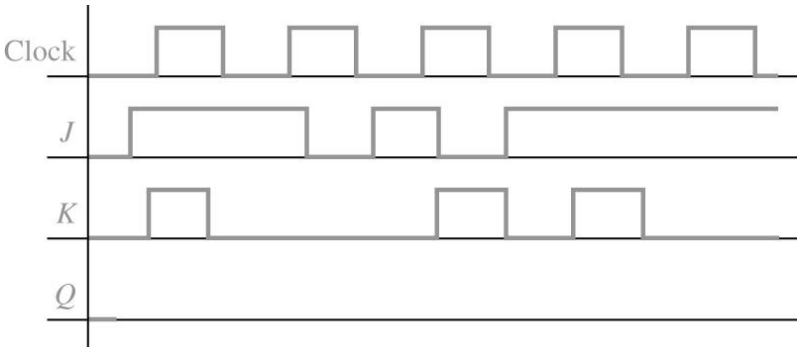
2. (10 points) Complete the following timing diagrams for a gated D latch. Assume Q begins at 0.



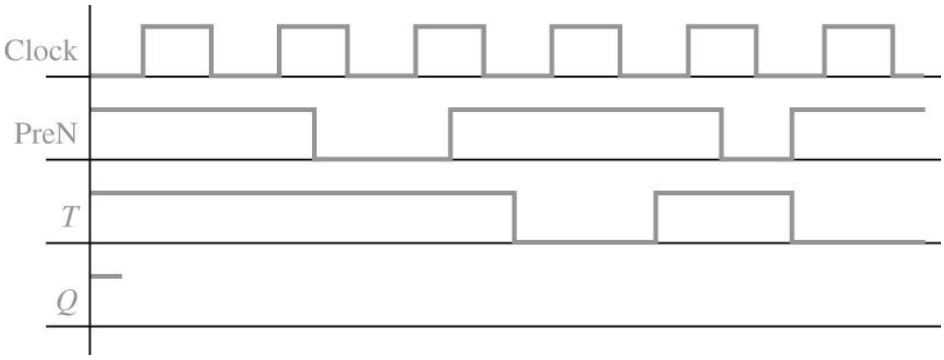
3. (10 points) Complete the following diagrams for the rising-edge triggered D flip-flop. Assume Q begins at 1.



4. (10 points) Fill in the timing diagram below for a falling-edge triggered J-K flip-flop. Assume Q begins at 0.



5. (15 points) Fill in the following timing diagram for a rising-edge triggered T flip-flop with an asynchronous active-low preset input (PreN, equivalent to set). Assume Q begins at 1.



6. (15 points) Design a 4-bit register with an enable signal "EN", such that when EN = 0, nothing can be loaded into the register, and when EN = 1, the register works as normal.
7. (15 points) Problem 3.19. Draw schematic.

3.19 Using four registers, design a circuit that stores the four values present at an 8-bit input D during the previous four clock cycles. The circuit should have a single 8-bit output that can be configured using two inputs s1 and s0 to output any one of the four registers. (Hint: use an 8-bit 4x1 mux.)

8. (15 points) Problem 3.20.

3.20 Consider three 4-bit registers connected as in Figure 3.103. Assume the initial values in the registers are unknown. Trace the behavior of the registers by completing the timing diagram of Figure 3.104.

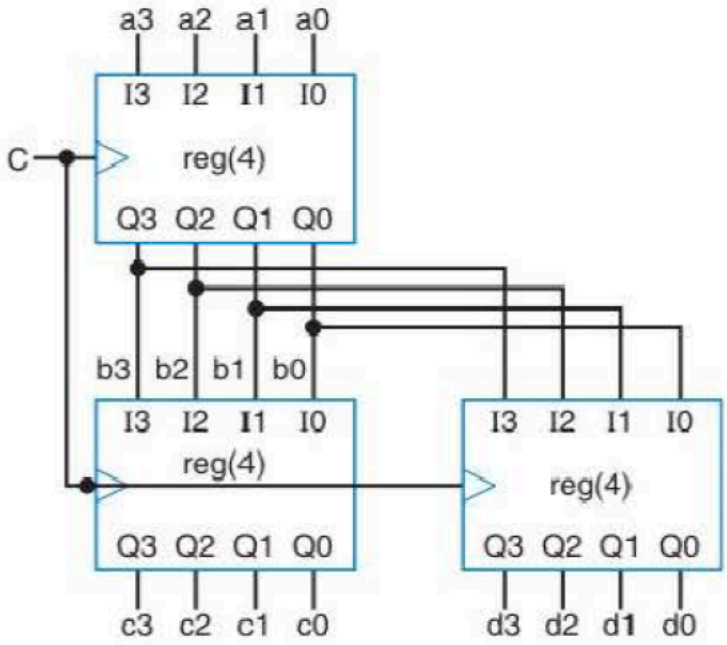


Figure 3.103 Register configuration.

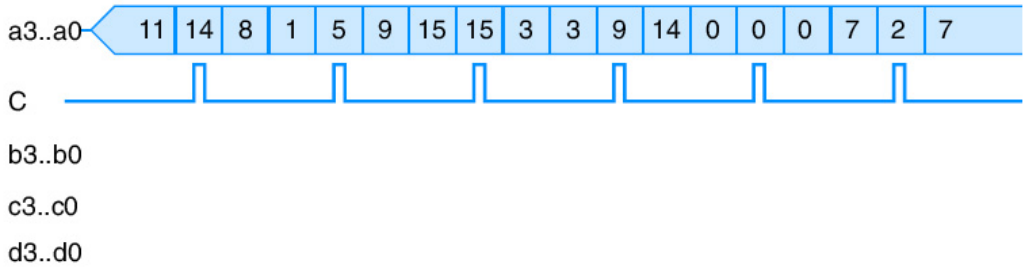


Figure 3.104 4-bit register input pattern timing diagram.