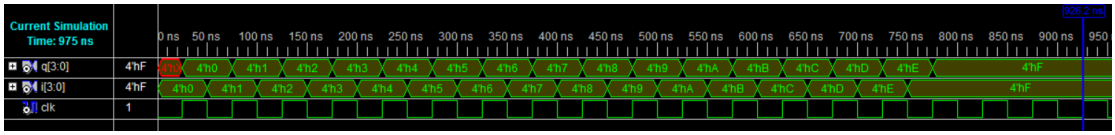
HW5 Report

Q1. (IF Q1 is “Describe a 4-bit register in Verilog. Simulate your Verilog module.”)

Verilog Code:

```
21  module Q1(i, o, clk);
22     input [3:0] i;
23     input clk;
24     output [3:0] o;
25     reg [3:0] o;
26     always @(posedge clk) begin
27        o<=i;
28     end
29  endmodule
```

Simulation Result:



// (Make sure all the characters in the figure are still visible)

Q2.

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