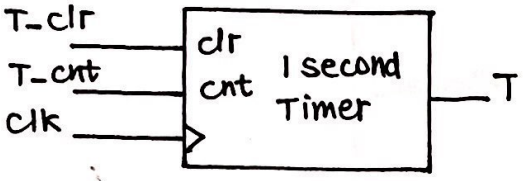
Prob1.

Specify the timer to use in the exercise.

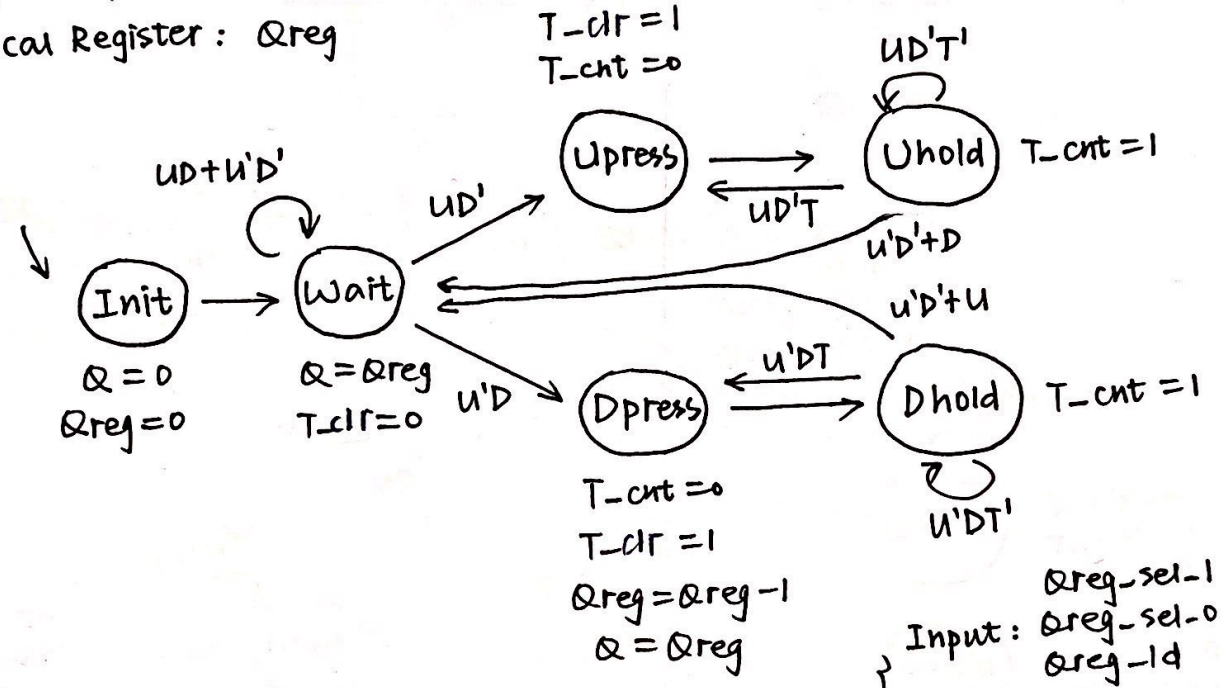


Step 1. Capture the HLSM :

Output : T_clr, T_cnt, Q

Input : T, U, D

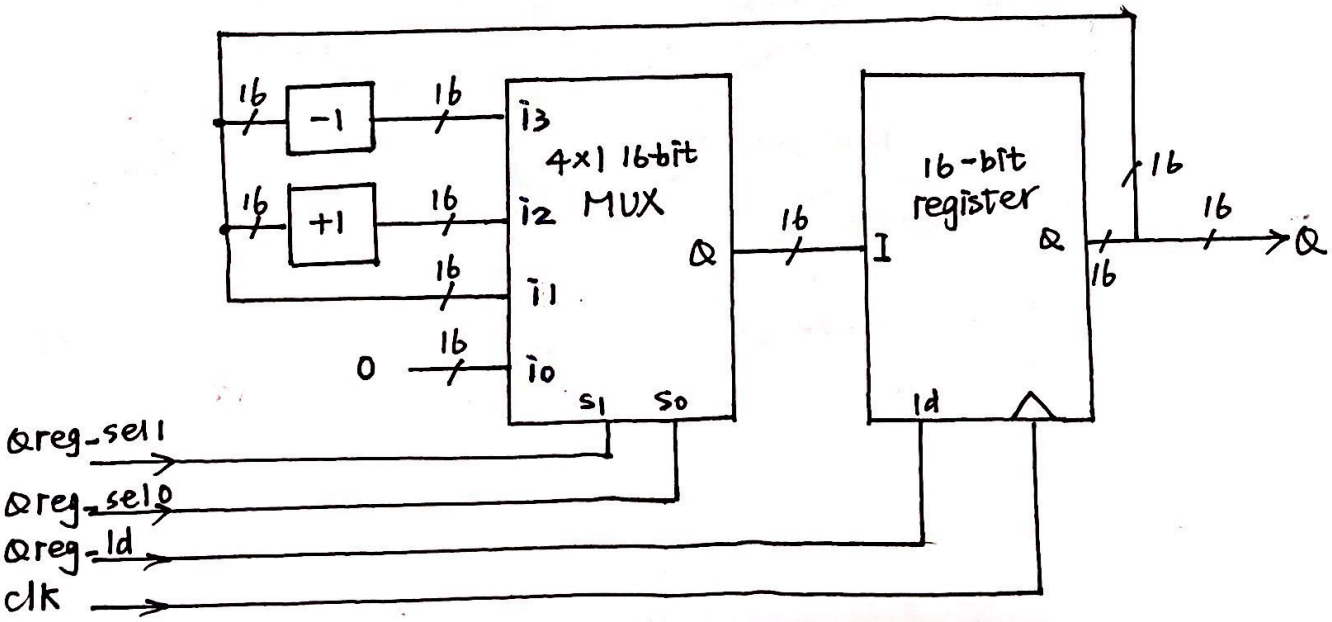
Local Register : Qreg

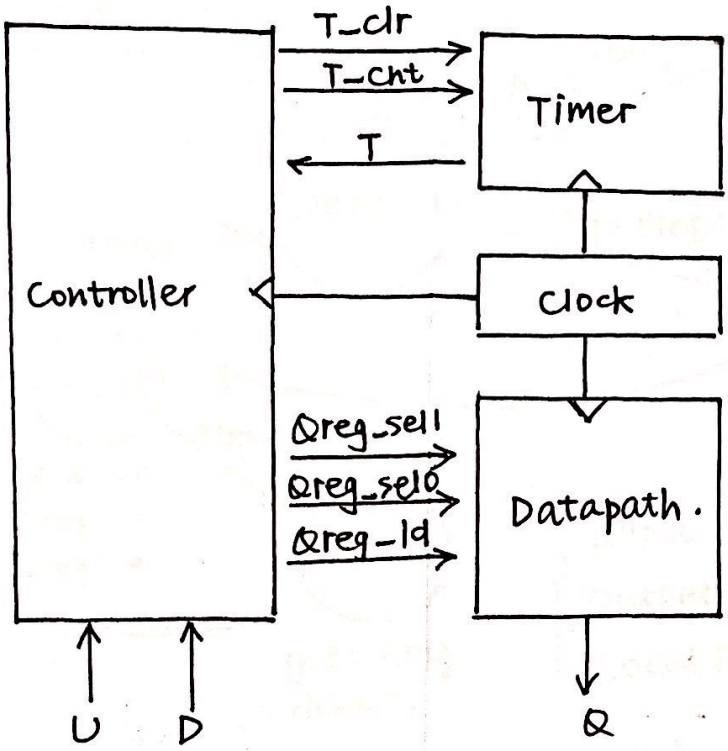


Input : Qreg_sel_1, Qreg_sel_0, Qreg_ld

Output : Q

Step 2. Design the datapath .

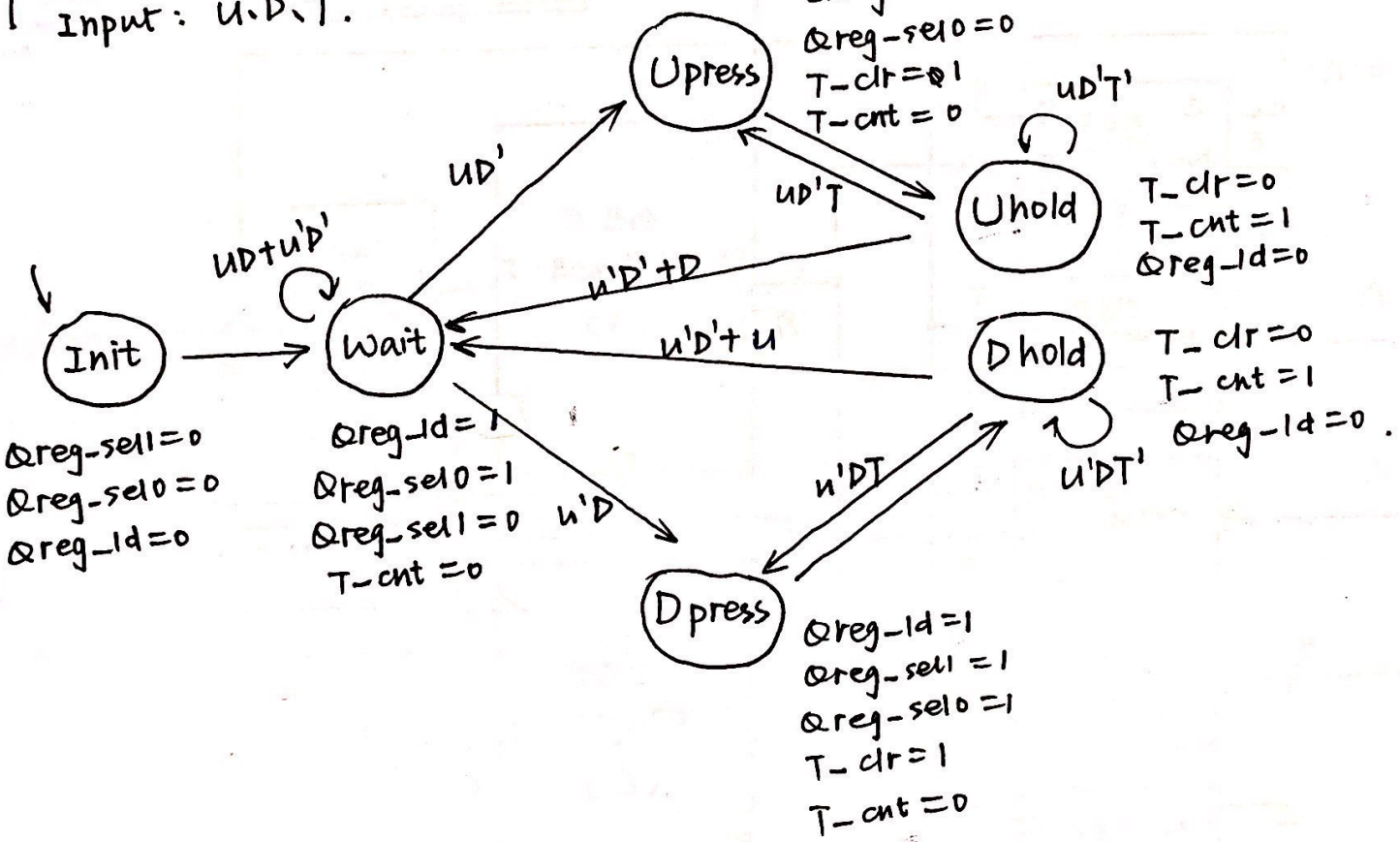




Step 4. Capture the FSM.

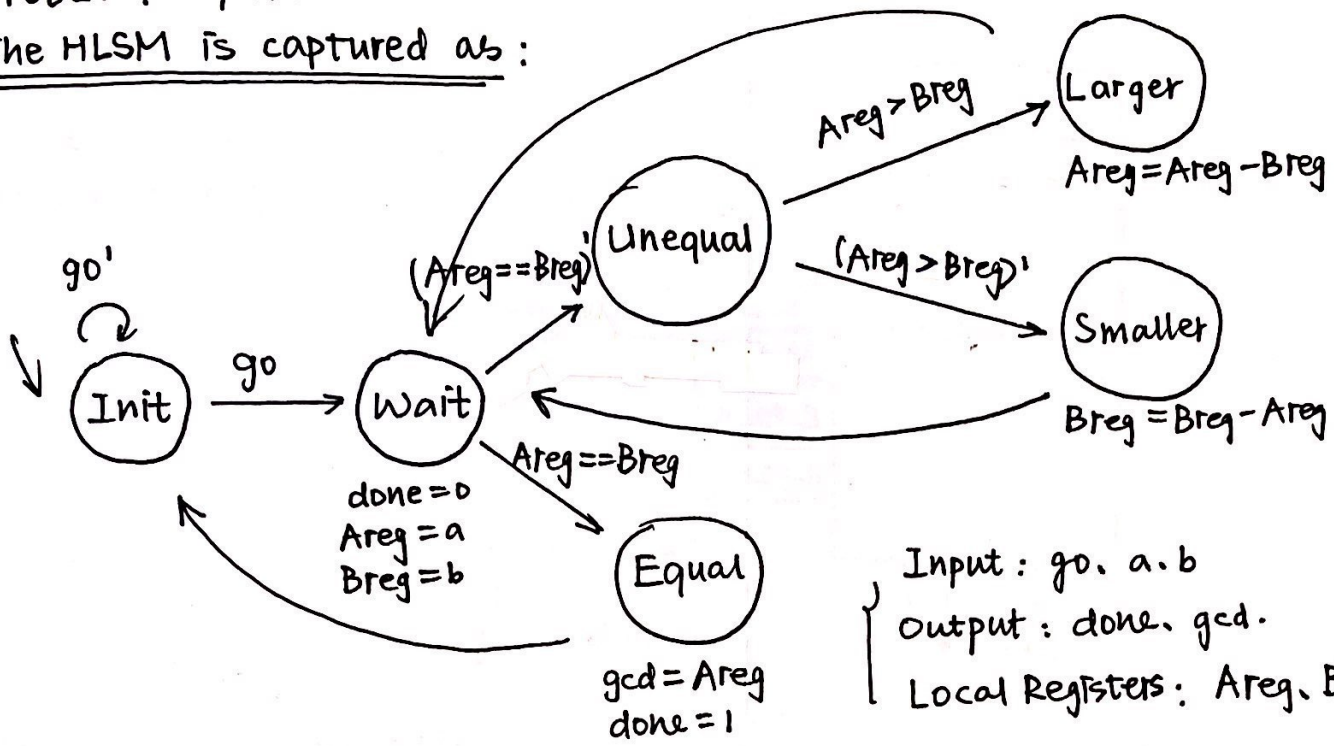
Output: T_cnt、T_clr、Qreg_sel_1、Qreg_sel_0、Qreg_ld.

Input: U、D、T.



Prob2. (Step 1).

The HLSM is captured as:



Input: go, a, b

Output: done, gcd.

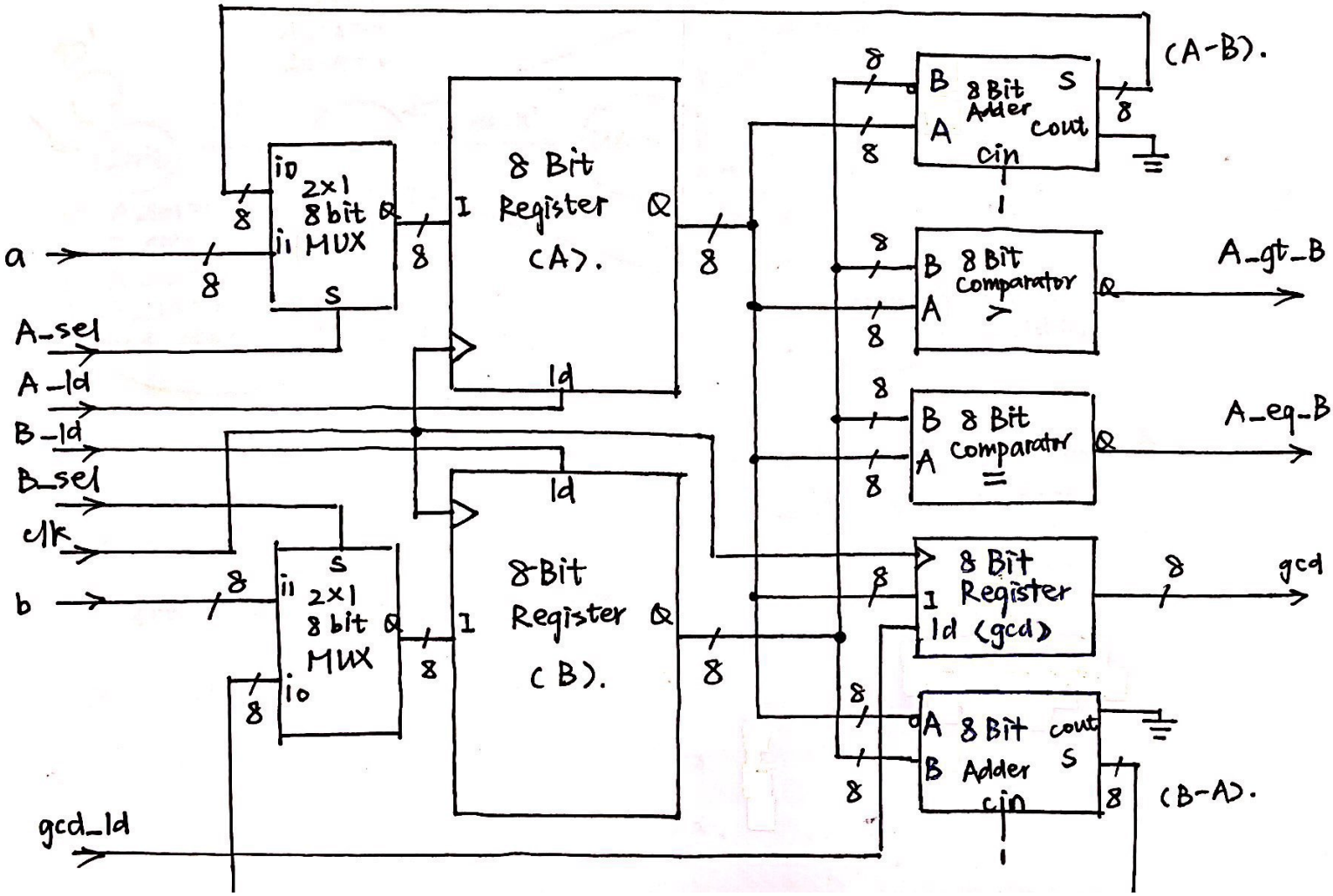
Local Registers: Areg, Breg.

Prob 3.

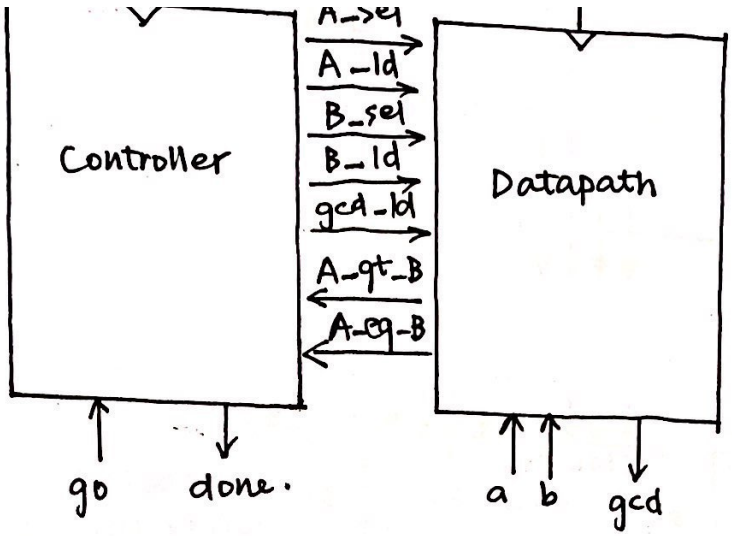
Step 2. Design the datapath.

Input: a, b, gcd_ld, A_sel, A_ld, B_sel, B_ld

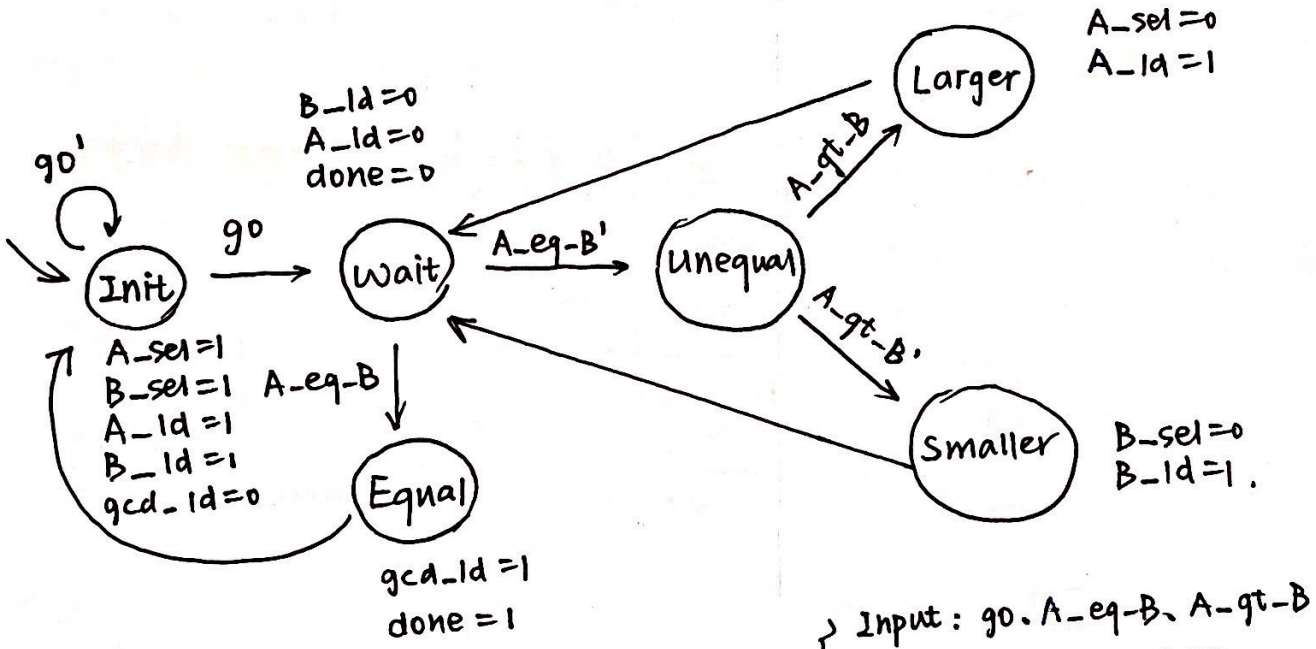
Output: gcd, A_gt_B, A_eq_B,



Output: done、gcd.



Step 4. Capture the FSM.



Input: go、A_eq_B、A_gt_B
Output: gcd_ld, done
A_sel、A_ld
B_sel、B_ld

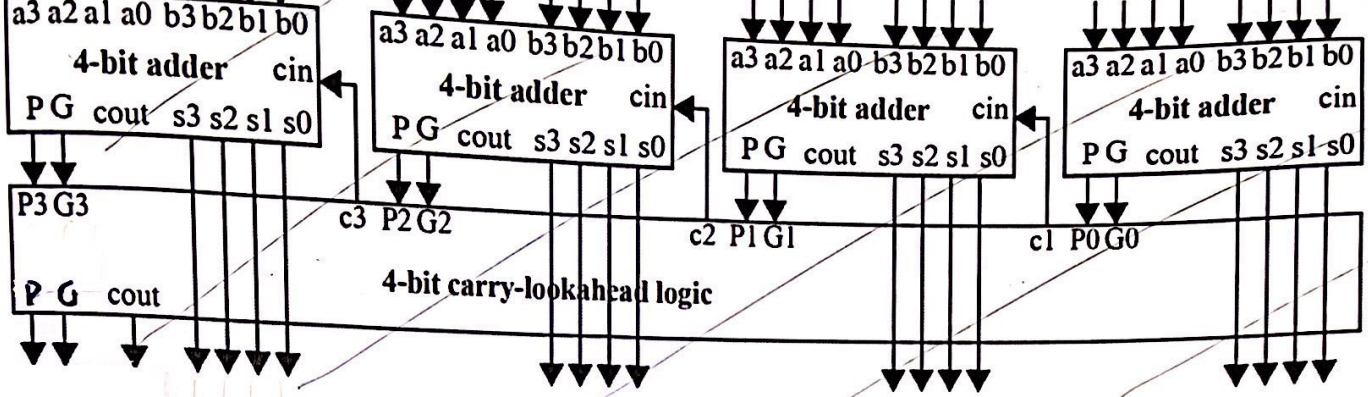
Prob 4.

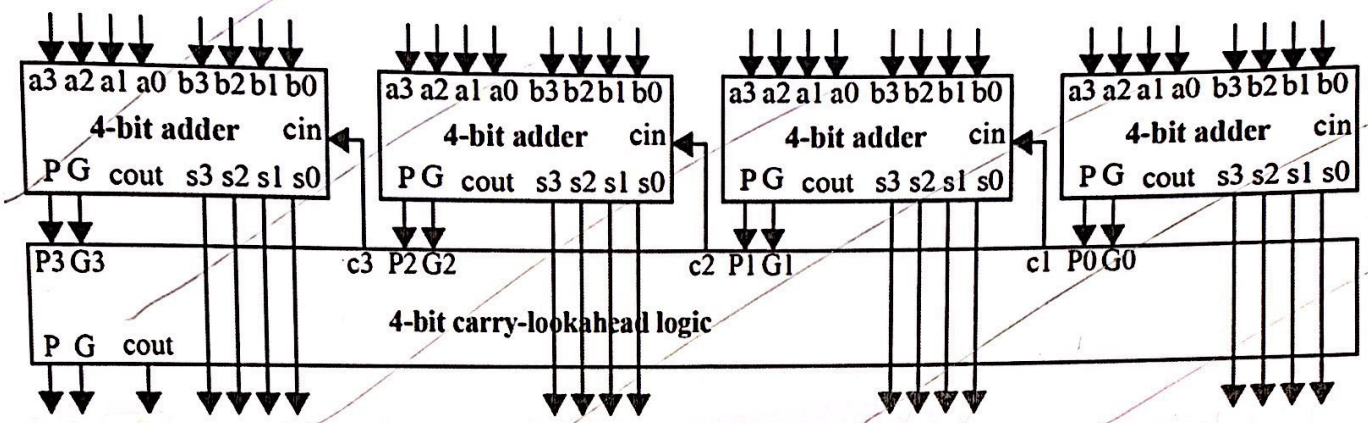
First convert the decimals into binary.

$a = (43690)_{10} = (1010\ 1010\ 1010\ 1010)_2$

$b = (21845)_{10} = (1010\ 1010\ 1010\ 101)_2$

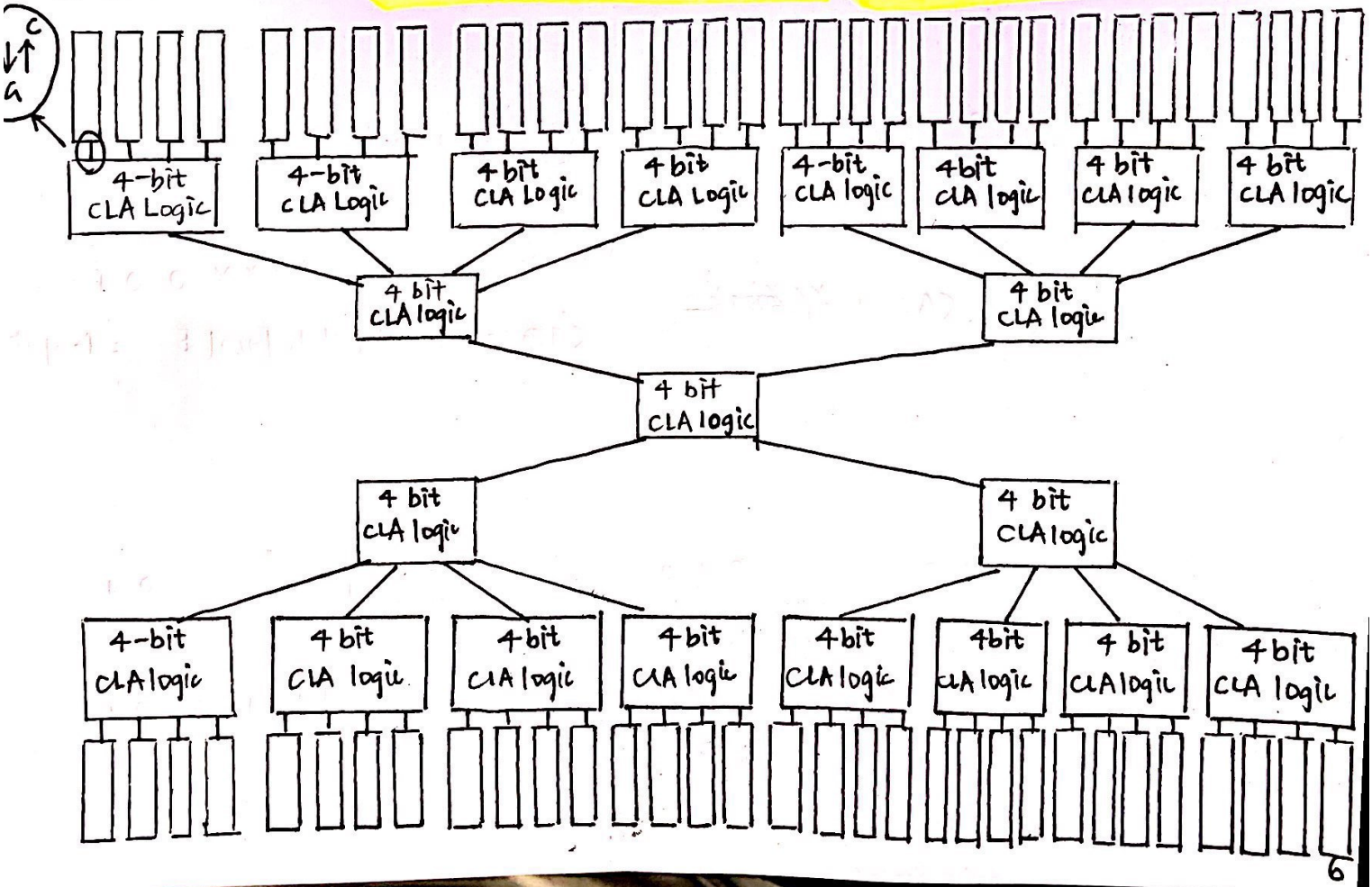
$= (0101\ 0101\ 0101\ 0101)_2$.





Prob 5. (a). The design is as follows.

Note: Each line —— stands for $\overset{P}{\underset{c}{\rightleftharpoons}}$ G, ▯ stands for SPG block.



(b). 12 gate delays.

2 : SPG block is 2-gate delay

2*5 : 3 levels of CLA logic, and
2 gate delays each, 2*3-1 = 5 calculations.

2+2×5 = 12.

(c). 10.7 times.

Carry Ripple adder :

64 full adders, 2 gate delays each.

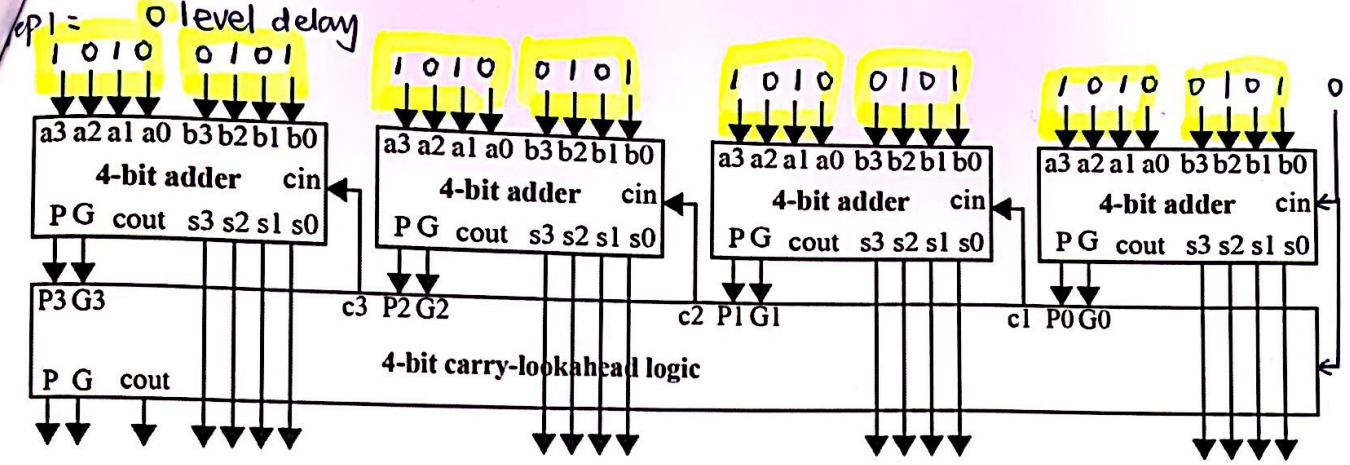
2×64 = 128.

Hence,

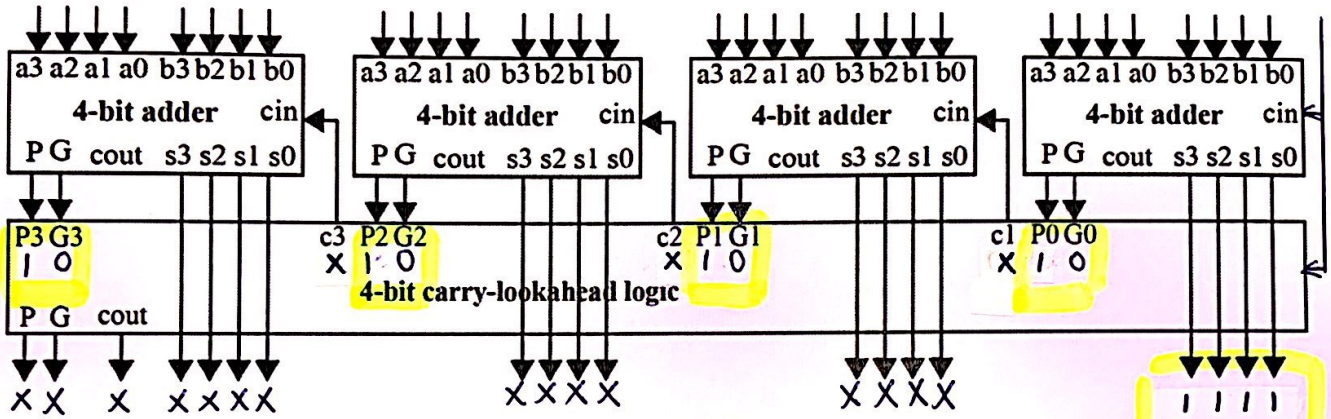
$$\text{speedup} = \frac{\text{slower}}{\text{faster}}$$

$$= \frac{128}{12}$$

$$= 10.7$$

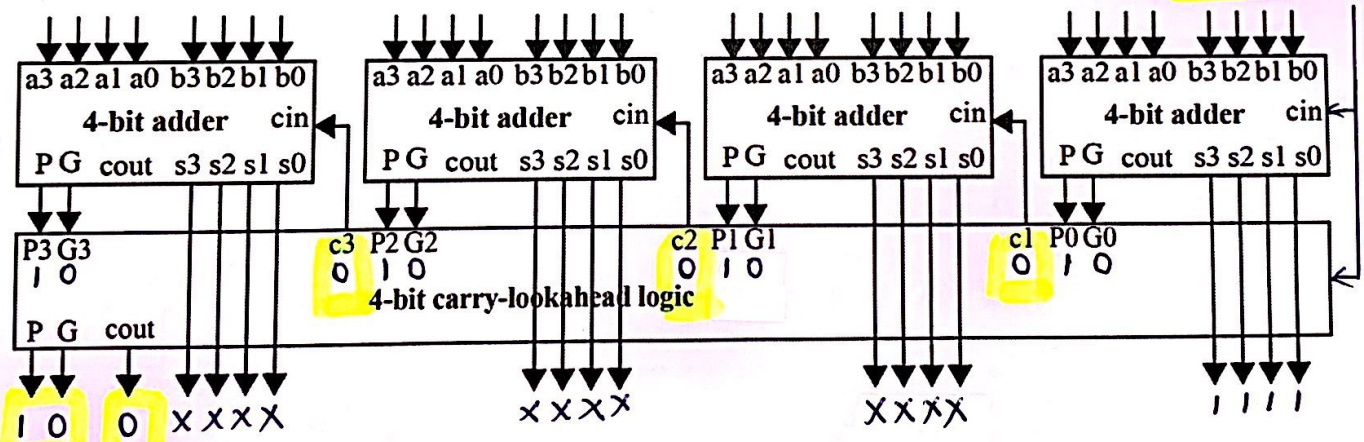


step2 = 3 level delay (1 from HA, 2 from internal CLA).

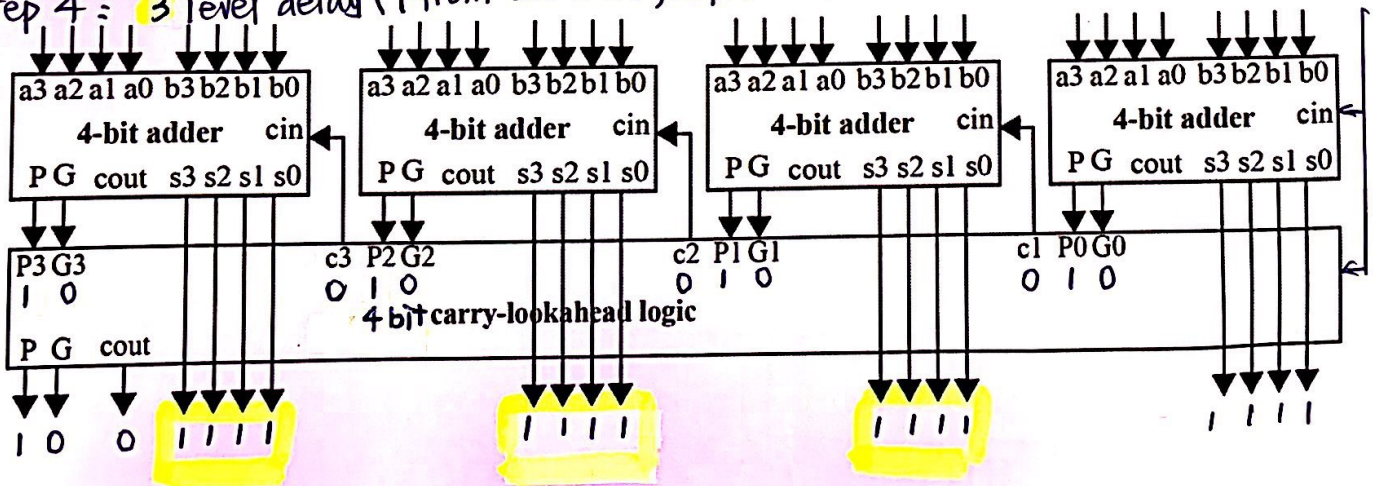


step 3 = 2 level delay (from external CLA).

(At 2 level delay)



step 4 = 3 level delay (1 from $s = c \oplus P$, 2 from internal CLA).



(In total = 8 levels).