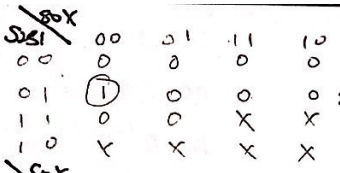
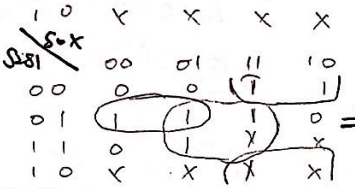
Present State			X	Next State			Y
S_2	S_1	S_0		n_2	n_1	n_0	
0	0	0	0	0	0	1	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	1	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	1	0
0	1	0	1	1	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	1	0	0	0
1	0	0	0	1	0	1	0
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

For n_2.



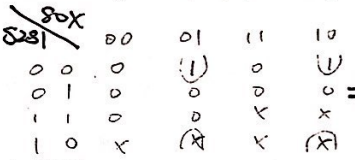
$\Rightarrow n_2 = S_2'S_1S_0'X'$

For n_1



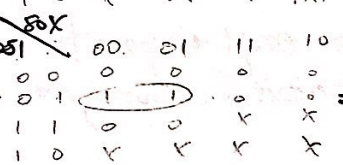
$\Rightarrow n_1 = S_2'S_1S_0' + S_1X + S_1'S_0$

For n_0

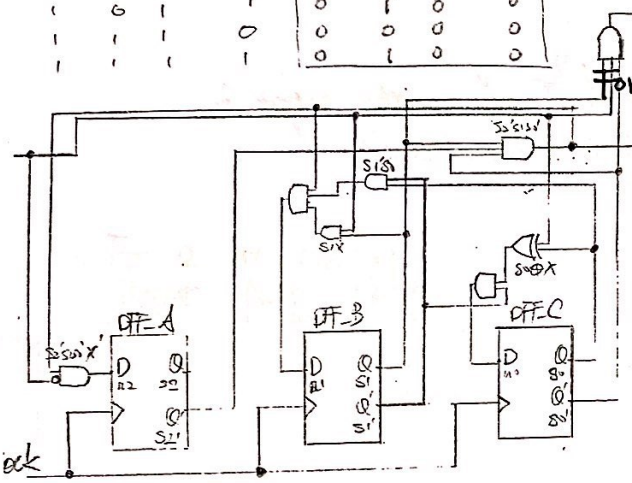


$\Rightarrow n_0 = S_1'S_0'X + S_1'S_0X'$
$= S_1'(S_0 \oplus X)$

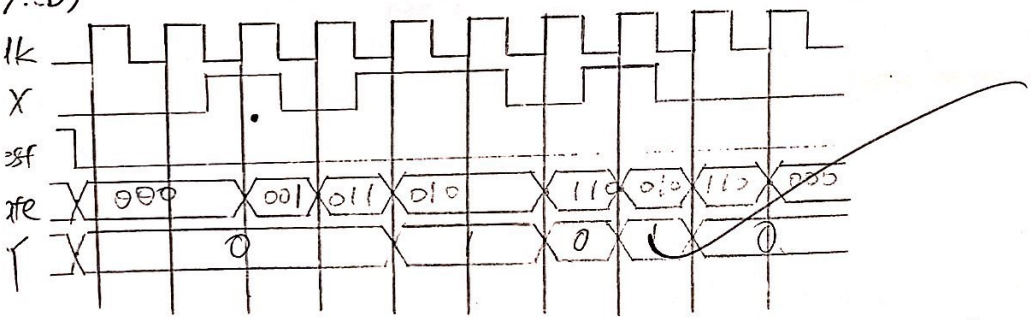
For Y



$\Rightarrow Y = S_2'S_1S_0'$

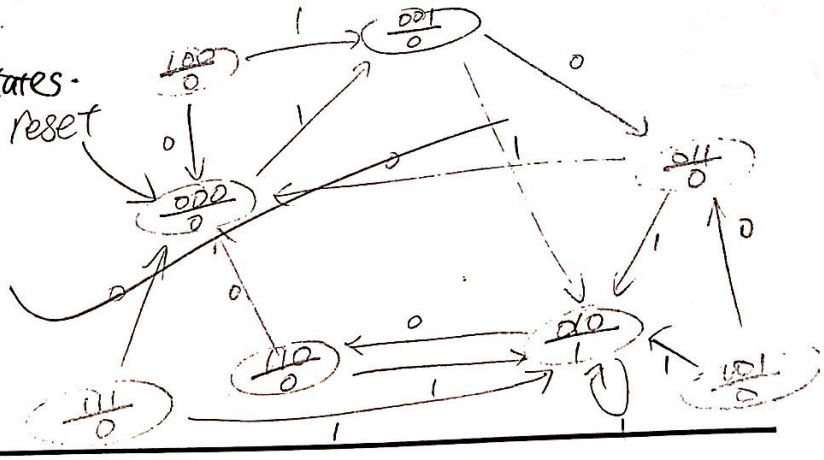


(b)



(c)

It's not self-starting, since there are 3 unused states.



2/(a)

Present State					Next State		
s_2	s_1	s_0	X	Y	n_2	n_1	n_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	1
0	1	0	1	0	0	1	1
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

For n_2, n_1, n_0 the equations are the same as those in the previous

$n_2 = s_2 s_1 s_0' x'$

$n_1 = s_2' s_1 s_0' + s_1 x$ [illegible] $+ s_1' s_0$

$n_0 = s_1'(s_0 \oplus x)$

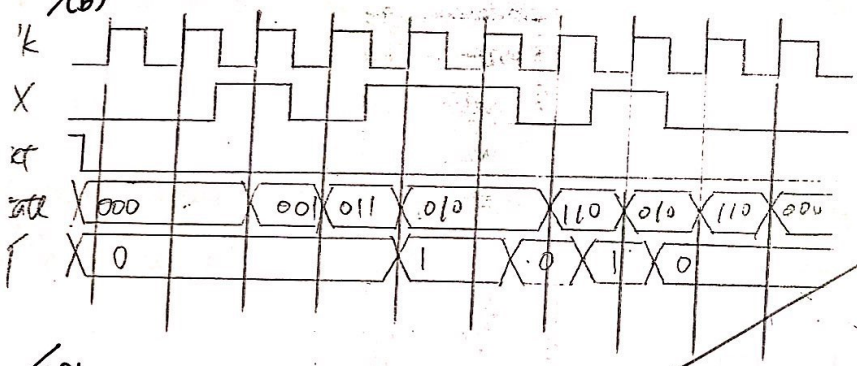
For Y

$s_2 s_1$ \ $s_0 x$	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	0	x	x	x
10	x	x	x	x

$\Rightarrow Y = s_1 s_0' x$

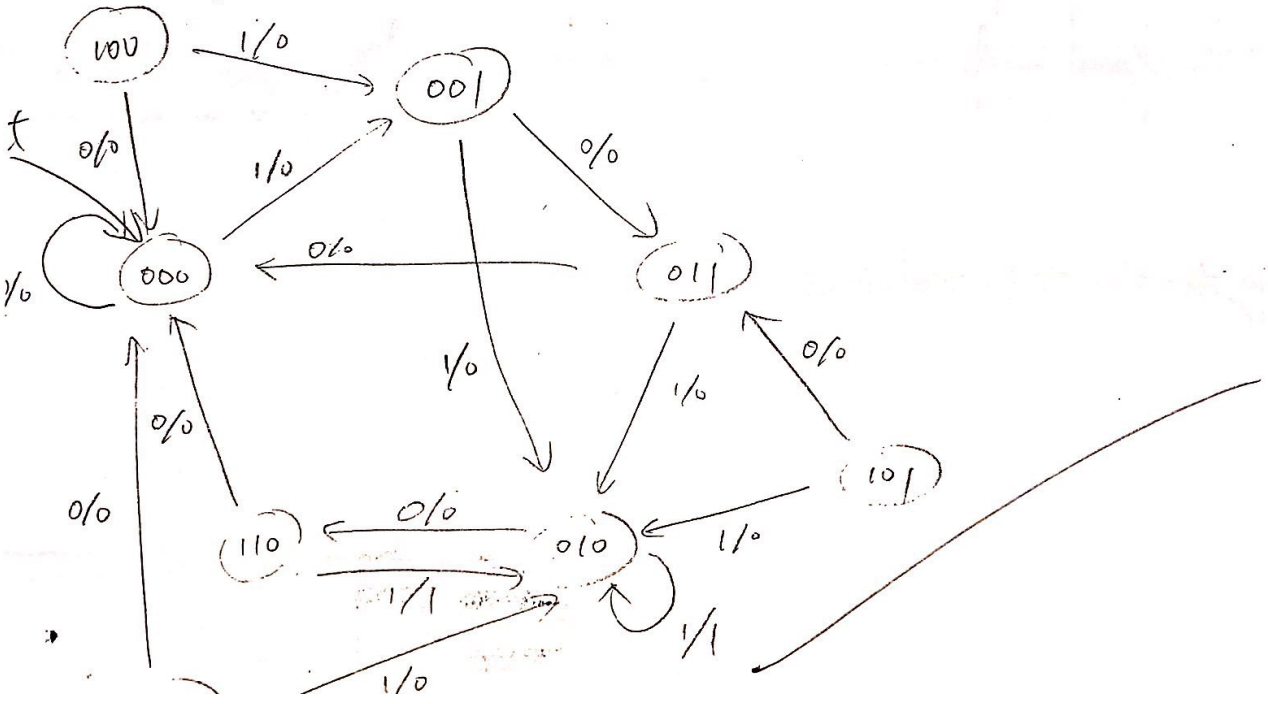
The circuit is exactly the same except the part for Y, so I add "Y new" as the output in this exercise to the previous circuit. (to delicately draw the circuit takes to much time)

/(b)



/(c)

It's not self-starting since there are unused states.



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different Output

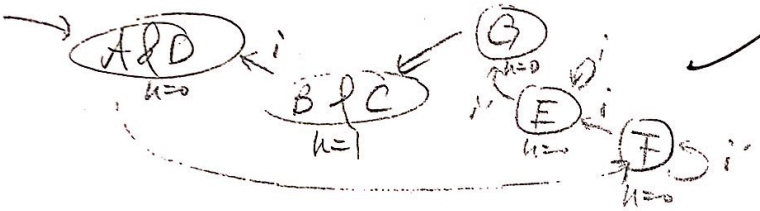
	A	B	C	D	E	F
B	X					
C	X					
D	X	X				
E	X	X				
F	X	X				
G	X	X				

Next state

	A	B	C	D	E	F
B	X					
C	X	(D,A) (E,F)				
D	(F,F)	X	X			
E	(E,F)	X	X	(E,F)		
F	(F,F)	X	X	(E,F) (E,F) (F,F) (F,G)		
G	(C,F)	X	X	(C,F) (C,B) (C,F)		

× first
× second
× third.

Thus we find A&D, B&C are equivalent



1. For 2-bit encoding

Present		Next		Output		
S1	S0	n1	n0	w	x	y
0	0	0	1	1	0	0
0	1	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	0	0	0

After applying K-map, we get
n1 = S0⊕S1
n0 = S0'
w = S1'S0'
x = S1'S0
y = S1S0'

The number of gate inputs is 8
The number of delays is 1

For 3-bit output encoding.

Present			Next			Output		
S2	S1	S0	n2	n1	n0	w	x	y
1	0	0	0	1	0	1	0	0
0	1	0	0	0	1	0	1	0
0	0	1	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0

All else is X

After applying K-map, we get
n2 = S2'S1'S0'
n1 = S2
n0 = S1
w = S2
x = S1
y = S0

The number of gate inputs is 3
The number of delays is 1

For one-hot encoding

Present				Next				Output		
S3	S2	S1	S0	n3	n2	n1	n0	w	x	y
1	0	0	0	0	1	0	0	1	0	0
0	1	0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0	0	0	0

After applying K-map, we get
n3 = S0
n2 = S3
n1 = S2
n0 = S1
w = S3
x = S2
y = S1

The number of gate inputs is 0
The number of delays is 0