**Ve270 Introduction to Logic Design Homework 5**

**Assigned: June 13, 2019**

**Due: June 20, 2018, 4:00pm (after the exam)**

**The homework should be submitted in hard copies.**

1. Describe a 32-bit 2-to-1 MUX in Verilog. Simulate your Verilog module. (20 points)

A

B

sel

F

Mux

32

32

32

0

1

1. Model the following circuit with Verilog HDL. The circuit should be modeled by instantiating four D flip-flops. Simulate your Verilog module. (20 points)



1. Model the following circuit with Verilog HDL. Simulate your Verilog module. (20 Points)

*x*

3

*x*

2

*x*

1

*x*

0

Clock

*f*

D

Q

Q

D

Q

Q

D

Q

Q

D

Q

Q

1. Design a 4-bit down-counter that has two control input: cnt enables counting down, clear synchronously resets the counter to all 0s, and set synchronously sets the counter to all 1s. Model the circuit in Verilog HDL. Simulate your Verilog module (20 Points)
2. Design a 4-bit up-counter with an additional output upper that outputs a 1 whenever the counter is within the upper half of the counter’s range, 8 to 15. Model the circuit in Verilog HDL. Simulate your Verilog module (20 Points)