Datasheet

GW3323HGU6

RISC-V based 32-bit MCU with Bluetooth

Version: V0.0.2

Table of Contents

1. Product Features

CPU and Flexible IO

- 32bit High performance CPU with DSP instruction;
- Program memory: internal 8M bit flash;
- 256 Kbytes of SRAM ; including 206 Kbytes for user;
- Flexible GPIO pins with Programmable pull-up and pull-down resistors;
- Support GPIO wakeup or interrupt;
- 160 MHz maximum frequency;

Bluetooth Radio

- Compliant to Bluetooth 5.2 and BLE specification;
- TX output power MAX +9dBm;
- RX Sensitivity with -94dBm @2M EDR;
- Support TWS communication with balance-efficiency Power consumption;
- Support TWS Master-slave switch;

Supports

- A2DP/AVDTP/AVRCP/RFCOMM/HFP/HSP/ SPP/HID

Peripheral and Interfaces

- Support AAC, mSBC high quality decode;
- Support Low power Touch Key;
- Support Low power enter ear detect;
- 200mA maximum charge current of Power management function;
- Three 32-bit timers;
- Three multi-function 32-bit timers, support Capture and PWM mode;
- WatchDog;
- Three full-duplex UART;
- Two SPI;
- IR controller;
- SD Card Host controller;
- Full speed USB 2.0 HOST/DEVICE controller;
- Sixteen Channels 10-bit ADC;13 Channels for user;
- Two Channels 12-bit DAC;
- Integrate IRTC;
- Build in PMU, such as charger/buck/LDO;

Package

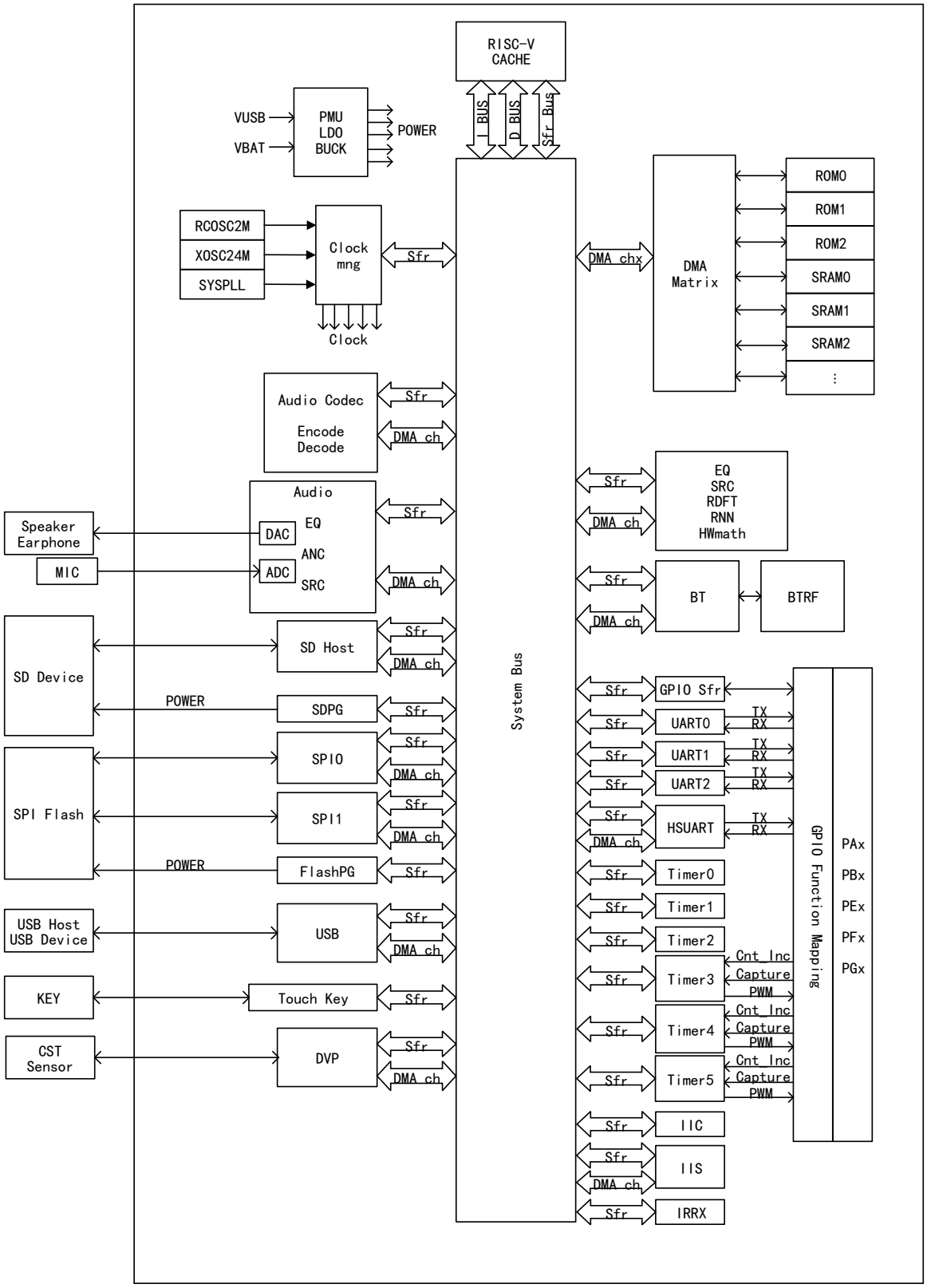
- QFN40;

Temperature

- Operating temperature: -40℃ to +85℃;
- Storage temperature: -65℃ to +150℃;

2. Block Diagram

2.1. Block Diagram



Note: Chx indicates the channel number x

2.2. Memory mapping

Start Address	Address	Name	Size	Include Register
0 (寄存器-4KB)	0x00	SFR0	256B	TICK0\UART0-1\RTC\WDT\TMR0-2\SPI0
	0x100	SFR1	256B	DAC
	0x200	SFR2	256B	-
	0x300	SFR3	256B	USB\PLL\CLK\PWR\LVD\RST
	0x400	SFR4	256B	PIC
	0x500	SFR5	256B	ADC\WKUP
	0x600	SFR6	256B	GPIOA-F
	0x700	SFR7	256B	GPIOG
	0x800	SFR8	256B	IRRX\USERKEY\PROT
	0x900	SFR9	256B	TIM3-5\UART2\SPI1\RTC
	0xa00	SFR10	256B	TK\PIAN\TONEDLY\TKA
	0xb00	SFR11	256B	-
	0xc00	SFR12	256B	-
	0xd00	SFR13	256B	-
	0xe00	SFR14	256B	-
	0xf00	SFR15	256B	-
0x00001000		-		
0x00010600 (SRAM- 190.5KB)	0X10600	cache	512B	cache_stack for loader
	0x10800	stack	1K	stack_ram，To avoid defining large parts in a function buf
	0x10c00	heap	12KB	heap
	0x13c00	data	13KB	Global variable, static variable, variable without AT.
	0x17000	comm	36KB	Interrupt and various interrupt detection codes, storage com_text, com_rodata,variable without AT.
	0x20000	bram	48KB	It was originally stored in "Bluetooth bottom layer, operating system and public area"; Users who do not use Bluetooth can assign at will.
	0x2c000	cram	80KB	Areas available to users,buff for storing ble.
0x00040000		-		
0x00050000 (SRAM- 49.2KB)	0x50000	aram	16KB	Users can also use.
	0x54000	eram	0xa00=2.5KB	fot_data, the upgraded data must be retained.
	0x55800	rram	608	for rnn input/output.(rnn algorithm) software cannot be accessed.
	0x58000	dram	0x4500=17.2KB	Space used for OTA upgrading.
0x0005c500		-		
0x10000000 （flash-1MB）	0x10000000	init	512B	Store reset settings.
	0x10000200	flash(rx)	511.5KB	Functions without AT, text\rodata is stored here.

	0x10080000		492KB	The data in the backup area is generally placed from here.
	0x100fb000	cm	20KB	System parameter area (write data to cache, etc.) at least 20k.
0x10100000				

```
.comm : {
    *(.vector)
    *(.plt)
    *(.com_text*)
    *(.com_text.stack.handler)
    *(.com_rodata*)
    *debug.o(.rodata*)
    *(.data*)
    *(.sdata*)
    *(.load_text)
    *(.load_rodata)
    . = ALIGN(512);
} > comm AT > flash
```

```
.bram __bram_vma (NOLOAD) : {
    *(.btmem.bthw)
    *(.btmem*)

    *(.ble_cache*)
    *(.ble_buf*)
    *(.spp_tx_buff.*)
    *(.ble_tx_buff.*)
} > bram
```

2.3. System Clock

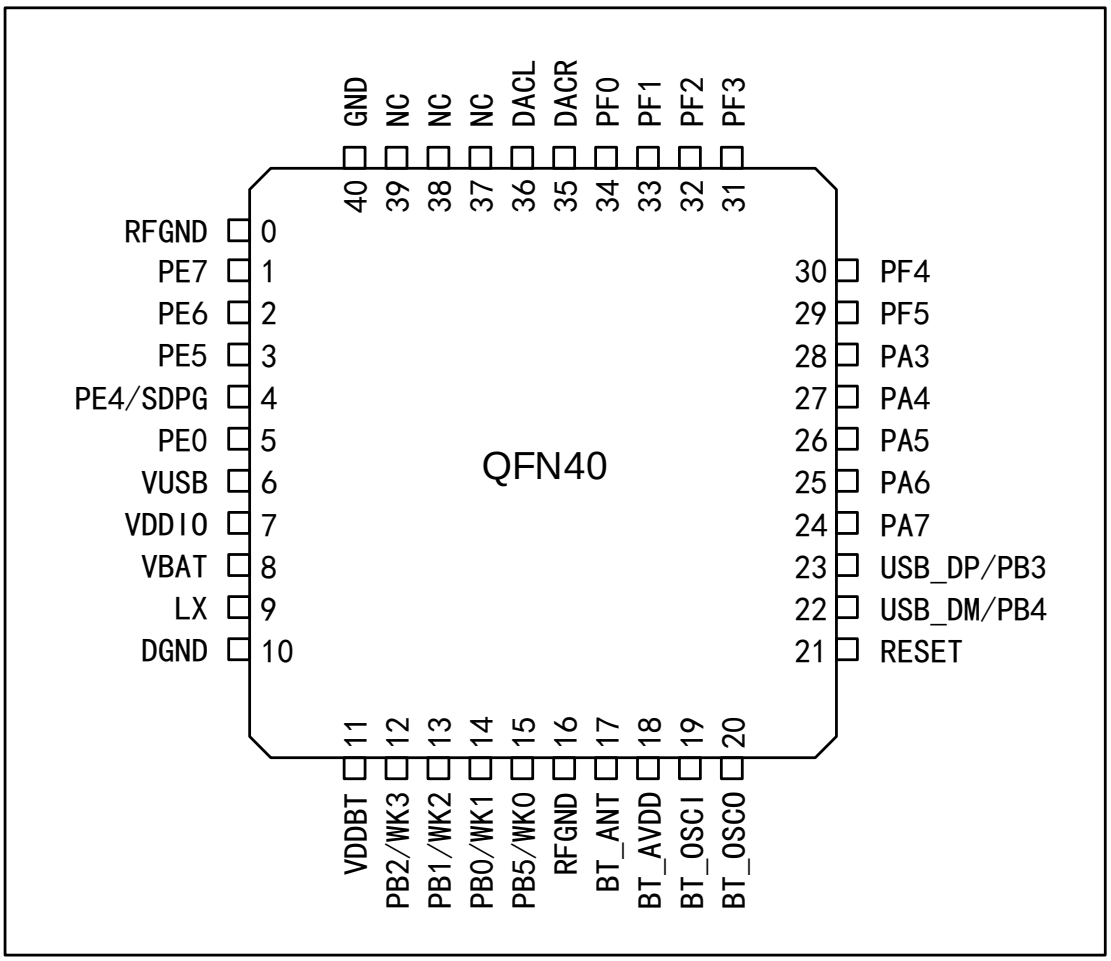
```
enum {
    SYS_2M,
    SYS_24M,
    SYS_48M,
    SYS_60M,
    SYS_80M,
    SYS_120M,
    SYS_147M,
    SYS_160M,
};

void set_sys_clk(u32 clk_sel);
```

The highest frequency of this chip is 160MHz, by set_ sys_ clk() can set the system frequency.

3. Package Definition

3.1. Pin Assignment



3.2. Pin Descriptions

Table 3-1 QFN40 pin description

Pin No.	Name	Type	Function
0	RFGND	GND	BT RF Ground
1	PE7	I/O	PDM_DATLR-G2 SDDAT0-G3 SPI1DO-G4 TX0-G4 HSTRX-G4 PWM2-T4-G1 IIC_DAT-G5 TMR4CAP_G1/IR_G8 PE7
2	PE6	I/O	PDM_CLKLR-G2 SDCLK-G3 SPI1CLK-G4 RX0-G4 HSTRX-G9 FMOSC-G6 PWM1-T4-G1 IIC_CLK-G5 IIC_CLK-G6 TMR3CAP_G7/IR_G7 PE6
3	PE5	I/O	SDCMD-G3 SPI1DI-G4 FMOSC-G5 PWM0-T4-G1 IIC_DAT-G6 TMR3CAP_G6/IR_G6 PE5
4	PE4/SDPG	I/O	SDPG PWM1-T3-G4 PE4
5	PE0	I/O	SPI0DI-G3 TX0-G5 PWM0-T3-G4 TMR3CAP_G5/IR_G5 PE0
6	VUSB	PWR	VUSB power input TX0-G8 TX1-G3 TX2-G3 HSTRX-G11
7	VDDIO	PWR	VDDIO power output
8	VBAT	PWR	VBAT power input
9	LX	PWR	Buck inductor connect pin

Pin No.	Name	Type	Function
10	DGND	GND	Digital Ground
11	VDDBT	PWR	BT power
12	PB2/WK3	I/O	SDDAT0-G2 SPI1DO-G3 TX0-G2 TX2-G2 HSTRX-G2 PWM2-T3-G1 IIC_DAT-G3 WKO PB2
13	PB1/WK2	I/O	SDCLK-G2 SPI1CLK-G3 RX0-G2 RX2-G2 HSTRX-G7 FMOSC-G4 PWM1-T3-G1 IIC_CLK-G3 IIC_CLK-G4 TMR3CAP_G4/IR_G4 WKO PB1
14	PB0/WK1	I/O	WK1 SPI1DI-G3 FMOSC-G3 PWM0-T3-G1 IIC_DAT-G4 TMR3CAP_G3/IR_G3 PB0
15	PB5/WK0	I/O	PWM2-T3-G2 WKO PB5
16	RFGND	GND	BT RF Ground
17	BT_ANT	A	BT ANT
18	BT_AVDD	PWR	BT RF Power
19	BT_OSCI	A	24M OSC input
20	BT_OSCO	A	24M OSC output
21	Reset	A	reset PIN
22	PB4/USB_DM	I/O	USB DM PDM_DATLR-G4 SDDAT0-G4 SDDAT0-G6 SPI0CLK-G3 RX0-G3

Pin No.	Name	Type	Function
			HSTRX-G8 PWM1-T3-G2 IIC_DAT-G8 PB4
23	PB3/USB_DP	I/O	USB DP PDM_CLKLR-G4 SDDAT0-G5 SDCMD-G6 SPI0DO-G3 TX0-G3 HSTRX-G3 PWM0-T3-G2 IIC_CLK-G8 PB3
24	PA7	I/O	PDM_DATLR-G3 SDDAT0-G1/G7 SPI1DO -G2 TX0-G1(RX) TX1-G1(RX) HSTRX-G1 PWM2-T5-G1 IIC_DAT-G1 PA7
25	PA6	I/O	PDM_CLKLR-G3 SDCLK-G1/G4/G5/G6 SPI1CLK-G2 RX0-G1 RX1-G1 HSTRX-G6 FMOSC-G2 PWM1-T5-G1 IIC_CLK-G1/G2 TMR3CAP_G2/IR_G2 PA6
26	PA5	I/O	SDCMD-G1/G4/G5 SPI1DI-G1 SPI1DI-G2 FMOSC-G1 PWM0-T5-G1 IIC_DAT-G2 TMR3CAP_G1/IR_G1 PA5
27	PA4	I/O	SPI1DO -G1 TX1-G2 PWM2-T3-G3 PA4
28	PA3	I/O	SPI1CLK-G1 RX1-G2 PWM1-T3-G3 PA3
29	PF5	I/O	PDM_DATLR-G1

Pin No.	Name	Type	Function
			SDCMD-G7 SPI1DO -G5 TX0-G7 PWM1-T5-G2 IIC_DAT-G7 PF5
30	PF4	I/O	PDM_CLKLR-G1 SDCLK-G7 SPI1CLK-G5 PWM0-T5-G2 IIC_CLK-G7 PF4
31	PF3	I/O	PWM2-T4-G2 PF3
32	PF2	I/O	PWM1-T4-G2 PF2
33	PF1	I/O	SPI1DI-G5 TX0-G6 PWM0-T4-G2 TMR5CAP_G1/IR_G9 PF1
34	PF0	I/O	PWM0-T3-G3 PF0
35	DACR	A	DAC0
36	DACL	A	DAC1
37	NC	-	-
38	NC	-	-
39	NC	-	-
40	GND	GND	Ground

Note: I/O: Digital input/output; I : Digital input; A : Analog Pin; PWR: Power Pin; GND: Ground.

4. Interrupts

Support vectorized interrupts, exceptions on illegal instructions and exceptions on load and store instructions to invalid addresses.

Exception vectors

Interrupt number	Address	Description
0	0x00	Reset
1	0x04	
2	0x08	
3	0x0c	
4	0x10	Low priority interrupt
5	0x14	
6	0x18	
7	0x1c	
8	0x20~0x9c	High priority interrupt(see the following table)

High priority interrupt vectors

Interrupt number	Address	Description
0	0x20	
1	0x24	
2	0x28	Software interrupt
3	0x2c	Timer0 interrupt
4	0x30	Timer1 interrupt
5	0x34	Timer2 interrupt
6	0x38	IR receiver interrupt
7	0x3c	
8	0x40	
9	0x44	
10	0x48	
11	0x4c	
12	0x50	
13	0x54	
14	0x58	UART0 interrupt UART1 interrupt UART2 interrupt
15	0x5c	
16	0x60	Timer3 interrupt
17	0x64	Timer4 interrupt
18	0x68	Timer5 interrupt

Interrupt number	Address	Description
19	0x6c	
20	0x70	
21	0x74	
22	0x78	
23	0x7c	
24	0x80	
25	0x84	
26	0x88	Port interrupt
27	0x8c	
28	0x90	SARADC interrupt
29	0x94	
30	0x98	
31	0x9c	

4.1. Interrupts Special Registers

Register 4-1 PICCON: Peripheral interrupt control Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	GIEM	WR	1	Global interrupt enable mask bit 0: disable interrupt 1: enable interrupt
15:7	-	-	-	Unused
6:5	HPSDEN	WR	0x0	High priority shadow register select bit 00: high priority 01: high priority 2 10/11: high priority 3
4:2	-	-	-	Unused
1	LPINTEN	WR	0	Low priority interrupt enable bit 0: disable 1: enable
0	GIE	WR	0	Global interrupt enable bit 0: disable interrupt 0: disable interrupt

Register 4-2 PICCONSET: Peripheral interrupt control set Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	GIEM	W	0	Write 1 enable Global interrupt enable mask

Bit	Name	Mode	Default	Description
15:8	-	-	-	Unused
7:3	-	-	-	Unused
2	HPINTEN	W	0	Write 1 enable High priority interrupt
1	LPINTEN	W	0	Write 1 enable Low priority interrupt
0	GIE	W	0	Write 1 enable Global interrupt

Register 4-3 PICCONCLR: Peripheral interrupt control clear Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	GIEMDIS	W	0	Write 1 disable Global interrupt enable mask
15:8	-	-	-	Unused
7:3	-	-	-	Unused
2	HPINTDIS	W	0	Write 1 disable High priority interrupt
1	LPINTDIS	W	0	Write 1 disable Low priority interrupt
0	GIEDIS	W	0	Write 1 disable Global interrupt

Register 4-4 PICEN: Peripheral interrupt enable Register

Bit	Name	Mode	Default	Description
31:0	IntEN	WR	0x0	Interrupt 31 to 0 enable bit 0: disable 1: enable

Register 4-5 PICENSET: Peripheral interrupt enable set Register

Bit	Name	Mode	Default	Description
31:0	IntEN	W	0x0	Write 1 enable Interrupt 31 to 0

Register 4-6 PICENCLR: Peripheral interrupt enable clear Register

Bit	Name	Mode	Default	Description
31:0	IntDIS	W	0x0	Write 1 disable Interrupt 31 to 0

Register 4-7 PICPR: Peripheral high priority interrupt selection Register

Bit	Name	Mode	Default	Description
31:0	IntPR	WR	0x0	Interrupt 31 to 0 priority selection bit 0: low priority interrupt

Bit	Name	Mode	Default	Description
				1: high priority interrupt

Register 4-8 PICPR1: Peripheral high priority interrupt selection Register1

Bit	Name	Mode	Default	Description
31:0	IntPR1	WR	0x0	Interrupt 31 to 0 priority selection 1 bit; {PICPR1, PICPR} 00: low priority interrupt 01: high priority interrupt 10: high priority 2 interrupt 11: high priority 3 interrupt

Register 4-9 PICADR: Peripheral interrupt address Register

Bit	Name	Mode	Default	Description
31:8	BADR	WR	0x800	Interrupt entry address
7:0	-	-	0x0	

Register 4-10 PICPND: Peripheral interrupt pending Register

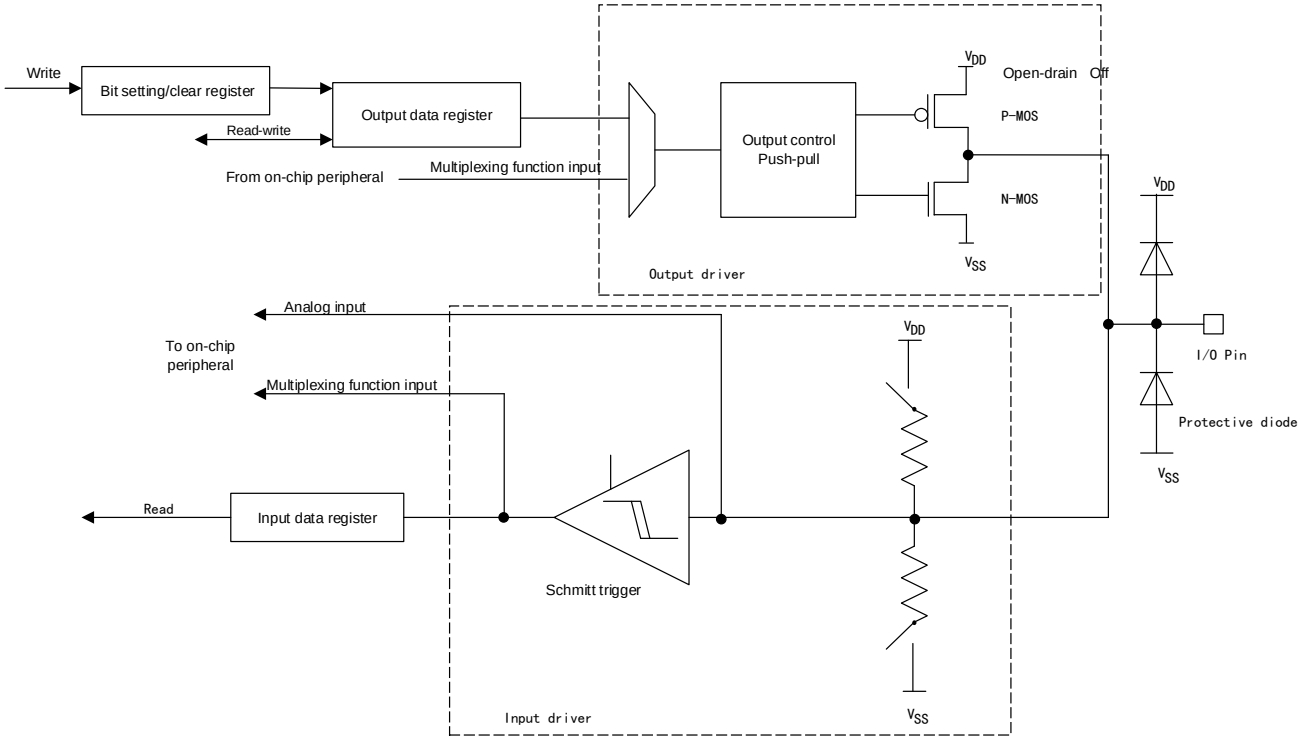
Bit	Name	Mode	Default	Description
31:3	IntPND[31:3]	R	0x0	Interrupt 31 to 3 pending bit 0: no interrupt pending 1: interrupt pending
2	SWIPND	WR	0	Software interrupt pending. Write 1 will clear software interrupt pending
1:0	IntPND[1:0]	R	0x0	Interrupt 1 to 0 pending bit 0: no interrupt pending 1: interrupt pending

5. GPIO Management

5.1. Features

1. Control GPIO input/output direction by using direction register;
2. Internal pull-up/pull-down resistor by using pull-up/pull-down resistor control register;
3. Select suitable output driving current capability;

5.2. GPIO internal block diagram



5.3. GPIO general control register

Register 5-1 GPIOA: Port A data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOA	WR	0x00	PAx data. Valid when PAx is used as GPIO 0: PAx is input low state when read and output low at PAx when write; 1:PAx is input high state when read and output high at PAx when write

Register 5-2 GPIOASET: Port A Set output data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused

Bit	Name	Mode	Default	Description
7:0	GPIOASET	WO	X	Set PAx output data. Write 1 set output data. Write 0 affect nothing.

Register 5-3 GPIOACLR: Port A clear output data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOACLR	WO	X	Clear PAx output data. Write 1 clear output data. Write 0 affect nothing.

Register 5-4 GPIOADIR: Port A direction Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOADIR	WR	0xFF	PAx direction control 0: Output 1: Input

Register 5-5 GPIOAPU: Port A pull-up Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPU	WR	0x0	PAx 10KΩ pull-up resister control. Valid when PAx is used as input 0: disable 1: enable

Register 5-6 GPIOAPD: Port A pull-down resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPD	WR	0x0	PAx 10KΩ pull-down resister control. Valid when PAx is used as input 0: disable 1: enable

Register 5-7 GPIOAPU200K: Port A pull-up resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPU	WR	0x0	PAx 200KΩ pull-up resister control. Valid when PAx is used as input 0: disable 1: enable

Register 5-8 GPIOAPD200K: Port A pull-down resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPD	WR	0x0	PAx 200KΩ pull-down resister control. Valid when PAx is used as input 0: disable 1: enable

Register 5-9 GPIOAPU300: Port A pull-up resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPU	WR	0x0	PAx 300Ω pull-up resister control. Valid when PAx is used as input 0: disable 1: enable

Register 5-10 GPIOAPD300: Port A pull-down resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPD	WR	0x0	PAx 300Ω pull-down resister control. Valid when PAx is used as input 0: disable 1: enable

Register 5-11 GPIOADE: Port A digital function enable register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOADE	WR	0xFF	PAx digital function enable 0: Port used as analog IO 1: Port used as digital IO

Register 5-12 GPIOAFEN: Port A function mapping enable register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAFEN	WR	0xFF	PAx function mapping enable 0: Port used as GPIO 1: Port used as function IO

Register 5-13 GPIOADRV: Port A output driving select Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused

Bit	Name	Mode	Default	Description
7:0	GPIOADRV	WR	0x0	PAx output driving select 0: 8mA 1: 32mA

5.4. GPIO function mapping

Register 5-14 FUNCMCON0: Port function mapping control Register 0

Bit	Name	Mode	Default	Description
31:28	UT1RXMAP	WR	0x0	UART1 RX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to TX pin by UT1TXMAP select 1111: Clear these bits Others is reserved
27:24	UT1TXMAP	WR	0x0	UART1 TX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits Others is reserved
23:20	-	-	-	-
19:16	-	-	-	-
15:12	UT0RXMAP	WR	0x0	UART0 RX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to TX pin by UT0TXMAP select 1111: Clear these bits Others is reserved
11:8	UT0TXMAP	WR	0x0	UART0 TX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1000: map to G8 1111: Clear these bits Others is reserved

Bit	Name	Mode	Default	Description
7:4	SPI0MAP	WR	0x0	SPI0 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits Others is reserved
3:0	SD0MAP	WR	0x0	SD0 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 1111: Clear these bits Others is reserved

Register 5-15 FUNCMCON1: Port function mapping control Register 1

Bit	Name	Mode	Default	Description
31:12	—	—	—	—
11:8	UT2RXMAP	WR	0x0	UART2 RX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to TX pin by UT2TXMAP select 1111: Clear these bits Others is reserved
7:4	UT2TXMAP	WR	0x0	UART2 TX mapping 0000: no affect 0001: map to G1 0010: map to G2 1111: Clear these bits Others is reserved
3:0	—	—	—	—

Register 5-16 FUNCMCON2: Port function mapping control Register 2

Bit	Name	Mode	Default	Description
31:28	-	-	-	Unused
27:24	IICMAP	WR	0x0	IIC mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1000: map to G8

Bit	Name	Mode	Default	Description
				1111: Clear these bits Others is reserved
23:20	IRMAP	WR	0x0	IR mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1000: map to G8 1001: map to G9 1111: Clear these bits Others is reserved
19:16	TMR5MAP	WR	0x0	Timer5 PWM mapping 0000: no affect 0001: map to G1 1111: Clear these bits Others is reserved
15:12	TMR4MAP	WR	0x0	Timer4 PWM mapping 0000: no affect 0001: map to G1 1111: Clear these bits Others is reserved
11:8	TMR3MAP	WR	0x0	Timer3 PWM mapping 0000: no affect 0001: map to G1 1111: Clear these bits Others is reserved
7:4	TMR3CPTMAP	WR	0x0	Timer3 capture Pin mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1111: Clear these bits Others is reserved
3:0				

Register 5-17 FUNCMCON3: Port function mapping control Register 3

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:4	MPDMMAP	WR	0x0	MPDM interface mapping 0000: no affect 0001: map to G1 0010: map to G2

Bit	Name	Mode	Default	Description
				0011: map to G3 0100: map to G4 1111: Clear these bits Others is reserved
3:0	PDMMAP	WR	0x0	PDM interface mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 1111: Clear these bits Others is reserved

5.5. External Port interrupt wake up

Support eight wakeup source input, as the following table. Wakeup circuit 6 and wakeup circuit 7 is special for 32 port interrupts wake up.

Port interrupt source is:

Port_intsrc = {PG[4:0], PF[5:0], PE[7:0], PB[4:0], PA[7:0]};

Wakeup source	Wakeup circuit
PA7	Wakeup circuit 0
PB1	Wakeup circuit 1
PB2	Wakeup circuit 2
PB3	Wakeup circuit 3
PB4	Wakeup circuit 4
WKO(PB5)	Wakeup circuit 5
PORT_INT_FALL	Wakeup circuit 6
PORT_INT_RISE	Wakeup circuit 7

Register 5-18 WKUPCON: Wake up control Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	WKIE	WR	0	Wake up interrupt enable 0: disable 1: enable
15:8	-	-	-	Unused

Bit	Name	Mode	Default	Description
7:0	WKEN	WR	0x0	Wake up input 7~0 enable 0: disable 1: enable

Register 5-19 WKUPEDG: Wake up edge select Register

Bit	Name	Mode	Default	Description
31:24	-	-	-	Unused
23:16	WKPND	R	0x0	Wake up input 7~0 pending 0: no pending 1: wake up pending
15:8	-	-	-	Unused
7:0	WKEDG	WR	0x0	Wake up input 7~0 wakeup edge select 0: rising edge 1: falling edge

Register 5-20 WKUPCPND: Wake up clear pending Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
23:16	WKCPND	W	0x0	Wake up input 7~0 clear pending 0: no affect 1: clear wake up pending
15:0	-	-	-	Unused

Register 5-21 PORTINTEN: Port interrupt enable Register

Bit	Name	Mode	Default	Description
31:0	PORTINTEN	WR	0x0	Port interrupt 0~31 enable bit 0: disable 1: enable

Register 5-22 PORTINTEDG: Port interrupt edge select Register

Bit	Name	Mode	Default	Description
31:0	PORTINTEDG	WR	0x0	Port interrupt 0~31 edge select bit 0: rise edge 1: fall edge

6. Timer

6.1. Features

1. Timer0/1/2, only support 32bit timer function
2. Timer3/4/5, can be configured to Timer-mode, Counter-mode, Capture-mode and PWM-mode

6.2. Timer0/1/2 Special Function Registers

Register 6-1 TMR0CON/TMR1CON/TMR2CON: Timer0/1/2 Control Register

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9	TPND	WR	0	Timer overflow pending 0: not overflow 1: overflow
8	-	-	-	Unused
7	TIE	WR	0	Timer overflow interrupt enable 0: disable 1: enable
6	INCSRC	WR	0	Increase source select 0: select TMR_INC 1: select external PIN
5:4	-	-	-	Unused
3:2	INCSEL	WR	0x0	Increase clock selection 00: System Clock 01: Counter input rising 10: Counter input falling 11: Counter input edge
1	-	-	-	Unused
0	TMREN	WR	0	Timer Enable Bit 0: Disable 1: Enable

Register 6-2 TMR0CPND/TMR1CPND/TMR2CPND: Timer0/1/2 clear pending Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
9	TPCLR	W	0	Timer overflow pending clear bit 0: inactive 1: clear pending
8:0	-	-	-	Unused

Register 6-3 TMR0CNT/TMR1CNT/TMR2CNT: Timer0/1/2 counter Register

Bit	Name	Mode	Default	Description
31:0	TMRCNT	WR	0x0	Timer counter. TMRCNT will increase when timer is enabled. It overflows when TMRCNT = TMRPR, TMRCNT will be clear to 0x0000 when overflow, and the interrupt flag will be set '1'.

Register 6-4 TMR0PR/TMR1PR/TMR2PR: Timer0/1/2 period Register

Bit	Name	Mode	Default	Description
31:0	TMRPR	WR	0xffffffff	Timer period = TMRPR + 1

6.3. Timer3/4/5 Special Function Registers

Register 6-5 TMR3CON/TMR4CON/TMR5CON: Timer3/4/5 Control Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	CPND	WR	0	Timer capture pending 0: not capture 1: capture
16	TPND	WR	0	Timer overflow pending 0: not overflow 1: overflow
15:12	-	-	-	Unused
11	PWM2EN	WR	0	Timer pwm2 enable bit 0: disable 1: enable
10	PWM1EN	WR	0	Timer pwm1 enable bit 0: disable 1: enable
9	PWM0EN	WR	0	Timer pwm0 enable bit 0: disable 1: enable
8	CIE	WR	0	Timer capture interrupt enable 0: disable 1: enable
7	TIE	WR	0	Timer overflow interrupt enable 0: disable 1: enable
6	INCSRC	WR	0	Increase source select 0: select TMR_INC 1: select external PIN
5:4	CPTEDSEL	WR	0x0	Timer Capture edge select 00: No Capture 01:Capture PIN rising edge 10: Capture PIN falling edge 11: Capture PIN edge

Bit	Name	Mode	Default	Description
3:2	INCSEL	WR	0x0	Increase clock selection 00: System Clock 01: Counter input rising 10: Counter input falling 11: Counter input edge
1	CPTEN	WR	0	Timer capture Enable Bit 0: Disable 1: Enable
0	TMREN	WR	0	Timer Enable Bit 0: Disable 1: Enable

Register 6-6 TMR3CPND/TMR4CPND/TMR5CPND: Timer3/4/5 clear pending Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	CPCLR	W	0	Capture pending clear bit 0: inactive 1: clear pending
16	TPCLR	W	0	Timer overflow pending clear bit 0: inactive 1: clear pending
15:0	-	-	-	Unused

Register 6-7 TMR3CNT/TMR4CNT/TMR5CNT: Timer3/4/5 counter Register

Bit	Name	Mode	Default	Description
31:0	TMRCNT	WR	0x0	Timer counter. TMRCNT will increase when timer is enabled. It overflows when TMRCNT = TMRPR, TMRCNT will be clear to 0x0000 when overflow, and the interrupt flag will be set '1'.

Register 6-8 TMR3PR/TMR4PR/TMR5PR: Timer3/4/5 period Register

Bit	Name	Mode	Default	Description
31:0	TMRPR	WR	0xffffffff	Timer period = TMRPR + 1

Register 6-9 TMR3CPT/TMR4CPT/TMR5CPT: Timer3/4/5 capture value Register

Bit	Name	Mode	Default	Description
31:0	TMRCPT	R	x	Timer capture value

Register 6-10 TMR3DUTY0/TMR4DUTY0/TMR5DUTY0: Timer3/4/5 pwm0 duty Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused

15:0	TMRDUTY0	W	x	Timer pwm0 duty PWM0 low level length is TMRDUTY0+1 PWM 0 high level length is TMRPR-TMRDUTY0

Register 6-11 TMR3DUTY1/TMR4DUTY1/TMR5DUTY1: Timer3/4/5 pwm1 duty Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	TMRDUTY1	W	x	Timer pwm1 duty PWM1 low level length is TMRDUTY1+1 PWM1 high level length is TMRPR-TMRDUTY1

Register 6-12 TMR3DUTY2/TMR4DUTY2/TMR5DUTY2: Timer3/4/5 pwm2 duty Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	TMRDUTY2	W	x	Timer pwm2 duty PWM2 low level length is TMRDUTY2+1 PWM2 high level length is TMRPR-TMRDUTY2

7. RTC

7.1. Features

1. Support 32bit Independent power supply real time counter
2. Support alarm interrupt and second interrupt

7.2. Special Function Registers

Register 7-1 RTCCON: RTC Control Register

Bit	Name	Mode	Default	Description
31:23	-	-	-	Unused
22	INBOX	R	0	INBOX state 0: out of box 1: in box
21	VUSBOFF	R	0	VUSB off state 0: online 1: off state
20	VUSBONLINE	R	0	VUSB online state 0: not online 1: online
19	RTCWKP	R	0	RTC WK pin state 0: WK pin state is 0 1: WK pin state is 1
18	RTCWKSLPPND	R	0	RTC wakeup sleep pending 0: no pending 1: pending
17	ALMPND	R	0	RTC alarm pending 0: no pending 1: alarm pending
16:9	-	-	-	Unused
8	ALM_WKEN	WR	0	RTC alarm wakeup enable 0: disable 1: enable
7	RTC_WKSLPEN	WR	0	RTC wakeup sleep enable 0: disable 1: enable
6	VUSBRSTEN	WR	0	VUSB insert reset system enable 0: disable 1: enable
5	WKUPRSTEN	WR	0	RTC wake up power down mode reset system enable 0: disable 1: enable
4	ALMIE	WR	0	RTC alarm interrupt enable 0: disable 1: enable

Bit	Name	Mode	Default	Description
3	RTC1SIE	WR	0	RTC 1S interrupt enable 0: disable 1: enable
2:1	BAUDSEL	WR	0x1	Increase clock selection 00: System Clock divide 4 01: System Clock divide 8 10: System Clock divide 16 11: System Clock divide 32
0	-	-	-	Unused

Register 7-2 RTCCPND: RTC clear pending Register

Bit	Name	Mode	Default	Description
31:19	-	-	-	Unused
18	CWKSLPPND	W	0	Write 1 will clear RTC wakeup sleep pending
17	CALMPND	W	0	Write 1 will clear RTC alarm pending
16:0	-	-	-	Unused

7.3. Independent Power RTC Registers

Register 7-3 RTCCNT: RTC counter Register

Bit	Name	Mode	Default	Description
31:0	RTCCNT	WR	0x0	32bit RTC counter

Register 7-4 RTCALM: RTC alarm Register

Bit	Name	Mode	Default	Description
31:0	RTCALM	WR	0xffffffff	32bit RTC alarm

Register 7-5 RTCCON0: RTC control Register 0

Bit	Name	Mode	Default	Description
31:18	-	-	-	-
17	TKSWRSTN	WR	0	Touch key reset 0: touch key reset 1: release touch key reset
16:15	VRTCSEL	WR	0x0	—
14	RCSEL	WR	0	RC select

Bit	Name	Mode	Default	Description
				0: RCOSC 1:RING RC
13	RCOSCEN	WR	0	—
12	VIOAONS	WR	0	—
11:10	CLK2MBTSSEL	WR	0x0	CLK2M to BT low power clock select bit 00: 0 01: RTC clock 32K 10: RTC 2M 11: XOSC 26M divide 8(3.25M)
9	CLK2MTKSSEL	WR	0	CLK2M in Touch Key power domain source select bit 0: RTC 2M 1: XOSC 26M divide 8(3.25M)
8	CLK2MRTCSSEL	WR	0	CLK2M in RTC power domain source select bit 0: RTC 2M 1: XOSC 26M divide 8(3.25M)
7	PWRUP1ST	WR	1	RTC first power up flag 0: not first power up 1: first power up
6	EXT32KS	WR	0	External 32K select 0: use RTC internal 32K osc 1: use external 32K osc
5	-	-	-	-
4	TKITF_EN	WR	1	Touch key between core interface enable bit 0: disable 1: enable
3	SNIFF_EN	WR	0	Sniff mode disable VDDCORE_EN enable 0: disable 1: enable
2	CLK2M_EN	WR	0	CLK2M divide to RTC 32K clock source enable 0: disable 1: enable
1	X32KEN	WR	0	XOSC32K enable bit 0: disable 1: enable
0	RCEN	WR	0	RCOSC enable bit 0: disable 1: enable

Register 7-6 RTCCON1: RTC control Register 1

Bit	Name	Mode	Default	Description
7	VRTCEN	WR	0	VRTC enable bit, VRTC voltage forADC 0: disable 1: enable
6	WKPLVLS	WR	0	WK pin wakeup level select bit 0: low level wakeup 1: high level wakeup

5	WKPAEN	WR	0	WK pin analog enable bit, output WKO voltage forADC 0: disable 1: enable
4	WKPPUEN	WR	1	WK pin pull up enable bit 0: disable 1: enable
3:2	WKPPUS	WR	0x1	WK pin pull up select bit 00: 80K 01: 90K 10: 100K 11: 400K
1	WKPPD	WR	0	WK pin pull down 10K enable bit 0: disable 1: enable
0	WKPIE	WR	1	WK pin input enable bit 0: disable 1: enable

Register 7-7 RTCCON2: RTC control Register 2

Bit	Name	Mode	Default	Description
7	SELVDDPU	WR	1	SEL VDD pullup enable 0: disable 1: enable
6	32KSEL	WR	0	32K osc select bit 0: 32.768K 1: 32K
5:4	RSV	WR	0x0	Reserve,can't be changed default value.
3:2	RSV	WR	0x0	Reserve,can't be changed default value.
1:0	RSV	WR	0x0	Reserve,can't be changed default value.

Register 7-8 RTCCON3: RTC control Register 3

Bit	Name	Mode	Default	Description
15	-	-	-	Unused
14	TK_WKEN	WR	0	Touch key long press wakeup enable bit 0: disable 1: enable
13	-	-	-	Unused
12	INBOX_WKEN	WR	0	INBOX wake up enable bit 0: disable 1: enable
11	VSUB_WKEN	WR	0	VUSB wake up enable bit 0: disable 1: enable

Bit	Name	Mode	Default	Description
10	WKP_WKEN	WR	0	WK pin wake up enable bit 0: disable 1: enable
9	RTC1S_WKEN	WR	0	RTC one second wakeup enable bit 0: disable 1: enable
8	ALM_WKEN	WR	0	RTC alarm wakeup enable bit 0: disable 1: enable
7	-	-	-	Unused
6	PDCOREEN	WR	1	Core power down enable bit 0: disable 1: enable
5	VCORESHTEN	WR	1	VDDCORE short enable bit 0: disable 1: enable
4	VDDXOEN	WR	1	VDDXO enable bit 0: disable 1: enable
3	VCOREAONEN	WR	1	VDDCORE AON enable bit 0: disable 1: enable
2	VCOREEN	WR	1	VDDCORE enable bit 0: disable 1: enable
1	VIOEN	WR	1	VDDIO enable bit 0: disable 1: enable
0	BUCKEN	WR	0	BUCK enable bit 0: disable 1: enable

Register 7-9 RTCCON5: RTC control Register 5

Bit	Name	Mode	Default	Description
7	RSV	WR	0	Reserve,can't be changed default value.
6	RSV	WR	0	Reserve,can't be changed default value.
5:4	RSV	WR	0x0	Reserve,can't be changed default value.
3:2	RSV	WR	0x0	Reserve,can't be changed default value.
1	BUCKLPM	WR	0	BUCK low power mode enable 0: disable 1: enable

0	LDOM	WR	1	BUCK LDO mode select bit 0: buck mode 1: LDO mode

Register 7-10 RTCCON10: RTC control Register 10

Bit	Name	Mode	Default	Description
10	WKP10SC	WR	0	When write WK pin 10s pending clear 0: no affect 1: clear 10s pending When read: WK pin 10s pending 0: no 10s pending 1: 10s pending
9	WK3P	R	0	WK pin3 wake up pending 0: no pending 1: pending
8	WK2P	R	0	WK pin2 wake up pending 0: no pending 1: pending
7	WK1P	R	0	WK pin1 wake up pending 0: no pending 1: pending
6	TKP	R	0	TK wake up pending 0: no pending 1: pending
5	-	-	-	unused
4	INBOXP	R	0	INBOX wake up pending 0: no pending 1: pending
3	VUSBP	R	0	VUSB wake up pending 0: no pending 1: pending
2	WKP	R	0	WK pin wake up pending 0: no pending 1: pending
1	RTC1SPC	WR	0	When write: RTC 1 second pending clear 0: no affect 1: clear 1s pending When read: RTC 1 second pending 0: no second pending 1: second pending

Bit	Name	Mode	Default	Description
0	ALMPC	WR	0	When write: RTC alarm pending clear 0: no affect 1: clear alarm pending When read: Alarm pending 0: no alarm pending 1: alarm pending

Register 7-11 RTCCON11: RTC control Register 11

Bit	Name	Mode	Default	Description
10	RTCWKSLPEN	WR	0	RTC timer wakeup sleep enable 0: disable 1: enable
9:8	RTCWKSLPS	WR	0x0	RTC timer wakeup sleep time select 00: 110ms 01: 220ms 10: 440ms 11: 880ms
7	VIOCHG_SWEN	WR	0	VUSB to VDDIO LDO select control bit 0: VUSB to VDDIO LDO enable by pmu_normal & VIOCHG_EN 1: VUSB to VDDIO LDO enable by VIOCHG_SWEN & VIOCHG_EN
6	VUSBWKSEL	WR	0	VUSB wakeup select 0: VUSB insert filter wakeup 1: VUSB pull out filter wakeup
5	VUSBFILSEL	WR	0	VUSB off filter select 0: 840us 1: 12ms
4	WKOPRT	WR	0	WKO protect bit
3	LVDDETEN	WR	0	LVD detect enable after power up by wake up 0:disable 1:enable
2	WKPFEN	WR	1	WK pin filter enable bit 0:disable 1:enable
1:0	WKPFSEL	WR	0x0	WK pin filter select bit 00:8ms 01:32ms 10:128ms 11:512ms

Register 7-12 RTCCON12: RTC control Register 12

Bit	Name	Mode	Default	Description
7:4	-	-	-	Unused
3:0	WKP10SEN	WR	0xa	WK pin 10s reset enable 0xa: disable Others: enable

8. UART

8.1. Features

1. UART is a serial port capable of asynchronous transmission.
2. The UART can function in full duplex mode.

8.2. UART Special Function Registers

Register 8-1 UARTCON: UART Control Register

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9	RXPND	R	0	RX pending 0: RX one byte not finish 1: RX one byte finish
8	TXPND	R	0	TX pending 0: TX one byte not finish 1: TX one byte finish
7	RXEN	WR	0	RX enable 0: RX disable 1: RX enable
6	ONELINE	WR	0	One-line mode 0: TX/RX separate 1: TX/RX one line
5	CLKSRC	WR	0	Clock source select 0: system clock 1: uart_inc
4	SB2EN	WR	0	Two Stop Bit enable 0: 1-bit Stop Bit 1: 2 bit Stop Bit
3	TXIE	WR	0	Transmit Interrupt Enable 0 = Transmit interrupt disable 1 = Transmit interrupt enable
2	RXIE	WR	0	Receive Interrupt Enable 0: Receiver interrupt disable 1: Receiver interrupt enable
1	BIT9EN	WR	0	BIT9 Enable Bit 0: Eight-bit mode 1: Nine-bit mode
0	UTEN	WR	0	UART Enable Bit 0: Disable UART module 1: Enable UART module

Register 8-2 UARTCPND: UART clear pending Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	CRSTKEYPND	W	0	Reset Key match pending clear 0: N/A 1: Clear Reset key match Pending
16	CKEYPND	W	0	Key match pending clear 0: N/A 1: Clear key match Pending
15:10	-	-	-	Unused
9	CRXPND	W	0	RX pending clear 0: N/A 1: Clear RX Pending
8	CTXPND	W	0	TX pending clear 0: N/A 1: Clear TX Pending. Writing data to UTBUF will clear TXPND
7:0	-	-	-	Unused

Register 8-3 UARTBAUD: UART Baud Rate Register

Bit	Name	Mode	Default	Description
31:16	UARTRXBAUD	W	0	UART RX Baud Rate Baud Rate =Fsys clock / (UART0RXBAUD + 1)
15:0	UARTTXBAUD	W	0	UART TX Baud Rate Baud Rate =Fsys clock / (UART0TXBAUD + 1)

Register 8-4 UARTDATA: UART Data Register

Bit	Name	Mode	Default	Description
31:9	-	-	-	Unused
8	UARTBIT8	WR	x	UART Data bit 8
7:0	UARTDAT	WR	x	UART Data Write this register will load the data to transmitter buffer. Read this register will read the data from the receiver buffer..

8.3. User Guide

1. Set IO in the correct direction.
2. Configure UART0BAUD to choose sample rate
3. Enable UART0 by setting
4. Set TXIE or RXIE ‘to 1’ if needed
5. write data to UART0DATA
6. Wait for PND to change to ‘1’, or wait for interrupt
7. Read received data from UART0DATA if needed

9. SPI0

9.1. Features

The flash SPI0 is the system clock's division-by-2,and the maximum speed of the SPI interface is 80MHz. The SPI flash start address is 0x1000 0000 and the size is 265Mbit.

SPI0 can support different mode.

1. general 3 wire mode, 1-bit clock in/out, 1-bit data output, 1-bit data input
2. 2 wire mode, 1-bit clock in/out, 1-bit data output or input;
3. 2 data bus mode, 1-bit clock in/out, 2-bit data output or input;
4. 4 data bus mode, 1-bit clock in/out, 4-bit data output or input;

9.2. SPI0 Special Function Registers

Register 9-1 SPI0CON: SPI0 Control Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	SPIPND	R	0	SPI pending 0: not finish SPI rx/tx 1: finish SPI rx/tx
15:14	-	-	-	Unused
13	HOLDENSW	WR	0	SPI software hold enable 0: disable 1: enable
12	HOLDENTX	WR	0	SPI hold enable when bt tx 0: disable 1: enable
11	HOLDENRX	WR	0	SPI hold enable when bt rx 0: disable 1: enable
10	SPIOSS	WR	0	SPI sample data is at the same clock edge with output data 0: SPI sample data is at the difference clock edge with output data 1: SPI sample data is at the same clock edge with output data
9	SPIMBEN	WR	0	SPI multiple bit bus enable bit 0: disable 1: enable
8	SPILF_EN	WR	0	SPI LFSR enable bit 0: disable 1: enable
7	SPIIE	WR	0	SPI interrupt enable 0: disable 1: enable
6	SMPS	WR	0	SPI output edge select bit, when SPIOSS = 0, sample data and output data is at different clock edge; when SPIOSS = 1, sample data and output data is at the same clock edge 0: output data at the falling edge;

Bit	Name	Mode	Default	Description
				1: output data at the rising edge;
5	CLKIDS	WR	0	SPI clock state when idle 0: clock stay at 0 1: clock stay at 1
4	RXSEL	WR	0	When in DMA mode or 2-wire mode, configure SPI Receive or Transmit select bit 0: transmit 1: receive
3:2	BUSMODE	WR	0x0	Data bus width select bit 00:3-wire mode; 1bit data in, 1bit data out 01:2-wire mode; 1bit data in/out 10: 2bit bidirectional data bus 11: 4bit bidirectional data bus
1	SPISM	WR	0	Slave mode select bit 0: master mode 1:slave mode
0	SPIEN	WR	0	SPI Enable bit 0: Disable 1: Enable

Register 9-2 SPI0BAUD: SPI Baud Rate Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	SPI0BAUD	W	0	SPI Baud Rate Baud Rate =Fsys clock / (SPI_BAUD+1)

Register 9-3 SPI0CPND: SPI clear pending Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	SPICPND	W	0	Write 1 will clear SPI pending
15:0	-	-	-	Unused

Register 9-4 SPI0BUF: SPI0 receive/send Data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	SPI0BUF	WR	x	SPI Data Write this register will load the data to transmitter buffer. Read this register will read the data from the receiver buffer..

Register 9-5 SPI0DMACNT: SPI0 DMA counter Register

Bit	Name	Mode	Default	Description
31:11	-	-	-	Unused
10:0	SPI0DMACNT	W	x	SPIDMA byte counter Write this register will kick start spi send/receive data Total number of bytes received / send is SPI0DMACNT

Register 9-6 SPI0DMAADR: SPI0 DMA address Register

Bit	Name	Mode	Default	Description
31:21	-	-	-	Unused
20:0	SPI0DMAADR	W	x	SPI DMA byte address

9.3. User Guide

SPI Normal 1bit-Mode Operation Flow:

1. Set 3-wire mode or 2-wire mode and select the pin map
2. Select RXSEL for Transmit or receive
3. Configure clock frequency
4. Select one of the four timing mode
5. Enable SPI module by setting SPIEN ‘1’
6. Set SPIIE ‘1’ if needed
7. Write data to SPIBUF to kick-start the process
8. Wait for SPIPND to change to ‘1’, or wait for interrupt
9. Read received data from SPIBUF if needed
10. Go to Step 8 to start another process if needed or turn off SPI0by clearing SPIIE and SPIEN

SPI Normal Multi-Bit-Mode Operation Flow:

1. Set data bus width (bus4 or bus 2) and select the pin map
2. Select RXSEL for Transmit or receive
3. Configure clock frequency
4. Select one of the four timing mode
5. Enable SPI module by setting SPIEN ‘1’
6. Set SPIIE ‘1’ if needed
7. Write data to SPIBUF to kick-start the process
8. If data bus width is 2 bit, write SPIBUF twice kick-start the transmission
9. If data bus widths are 4 bit, write SPIBUF four times kick-start the transmission
10. However, when receive data, only need write once to kick-start receive process
11. Wait for SPIPND to change to ‘1’, or wait for interrupt
12. Read received data from SPIBUF if needed
13. Go to Step 8 to start another process if needed or turn off SPI by clearing SPIIE and SPIEN

SPI0 DMA Mode Operation Flow:

1. Set IO in the correct direction and data width mode.
2. Select RXSEL for DMA direction
3. Configure clock frequency
4. Select one of the four timing modes
5. Enable SPI module by setting SPIEN to ‘1’
6. Set SPIIE ‘1’ if needed
7. configure SPI0DMAADR；
8. Write data to SPI0_DMACNT to kick-start a DMA process
9. Wait for SPIPND to change to ‘1’, or wait for interrupt
10. Go to Step 8 to start another DMA process if needed or turn off SPI0 by clearing SPI0EN

10. IIC

10.1. Features

1. Support IIC one master
2. Support asynchronous clock source from RC2M or XOSC26M
3. Support out data maximum 4 Byte
4. Support in data maximum 4 Byte
5. Support IIC done interrupt

10.2. IIC Special Function Registers

Register 10-1 IICON0: IIC Control Register

Bit	Name	Mode	Default	Description
31	DONE	R	0	IIC DONE flag
30	ACKSTATUS	R	0	RX IIC slave ACK status 0: RX ACK 1: RX NAK
29	CLR_DONE	W	0	DONE flag clear 0: 1: clear
28	KS	W	0	Kick start 0: 1: Kick start
27	CLR_ALL	W	0	Clear All status 0: 1: clear
26:10	Rev.	WR	-	Unused
9:4	POSDIV	WR	0	IIC SCL pose div counter 0: div 1 1: div2 … N: div N+1
3:2	HOLDCNT	WR	0	SDA hold cnt when SCL failing 0: 1 cycle 1: 2 cycle …
1	INTEN	WR	0	IIC interrupt 0: disable 1: enable
0	IIC_EN	WR	0	IIC Enable Bit 0: Disable 1: Enable

Register 10-2 IICON1: IIC Control Register

Bit	Name	Mode	Default	Description
31:13	-	-	-	Unused
12	TXNAK_EN	WR	0	IIC TX NAK when read last data enable
11	STOP_EN	WR	0	IIC TX STOP enable
10	WDAT_EN	WR	0	IIC TX DATA enable
9	RDAT_EN	WR	0	IIC RX data enable
8	CTL1_EN	WR	0	IIC TX ctl 1 enable
7	START1_EN	WR	0	IIC TX start 1 enable
6	ADR1_EN	WR	0	IIC TX adr 1 enable
5	ADR0_EN	WR	0	IIC TX adr 0 enable
4	CTL0_EN	WR	0	IIC TX ctl 0 enable
3	START0_EN	WR	0	IIC TX start 0 enable
2:0	DATA_CNT	WR	0	RX/TX data counter 0: 0 byte 1: 1 byte … N: N byte

Master mode baud rate configure
IICCLK = source clk / (preclkdiv+1)
SCL = IICCLK / (posdiv+1)

Register 10-3 IICCMDA: IIC CMD/ADR Register

Bit	Name	Mode	Default	Description
31:24	CTL1	WR	0	Control 1 data
23:16	ADR1	WR	0	Address 1 data
15:8	ADR0	WR	0	Address 0 data
7:0	CTL0	WR	0	Control 0 data

Register 8-4 IICDATA: IIC DATA Register

Bit	Name	Mode	Default	Description
31:24	DATA3	WR	0	Data 3

Bit	Name	Mode	Default	Description
23:16	DATA2	WR	0	Data 2
15:8	DATA1	WR	0	Data 1
7:0	DATA0	WR	0	Data 0

10.3. User Guide

IIS master mode Operation Flow:

1. Configure IO mapping, SDA set pullup enable
2. Configure IIC clock select from RC 2M or XOSC 26M, set pre_div clock
3. Configure IIC IICCON0
4. Configure IICCMDA for control byte and address byte
5. Configure IICDATA for WRITE data
6. Configure IICCON1
7. Kick start
8. Wait done flag or interrupt if need
9. Clear DMA DONE flag and update IICCMDA or IICDATA
10. Loop step 7

11. SARADC_CTL

11.1. Features

1. Support 16 channel;
2. The maximum sample rate is 78k/s; SARADC bit clock maximum is 1MHz;
3. ADC has internal 100K pull up resister.

11.2. SARADC_CTL Special Function Registers

Register 11-1 SADCCON: SARADC Control Register

Bit	Name	Mode	Default	Description
31:20	-	-	-	Unused
19	ADCAEN	WR	0	Saradc auto enable analog enable bit 0: disable 1: enable
18	ADCANGIO	WR	0	Saradc auto enable analog IO enable bit 0: Disable 1: Enable
17	ADCIE	WR	0	Saradc interrupt enable bit 0: Disable 1: Enable
16	ADCEN	WR	0	Saradc enable bit 0: Disable 1: Enable
15	CH15PUEN	WR	0	Channel 15 internal pullup enable bit 0: Disable 1: Enable
14	CH14PUEN	WR	0	Channel 14 internal pullup enable bit 0: Disable 1: Enable
13	CH13PUEN	WR	0	Channel 13 internal pullup enable bit 0: Disable 1: Enable
12	CH12PUEN	WR	0	Channel 12 internal pullup enable bit 0: Disable 1: Enable
11	CH11PUEN	WR	0	Channel 11 internal pullup enable bit 0: Disable 1: Enable
10	CH10PUEN	WR	0	Channel 10 internal pullup enable bit 0: Disable 1: Enable
9	CH9PUEN	WR	0	Channel 9 internal pullup enable bit 0: Disable 1: Enable

Bit	Name	Mode	Default	Description
8	CH8PUEN	WR	0	Channel 8 internal pullup enable bit 0: Disable 1: Enable
7	CH7PUEN	WR	0	Channel 7 internal pullup enable bit 0: Disable 1: Enable
6	CH6PUEN	WR	0	Channel 6 internal pullup enable bit 0: Disable 1: Enable
5	CH5PUEN	WR	0	Channel 5 internal pullup enable bit 0: Disable 1: Enable
4	CH4PUEN	WR	0	Channel 4 internal pullup enable bit 0: Disable 1: Enable
3	CH3PUEN	WR	0	Channel 3 internal pullup enable bit 0: Disable 1: Enable
2	CH2PUEN	WR	0	Channel 2 internal pullup enable bit 0: Disable 1: Enable
1	CH1PUEN	WR	0	Channel 1 internal pullup enable bit 0: Disable 1: Enable
0	CH0PUEN	WR	0	Channel 0 internal pullup enable bit 0: Disable 1: Enable

Register 11-2 SADCCH: SARADC channel enable Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	ADCPND	WR	0	Saradc finish pending 0:Not finish 1:Finish Write SARADCH register will clear this bit
15	CH15EN	WR	0	Channel 15 enable bit 0: Disable 1: Enable
14	CH14EN	WR	0	Channel 14 enable bit 0: Disable 1: Enable
13	CH13EN	WR	0	Channel 13 enable bit 0: Disable 1: Enable
12	CH12EN	WR	0	Channel 12 enable bit 0: Disable

Bit	Name	Mode	Default	Description
				1: Enable
11	CH11EN	WR	0	Channel 11 enable bit 0: Disable 1: Enable
10	CH10EN	WR	0	Channel 10 enable bit 0: Disable 1: Enable
9	CH9EN	WR	0	Channel 9 enable bit 0: Disable 1: Enable
8	CH8EN	WR	0	Channel 8 enable bit 0: Disable 1: Enable
7	CH7EN	WR	0	Channel 7 enable bit 0: Disable 1: Enable
6	CH6EN	WR	0	Channel 6 enable bit 0: Disable 1: Enable
5	CH5EN	WR	0	Channel 5 enable bit 0: Disable 1: Enable
4	CH4EN	WR	0	Channel 4 enable bit 0: Disable 1: Enable
3	CH3EN	WR	0	Channel 3 enable bit 0: Disable 1: Enable
2	CH2EN	WR	0	Channel 2 enable bit 0: Disable 1: Enable
1	CH1EN	WR	0	Channel 1 enable bit 0: Disable 1: Enable
0	CH0EN	WR	0	Channel 0 enable bit 0: Disable 1: Enable

Register 11-3 SADCST: SAR ADC setup timing Register

Bit	Name	Mode	Default	Description
31:30	CH15ST	WO	0x0	Channel 15 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK

Bit	Name	Mode	Default	Description
				10: 4 SARADC_CLK 11: 8 SARADC_CLK
29:28	CH14ST	WO	0x0	Channel 14 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
27:26	CH13ST	WO	0x0	Channel 13 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
25:24	CH12ST	WO	0x0	Channel 12 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
23:22	CH11ST	WO	0x0	Channel 11 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
21:20	CH10ST	WO	0x0	Channel 10 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
19:18	CH9ST	WO	0x0	Channel 9 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
17:16	CH8ST	WO	0x0	Channel 8 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
15:14	CH7ST	WO	0x0	Channel 7 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
13:12	CH6ST	WO	0x0	Channel 6 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
11:10	CH5ST	WO	0x0	Channel 5 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK

Bit	Name	Mode	Default	Description
				10: 4 SARADC_CLK 11: 8 SARADC_CLK
9:8	CH4ST	WO	0x0	Channel 4 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
7:6	CH3ST	WO	0x0	Channel 3 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
5:4	CH2ST	WO	0x0	Channel 2 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
3:2	CH1ST	WO	0x0	Channel 1 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
1:0	CH0ST	WO	0x0	Channel 0 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK

Register 11-4 SADCBAUD: SARADC Baud Rate Register

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9:0	SADCBAUD	WO	0x0	SARADC Baud Rate Baud Rate =Fadc clock / [2(SADCBAUD+1)].

Register 11-5 SADCDAT0~15: SARADC channel 0~15 Data Register

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9:0	SADCDAT	R	0x0	SARADC data, channel 0 to channel 15 register

11.3. User Guide

1. Configure SADCBAUD
2. Configure SADCST if need
3. Enable SARADC

4. Write SADCCH to enable channel to convert. Can enable more than one channel.
   Write SADCCH will kick start ADC convert.
5. Wait for ADC_PND

12. WatchDog

12.1. WDT Special Function Registers

Register 12-1 WDTCON: WDT Control Register

Bit	Name	Mode	Default	Description
31	WDTPND	R	0	WDT time out pending 0: no pending 1: pending
30:28	-	-	-	Unused
27:24	TMRSEL_WR	W	0	WDT time select bit write enable When write 0xa, bit20~bit22 can be write to TMRSEL, other value will no affect
23	-	-	-	Unused
22:20	TMRSEL	R	0x4	WDT time select bit 000: 1ms 001: 256ms 010: 512ms 011: 1024ms 100: 2048ms 101: 4096ms 110: 8192ms 111: 16384ms
19:16	WDTCSEL_WR	W	0	WDT clock select When write 0xa, WDTCSEL =0, when write 0x5, WDTCSEL =1. other value will no affect
16	WDTCSEL	R	0	WDT clock select bit 0:RC32K 1:X32K from 26M divider
15:12	WDTIE_WR	W	0	WDT interrupt disable When write 0xa, WDTIE will disable, when write 0x5, WDTIE will enable. other value will no affect
12	WDTIE	R	0	WDT interrupt enable bit 0: Disable 1: Enable
11:8	WDTRSTEN_WR	W	0	WDT reset disable When write 0xa, WDTRSTEN will disable, other value will no affect
8	WDTRSTEN	WR	1	WDT reset enable bit 0: Disable 1: Enable
7:4	WDTEN_WR	W	0	WDT disable When write 0xa, WDTEN will disable, other value will no affect
4	WDTEN	WR	1	WDT enable bit 0: Disable 1: Enable
3:0	WDTCLR	W	0	WDT clear bit When write 0xa, WDT counter and WDTPND will be clear

12.2. User Guide

1. configure WDT reset or interrupt
2. Select WDT time out
3. Clear WDT

13. Characteristics

13.1. PMU Parameters

Table 13-1 PMU voltage input Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VUSB	Charger Voltage input	4.6	5.0	5.5	V	
VBAT	Voltage input	3.0	3.7	4.5	V	

Table 13-2 3.3V LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDIO	3.3V LDO voltage output	-	3.3	-	V	Light Loading condition
△VVDDIO	Output Mismatch 1-sigma	-	43	-	mV	VDDIO=3.3v
ILOAD	Maximum output current	-	-	150	mA	@VBAT=3.6v
ISC	Short Circuit Current Limit	-	-	300	mA	@VBAT=3.8v

Table 13-3 1.2V LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDBT	1.2V LDO voltage output	-	1.2	-	V	Light Loading condition
△VVDDBT	Output Mismatch 1-sigma	-	16	-	mV	VDDBT=1.2v
ILOAD	Maximum output current	-	-	100	mA	@VBAT=3.0v
ISC	Short Circuit Current Limit	-	-	200	mA	@VBAT=3.8v

Table 13-4 1.1V LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDCORE	1.1V LDO voltage output	-	1.1	-	V	Light Loading condition
△VVDDCORE	Output Mismatch 1-sigma	-	15	-	mV	VDDCORE=1.1v
ILOAD	Maximum output current	-	-	60	mA	@VBAT=3.6v
ISC	Short Circuit Current Limit	-	-	120	mA	@VBAT=3.8v

13.2. IO Parameters

Table 13-5 I/O Parameters

GPIO—Electrical Characteristics							
Symbol	**Description**	**Related GPIO**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
VIL	Low-level input voltage		-0.3		1.27	V	VDDIO=3.3V

GPIO—Electrical Characteristics							
Symbol	**Description**	**Related GPIO**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
VIH	High-level input voltage		2.03		3.6	V	VDDIO=3.3V
Driver Ability 1	Output Driver Ability 1			32		mA	VDDIO=3.3V
Driver Ability 0	Output Driver Ability 0			8		mA	VDDIO=3.3V
RPUP0	Internal pull-up resister 0		8	10	12	KΩ	
RPUP1	Internal pull-up resister 1		0.24	0.3	0.36	KΩ	
RPUP2	Internal pull-up resister 2		160	200	240	KΩ	
RPDN0	Internal pull-down resister 0		8	10	12	KΩ	
RPDN1	Internal pull-down resister 1		0.24	0.3	0.36	KΩ	
RPDN2	Internal pull-down resister 2		160	200	240	KΩ	

13.3. BT Parameters

Table 13-6 BT Parameters

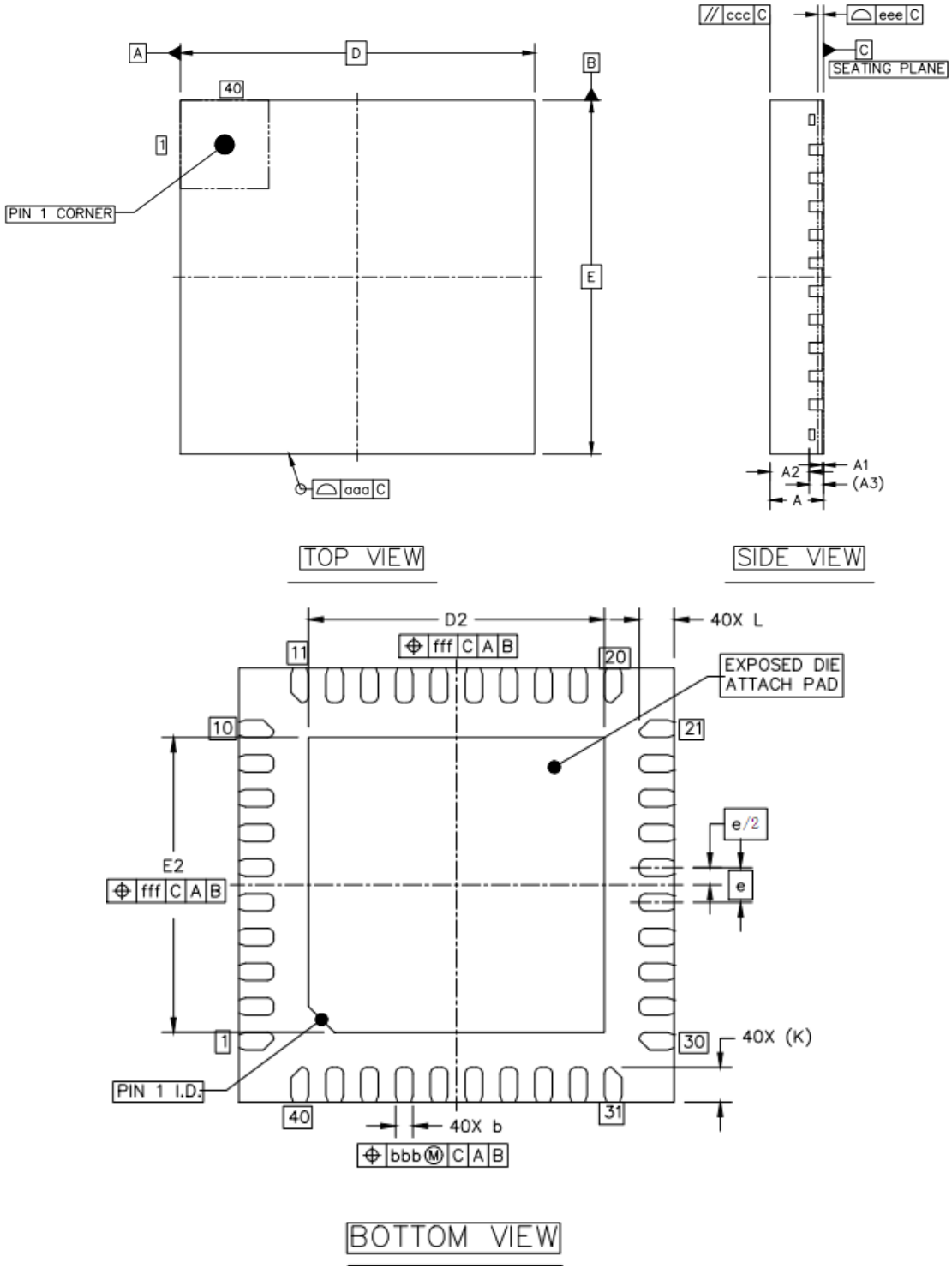
Characteristics	**Min**	**Typical**	**Max**	**Unit**	**Conditions**
Transmit Power	-	8	9	dBm	
RMS DEVM	-	5.5	-	%	Maximum TX power 2-DH5 packet
Peak DEVM	-	12.5		%	
EDR Relative Transmit Power		-0.2		dB	
Sensitivity @ Basic Rate		-91.8		dBm	BER=0.1%, using DH5 packet
Sensitivity @ EDR		-94		dBm	BER=0.01%, using 2-DH5 packet

13.4. Current Parameters

Table 13-7 Current Parameters

Sym	**Characteristics**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
IRTC	RTC mode current	-	4	-	uA	4.2V input, room temp.
Sleep	Sleep current	-	500	2000	uA	3.3V input, room temp

14. Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

15. Revision history

Table 15.1 Document Revision History

Date	Revision	Change
2022-09-23	0.0.1	First draft
2022-10-08	0.0.2	The RFOMM in the protocol part is changed to RFCOMM; Remove QDID number

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