Instructions of CAN bus for STM32F105x

porting program to APM32F103xCxE

1、Mannual difference instructions.

a、Offset address 0x200 to 0x31C.

STM32F105x:

24.9.5 bxCAN register map

Refer to *Section 2.3: Memory map* for the register boundary addresses. In connectivity line devices, the registers from offset 0x200 to 31C are present only in CAN1.

According the STM32F105x reference mannuals,the registers from offset 0x200 to 0x31c are present only in CAN1,this means that when using CAN2 peripherals,CAN1 is enabled and the associated registers are configured through CAN1.

APM32E103xCxE:

24.5 Register Address Mapping

CAN1 base address: 0x4000_6400

CAN2 base address: 0x4000_6800

Note: Except base address, the register and offset addresses of CAN1 and CAN2 are exactly the same.

According the APM32E103xCxE reference mannuals,except base address,the register and offset address of CAN1 and CAN2 are exactly the same,this means that the associated registers from offset 0x200 to 0x31C are configured through CAN1 and CAN2,different from STM32F105x, STM32F105x only oprates CAN1.

b、CAN2 interrupt vector table

STM32F105x:

Table 62. Vector table for XL-density devices (continued)

Position	Priority	Type of priority	Acronym	Description	Address
41	48	settable	RTCAlarm	RTC alarm through EXTI line interrupt	0x0000_00E4
42	49	settable	USBWakeUp	USB wakeup from suspend through EXTI line interrupt	0x0000_00E8
43	50	settable	TIM8_BRK_TIM12	TIM8 Break interrupt and TIM12 global interrupt	0x0000_00EC
44	51	settable	TIM8_UP_TIM13	TIM8 Update interrupt and TIM13 global interrupt	0x0000_00F0
45	52	settable	TIM8_TRG_COM_TIM14	TIM8 Trigger and Commutation interrupts and TIM14 global interrupt	0x0000_00F4
46	53	settable	TIM8_CC	TIM8 Capture Compare interrupt	0x0000_00F8
47	54	settable	ADC3	ADC3 global interrupt	0x0000_00FC
48	55	settable	FSMC	FSMC global interrupt	0x0000_0100
49	56	settable	SDIO	SDIO global interrupt	0x0000_0104
50	57	settable	TIM5	TIM5 global interrupt	0x0000_0108
51	58	settable	SPI3	SPI3 global interrupt	0x0000_010C
52	59	settable	UART4	UART4 global interrupt	0x0000_0110
53	60	settable	UART5	UART5 global interrupt	0x0000_0114
54	61	settable	TIM6	TIM6 global interrupt	0x0000_0118
55	62	settable	TIM7	TIM7 global interrupt	0x0000_011C
56	63	settable	DMA2_Channel1	DMA2 Channel1 global interrupt	0x0000_0120
57	64	settable	DMA2_Channel2	DMA2 Channel2 global interrupt	0x0000_0124
58	65	settable	DMA2_Channel3	DMA2 Channel3 global interrupt	0x0000_0128
59	66	settable	DMA2_Channel4_5	DMA2 Channel4 and DMA2 Channel5 global interrupts	0x0000_012C

APM32E103xCxE:

Exception type	Vector No.	Priority	Vector address	Description
TMR8_CC	46	Can be set	0x0000_00F8	TMR8 capture/compare interrupt
ADC3	47	Can be set	0x0000_00FC	ADC3 global interrupt
EMMC	48	Can be set	0x0000_0100	EMMC interrupt
SDIO	49	Can be set	0x0000_0104	SDIO interrupt
TMR5	50	Can be set	0x0000_0108	TMR5 interrupt
SPI3	51	Can be set	0x0000_010C	SPI3 interrupt
UART4	52	Can be set	0x0000_0110	UART4 interrupt
UART5	53	Can be set	0x0000_0114	UART5 interrupt
TMR6	54	Can be set	0x0000_0118	TMR6 interrupt
TMR7	55	Can be set	0x0000_011C	TMR7 interrupt
DMA2_CH1	56	Can be set	0x0000_0120	DMA2 channel 1 interrupt
DMA2_CH2	57	Can be set	0x0000_0124	DMA2 channel 2 interrupt
DMA2_CH3	58	Can be set	0x0000_0128	DMA2 channel 3 interrupt
DMA2_CH4/5	59	Can be set	0x0000_012C	DMA2 channel 4/5 interrupt
-	-	-	0x0000_0130-0x0000_0133	Reserved
USBD2_HP_CAN2_TX	61	Can be set	0x0000_0134	USBD2 high-priority interrupt/CAN2 sending interrupt
USBD2_LP_CAN2_RX0	62	Can be set	0x0000_0138	USBD2 low-priority interrupt/CAN2 receiving 0 interrupt
CAN2_RX1	63	Can be set	0x0000_013C	CAN2 receiving 1 interrupt
CAN2_SCE	64	Can be set	0x0000_0140	CAN2 SCE interrupt

Programming needs to take care to modify the interrupt vector number.

2、STM32F105x HAL library compatible APM32E103xCxE example.

IDE:STM32CubeIDE 1.4.0 (The IDE version requires V1.4),online debugging please refer to《Sxx32CubeIDE online debugging solution》

MINI BOARD: APM32F103ZET6 MINI BOARD V1.0

The changes are as follows.

a、can_ip=CAN1 need change to can_ip=CAN2

stm32f1xx_hal_can.c

```
835   *          contains the filter configuration information.
836   * @retval None
837   */
838 HAL_StatusTypeDef HAL_CAN_ConfigFilter(CAN_HandleTypeDef *hcan, CAN_FilterTypeDef *sFilterConfig)
839 {
840   uint32_t filternbrbitpos;
841   CAN_TypeDef *can_ip = hcan->Instance;
842   HAL_CAN_StateTypeDef state = hcan->State;
843
844   if ((state == HAL_CAN_STATE_READY) ||
845       (state == HAL_CAN_STATE_LISTENING))
846   {
847     /* Check the parameters */
848     assert_param(IS_CAN_FILTER_ID_HALFWORD(sFilterConfig->FilterIdHigh));
849     assert_param(IS_CAN_FILTER_ID_HALFWORD(sFilterConfig->FilterIdLow));
850     assert_param(IS_CAN_FILTER_ID_HALFWORD(sFilterConfig->FilterMaskIdHigh));
851     assert_param(IS_CAN_FILTER_ID_HALFWORD(sFilterConfig->FilterMaskIdLow));
852     assert_param(IS_CAN_FILTER_MODE(sFilterConfig->FilterMode));
853     assert_param(IS_CAN_FILTER_SCALE(sFilterConfig->FilterScale));
854     assert_param(IS_CAN_FILTER_FIFO(sFilterConfig->FilterFIFOAssignment));
855     assert_param(IS_CAN_FILTER_ACTIVATION(sFilterConfig->FilterActivation));
856
857 #if   defined(CAN2)
858     /* CAN1 and CAN2 are dual instances with 28 common filters banks */
859     /* Select master instance to access the filter banks */
860     can_ip = CAN2;
861
862     /* Check the parameters */
863     assert_param(IS_CAN_FILTER_BANK_DUAL(sFilterConfig->FilterBank));
864     assert_param(IS_CAN_FILTER_BANK_DUAL(sFilterConfig->SlaveStartFilterBank));
865 #else
```

b、Change interrupt vector number