ASSIGNMENT 3

ASIC flow with Synopsys Tools

{System}Verilog for ASIC/FPGA Design & Simulation

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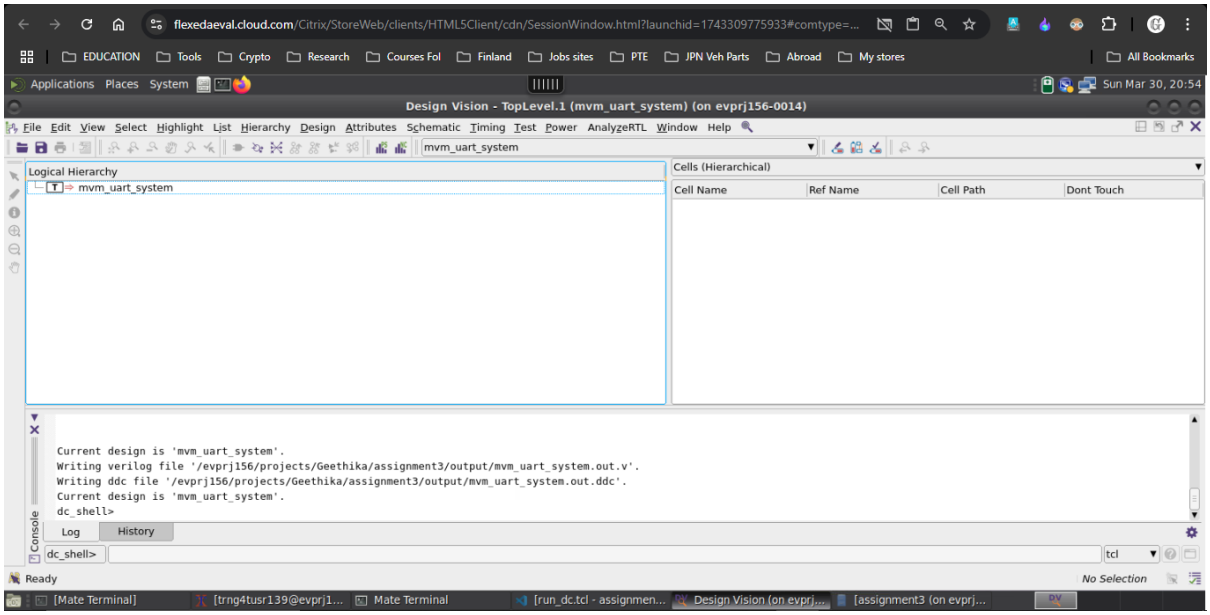
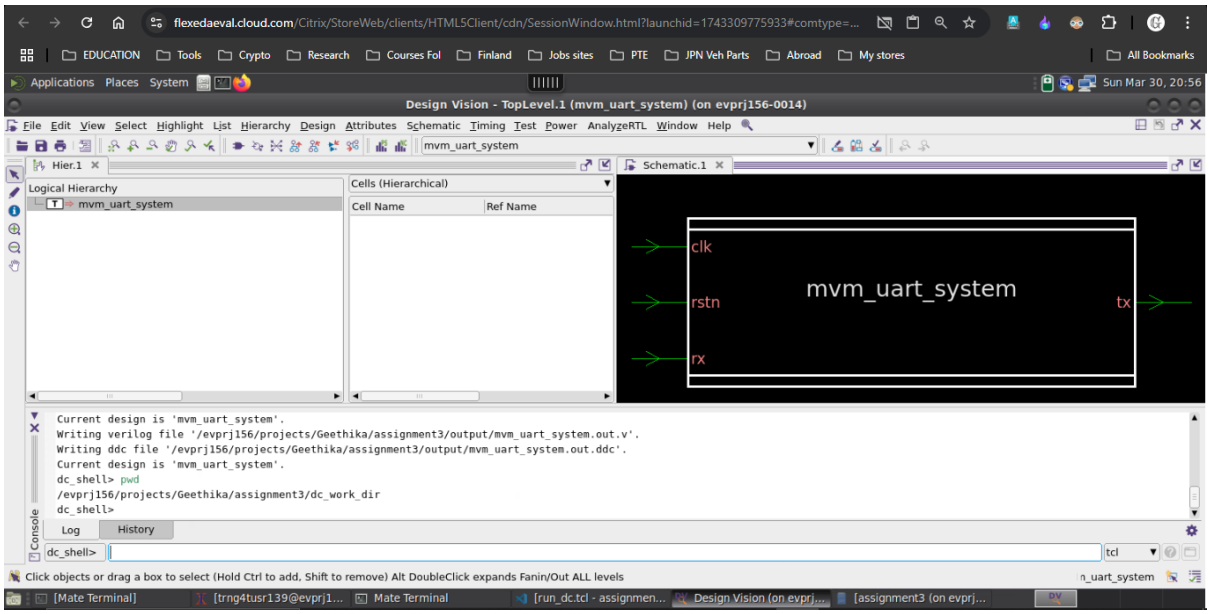
ASICS FLOW

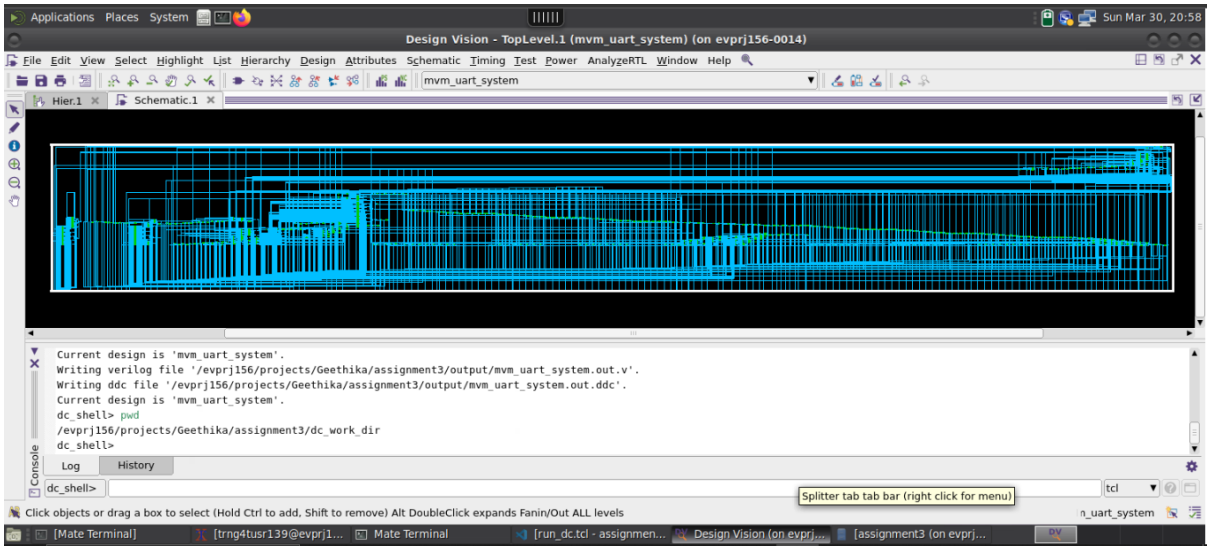
Following Screenshots shows the different sections of the ASICS flow that I have followed. For this design I have selected the parameter values as R=2. C=2, W_X=2, W_K=2. The path of the directory of the assignment related files as follows "/evprj156/projects/Geethika/assignment3 ".



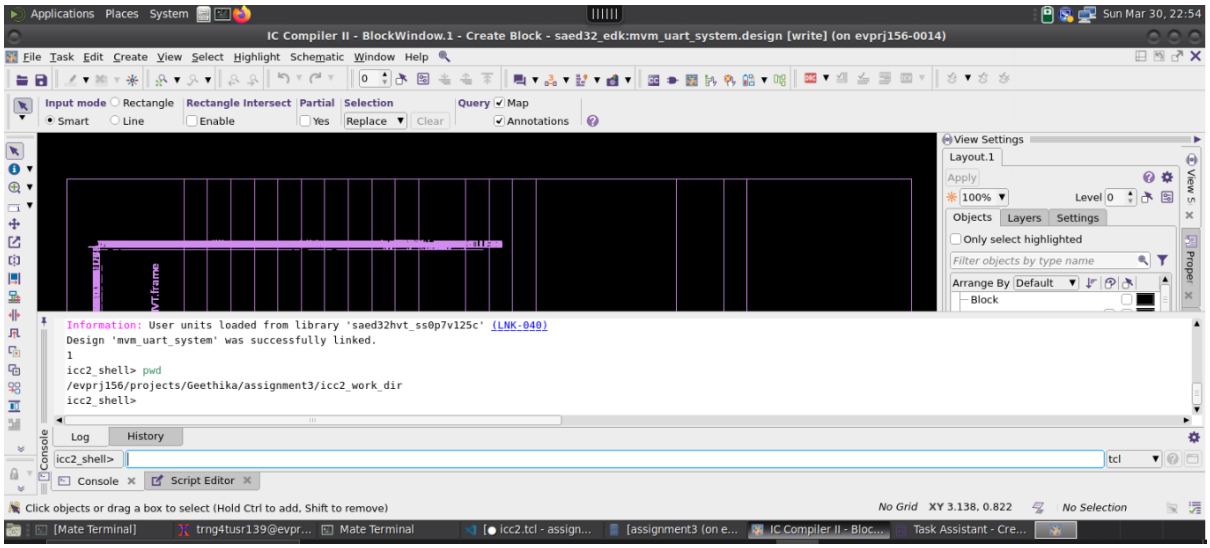
After running the dc_run.tcl file in the dc_shell



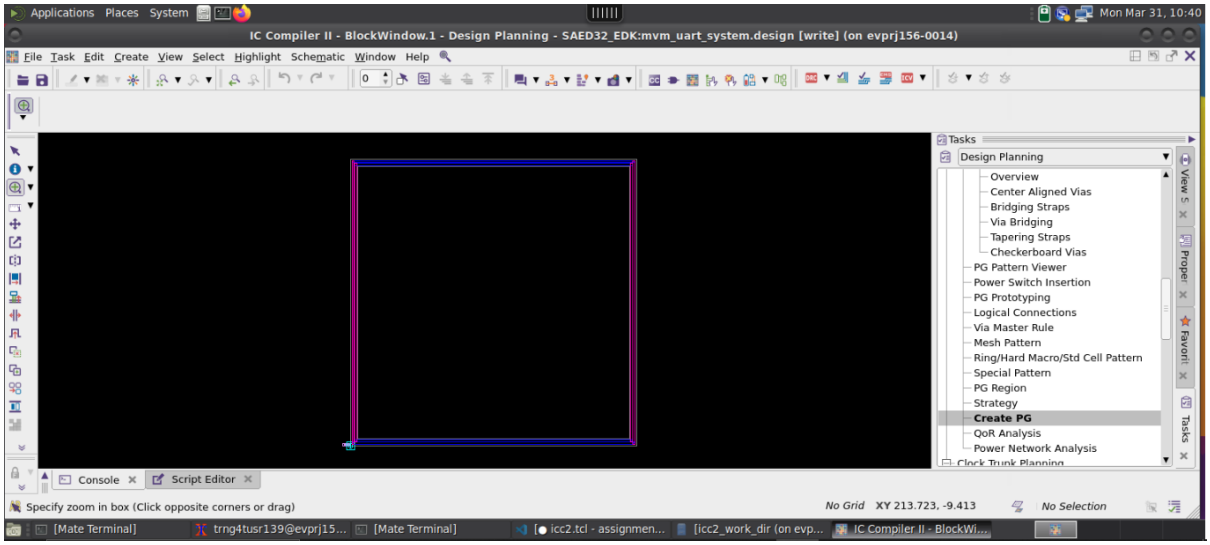
Top module "mvm_uart_system"



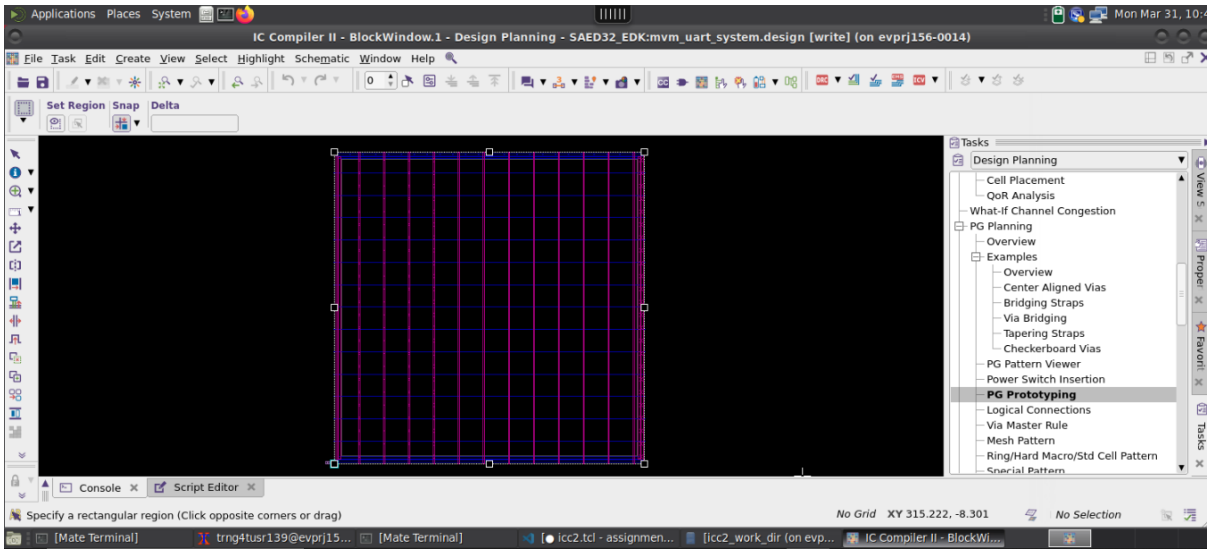
Schematic view of the mvm_uart_system



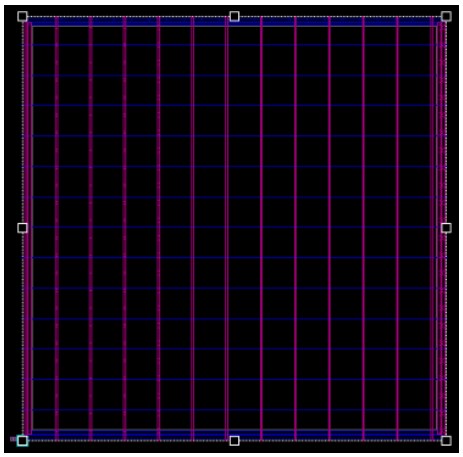
After running the icc2.tcl commands upto create block



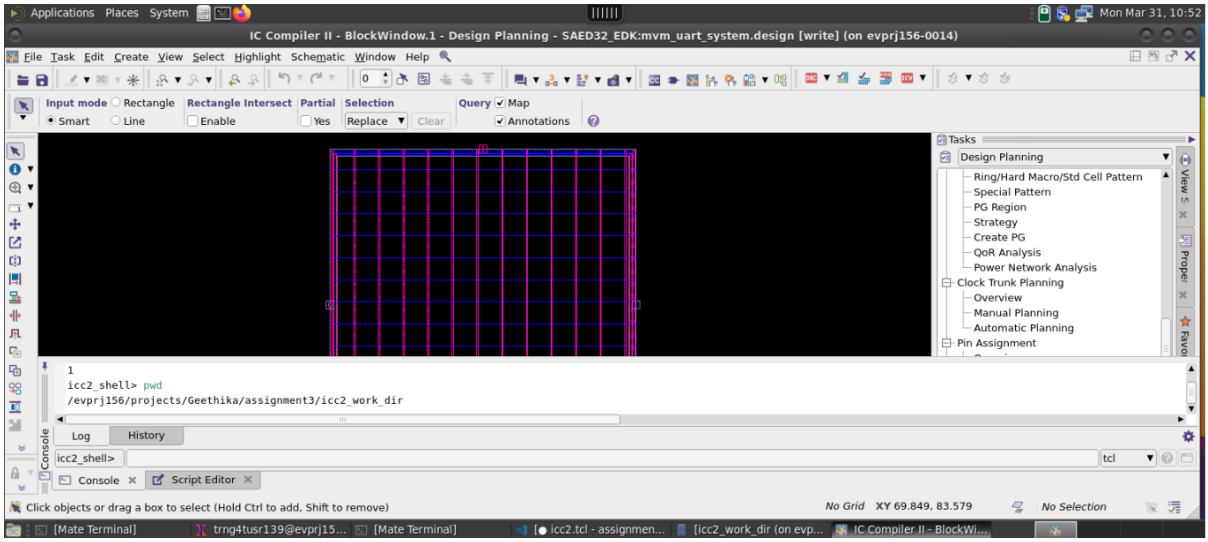
IC Compiler after create PG (After creating VDD VSS power rings)



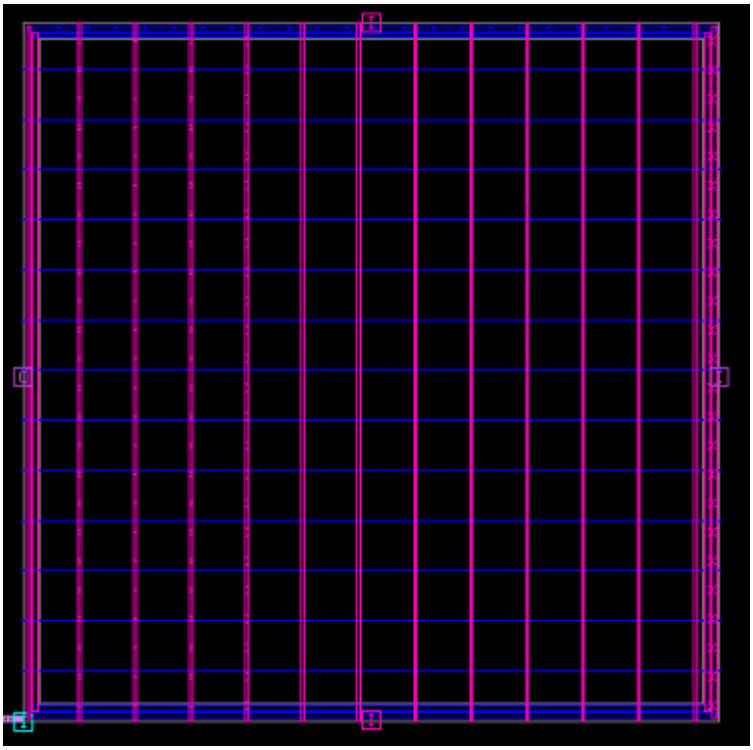
IC compiler after PG prototyping (Routing between VDD and VSS power rings)



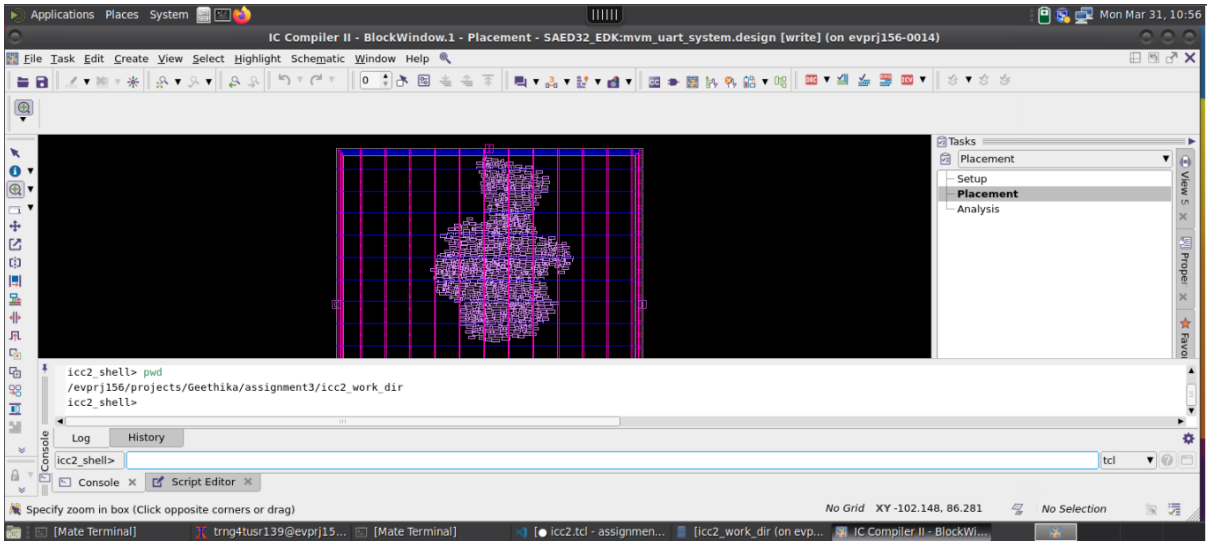
Routing between VDD and VSS power rings



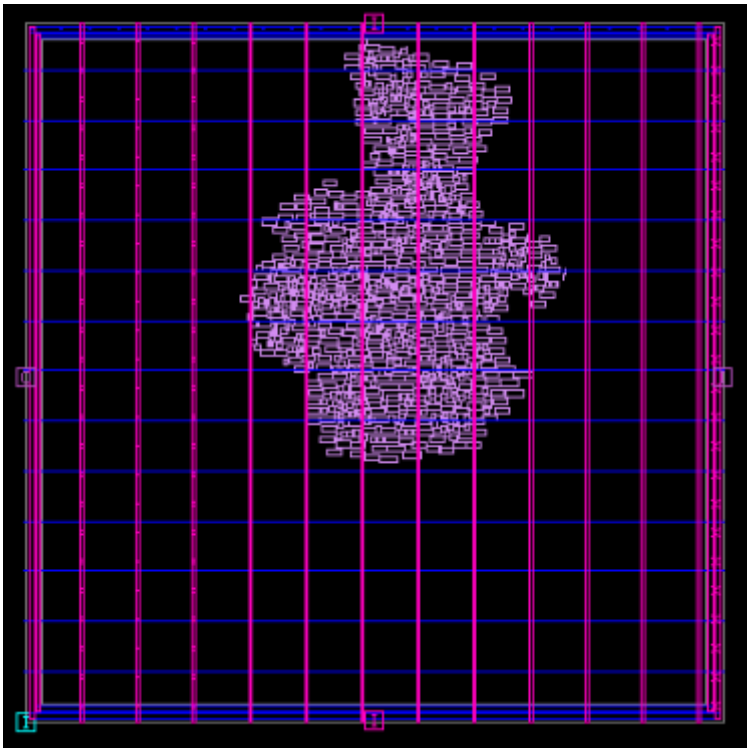
After the pin assignment



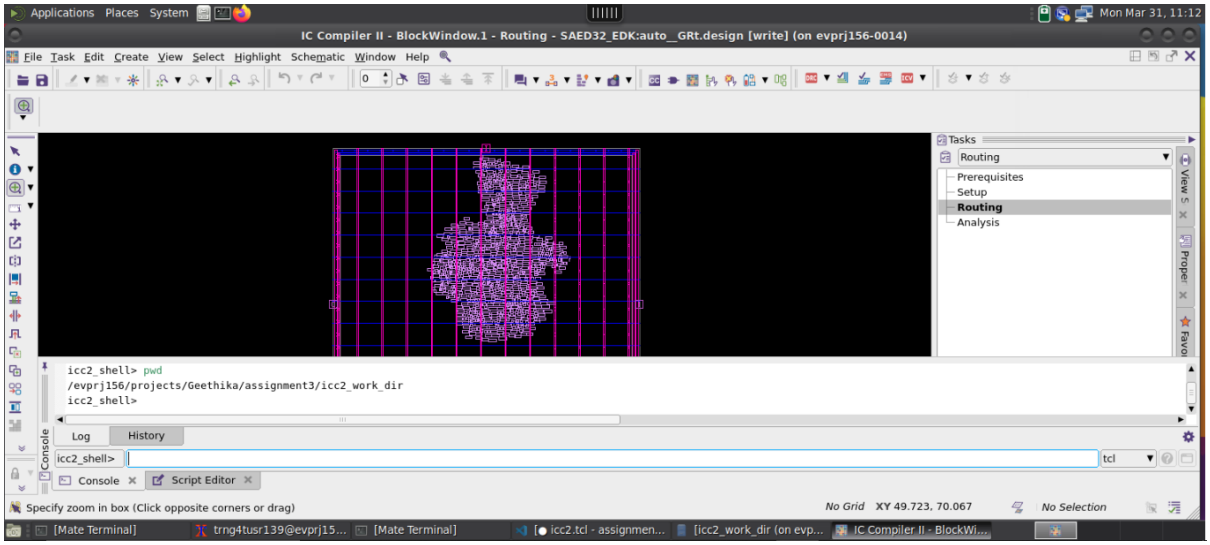
Closer view of the pin assigned core



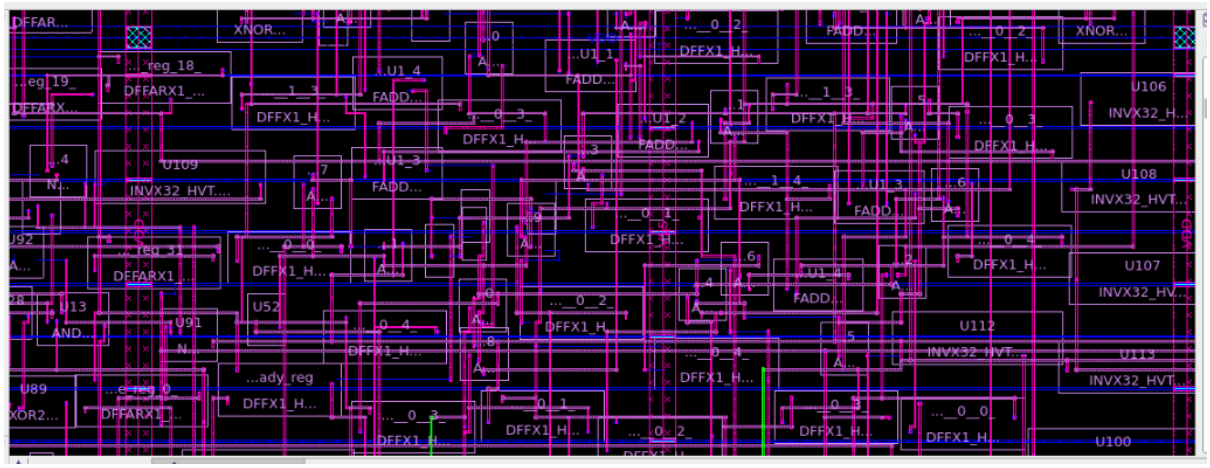
After the cell placement



Closer view of the placed cells in the core

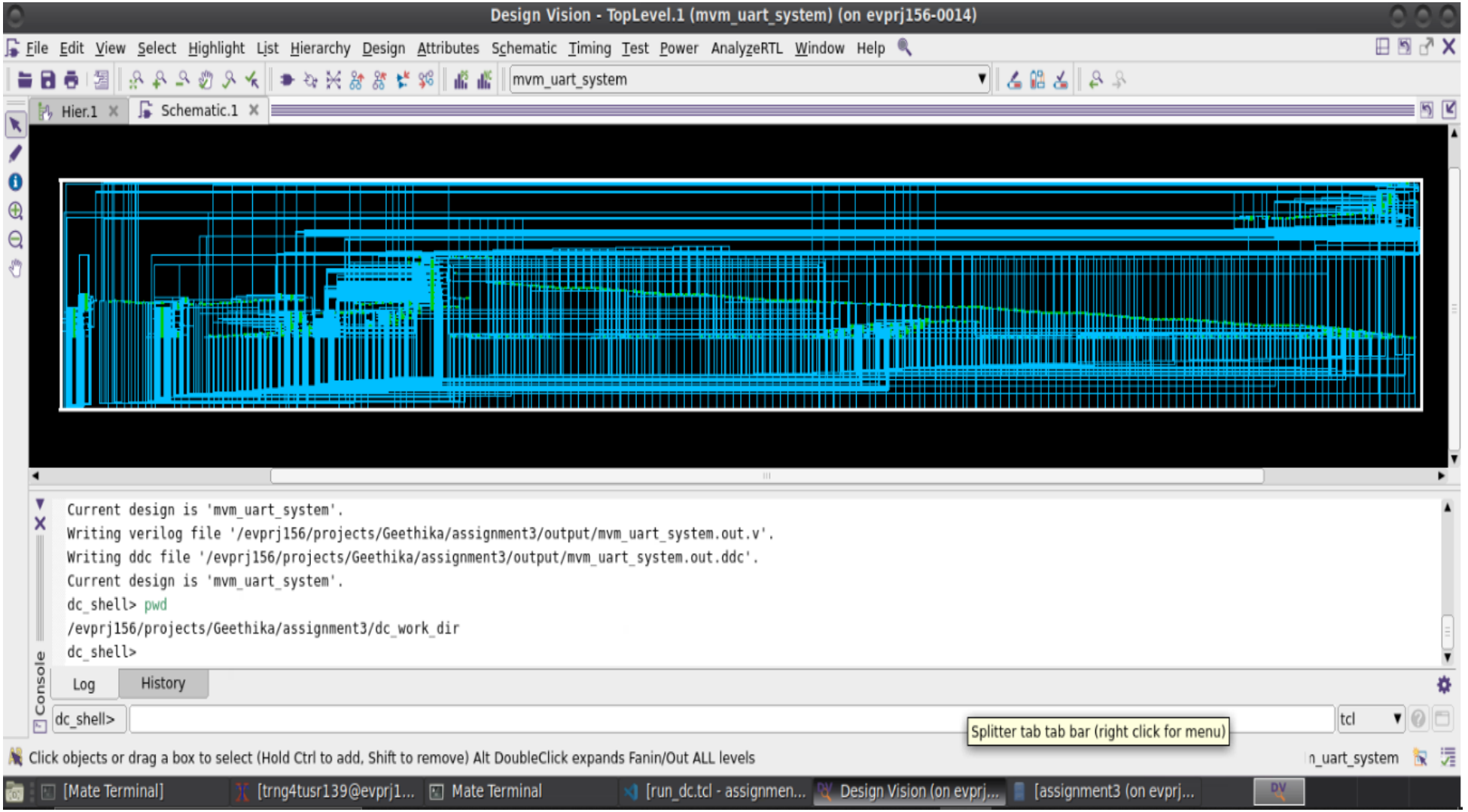


After the routing step



Closer view of the routed cells in the core

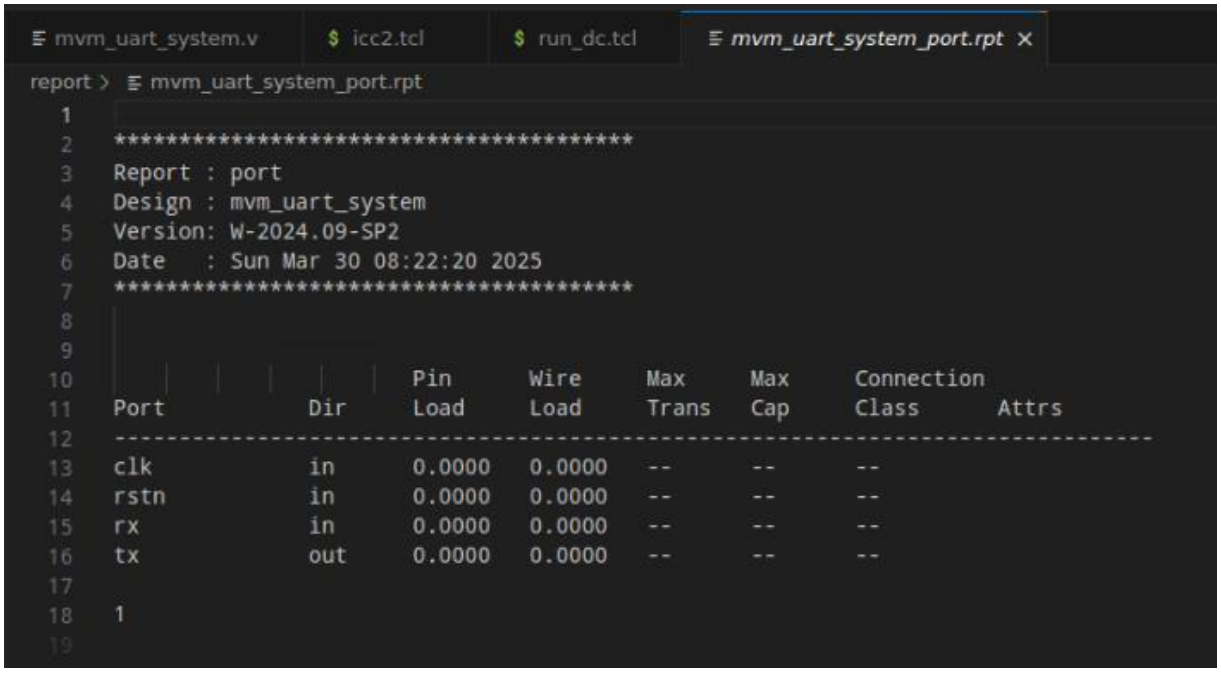
1. The synthesized RTL design schematic visualized in Design Vision of DC



2. Reports generated by the Synthesis (parameter values used in the design R=2, C=2, W_X=2, W_K=2)

a. Ports

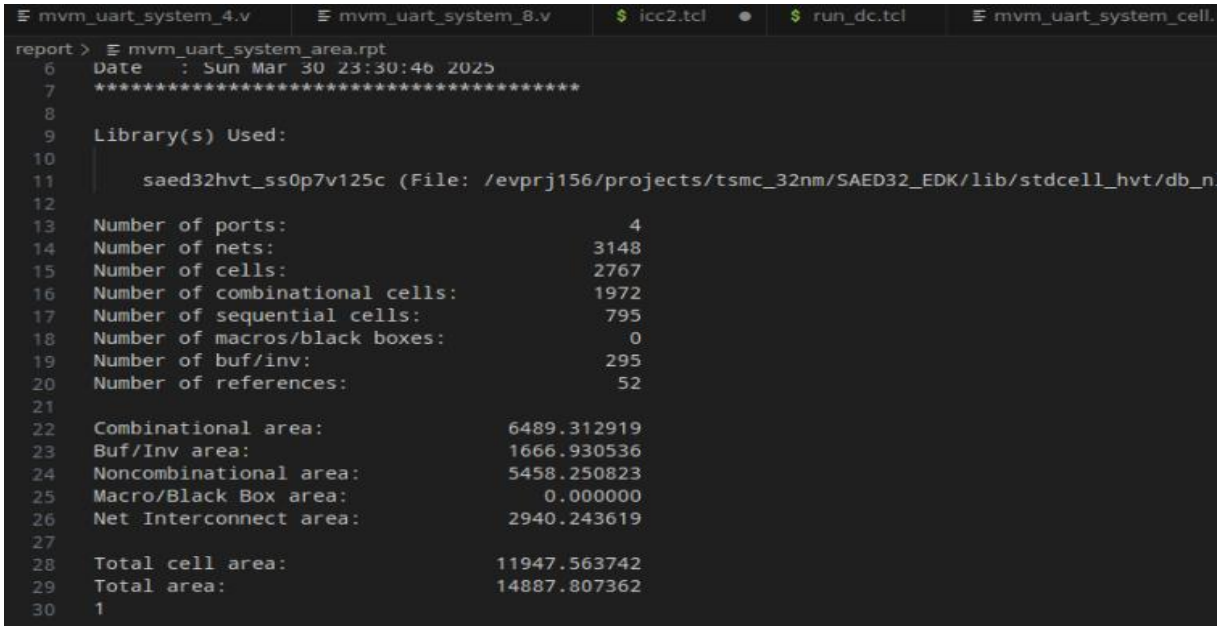
Report generated regarding the ports in the synthesized design as shown in the screenshot below.



```
mvm_uart_system.v | $ icc2.tcl | $ run_dc.tcl | mvm_uart_system_port.rpt
report > mvm_uart_system_port.rpt
1
2  ****************************************
3  Report : port
4  Design : mvm_uart_system
5  Version: W-2024.09-SP2
6  Date   : Sun Mar 30 08:22:20 2025
7  ****************************************
8
9
10                                  Pin     Wire    Max     Max     Connection
11 Port            Dir              Load    Load    Trans   Cap     Class       Attrs
12 --------------------------------------------------------------------------------
13 clk             in               0.0000  0.0000  --      --      --
14 rstn            in               0.0000  0.0000  --      --      --
15 rx              in               0.0000  0.0000  --      --      --
16 tx              out              0.0000  0.0000  --      --      --
17
18 1
19
```

b. Area

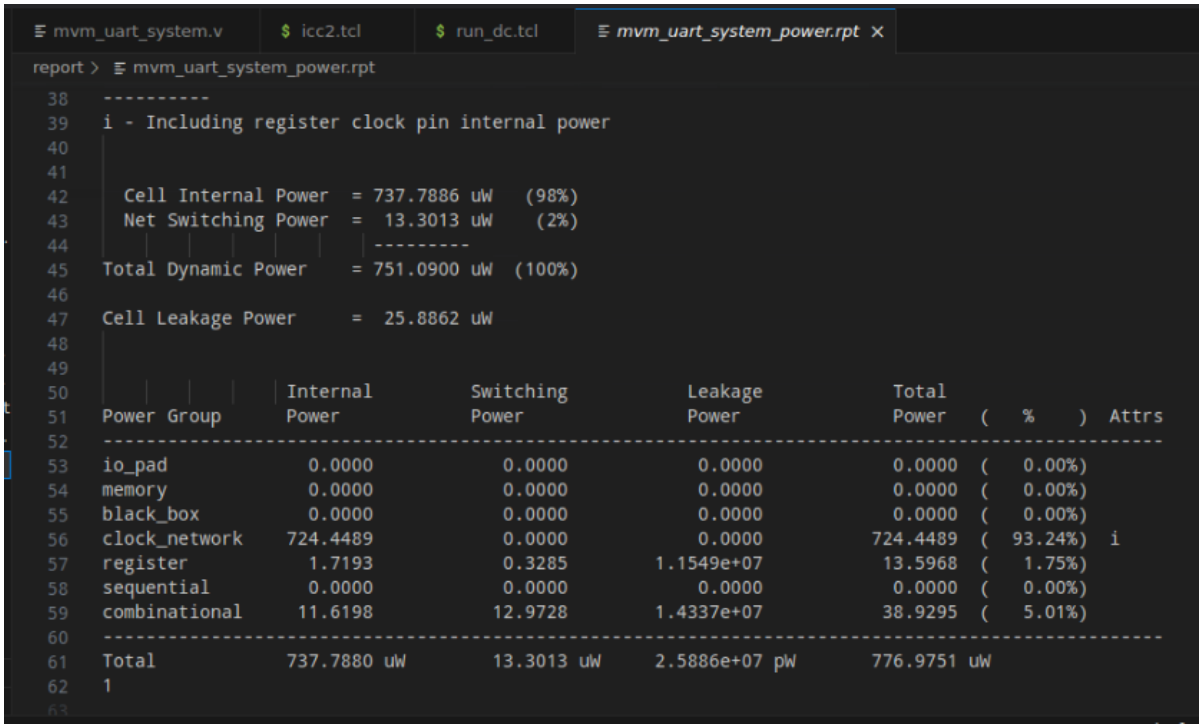
According to the generated report the total area of the synthesized design is 14887.80 square micrometres and other area details of the design as follows in the screenshot.



```
mvm_uart_system_4.v | mvm_uart_system_8.v | $ icc2.tcl | $ run_dc.tcl | mvm_uart_system_cell.
report > mvm_uart_system_area.rpt
6  Date   : Sun Mar 30 23:30:46 2025
7  ****************************************
8
9  Library(s) Used:
10
11     saed32hvt_ss0p7v125c (File: /evprj156/projects/tsmc_32nm/SAED32_EDK/lib/stdcell_hvt/db_n
12
13 Number of ports:                          4
14 Number of nets:                       3148
15 Number of cells:                      2767
16 Number of combinational cells:        1972
17 Number of sequential cells:            795
18 Number of macros/black boxes:            0
19 Number of buf/inv:                     295
20 Number of references:                   52
21
22 Combinational area:               6489.312919
23 Buf/Inv area:                     1666.930536
24 Noncombinational area:            5458.250823
25 Macro/Black Box area:                0.000000
26 Net Interconnect area:            2940.243619
27
28 Total cell area:                 11947.563742
29 Total area:                      14887.807362
30 1
```

c. Power

Power details of the design as shown in the screenshot below.



mvm_uart_system.v | icc2.tcl | run_dc.tcl | mvm_uart_system_power.rpt

report > mvm_uart_system_power.rpt

```
38  ----------
39  i - Including register clock pin internal power
40
41
42    Cell Internal Power  = 737.7886 uW   (98%)
43    Net Switching Power  =  13.3013 uW    (2%)
44                         ---------
45  Total Dynamic Power    = 751.0900 uW  (100%)
46
47  Cell Leakage Power     =  25.8862 uW
48
49
50                         Internal         Switching           Leakage            Total
51  Power Group            Power            Power               Power              Power   (   %    ) Attrs
52  ----------------------------------------------------------------------------------------------------
53  io_pad                   0.0000           0.0000              0.0000             0.0000  (   0.00%)
54  memory                   0.0000           0.0000              0.0000             0.0000  (   0.00%)
55  black_box                0.0000           0.0000              0.0000             0.0000  (   0.00%)
56  clock_network          724.4489           0.0000              0.0000           724.4489  (  93.24%)  i
57  register                 1.7193           0.3285          1.1549e+07            13.5968  (   1.75%)
58  sequential               0.0000           0.0000              0.0000             0.0000  (   0.00%)
59  combinational           11.6198          12.9728          1.4337e+07            38.9295  (   5.01%)
60  ----------------------------------------------------------------------------------------------------
61  Total                  737.7880 uW       13.3013 uW       2.5886e+07 pW        776.9751 uW
62  1
63
```

d. Timings

According to the report generated slack has violated in almost every max paths. It is showing a negative slack. Below are the two-timing reports and a screenshot extracted from the generated report during the synthesize.

```
****************************************
Report : timing
        -path full
        -delay max
        -nets
        -max_paths 100
        -transition_time
        -capacitance
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Mon Mar 31 09:21:43 2025
****************************************
Operating Conditions: ss0p7v125c   Library: saed32hvt_ss0p7v125c
Wire Load Model Mode: enclosed
```

```
Startpoint: UART_TX_state_reg_15_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: AXIS_MVM_SKID_buffer_reg_6_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
mvm_uart_system    8000                  saed32hvt_ss0p7v125c

Point                                Fanout       Cap     Trans      Incr       Path
-----------------------------------------------------------------------------------------
clock clk (rise edge)                                                0.000      0.000
clock network delay (ideal)                                          0.000      0.000
UART_TX_state_reg_15_/CLK (DFFARX1_HVT)                    0.000     0.000      0.000 r
UART_TX_state_reg_15_/QN (DFFARX1_HVT)                     0.172     0.508      0.508 r
n52 (net)                            1        0.486                0.000      0.508 r
U58/Y (NAND4X0_HVT)                                        0.324     0.433      0.941 f
UART_TX_n218 (net)                   1        0.585                0.000      0.941 f
U59/Y (NOR4X1_HVT)                                         0.114     0.560      1.502 r
UART_TX_n214 (net)                   3        1.324                0.000      1.502 r
U27/Y (AND2X1_HVT)                                         0.097     0.273      1.775 r
n13 (net)                            1        0.484                0.000      1.775 r
U28/Y (AND3X1_HVT)                                         0.148     0.345      2.120 r
m_ready (net)                        1        1.170                0.000      2.120 r
U89/Y (XOR2X2_HVT)                                         0.160     0.344      2.464 r
AXIS_MVM_SKID_n73 (net)              3        1.389                0.000      2.464 r
U75/Y (OAI22X2_HVT)                                        0.109     0.499      2.964 f
n55 (net)                            5        2.373                0.000      2.964 f
U78/Y (AO21X1_HVT)                                         0.155     0.260      3.224 f
n72 (net)                            6        2.492                0.000      3.224 f
AXIS_MVM_SKID_U65/Y (NAND2X0_HVT)                          0.135     0.182      3.406 r
AXIS_MVM_SKID_n49 (net)              1        0.486                0.000      3.406 r
```

```
AXIS_MVM_SKID_U49/Y (NAND4X0_HVT)                       0.312     0.402      3.808 f
AXIS_MVM_SKID_n35 (net)              1        0.510                0.000      3.808 f
U88/Y (NOR4X1_HVT)                                      0.102     0.726      4.535 r
AXIS_MVM_SKID_n33 (net)              2        0.849                0.000      4.535 r
U90/Y (AND3X1_HVT)                                      0.131     0.325      4.859 r
AXIS_MVM_SKID_n27 (net)              1        0.515                0.000      4.859 r
AXIS_MVM_SKID_U42/Y (NAND2X0_HVT)                       0.158     0.178      5.037 f
AXIS_MVM_SKID_n26 (net)              1        0.630                0.000      5.037 f
U67/Y (OR4X4_HVT)                                       0.088     0.569      5.606 f
AXIS_MVM_SKID_n25 (net)              4        2.348                0.000      5.606 f
U86/Y (NOR4X1_HVT)                                      0.093     0.463      6.069 r
AXIS_MVM_SKID_n16 (net)              1        0.489                0.000      6.069 r
U18/Y (AOI21X1_HVT)                                     0.114     0.482      6.551 f
n6 (net)                             4        1.797                0.000      6.551 f
U15/Y (NAND2X0_HVT)                                     0.129     0.150      6.701 r
n4 (net)                             1        0.515                0.000      6.701 r
U17/Y (NAND2X0_HVT)                                     0.143     0.168      6.870 f
AXIS_MVM_SKID_n91 (net)              1        0.510                0.000      6.870 f
AXIS_MVM_SKID_buffer_reg_6_/D (DFFX1_HVT)               0.143     0.000      6.870 f
data arrival time                                                            6.870

clock clk (rise edge)                                                1.400      1.400
clock network delay (ideal)                                          0.000      1.400
AXIS_MVM_SKID_buffer_reg_6_/CLK (DFFX1_HVT)                          0.000      1.400 r
library setup time                                                  -0.323      1.077
data required time                                                               1.077
--------------------------------------------------------------------------------------
data required time                                                               1.077
data arrival time                                                               -6.870
--------------------------------------------------------------------------------------
slack (VIOLATED)                                                                -5.792
```

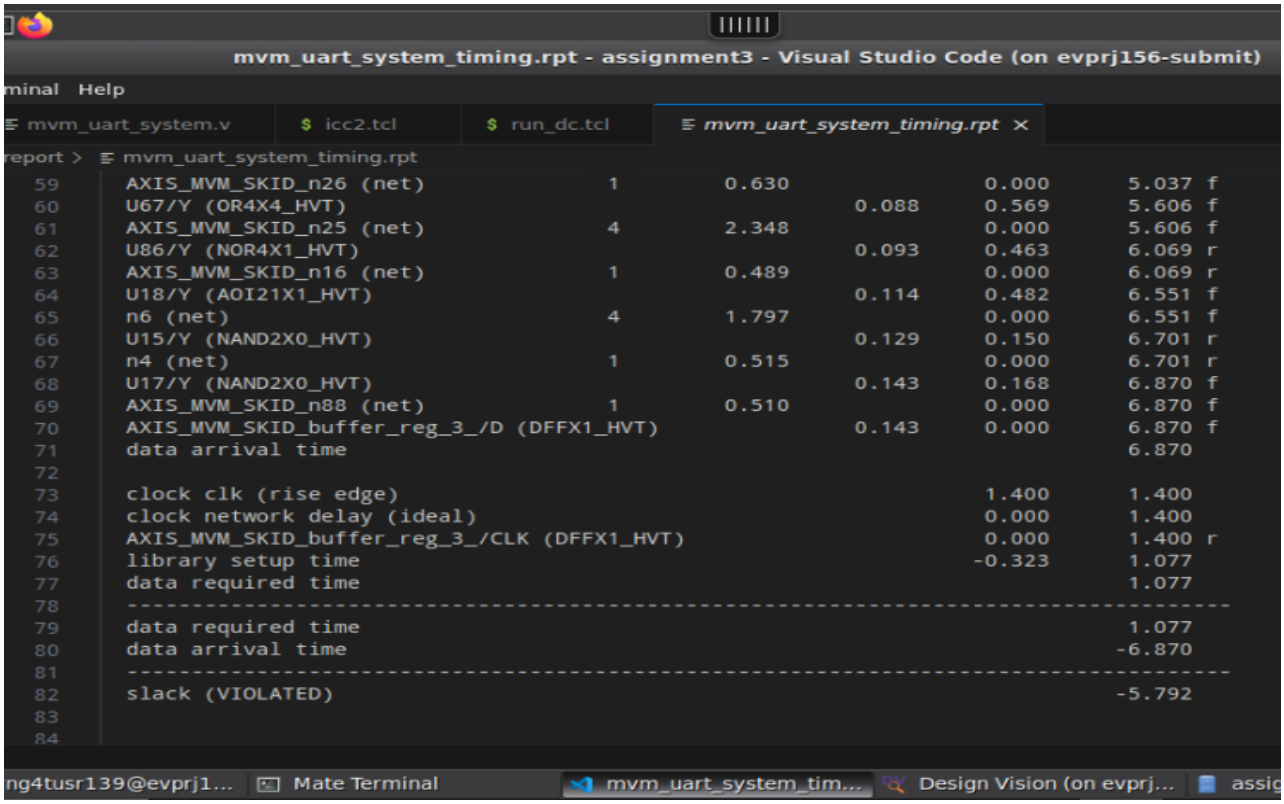
```
Startpoint: UART_TX_state_reg_15_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: AXIS_MVM_SKID_buffer_reg_7_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
mvm_uart_system    8000                  saed32hvt_ss0p7v125c

Point                                Fanout       Cap     Trans      Incr       Path
-------------------------------------------------------------------------------------
clock clk (rise edge)                                                0.000      0.000
clock network delay (ideal)                                          0.000      0.000
UART_TX_state_reg_15_/CLK (DFFARX1_HVT)                  0.000     0.000      0.000 r
UART_TX_state_reg_15_/QN (DFFARX1_HVT)                   0.172     0.508      0.508 r
n52 (net)                            1        0.486              0.000      0.508 r
U58/Y (NAND4X0_HVT)                                      0.324     0.433      0.941 f
UART_TX_n218 (net)                   1        0.585              0.000      0.941 f
U59/Y (NOR4X1_HVT)                                       0.114     0.560      1.502 r
UART_TX_n214 (net)                   3        1.324              0.000      1.502 r
U27/Y (AND2X1_HVT)                                       0.097     0.273      1.775 r
n13 (net)                            1        0.484              0.000      1.775 r
U28/Y (AND3X1_HVT)                                       0.148     0.345      2.120 r
m_ready (net)                        1        1.170              0.000      2.120 r
U89/Y (XOR2X2_HVT)                                       0.160     0.344      2.464 r
AXIS_MVM_SKID_n73 (net)              3        1.389              0.000      2.464 r
U75/Y (OAI22X2_HVT)                                      0.109     0.499      2.964 f
n55 (net)                            5        2.373              0.000      2.964 f
U78/Y (AO21X1_HVT)                                       0.155     0.260      3.224 f
n72 (net)                            6        2.492              0.000      3.224 f
AXIS_MVM_SKID_U65/Y (NAND2X0_HVT)                        0.135     0.182      3.406 r
AXIS_MVM_SKID_n49 (net)              1        0.486              0.000      3.406 r
AXIS_MVM_SKID_U49/Y (NAND4X0_HVT)                        0.312     0.402      3.808 f
```

```
AXIS_MVM_SKID_n35 (net)              1        0.510              0.000      3.808 f
U88/Y (NOR4X1_HVT)                                      0.102   0.726      4.535 r
AXIS_MVM_SKID_n33 (net)              2        0.849              0.000      4.535 r
U90/Y (AND3X1_HVT)                                      0.131   0.325      4.859 r
AXIS_MVM_SKID_n27 (net)              1        0.515              0.000      4.859 r
AXIS_MVM_SKID_U42/Y (NAND2X0_HVT)                       0.158   0.178      5.037 f
AXIS_MVM_SKID_n26 (net)              1        0.630              0.000      5.037 f
U67/Y (OR4X4_HVT)                                       0.088   0.569      5.606 f
AXIS_MVM_SKID_n25 (net)              4        2.348              0.000      5.606 f
U86/Y (NOR4X1_HVT)                                      0.093   0.463      6.069 r
AXIS_MVM_SKID_n16 (net)              1        0.489              0.000      6.069 r
U18/Y (AOI21X1_HVT)                                     0.114   0.482      6.551 f
n6 (net)                             4        1.797              0.000      6.551 f
AXIS_MVM_SKID_U25/Y (AO22X1_HVT)                        0.097   0.339      6.890 f
AXIS_MVM_SKID_n92 (net)              1        0.510              0.000      6.890 f
AXIS_MVM_SKID_buffer_reg_7_/D (DFFX1_HVT)               0.097   0.000      6.890 f
data arrival time                                                          6.890

clock clk (rise edge)                                                      1.400      1.400
clock network delay (ideal)                                                0.000      1.400
AXIS_MVM_SKID_buffer_reg_7_/CLK (DFFX1_HVT)                                0.000      1.400 r
library setup time                                                        -0.294      1.106
data required time                                                                    1.106
--------------------------------------------------------------------------------------------
data required time                                                                    1.106
data arrival time                                                                    -6.890
--------------------------------------------------------------------------------------------
slack (VIOLATED)                                                                     -5.784
```

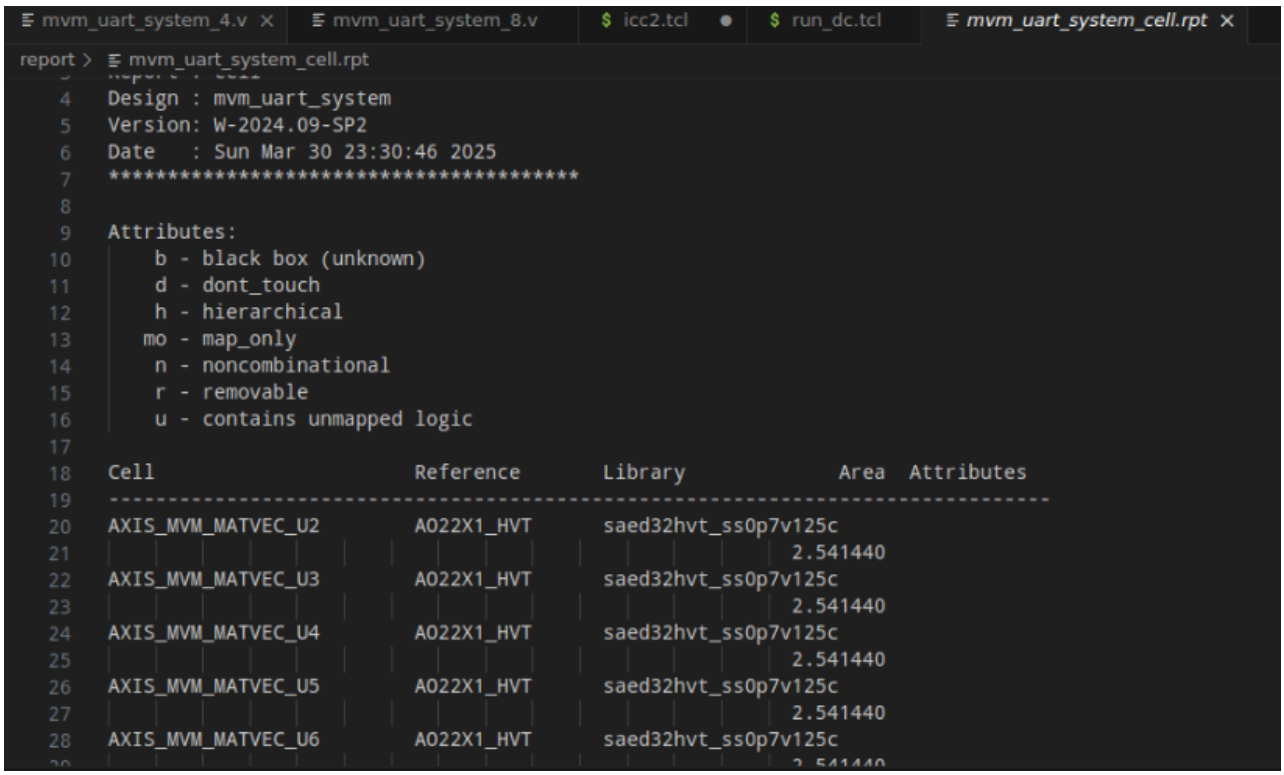


```
mvm_uart_system_timing.rpt - assignment3 - Visual Studio Code (on evprj156-submit)
minal  Help
mvm_uart_system.v | $ icc2.tcl | $ run_dc.tcl | mvm_uart_system_timing.rpt
report > mvm_uart_system_timing.rpt
  AXIS_MVM_SKID_n26 (net)                          1       0.630                0.000       5.037 f
  U67/Y (OR4X4_HVT)                                                     0.088   0.569       5.606 f
  AXIS_MVM_SKID_n25 (net)                          4       2.348                0.000       5.606 f
  U86/Y (NOR4X1_HVT)                                                    0.093   0.463       6.069 r
  AXIS_MVM_SKID_n16 (net)                          1       0.489                0.000       6.069 r
  U18/Y (AOI21X1_HVT)                                                   0.114   0.482       6.551 f
  n6 (net)                                         4       1.797                0.000       6.551 f
  U15/Y (NAND2X0_HVT)                                                   0.129   0.150       6.701 r
  n4 (net)                                         1       0.515                0.000       6.701 r
  U17/Y (NAND2X0_HVT)                                                   0.143   0.168       6.870 f
  AXIS_MVM_SKID_n88 (net)                          1       0.510                0.000       6.870 f
  AXIS_MVM_SKID_buffer_reg_3_/D (DFFX1_HVT)                             0.143   0.000       6.870 f
  data arrival time                                                                         6.870

  clock clk (rise edge)                                                             1.400   1.400
  clock network delay (ideal)                                                       0.000   1.400
  AXIS_MVM_SKID_buffer_reg_3_/CLK (DFFX1_HVT)                                       0.000   1.400 r
  library setup time                                                               -0.323   1.077
  data required time                                                                        1.077
  ------------------------------------------------------------------------------------------------
  data required time                                                                        1.077
  data arrival time                                                                        -6.870
  ------------------------------------------------------------------------------------------------
  slack (VIOLATED)                                                                         -5.792
ng4tusr139@evprj1... | Mate Terminal | mvm_uart_system_tim... | Design Vision (on evprj... | assig
```

e. No. of cells

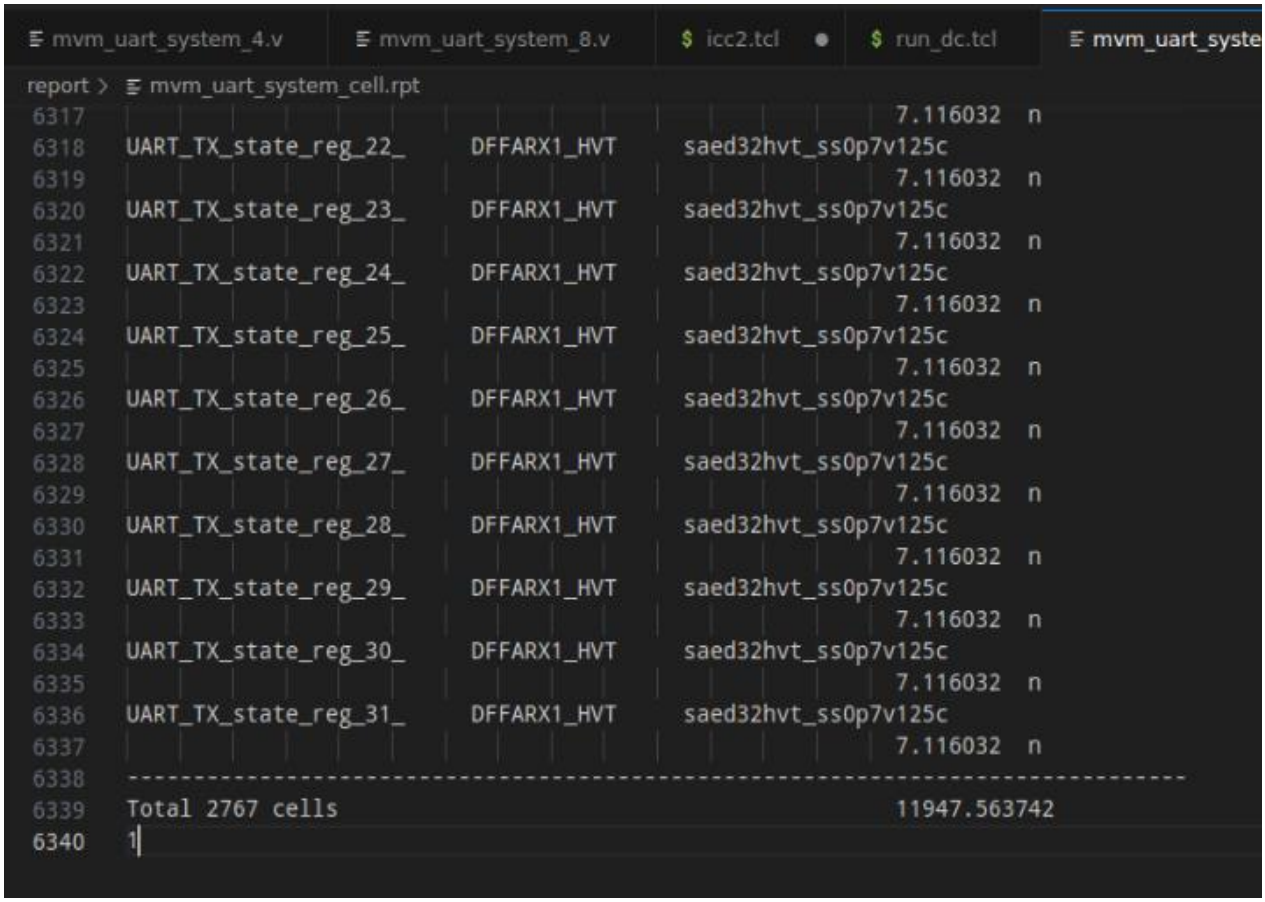
According to the report there are 2767 cells in the synthesized design spreading over 11947.56 square micrometres.



```
mvm_uart_system_4.v | mvm_uart_system_8.v | $ icc2.tcl | $ run_dc.tcl | mvm_uart_system_cell.rpt
report > mvm_uart_system_cell.rpt
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Sun Mar 30 23:30:46 2025
****************************************

Attributes:
    b - black box (unknown)
    d - dont_touch
    h - hierarchical
   mo - map_only
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library             Area  Attributes
------------------------------------------------------------------------------
AXIS_MVM_MATVEC_U2      AO22X1_HVT      saed32hvt_ss0p7v125c
                                                          2.541440
AXIS_MVM_MATVEC_U3      AO22X1_HVT      saed32hvt_ss0p7v125c
                                                          2.541440
AXIS_MVM_MATVEC_U4      AO22X1_HVT      saed32hvt_ss0p7v125c
                                                          2.541440
AXIS_MVM_MATVEC_U5      AO22X1_HVT      saed32hvt_ss0p7v125c
                                                          2.541440
AXIS_MVM_MATVEC_U6      AO22X1_HVT      saed32hvt_ss0p7v125c
```


mvm_uart_system_4.v
mvm_uart_system_8.v
icc2.tcl
run_dc.tcl
mvm_uart_syste
report > mvm_uart_system_cell.rpt
6317 7.116032 n
6318 UART_TX_state_reg_22_ DFFARX1_HVT saed32hvt_ss0p7v125c
6319 7.116032 n
6320 UART_TX_state_reg_23_ DFFARX1_HVT saed32hvt_ss0p7v125c
6321 7.116032 n
6322 UART_TX_state_reg_24_ DFFARX1_HVT saed32hvt_ss0p7v125c
6323 7.116032 n
6324 UART_TX_state_reg_25_ DFFARX1_HVT saed32hvt_ss0p7v125c
6325 7.116032 n
6326 UART_TX_state_reg_26_ DFFARX1_HVT saed32hvt_ss0p7v125c
6327 7.116032 n
6328 UART_TX_state_reg_27_ DFFARX1_HVT saed32hvt_ss0p7v125c
6329 7.116032 n
6330 UART_TX_state_reg_28_ DFFARX1_HVT saed32hvt_ss0p7v125c
6331 7.116032 n
6332 UART_TX_state_reg_29_ DFFARX1_HVT saed32hvt_ss0p7v125c
6333 7.116032 n
6334 UART_TX_state_reg_30_ DFFARX1_HVT saed32hvt_ss0p7v125c
6335 7.116032 n
6336 UART_TX_state_reg_31_ DFFARX1_HVT saed32hvt_ss0p7v125c
6337 7.116032 n
6338 ---
6339 Total 2767 cells 11947.563742
6340 1

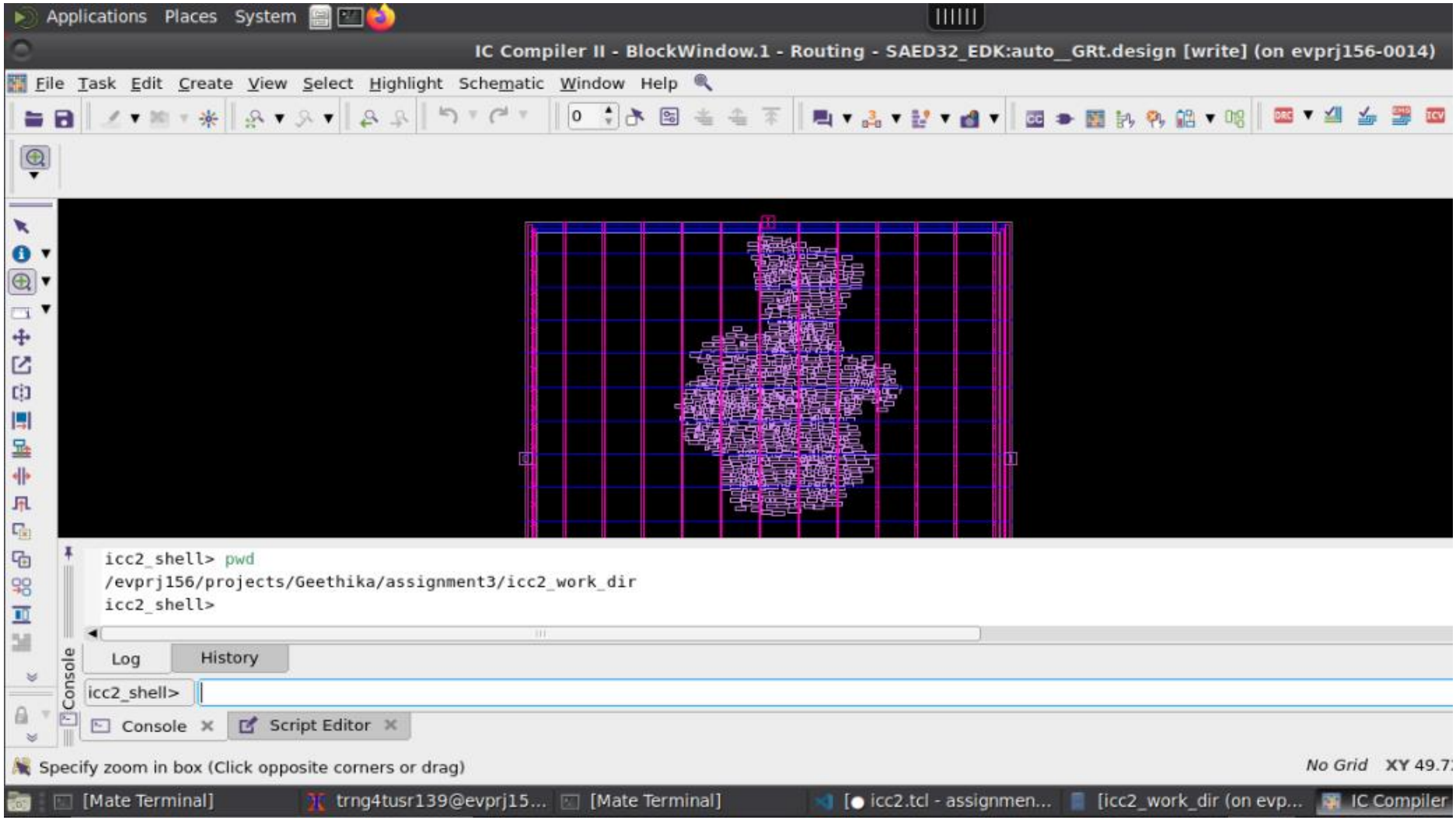
3. Comparison of the area and the power values of the design for different Parameter values

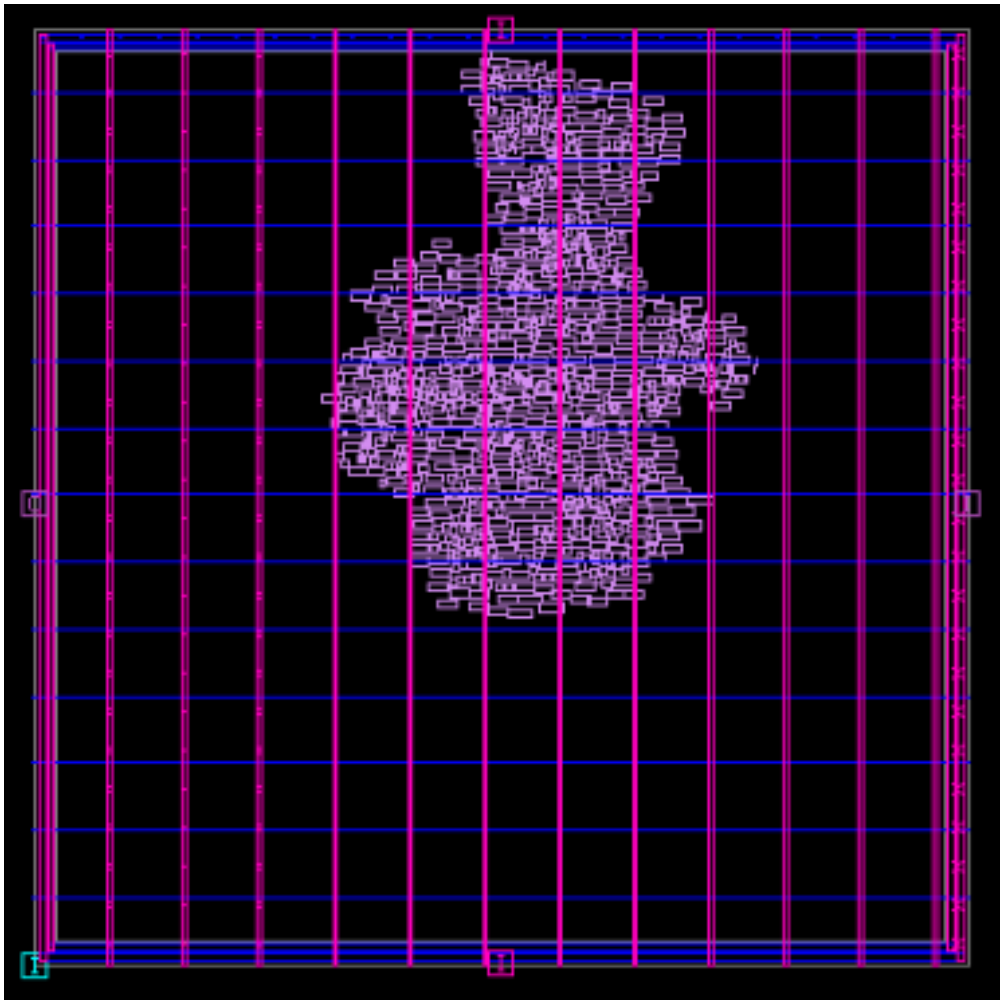
Following table shows the area and the power values for different parameter values of the “mvm_uart_system.sv”.

S/N	Parameter Values				Area (um^2)	Power (uW)
	R	C	W_X	W_K		
1	2	2	2	2	4950.25	776.98
2	4	4	4	4	14887.80	1996.1
3	8	8	8	8	107798.54	8873.3

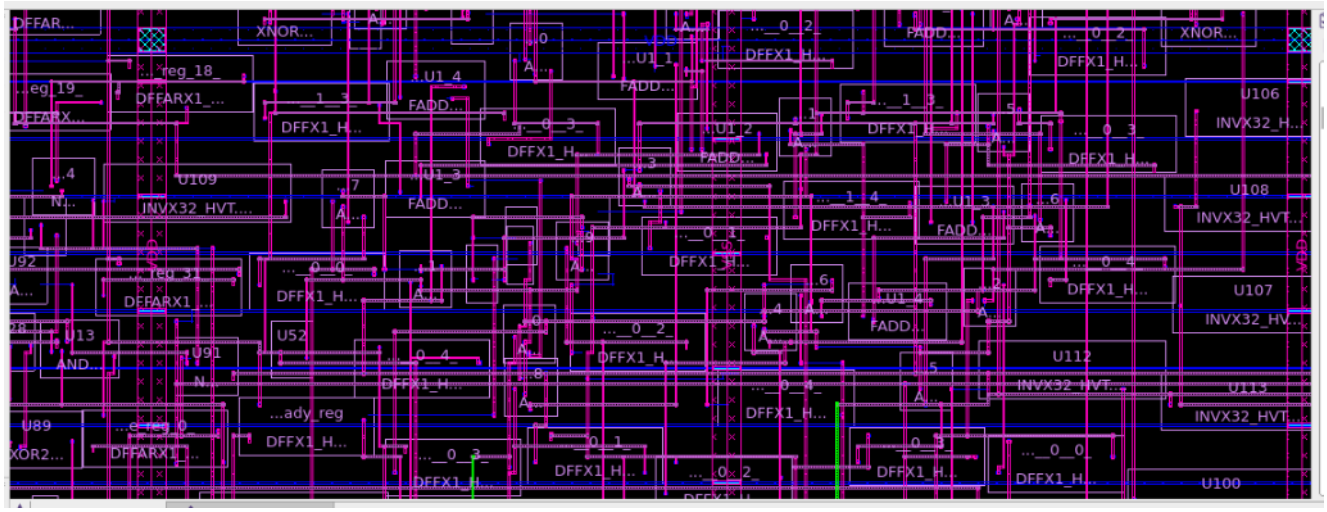
4. PnR layout visualized inside ICC2

Below is the P&R layout of the synthesized design of the “mvm_uart_system.sv”. In here I have came across an issue that cells have not distributed inside the core area.





After the placement and routing of the cells



Routing of the cells (Zoomed view of the design after the routing)