CSE 201: Digital Logic Design
SR Flip Flop

Prepared By

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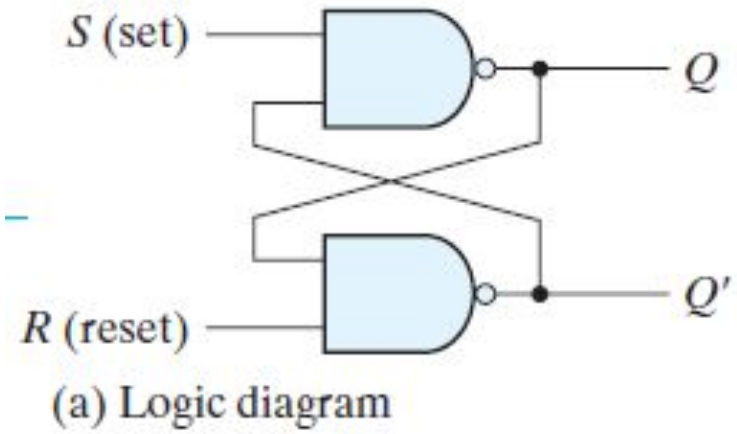
CSE, MIST

SR LATCH



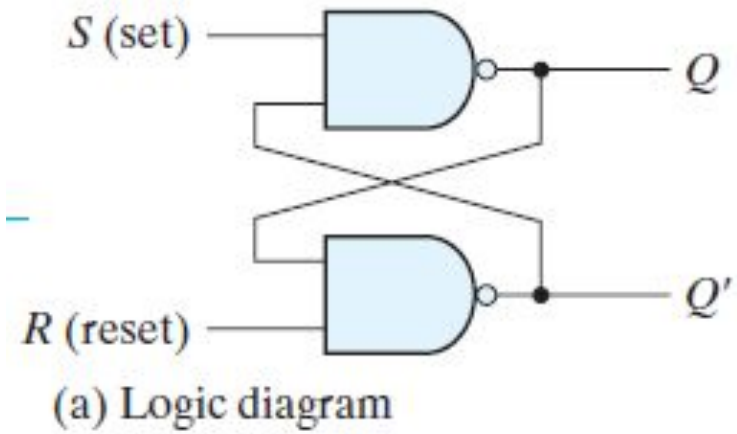
(a) Logic diagram

S	R	Q	Q’	
1	0	0	1	
1	1	0	1	Memory
0	1	1	0	
1	1	1	0	Memory
0	0	Forbidden		

Truth Table of NAND gate

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

SR FLIP FLOP

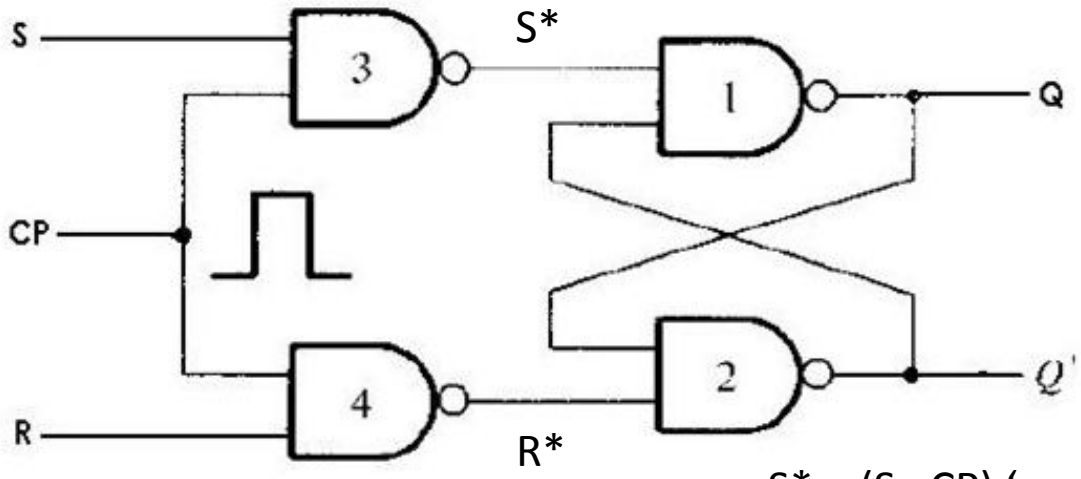


(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	Memory
0	1	1	0	
1	1	1	0	Memory
0	0	Invalid		

S	R	Q	Q'
0	0	Invalid	
0	1	1	0
1	0	0	1
1	1	Memory	

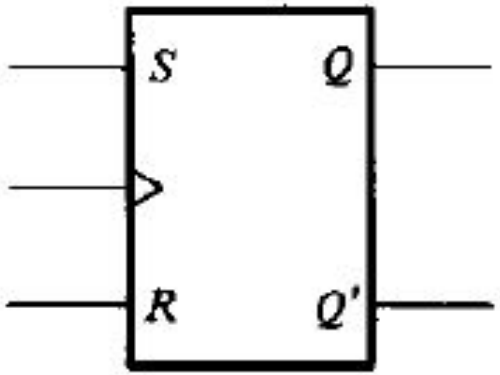
SR FLIP FLOP



S* = (S . CP) '
= S' + CP'

R* = (R . CP) '
= R' + CP'

Graphic symbol of SR flip flop



(a) *RS*

S*	R*	Q	Q'
0	0	Invalid	
0	1	1	0
1	0	0	1
1	1	Memory	

CP	S	R	Q	Q'
0	x	x	Memory	
1	0	0	Memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	

SR FLIP FLOP

Truth Table of SR flip flop

CP	S	R	Q_{t+1}	
0	x	x	Q_t	
1	0	0	Q_t	
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Invalid	

Characteristics Table of SR flip flop

Q_t	S	R	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	invalid
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	invalid

Excitation Table of SR flip flop

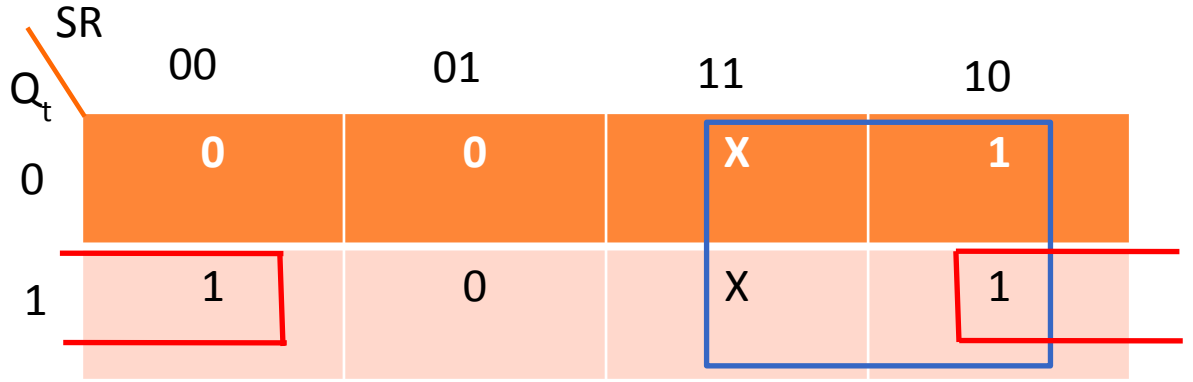
Q_t	Q_{t+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

SR FLIP FLOP

Characteristics Table of SR flip flop

Q_t	S	R	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	invalid
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	invalid

Characteristics Equation of SR flip flop



$$Q_{t+1} = S + Q_t R'$$

What is the value of Q'_{t+1}?

SR FLIP FLOP

Excitation Table of SR flip flop

Q_t	Q_{t+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Similarly find the value of S and R