

# CSE 306

## (Microprocessors, Micro-controllers and Assembly Language Sessional)

### Assembly Language Basics

Iyolita Islam

Department of Computer Science and Engineering  
Military Institute of Science and Technology

Last Updated: March 22, 2021

# Outline

- 1 Number System
- 2 CPU Organization
- 3 Input-Output

# Number Systems

- Decimal
- Binary
- Octal
- Hexadecimal
- Conversion between the number systems

Number System	Required memory for each digit
Decimal	4 bit
Binary	1 bit
Octal	3 bit
Hexa decimal	4 bit

# How integers are represented?

- **Byte:** A string of eight bits.
- **Word:** Two bytes form a word.
- **LSB:** The rightmost bit in a byte or word.
- **MSB:** The leftmost bit in a byte or word.



# Unsigned Integers

- Represents a magnitude only
- Can never be negative
- No bit is required to represent the sign
- i.e.: addresses of memory locations, counters, ASCII character codes etc.
- Largest value in a byte:  $1111\ 1111 = FFh = 255$
- Largest value in a word:  $1111\ 1111\ 1111\ 1111 = FFFFh = 65535$

# Signed Integers

- Can be positive or negative
- The MSB is reserved to represent the sign: 1 = Negative; 0 = Positive
- Negative numbers can be represented in either *1's complement* or *2's complement*.
- **1's Complement:** Complement each bit of a number
- **2's Complement:** Add 1 to the 1's complement of a number

# 1's Complement and 2's Complement

- Find 1's complement of 5 as a word.

$$\begin{array}{r} 0000\ 0000\ 0000\ 0101 \\ 1's\ complement = 1111\ 1111\ 1111\ 1010 \end{array}$$

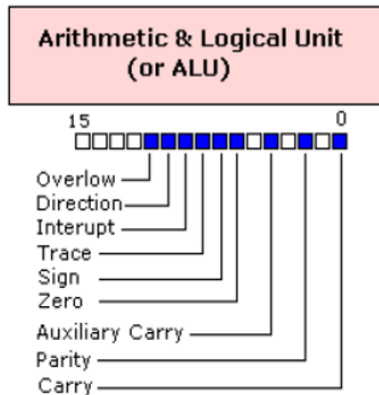
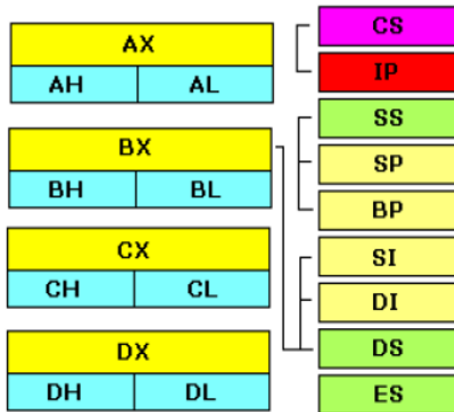
- Note that, if we add 5 and its 1's complement we get *1111 1111 1111 1111*.

- Find 2's complement of 5 as a word.

$$\begin{array}{r} 0000\ 0000\ 0000\ 0101 \\ 1's\ complement = 1111\ 1111\ 1111\ 1010 \\ \phantom{1's\ complement = 1111\ 1111\ 1111\ } + 1 \\ \hline 2's\ complement = 1111\ 1111\ 1111\ 1011 \end{array}$$

# Inside CPU

## Central Processing Unit (or CPU)





# CPU Registers

- Data registers
- Segment registers
- Pointer and Index registers
- Flags register
- Special purpose registers:
  - Debug registers
  - Machine Control registers

# Data registers

- 4 16-bit registers
- Used for general data manipulation.
- Each register is divided into high and low bytes.
- For example: High byte of AX is AH and low byte is AL.

AX	Accumulator register: arithmetic, logic and data transfer functions
BX	Address register
CX	Count register: loop counter
DX	Data register: multiplication, division

AX	16 bit access (bits 15:0)
AH	High byte access (15:8)
AL	Low byte access (7:0)

# Memory Basics

- **Memory segment:** A block of  $2^{16}$  or 64K consecutive memory bytes.
  - Each segment is identified by a segment number, starting with 0.
  - Segment number is 16 bits.
- **Physical address:** A memory location is assigned a 20-bit physical address.
- **Logical address:** A memory location can be specified as segment:offset.
  - For example, A4FB:4872 means segment = A4FBh and offset = 4872h
  - To obtain 20-bit physical address, shift segment address by 4 bits left and add the offset

Segment address: A4FBh  
Left Shift: A4FB0h  
Offset: + 4872h

---

Physical address = A9822h

# Segment registers

- 4 16-bit registers
- Used by the processor to access memory location.

Register	Name	Starting Address
SS	Stack Segment	0F69h
DS	Data Segment	0F89h
CS	Code Segment	0F8Ah
ES	Extra Segment	

# Pointer and Index Registers

- 4 16-bit registers
- Can be used for arithmetic and other operations.

SI	Source Index to point memory locations in DS
DI	Destination Index to perform same function as SI
SP	Stack pointer
BP	Base pointer to access stack as well as other segments

- Instruction Pointer (IP):
  - To access instructions, 8086 uses CS and IP
  - CS contains the segment number of the next instruction
  - IP contains the offset

# FLAGS Register

- Contains the status of the microprocessor by setting individual bits called FLAGS
- Two kinds of flags: Status flags and Control flags
- **Status Flags:** Reflect the result of an instruction executed by the processor.
- **Controls Flags:** Enable or disable certain operations of the processor.

# FLAGS Register

Flag	Intel Mnemonic	Description
Overflow	OF	
Direction	DF	the direction of string processing. 1= highest address to lowest 0= lowest address to highest
Interrupt Enable	IF	1= if interrupts are enable
Sign	SF	
Zero	ZF	
Auxiliary Carry	AF	carry/borrow in BCD arithmetic
Parity	PF	
Carry	CF	

Function Number	Routine
1	Single key input
2	Single character output
9	Character string output



