CSE-323
Computer Architecture

Superscalar Processor

Lecturer Afia Anjum
Military Institute of Science and technology

Pipeline

	1	2	3	4	5	6	7	8	9	10	11	12
Instruction 1	FI	DI	CO	FO	EI	WO						
Instruction 2							FI	DI	CO	FO	EI	WO

Parallelism in Pipeline

	1	2	3	4	5	6	7	8	9	10
Instruction 1	FI	DI	CO	FO	EI	WO				
Instruction 2		FI	DI	CO	FO	EI	WO			
Instruction 3			FI	DI	CO	FO	EI	WO		
Instruction 4				FI	DI	CO	FO	EI	WO	
Instruction 5					FI	DI	CO	FO	EI	WO

Superscalar Processor

- Superscalar architecture (SSA) is a method of parallel computing used in many processors.
- In a superscalar computer, the central processing unit (CPU) manages multiple instruction pipelines to execute several instructions concurrently during a clock cycle. This is achieved by feeding the different pipelines through a number of execution units within the processor.
- In a SSA design, the processor or the instruction compiler is able to determine whether an instruction can be carried out independently of other sequential instructions, or whether it has a dependency on another instruction and must be executed sequentially.
- A SSA processor fetches multiple instructions at a time, and attempts to find nearby instructions that are independent of each other and therefore can be executed in parallel.
- Based on the dependency analysis, the processor may issue and execute instructions in an order that differs from that of the original machine code.
- SSA introduces a new level of parallelism, called instruction-level parallelism.

Superscalar Processor

	1	2	3	4	5	6	7	8	9	10		
Instruction 1	FI	DI	CO	FO	EI	WO						
Instruction 2	FI	DI	CO	FO	EI	WO						
Instruction 3							FI	DI	CO	FO	EI	WO
Instruction 4							FI	DI	CO	FO	EI	WO

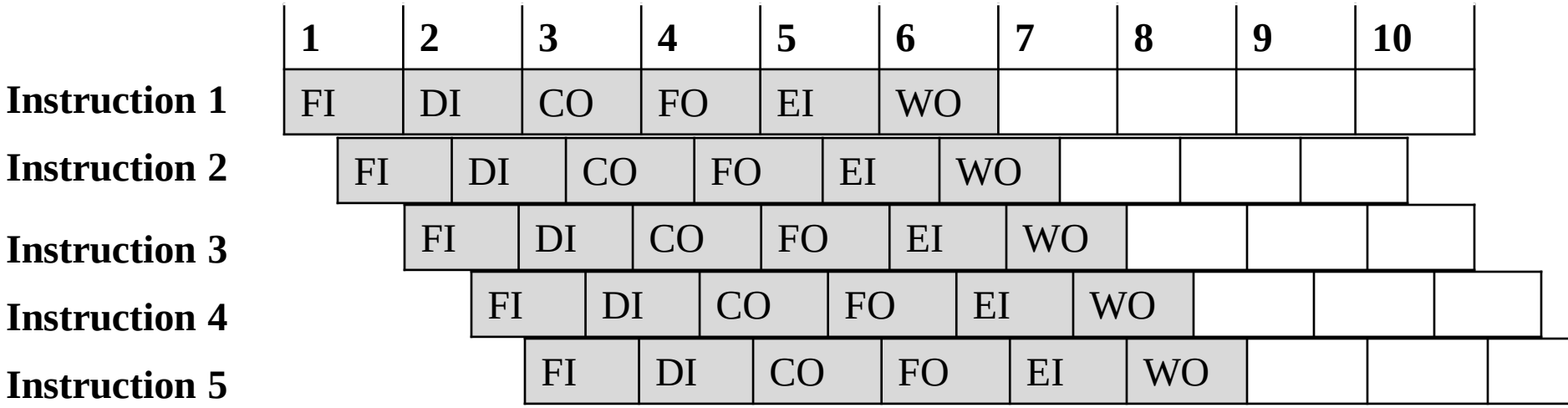
Parallelism in Superscalar Processor

	1	2	3	4	5	6	7	8	9	10
Instruction 1	FI	DI	CO	FO	EI	WO				
Instruction 2	FI	DI	CO	FO	EI	WO				
Instruction 3		FI	DI	CO	FO	EI	WO			
Instruction 4		FI	DI	CO	FO	EI	WO			
Instruction 5			FI	DI	CO	FO	EI	WO		
Instruction 6			FI	DI	CO	FO	EI	WO		
Instruction 7				FI	DI	CO	FO	EI	WO	
Instruction 8				FI	DI	CO	FO	EI	WO	
Instruction 9					FI	DI	CO	FO	EI	WO
Instruction 10					FI	DI	CO	FO	EI	WO

Superpipeline Processor

- An alternative approach to achieving greater performance is referred to as super- pipelining.
- Many pipeline stages need less than half a clock cycle.
- Super-pipelining is the breaking of stages of a given pipeline into smaller stages (thus making the pipeline deeper) in an attempt to shorten the clock period and thus enhancing the instruction throughput by keeping more and more instructions in flight at a time.

Superpipeline



Superscalar Hazards – Resource Hazard

- Same as pipeline Resource/ Structural Hazard, follow that slide

Superscalar Hazards – Resource Hazard

Solution:

- Separate input output port
- Renaming : According to renaming, we divide the memory into two independent modules used to store the instruction and data separately called Code memory (CM) and Data memory (DM) respectively. CM will contain all the instructions and DM will contain all the operands that are required for the instructions.

Superscalar Hazards – Data Hazard

- Same as pipeline Data Hazard, follow that slide

Superscalar Hazards – Control Hazard

- Same as pipeline Control Hazard, follow that slide