CSE 201: Digital Logic Design
SR Latch, Memory elements

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CSE, MIST

SEQUENTIAL CIRCUIT

- Consist of a **combinational circuit** to which **storage elements** are connected to form a feedback path
- The storage elements are devices capable of storing binary information.
- **State of a circuit**: Binary information stored in these elements at any given time
- The state of the memory devices now, also called current state
- **Next states and outputs** are functions of **inputs and present states of storage elements**
- Memory elements examples- latch, flip-flop

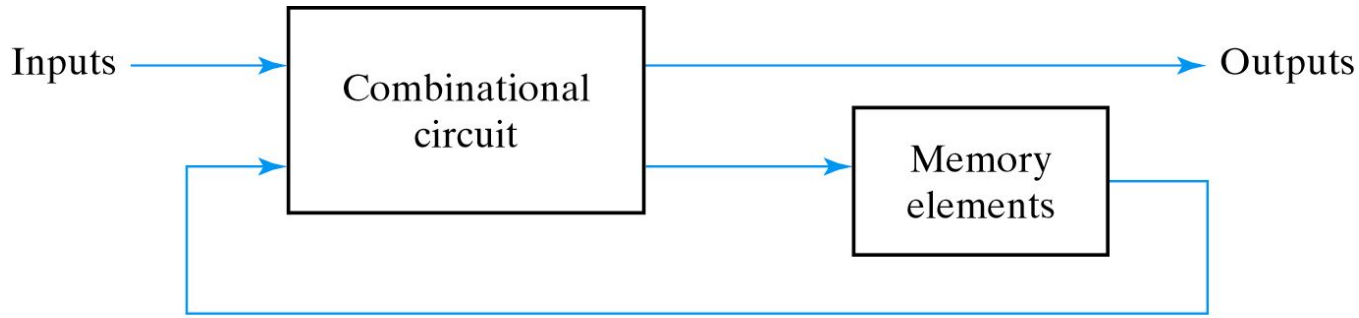
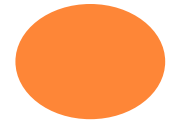


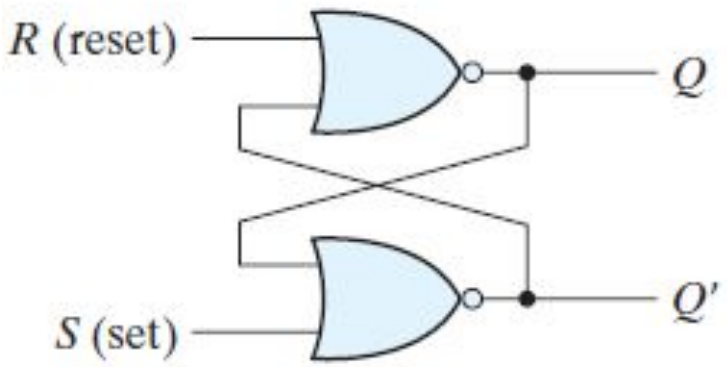
Fig. 5-1 Block Diagram of Sequential Circuit

LATCH

- Can store binary information(0 or 1) indefinitely (as long as power is provided)
- Building block or basic circuit of other memory elements
- Level-triggered memory element
- Constructed with NOR gates or NAND gates



SR LATCH



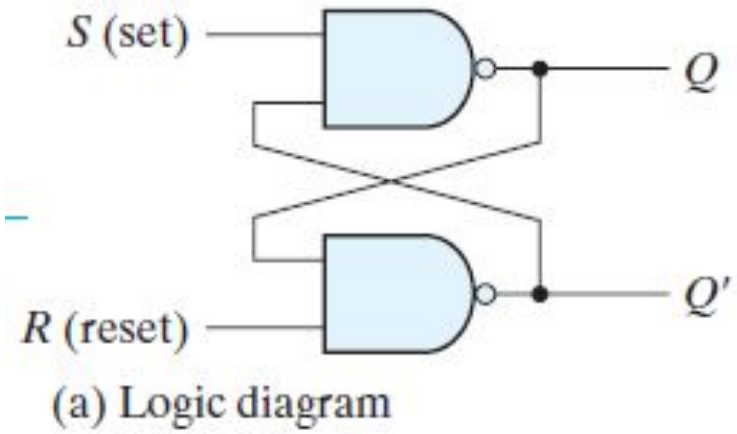
(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	Memory
0	1	0	1	
0	0	0	1	Memory
1	1	Forbidden		

Truth Table of NOR gate

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

SR LATCH



(a) Logic diagram

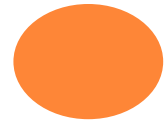
S	R	Q	Q’	
1	0	0	1	
1	1	0	1	Memory
0	1	1	0	
1	1	1	0	Memory
0	0	Forbidden		

Truth Table of NAND gate

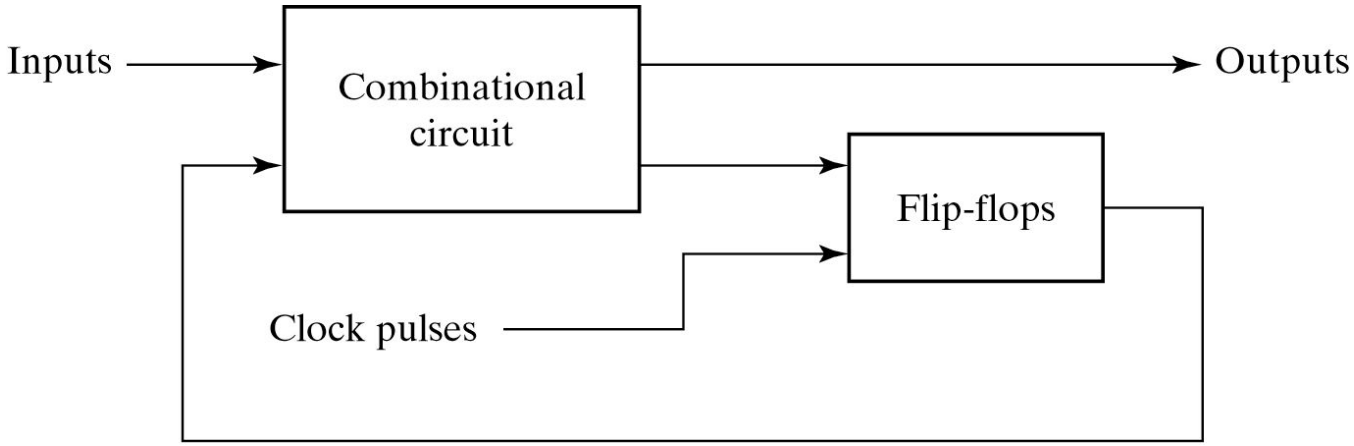
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

TWO TYPES OF SEQUENTIAL CIRCUIT

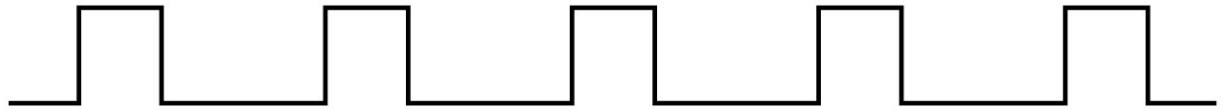
- Asynchronous sequential circuit
  - Depends upon the input signals at any instant of time and their change order
  - Hard to design
  - Works faster as there is no clock
  - Status of the memory element is affected any time as soon as the input is changed
  - Example - Latch
- Synchronous sequential circuit
  - Defined from the knowledge of its signals at discrete instants of time
  - Much easier to design
  - Works slower
  - Status of the memory element is affected only at the active edge of clock if input is changed
  - Example – flip flop



SYNCHRONOUS CLOCKED SEQUENTIAL CIRCUIT



(a) Block diagram



(b) Timing diagram of clock pulses

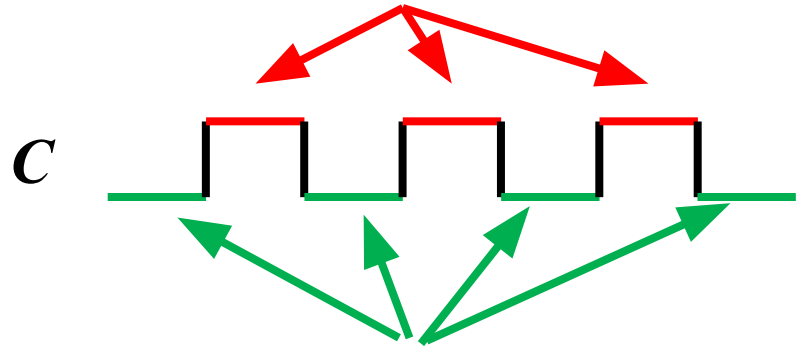
Fig. 5-2 Synchronous Clocked Sequential Circuit

MEMORY ELEMENTS

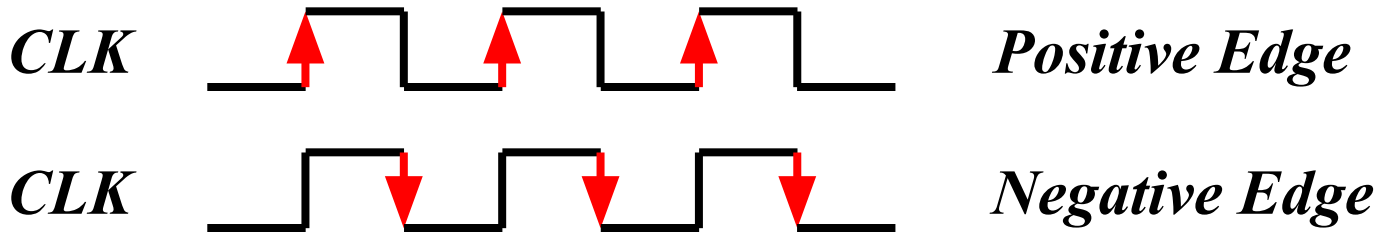
- Latch -— a **level-sensitive** memory element

  Examples -

  - SR latches
  - D latches



- Flip-Flop —- an **edge-triggered** memory element



Examples-

  - Master-slave flip-flop
  - Edge-triggered flip-flop

- RAM and ROM — a mass memory element