Aaron Reed Young

Email: ayoung3210@gmail.com
Website: https://web.eecs.utk.edu/~ayoung48/

Education

- University of Tennessee, Knoxville, Ph.D. in Computer Engineering, Fall 2017–Fall 2020, GPA: 4.0. Advisor: Dr. Mark E. Dean.
- University of Tennessee, Knoxville, Master's Degree in Computer Engineering, Fall 2016–Summer 2017, GPA: 4.0. Advisor: Dr. Mark E. Dean.
- University of Tennessee, Knoxville, Bachelor's Degree in Computer Engineering, Summa Cum Laude, Chancellor's Honors Program, EECS Honors. Fall 2012–Spring 2016, GPA: 4.0.

Work Experience

Oak Ridge National Laboratory, Knoxville, TN

- July 2020–Present: Software Engineer with the Architectures and Performance Group at Oak Ridge National Laboratory.

University of Tennessee, Knoxville

- January 2016–May 2020: Research with the TENNLab Neuromorphic Computing Research Group. See Research section and https://web.eecs.utk.edu/~ayoung48/research/ for more information.
- August 2016–August 2017: Graduate teaching assistant for Dr. James S. Plank. Assisted with the following classes by leading lab sections, grading labs and helping students: COSC 302 Data Structures and Algorithms II, COSC 360 Systems Programming, and COSC 494 Advanced Programming and Algorithms.

Garmin International, Inc., Olathe, KS

- Summer 2015: On the Aviation Software-Navigation Library Team. Improved the Navigation Library by revising requirements, making changes to the code base, and creating new test cases.

Oak Ridge National Laboratory, Manufacturing Demonstration Facility, Knoxville, TN

- Summer 2014: Programmed slicing engine to generate G-code for use with ORNL's two large-scale additive manufacturing 3D-printers using C++ and C#. Software was used to print the world's first 3D printed car.

Siemens Medical Systems, Knoxville, TN

- Summer 2013: Implemented embedded system control software using MQX RTOS on an ARM9 processor. Development included interfacing with GPIO, I^2C, SPI, CANopen, RS-323, and Ethernet. Embedded software supported interfacing to LEDs, LCD, FPGA, Temperature and Humidity sensors, EEPROM, DACs, SFP+, and a Power Controller. Designed a C# testing interface to communicate with the processor over TCP/IP.
- Summer 2012: Designed a system using an Altera Stratix IV FPGA development board to read data from two TI 1 GHz ADCs. Developed a NIOS II FPGA soft-core running µC/OS-II using Quartus II. Designed a C# application to interface with the development board using UDP/IP.
- Summer 2011: Used C# and ASP.NET to develop a database-driven website to keep track of employee's tasks. Learned and utilized LINQ to access the SQL database records.

Awards & Recognition

- Bodenheimer Fellowship Recipient, August 2016–Present.
- Top Collegiate Scholar, College of Engineering, The University of Tennessee, May 2016.
- Outstanding Computer Engineering Senior, Department of Electrical Engineering and Computer Science at the University of Tennessee, December 2015.
- Outstanding Computer Engineering Senior, Department of Electrical Engineering and Computer Science at the University of Tennessee, December 2014.
- Outstanding Computer Engineering Junior, Department of Electrical Engineering and Computer Science at the University of Tennessee, December 2013.
- Min H. Kao Electrical and Computer Engineering Scholarship Recipient, 2013–2015.
- Alcoa—College of Engineering Study Abroad Fellowship, 2013.
- Tau Beta Pi, The Engineering Honor Society, 2013.

Publications

Ph.D. Dissertation (https://trace.tennessee.edu/utk_graddiss/5843/)

SNACC: The Scaled-up Neuromorphic Array Communications Controller

To ensure robust communication, a custom, hardware-based, go-back-n, automatic repeat request protocol is presented, which allows for high-throughput, low-latency, error-free communication using the Aurora link-level protocol over the GTX/GTH high-speed serial transceivers found on Xilinx FPGAs. Multiple Dynamic Adaptive Neural Network Arrays Two (DANNA2) element cores are tiled into a grid array and placed within a KCU1500 Kintex Ultrascale FPGA to build a reconfigurable hardware neuromorphic processor. For resource-constrained environments, these element cores can also be densely packed onto the FPGA for a specific network, requiring less resources for a non-reconfigurable neuromorphic processor. For high-performance computation, multiple reconfigurable neuromorphic processors with grid arrays are tiled together with a Neuromorphic Array Communication Controller (NACC) to build a large-scale neuromorphic

system called Scaled-up NACC (SNACC). SNACC uses scalable, high-performance, point-to-point connections to network the neuromorphic processors into a two-dimensional array. The neuromorphic processors are connected back to the host PC through a hierarchical, high-speed network made possible through the use of one or more NACCs. These new hardware DANNA2 neuromorphic processors are used to further research with recurrent spiking neural networks (RSNNs). Specifically, this work uses the new hardware for evolutionary optimization of neural networks using genetic algorithms, for reservoir computing, and for solving graph algorithms. Additionally, the hardware can be used for real-time processing as demonstrated with target acquisition and obstacle avoidance on a ground-roaming autonomous robot.

Master's Thesis (https://trace.tennessee.edu/utk_gradthes/4916/)

Scalable High-Speed Communications for Neuromorphic Systems

To alleviate communication limitations and to expand scalability, a new communications solution is presented which takes advantage of the GTX/GTH high-speed serial transceivers found on Xilinx FPGAs. A Xilinx VC707 evaluation kit is used to prototype a new neuromorphic array communication controller for use as a communication solution for neuromorphic systems. The high-speed transceivers are used to communicate to the host computer via PCIe and to communicate to the DANNA arrays with the link layer protocol Aurora. The new communications system is able to outperform the FX3, reducing the latency in the communication and increasing the throughput of data. This new communications setup will be used to further DANNA research by allowing the DANNA arrays to scale to larger sizes and for multiple DANNA arrays to be connected to a single communication board.

Journal, Conference, and Workshop Papers (https://web.eecs.utk.edu/~ayoung48/publications/)

- A survey on processing-in-memory techniques: Advances and challenges, Kazi Asifuzzaman, Narasinga Rao Miniskar, **Aaron R. Young**, Frank Liu, Jeffrey S. Vetter, *Memories - Materials, Devices, Circuits and Systems*, 2022.
- A Neuromorphic Algorithm for Radiation Anomaly Detection, James Ghawaly, **Aaron Young**, Dan Archer, Nick Prins, Brett Witherspoon, Catherine Schuman, *Proceedings of the International Conference on Neuromorphic Systems 2022*, 2022.
- Design and Analysis of CXL Performance Models for Tightly-Coupled Heterogeneous Computing, Anthony M. Cabrera, **Aaron R. Young**, Jeffrey S. Vetter, *ExHET '22: Proceedings of the 1st International Workshop on Extreme Heterogeneity Solutions*, 2022.
- Heterogeneous Memory System Framework for HPC, Kazi Asifuzzaman, Narasinga Rao Miniskar, **Aaron R. Young**, Frank Liu, and Jeffrey S. Vetter, *ASCR Workshop on the Management and Storage of Scientific Data*, 2022.
- A Hierarchical Task Scheduler for Heterogeneous Computing, Narasinga Rao Miniskar, Frank Liu, **Aaron R. Young**, Dwaipayan Chakraborty, Jeffrey S. Vetter, *International Conference on High Performance Computing*, 2021, 57-76.
- Toward Evaluating High-Level Synthesis Portability and Performance between Intel and Xilinx FPGAs, Anthony Cabrera, **Aaron Young**, Jacob Lambert, Zhili Xiao, Amy An, Seyong Lee, Zheming Jin,

Jungwon Kim, Jeremy Buhler, Roger Chamberlain, and Jeffrey Vetter, *IWOCL'21: International Workshop on OpenCL*, 2021.

- Emerging Heterogeneous Systems Provide Great Opportunities for Codesign, **Aaron R. Young**, Jeffrey S. Vetter, Frank Liu, Narasinga Rao Miniskar, Sarat Sreepathi, and Anthony M. Cabrera, *ASCR Workshop on Reimagining Codesign*, 2021.
- Scaled-up Neuromorphic Array Communications Controller (SNACC) for Large-scale Neural Networks, **Aaron R. Young**, Adam Foshie, Mark E. Dean, James S. Plank, Garrett S. Rose, John Mitchell, and Catherine D. Schuman, *IJCNN: The International Joint Conference on Neural Networks*, 2020.
- A Review of Spiking Neuromorphic Hardware Communication Systems, **A. R. Young**, M. E. Dean, J. S. Plank and G. S. Rose, in *IEEE Access*, vol. 7, pp. 135606-135620, 2019. Impact factor of 4.098.
- Understanding Selection and Diversity for Evolution of Spiking Recurrent Neural Networks, Catherine D. Shuman, Grant Bruer, **Aaron R. Young**, Mark Dean and James S. Plank, *IJCNN: The International Joint Conference on Neural Networks*, 2018. Acceptance rate of 65.69%.
- Neuromorphic Array Communications Controller to Support Large-Scale Neural Networks, **Aaron R. Young**, Mark E. Dean, James S. Plank, Garrett S. Rose and Catherine D. Schuman, *IJCNN: The International Joint Conference on Neural Networks*, 2018. Acceptance rate of 65.69%.
- DANNA: A Neuromorphic Software Ecosystem, Adam Disney, John Reynolds, Catherine D. Schuman, Aleksander Klibisz, **Aaron Young**, and James S. Plank, *Biologically Inspired Cognitive Architectures, Volume 9*, 2016.

Reports

- Hardware Evaluation Analytical Modeling and Node Simulation: Benefits of Tighter GPU Integration, Brian Austin, Ray Bair, Kevin Barker, Anthony Cabrera, Andrew Chien, Nan Ding, Jesun Firoz, Khaled Ibrahim, Joseph Manzano, Vitali Morozov, Tan Nguyen, Leonid Oliker, Joshua Suetterlein, Li Tang, Jeffrey Vetter, Samuel Williams, Kazutomo Yoshii, **Aaron Young**, *Lawrence Berkeley National Laboratory*, ECP-HIHE01-35, 2021.

Posters

- Poster: Neuromorphic Array Communications Controller, **Aaron R. Young** and Mark E. Dean, *JDRD Symposium*, 2019.
- Poster: DANNA Neuromorphic Application Development Kit Demo, Mark Dean, **Aaron Young**, Parker Mitchell, Patricia Eckhart, John Reynolds, Grant Bruer, Adam Disney, James Plank, and Catherine Schuman. *5th Neuro Inspired Computational Elements Workshop (NICE 2017)*, 2017.

Patents

- Hierarchical task scheduling for accelerators, Narasinga Rao Miniskar, Frank Y Liu, **Aaron R Young**, Jeffrey S Vetter, Dwaipayan Chakraborty, *US-17542022*, 2022.

Research

I am part of the TENNLab—Neuromorphic Architectures, Learning, Applications research group. (See https://neuromorphic.eecs.utk.edu/.) The group is lead by Dr. Mark Dean, Dr. James Plank, Dr. Garrett Rose, Dr. Catherine Schuman, Dr. Nathaniel Cady, and Dr. J. Douglas Birdwell. We are researching a new paradigm of computing, inspired by the human brain. Our research encompasses nearly every facet of the neuromorphic area, including current and emergent hardware implementations, theoretical models, programming techniques and applications. Specifically, I have worked on framework development, the DANNA and DANNA2 digital neuromorphic processors, and neuromorphic application development. I have also helped with the development of multiple neuromorphic robots, including NeoN (Neuromorphic Control System for Autonomous Robotic Navigation), GRANT (Ground-Roaming Autonomous Neuromorphic Targeter), and SABR (Self-Adjusting Balancing Robot). My focus has been on communication between traditional computers and neuromorphic processors. I have developed the NACC (Neuromorphic Array Communications Controller) to support high-speed, low-latency communication between the host PC and the neuromorphic system. I have also designed and built SNACC (Scaled-up Neuromorphic Array Communications Controller), which uses a NACC to connect multiple neuromorphic processors together for the purpose of building a large unified neuromorphic system. This system is designed to run large neural networks and also supports real-time communication with the Host PC.

Projects

Neuro-Cluster

Using the skills gained from the BOB and Alice projects, I built a large, high-performance cluster from donated servers for the use of the TENNLab research group. This cluster consists of 8 Sun x2200s, 36 Dell PowerEdge C6145, and a Synology RS816 NAS with a Synology RX418 NAS Expansion unit. The cluster is set up with LDAP, Slurm, MPI, OpenMP, Ansible, Jenkins, MAAS, Infiniband, Firewall, Custom Monitoring GUI, and Git Server. The main compute partition has 1728 total cores and 3456 GB total RAM. In addition to setting up the system, I have also been the sole administrator of the system for 3 years, responsible for hardware maintenance, account management, and configuration maintenance. The system is being used by the TENNLab group as a valuable computing resource and results collected on the cluster have been published in multiple papers.

Security Plan

As part of my computer system management duties, I helped create the Galápagos Security Plan and Acceptable Use Policy. The Plan covers the Neuro-Cluster, BOB (details below), and various benchtop workstations used by TENNLab. The security plan follows the National Standards and Guidance, NIST FIPS 199, Standards for Security Categorization of Federal Information and Information Systems (FIPS 199); National Standards and Guidance, NIST SP 800-53, Revision 4, Recommended Security Controls for Federal Information Systems and Systems (NIST 800-53); the Tennessee Code Annotated § 47-18-2107, 2010 S.B. 2793, Release of personal consumer information; University of Tennessee System Policy IT0110, Acceptable Use of Information Technology Resources; and University of Tennessee, Knoxville, Banner Data Standards Manual.

ECE 651—TRASHCAN on a Chip

The Tiny RISC Architecture System with Homogeneous Communication Across a Network on a chip (TRASHCAN) project aimed to design and implement a multi-core RISC-V processor with cores communicating through an embedded network-on-chip (NoC). The NoC follows a basic two-dimensional mesh topology for simplicity, and the processor cores are 5 stage, in order, RISC-V cores. By scaling out with more cores and a simple mesh interconnect, we hoped to see the potential for large many-core systems beyond today's offerings. Much of the project drew from three open source hardware projects: RISC-V, OpenSoC, and Parallela. Through the project, we looked to extend and incorporate the Rocket Chip generator for RISC-V with the network-on-chip generator from OpenSoC to build a processor inspired by the principles of the Adapteva Parallela.

ECE 599—BOB (Big Orange Bramble)
https://web.eecs.utk.edu/~ayoung48/tech/bob/

This project involved the design and construction of a high-performance cluster composed of 68 quad-core ARMv8 64-bit Raspberry Pi 3s. The primary intent of the project was to establish the operating environment, communication structure, application frameworks, application development tools, and libraries necessary to support the effective operation of a high performance computer model for the students and faculty in the Electrical Engineering and Computer Science Department of the University of Tennessee to utilize. As a foundation, the system borrowed heavily from the Tiny Titan system constructed by the Oak Ridge National Laboratory, which was a similar but smaller-scale project consisting of 9 first generation Raspberry Pis. Beyond the primary target of delivering a functional system, efforts were focused on application development, performance benchmarking, and delivery of a comprehensive build/usage guide to aid those who wish to build upon the efforts of this project.

CS 594—ALICE (A Linux Integrated Computing Environment)
https://web.eecs.utk.edu/~ayoung48/tech/alice/

This project was an expansion of The University of Tennessee's Big Orange Bramble (BOB) project from Summer 2016. The success of the BOB project led to a proposal for a secondary cluster, which was intended to be combined with BOB to form a larger, heterogeneous cluster. This secondary cluster was created from 32 64-bit Pine64s and 12 Nvidia TX1 GPUs. It was also a requirement to perform benchmarking on each subset of architecture and provide a performance comparison to BOB. Additionally, several more applications were developed for BOB, including facial recognition, weather forecasting, and a Gillespie algorithm. An installation and usage guide was also developed for these applications for anyone wishing to utilize them.

Senior Design—Second Creek Monitoring
https://trace.tennessee.edu/utk_chanhonoproj/1908/

My senior design project was to build a Second Creek Monitoring database and website to help Dr. Jon Hathaway, UTK Department of Civil and Environmental Engineering, with his ongoing effort to collect high-resolution data from Second Creek and a weather station located on the University of Tennessee-Knoxville campus. This project built a website to which students and the general public can navigate and see the conditions of the local environment and creek, thereby promoting water quality and watershed awareness. The website provided a user-friendly,

aesthetically pleasing interface and better access to real-time information about the local environment. The project also built an SQL database to collect information from the sensors and provide the information to the website. Another goal of this project was to ensure data security since it is critical to minimize any data loss that could potentially affect the ongoing research.

Relevant Coursework

ECE	692	Advanced Special Topics — Deep Learning	Final Grade: A
ECE	651	Computer-aided Design of VLSI Systems	Final Grade: A
COSC	594	Supercomputer Design & Analysis	Final Grade: A
COSC	594	Computer Graphics	Final Grade: A
ECE	593	Advanced Supercomputer Design & Analysis	Final Grade: A
COSC	565	Databases/Scripting Languages	Final Grade: A
COSC	560	Software Systems	Final Grade: A
ECE	555	Embedded Systems	Final Grade: A
ECE	551	Digital System Design I	Final Grade: A
COSC	530	Computer Systems Organization	Final Grade: A
COSC	528	Intro to Machine Learning	Final Grade: A
COSC	527	Biologically-Inspired Computation	Final Grade: A
COSC	494	Advanced Programming and Algorithms	Final Grade: A
COSC	462	Parallel Programming	Final Grade: A
ECE	457	Honors: Computer Systems Architecture	Final Grade: A
COSC	453	Introduction to Computer Networks	Final Grade: A
COSC	361	Operating Systems	Final Grade: A
COSC	360	Systems Programming	Final Grade: A
ECE	201/202	Circuits I & II	Final Grade: A/A
COSC	140/302	Data Structures & Algorithms I & II	Final Grade: A/A

Study Abroad

- Engineering in London Study Abroad Program: Spent five weeks in London earning six University of Tennessee engineering credit hours, June 2013. (See https://web.eecs.utk.edu/~ayoung48/life/engineering-in-england/)

Relevant Skills

Programming Languages

Bash, C, C#, C++, Chisel, CSS, G-code HTML, Java, Javascript, MPI, OpenGL, OpenMP, Perl, PHP, Python, SKILL, SQL, SystemVerilog, Tcl, VHDL

Frameworks

ASP.NET, Django, Jekyll

Libraries

GTK, Keras, NumPy, OpenGL, pandas, SciPy, TensorFlow

Tools

Ansible, Beamer, Blender, Firewall, FreeCAD, GIMP, Git, Inkscape, Jenkins, LaTeX, Linux, MAAS, Slurm, Vivado

Protocols

CANopen, I^2C, Infiniband, LDAP, RS-323, SPI, TCP/IP

Relevant Extracurriculars

FIRST Robotics Participation

- Mentor for Hardin Valley Academy FIRST Robotics Team. Set-up source code version control. Assisted with teaching programming to students. Provided support at Regional Competition, 2012–2013.
- Computer Programmer for Hardin Valley Academy FIRST Robotics Team. Used C++ to design, simulate and implement the robot's control system and autonomous mode. Assisted with electrical set-up and mechanical manufacturing. Participated in regional and national competitions, 2011 & 2012.

References

References available upon request.