DEVICES AND COMMUNICATION BUSES FOR DEVICES NETWORK–

Lesson-9: Parallel Port Interfacing with LCD Controller

LCD controller– A processing element (single purpose processor)

- Processing element generates all required signals for LCD matrix displays (multi-lane).
- Interfaces Eight-bit *parallel output port B* pins PB0-PB7, which sends commands for programming the controller and send data for display

Port Interfacing — Parallel port outputs and control signals

- Three control signals IO PC0-PC2 as inputs to LCD controller
- PB0 to PB7 8 input/output bits for parallel set of 8 IO bits for commands and data

Control Bits

- LCD controller is sent control words and data words for initialization and programming by setting the PB0-PB7, PC0 and PC1 outputs for each word to LCD controller.

Register Select Control bit

- One bit PC0 at an output port for RS (register select).
- When RS is reset as 0, the PB0-PB7 communicates a control word to control register of the LCD controller.
- When RS is set as 1, the PB0-PB7 communicates data to LCD controller

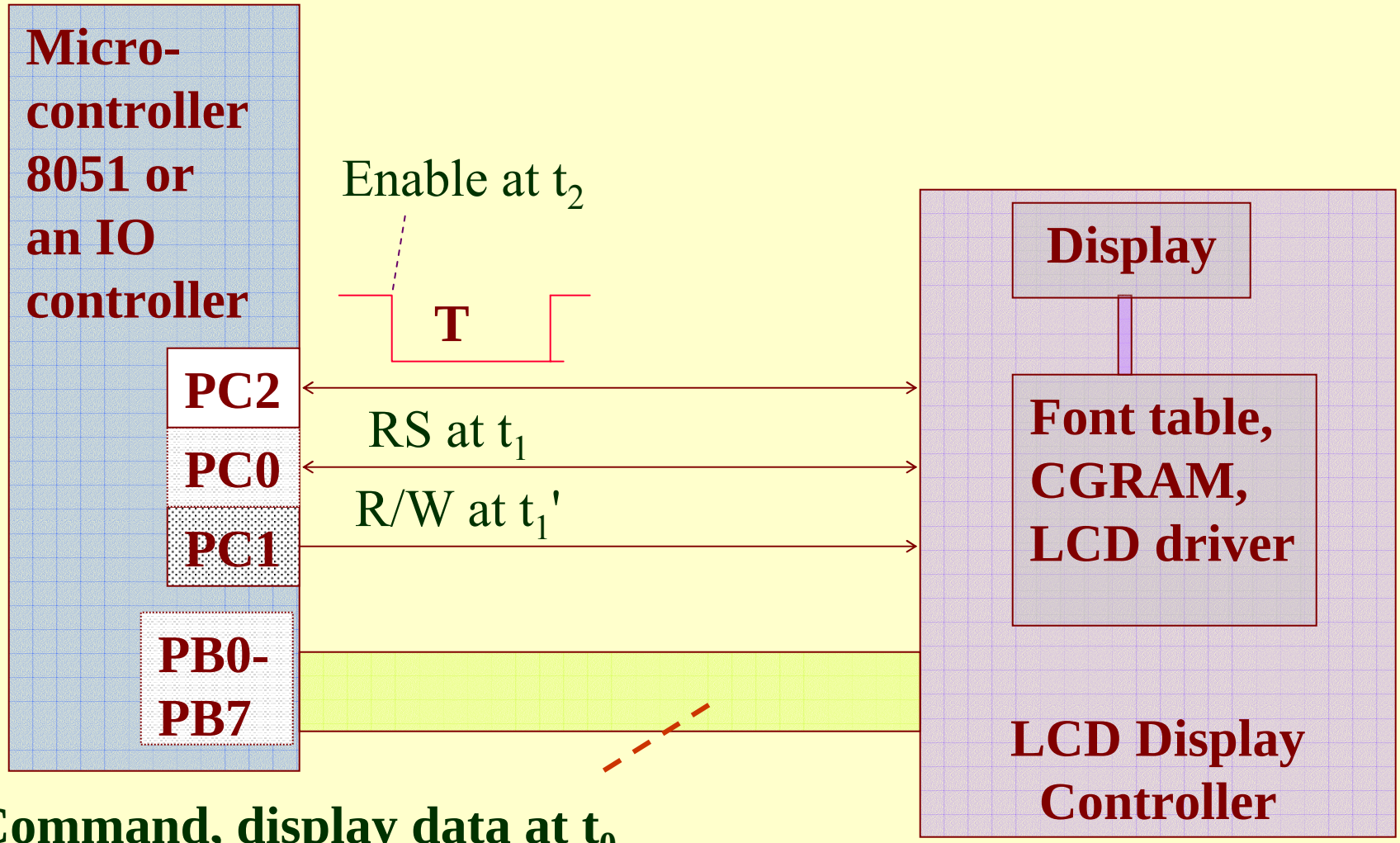
R/W (read/write) Control bit

- One bit PC1 at an output port
- Set to 1 when status register of LCD controller is read using PB0-PB7.
- PC1 is reset to 0 when write into LCD controller using PB0-PB7 bits.

Enable Control bit

- After setting R/W, RS and data-bits the LCD controller enables
- Enables by setting 1 at E pin.
- LCD controller connects to one bit PC2 at an output port for E (enable). There is an interval depending on the LCD controller, the controller is disabled. This is because during this interval, the LCD controller cannot accept instructions or data through output of other port pins.

Interfacing LCD Controller



Command, display data at t_0 and Status bits at t_3

Enabling Pulse Interval *T*

- Assume a command instruction is to clear display. The internal processing element has to clear the bytes at all the N addresses in N characters LCD display. It takes time, *T*, for example, 150 µs
- When first 1 is written at PC2, then 0 is written for enabling pulse 0 using 150 µs delay program,
- PC2 output creates a –ve going pulse (1 followed by 0) at LCD controller. It disables transfer of any control word or data for a period of *T to enable* internal processing.

LCD controller

- M displayed character ROM addresses. M = 128 for 128 ASCII codes.
- For Each distinct ASCII character, there is 64-bit graphic.
- LCD controller has internal CGRAM (Character graphic RAM).
- For each ASCII character, 8 bytes are sent from the ROM to the CGRAM.

CGRAM

- Has N addresses. N = 64 for 64 characters that can be displayed.
- An address changes by incrementing or decrementing cursor position to previous address on the screen or next address on the screen.
- Sending appropriate control words followed by data, the LCD controller is programmed to display up to characters on the screen when N = 64.

Summary

We learnt

- LCD controller has LCD driver, font table, and CGRAM for the display control
- Parallel port having 8 bit output data and 3 control bits E, RS and R/W used to interface to an LCD controller

End of Lesson 9 of Chapter 3