Department of Computer Engineering
Faculty of Engineering, University of Peradeniya

CO221 : Digital Design
Lab 9 - Prelab

- Each individual should have a written/printed pre-report.
- No need to waste your time unnecessarily on neatness. But answers should be **readable**.
- Write down the intermediate steps while you solve the problem.
- If you need help put a post in the forum for CO221 in FEeLS rather than copying from someone else.
- If you are caught copying you get 0 for the prelab and also the marks for the rest of the lab would be reduced by 50%.

THEORY

This laboratory session focusses on design procedure of sequential circuit. If you are not familiar with design procedure yet, refer the guide given below.

Sequential circuits

Sequential circuits are logic circuits which consist of some combinational logic to which storage elements are connected to form a feedback path. Hence, outputs of a sequential circuit are a function of both the inputs as well as the present state of the storage elements. Storage elements are devices capable of storing binary information. Examples being latches and flip-flops.

State Tables

State table is used to describe the inputs, outputs and flip-flop states of a sequential circuit. The table consists of four sections namely *present state*, *input*, *next state* and *output*.

- Present state: States of the flip-flops
- Input: All input values for each possible present state.
- Next state: Next states of the flip-flops.
- Output: Outputs of the sequential circuit.

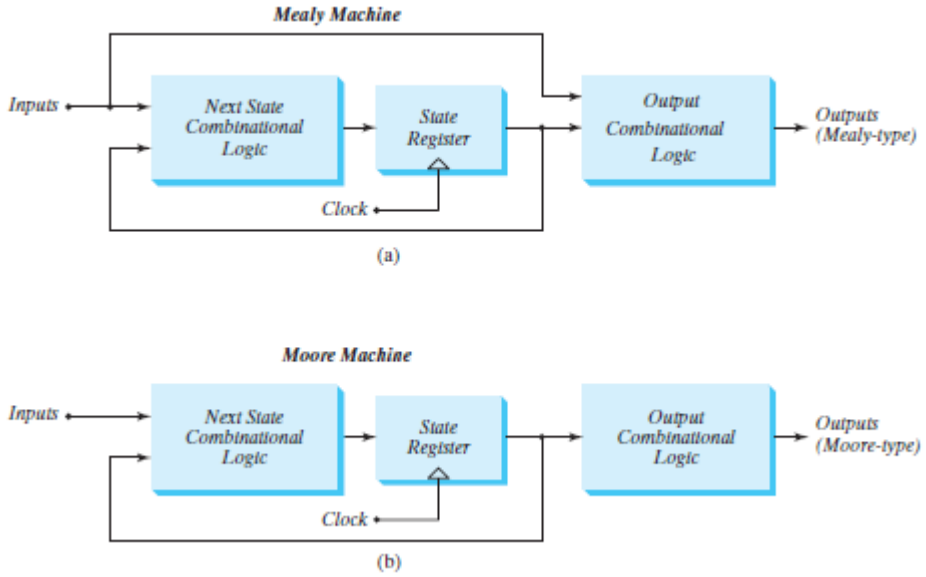
State Diagram

A state table can be graphically represented by a state diagram. In a state diagram, a state is represented by a circle and the state transitions are given by directed lines

connecting states. States of the flip-flops are given as binary numbers inside the circles. Inputs given to the circuits which result in state transitions are shown on top of directed arrow. Outputs resulted by given inputs are represented alongside inputs, separated by a back-slash.

Mealy and Moore Models of sequential circuits

There are two models of sequential circuits namely, Mealy model and Moore model. Block diagrams of the two models are given below.



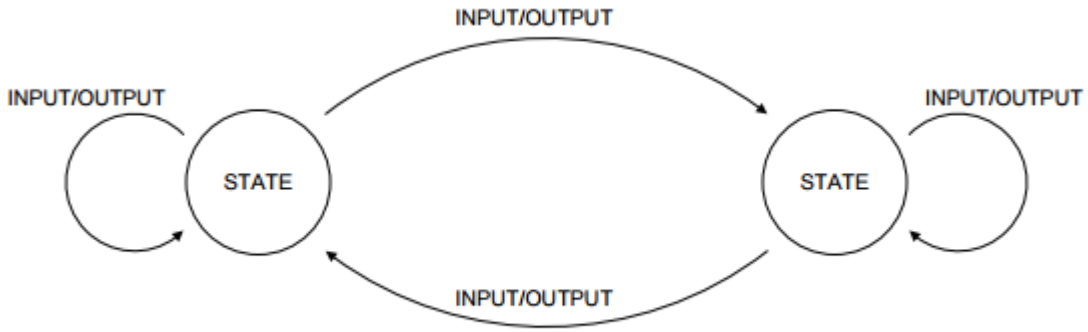
The two models differ only by the way the outputs are generated.

- Mealy model: Output is a function of both the **present state** and the **input**.
- Moore model: Output is a function of **only** the **present state**.

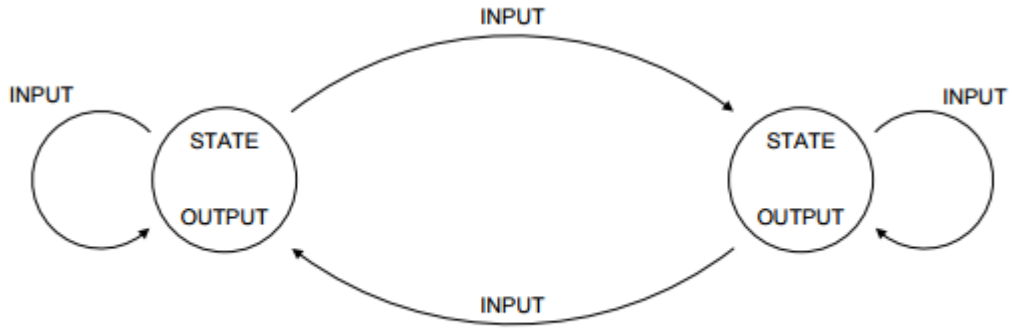
These models can be represented graphically using Finite State Machines (similar to state diagrams).

In Mealy machines, inputs and outputs are separated by a slash and given on top of state transition lines. On the other hand, outputs of Moore machines are given inside circles together with the present state. This is because outputs are functions of the present state only.

Two types of Finite State Machines are given in the following figure.



GENERIC MEALY STATE MACHINE



GENERIC MOORE STATE MACHINE

Designing synchronous sequential circuits

Design procedure of a synchronous sequential circuit can be done by the given set of steps.

1. Derive a state diagram from the problem specification.
2. Reduce the number of state if necessary (not required at this stage).
3. Assign binary values to the states.
4. Obtain the binary-coded state table.
5. Choose the type of flip-flop to be used.
6. Derive the simplified flip-flop input equations and output equations (using K-maps).
7. Draw the logic diagram.

An example design procedure is given below.

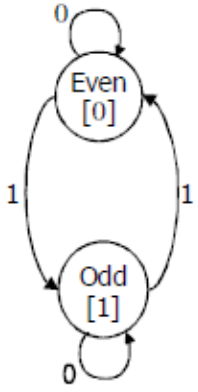
Problem: Design a sequential circuit to check the odd parity of an input bit sequence.

Let us obtain the circuit using both Mealy and Moore models.

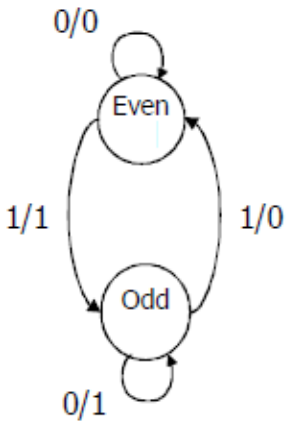
Step 1

Obtaining the state diagram.

Moore



Mealy



Step 2

No reduction necessary.

Step 3

Binary numbers are assigned to the two states, *Odd* and *Even* as follows.

Odd – 0 and Even – 1.

Since there are only two states, one bit is sufficient to represent states.

Step 4

The binary coded state tables are given below.

Present State	Input	Next State	Present Output
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	1

Moore

Present State	Input	Next State	Present Output
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Mealy

Step 5

Let us use D flip-flops for the design (Simplest type).

Step 6

Karnaugh maps can be used to obtain flip-flop input equations and output equations.

But, in this case, even without Karnaugh maps, we can obtain the equations by observing the state tables.

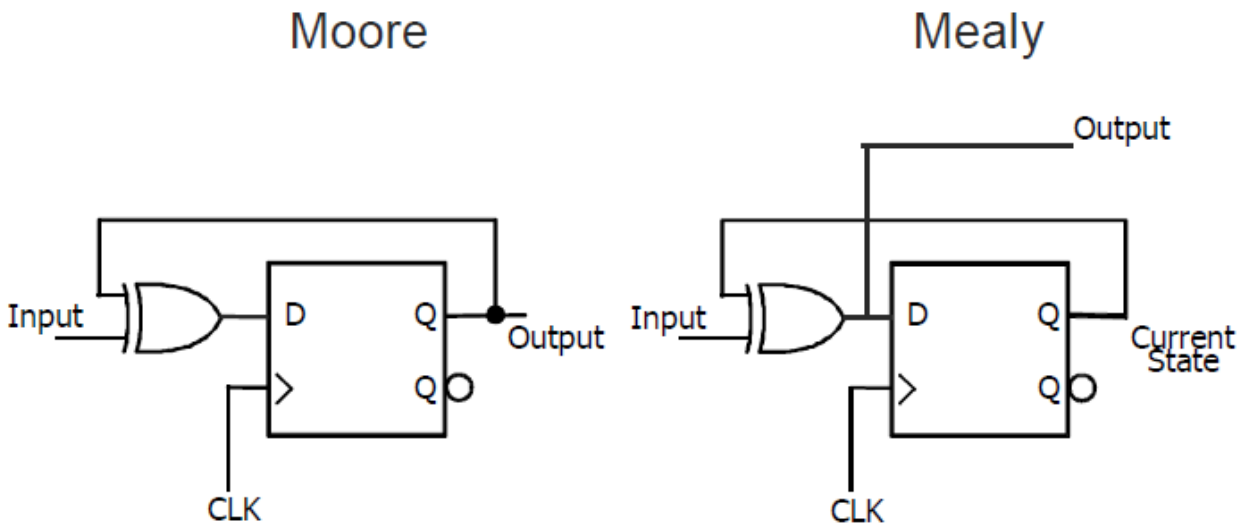
For both models, **Flip-flop input = (Present State) XOR (Input)**

For Mealy model, **Output = (Present State) XOR (Input)**

For Moore model, **Output = Present state**

Step 7

Based on equations, logic diagrams are drawn as follows.



Note

In a Moore machine, the outputs of the circuit are synchronized with the clock, because they depend only on the flip-flop outputs that are synchronized with the clock. But in a Mealy machine, outputs may change when the inputs change during a clock cycle.

QUESTIONS

1. Parity bits are the simplest form of error checking mechanism used in digital communication systems. A parity checker can be implemented using sequential logic.
   Design an Even parity checker using D flip-flops and combinational logic using,

   a. Mealy model
   b. Moore model

2. Combinations of bit patterns are used as passcodes or passwords when locking doors and safes. A pattern detector which detect a given pattern can be implemented using sequential logic.
   Design a sequential circuit which detects the pattern '011' in an input bit stream. The circuit should be in Moore model. Use D flip-flops as the type of flip-flop.

3. Implement a 3-bit synchronous binary counter with D flip-flops and combinational logic. Use Moore model.

REFERENCE

Digital Design (Fifth edition) by Morris Mano and Michael Ciletti