Department of Computer Engineering
University of Peradeniya

CO221 - Digital Design
Introduction to Verilog HDL

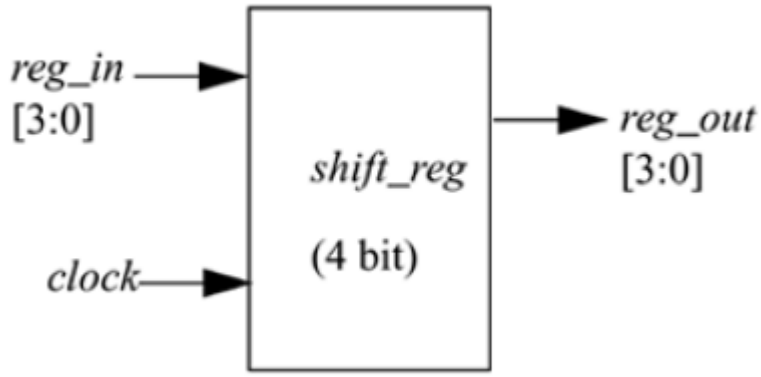
Exercise 1

Write a Verilog stimulus module which displays the message “Hello World!” and simulate it.

Exercise 2

A 4-bit parallel shift register has I/O pins as shown in the figure below. Write the module definition for this module shift_reg. Include the list of ports and port declarations. You do not need to show the internals.

Next, write a Declare a top-level module stimulus. Define REG_IN (4 bit) and CLK (1 bit) as reg register variables and REG_OUT (4 bit) as wire. Instantiate the module shift_reg and call it sr1.



Exercise 3

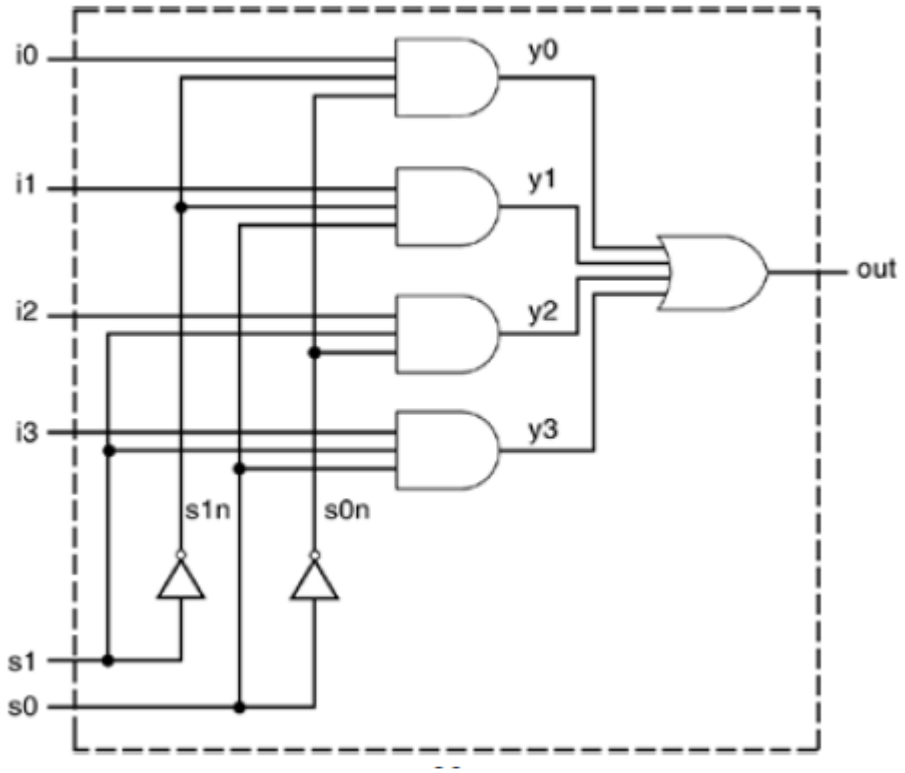
Create your own 2-input Verilog gates called my-or, my-and and my-not from 2-input nand gates. Check the functionality of these gates with a stimulus module.

Exercise 4

A 2-input xor gate can be built from my_and, my_or and my_not gates. Construct an xor module in Verilog that realizes the logic function, z = xy' + x'y. Inputs are x and y, and z is the output. Write a stimulus module that exercises all four combinations of x and y inputs.

Exercise 5

Build a 4 x 1 multiplexer using the logic circuit given below. Test the functionality of the circuit using a stimulus module.



Exercise 6

Build a 2 x 4 decoder using the logic circuit given below. Test the functionality of the circuit using a stimulus module.