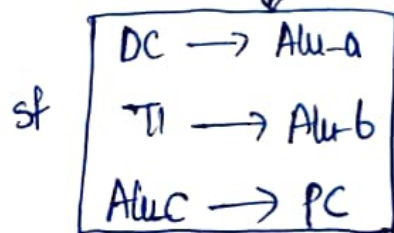
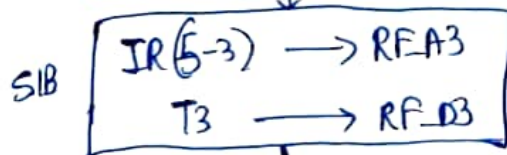
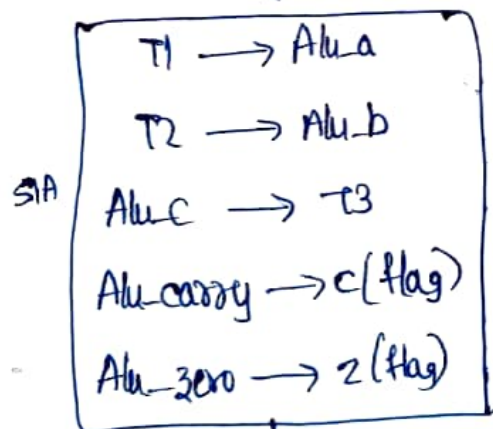
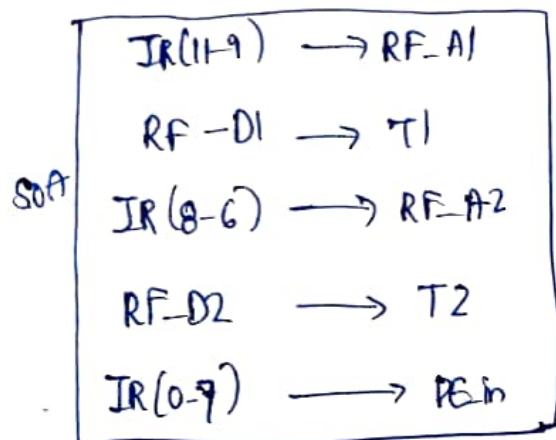
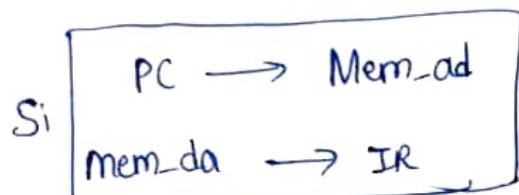


Datapaths

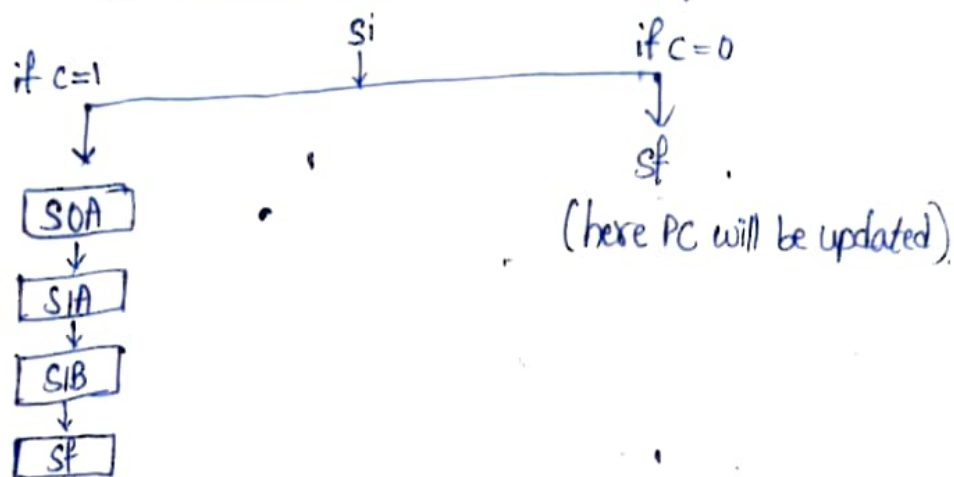
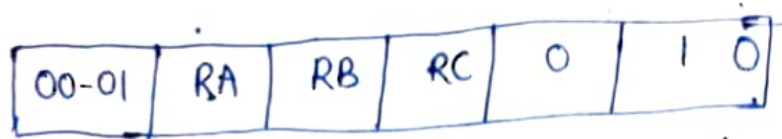
① ADD : add r_c, r_a, r_b



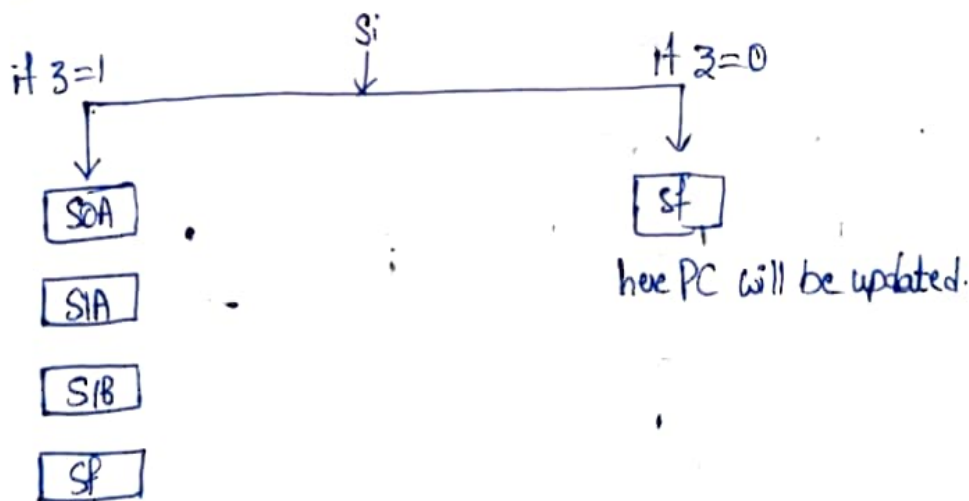
$r_c = r_a + r_b$ & c, z modifies.



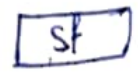
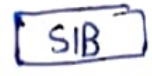
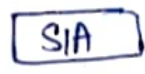
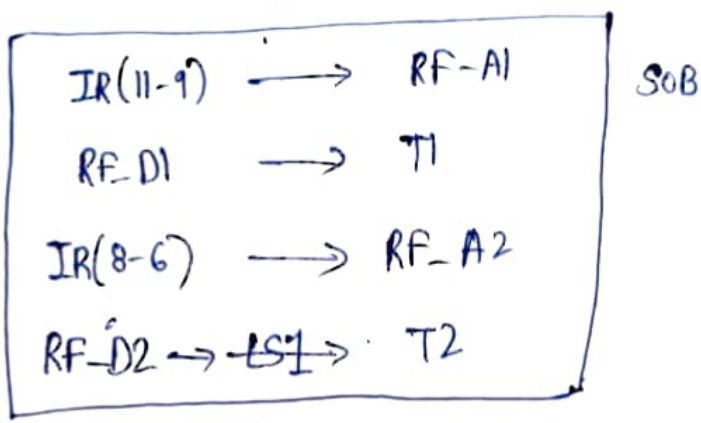
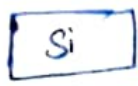
② ADC : adc rc, ra, rb



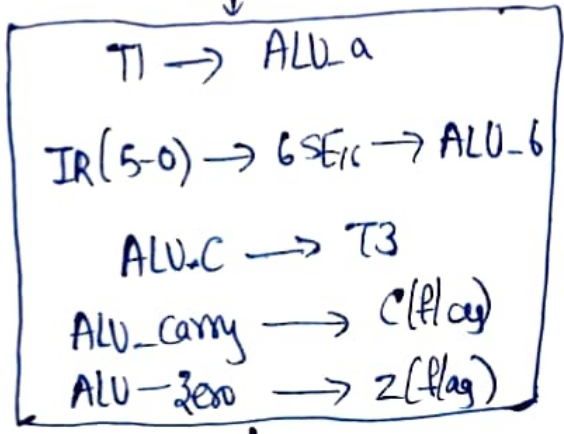
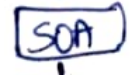
③ ADZ : adz rc, ra, rb

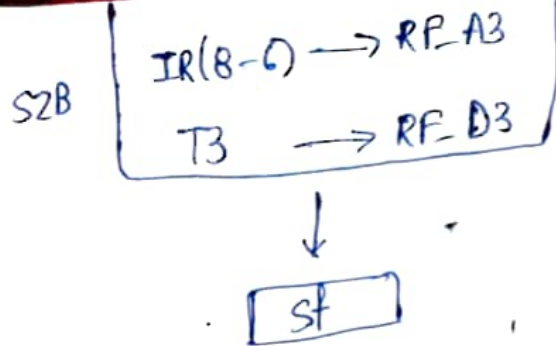


④ ADL : Adl rc, ra, rb



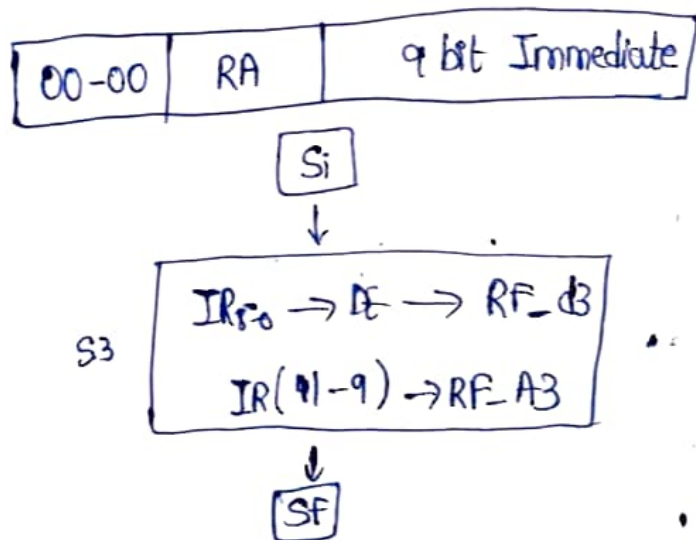
⑤ ADI : adi rb, ra, imm6



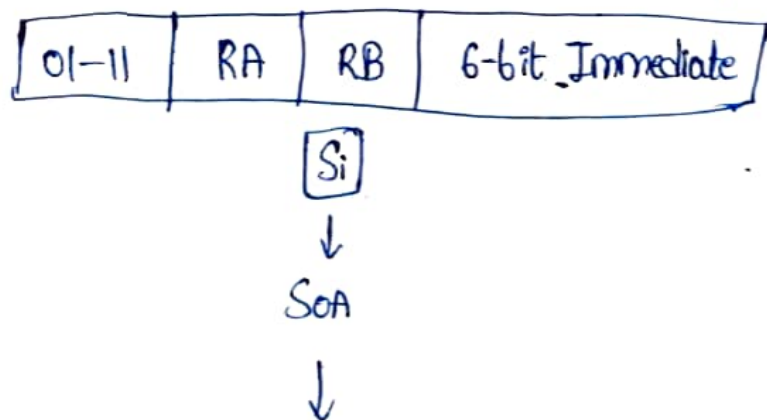


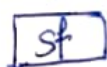
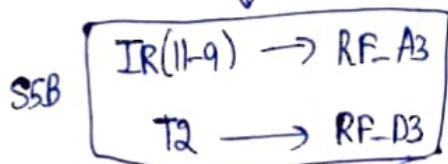
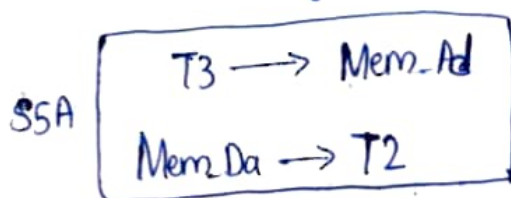
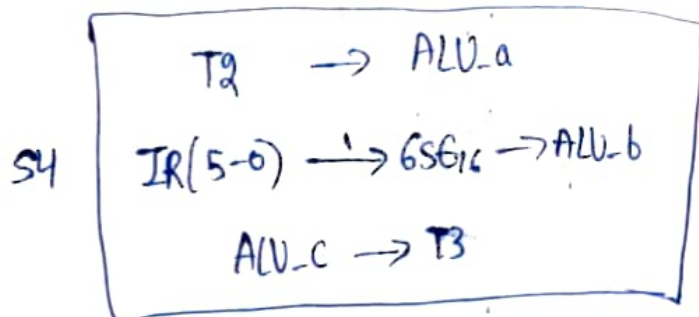
- ⑥ NDU : ndu ra, rb,
 → similar as add instruction, but the operation in ALU is nand which is decided by alu-control.
 Similarly for NDC and NDZ.

- ⑨ LHI : lhi ra, Imm

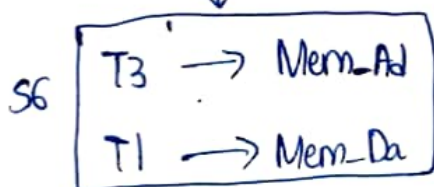
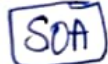
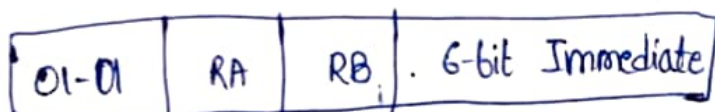


- ⑩ LW : lw ra, rb, Imm

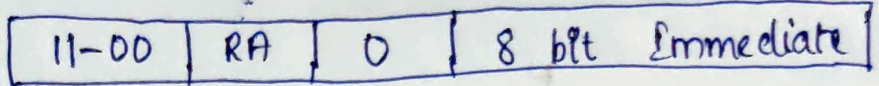




② SW : Sw ra, rb, Imm



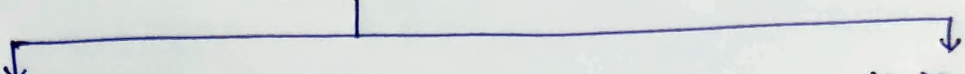
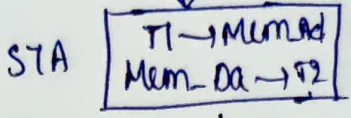
⑫ LM : lw Ra, Imm



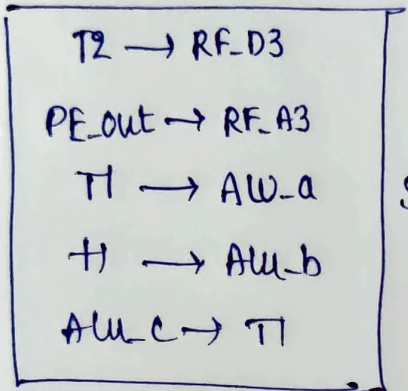
SP



SOA



if PE = 1



STB



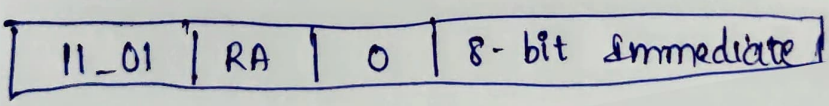
SFA

if PE = 0

Sf

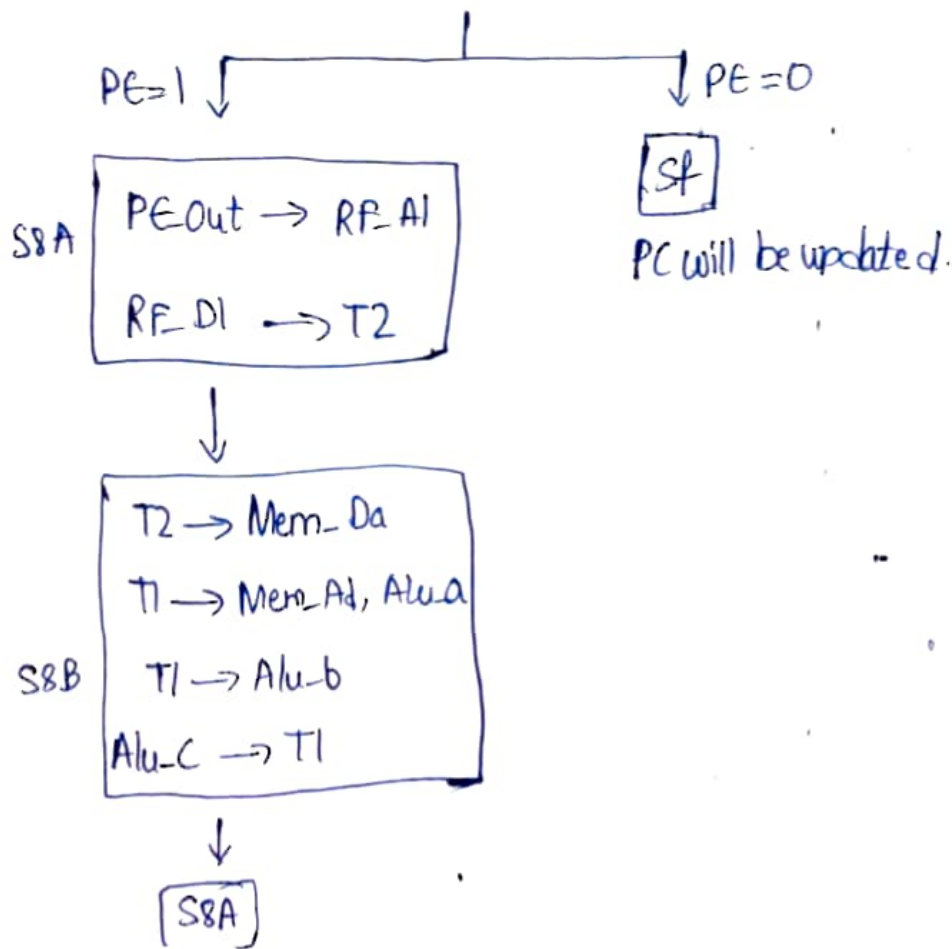
PC will be updated

⑬ SM : Sm, Ra, Imm

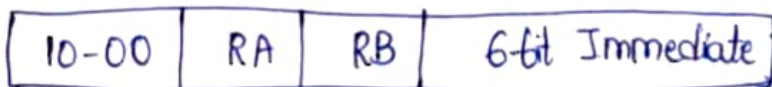


SOA





(14) BEQ : beq ra,rb,Imm

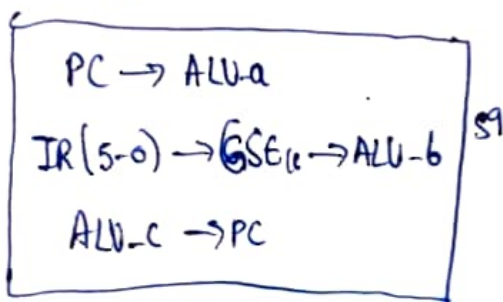


Sf

S8A

BEQ condition met

BEQ condition not met



Sf

PC will be updated.

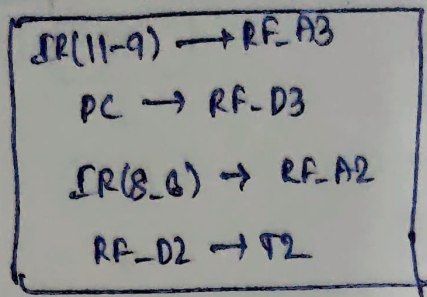
⑮ JAL : jalr ra, imm

10-01	RA	9 bit imm
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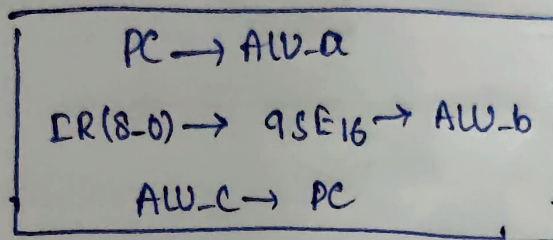
SE, SF



S10



S11



⑯ JLR : jalr ra, rb

10-10	RA	RB	000-000
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SE, SF



S10



T2 → PC S12

⑰ JRI : jri ra, imm

10-11	RA	9 bit Immediate
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SP



IR(11-9) → RF_A1

RF_D1 → ALU_a

IR(8-0) → 9SE16 → ALU_b

ALU_c → PC

813

Connections :

RF_A1 : (M1)

IR(11-9) → RF_A1 0

PE_Out → RF_A1 1

RF_A2 :

IR(8-6) → RF_A2

RF_A3 : (M2)

IR(5-3) → RF_A3 00

IR(8-6) → RF_A3 01

IR(9-7) → RF_A3 10

PE_Out → RF_A3 11

RF_D3 : (M3)

T3 → RF_D3 00

IR(8-0) → DE → RF_D3 01

T2 → RF_D3 10

PC → RF_D3 11

PC : (M4)

ALU_c → PC 0

T2 → PC 1

T1 : (M5)

RF_D1 → T1 0

ALU_c → T1 1

T2 : (M6)

RF_D2 → T2 00

RF_D2 → LSI → T2 01

RF_D1 → T2 10

Mem_da → T2 11

T3 : (M7)

Mem_da → T3 0

ALU_c → T3 1

ALU_a : (M8)

T1 → ALU_a 00

PC → ALU_a 01

T2 → ALU_a 10

RF_D1 → ALU_a 11

Аш-б :

TZ \rightarrow ALU-b 00

71 → Алл-б 01

DR(5-0) \rightarrow GSE₁₆ \rightarrow Alub 10

$IR(8-0) \rightarrow 9SE_{16} \rightarrow A_{11} - b \quad 11$

Mem_da! (MIO)

71 → Memda 0

T9 → Mum-Da 1

Mem-Ad: MU

PC \rightarrow Mem-Ad 00

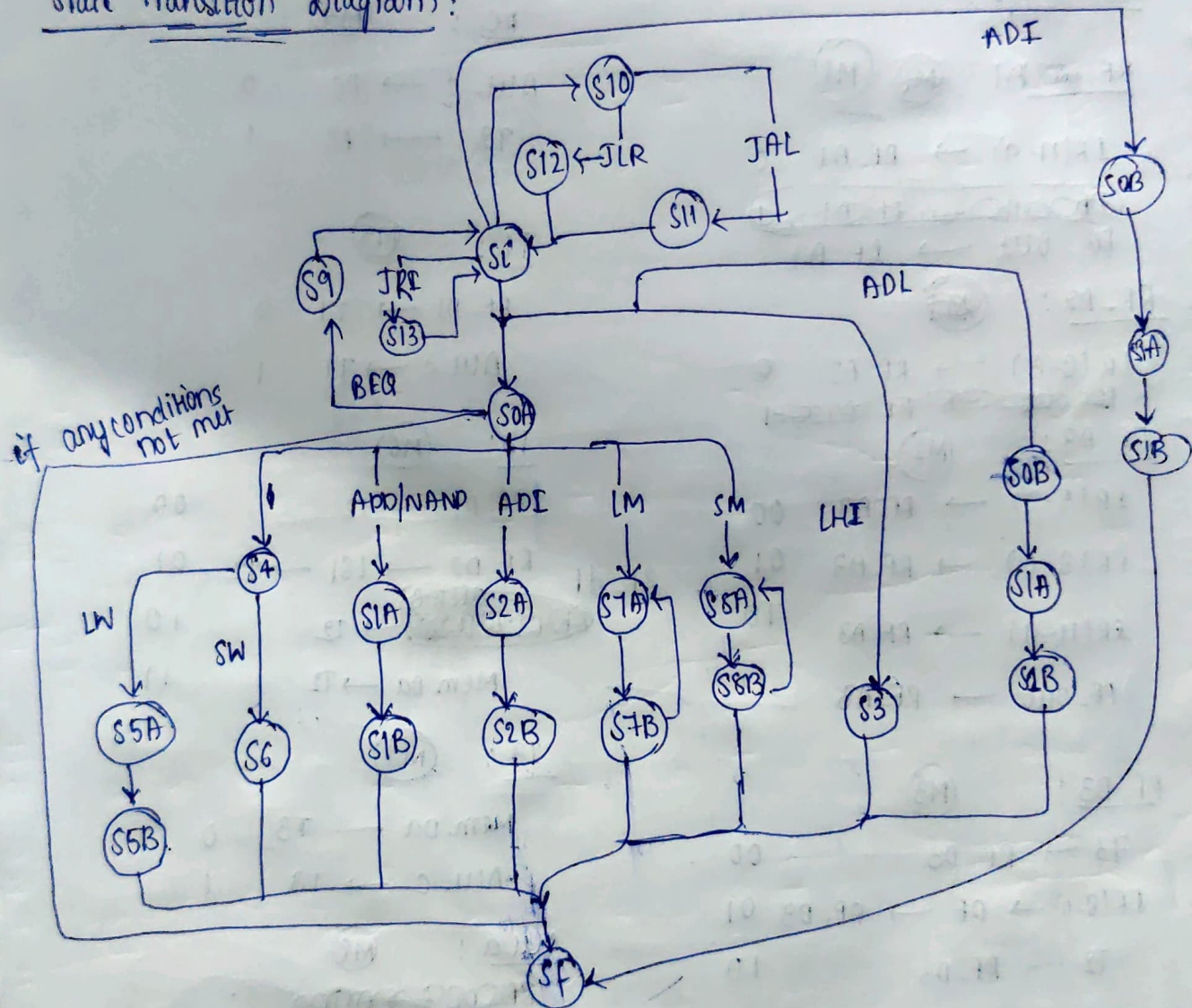
\rightarrow Mem-Ad 01

T3 ~~Q~~ ~~Q~~ → Mem-Ad

- ALU-C \rightarrow Mem-Ad. 10

TI \rightarrow Mem-Ad 11

State Transition Diagram:



	W-PC	W-LR	W-Mem	W-RF	M1 (RF-01)	M2 (RF-02)	M3 (RF-03)	M4 PC	M5 T1	M6 T2	M7 T3	M8 Aua	M9 Aub	M10 Mem-0	M11 Mem-Ad
Si	0	1	0	0	x	00	xx	xx	x	xx	x	xx	xx	x	xx
SOA	0	0	0	0	0	xx	xx	xx	0	00	x	xx	xx	x	xx
SOB	0	0	0	0	0	xx	xx	xx	0	01	x	xx	xx	x	xx
S1A	0	0	0	0	x	xx	xx	xx	x	xx	1	00	00	x	xx
S1B	0	0	0	1	x	00	00	xx	x	xx	x	xx	xx	x	xx
S2A	0	0	0	0	x	xx	xx	xx	x	xx	x	00	10	x	xx
S2B	0	0	0	1	x	001	00	xx	x	xx	x	xx	xx	x	xx
S3	0	0	0	0	x	10	001	xx	x	xx	x	xx	xx	x	xx
S4	0	0	0	0	x	xx	xx	xx	x	xx	1	10	10	x	xx
S5A	0	0	0	0	x	xx	xx	xx	x	11	x	xx	xx	x	10
S5B	0	0	0	1	x	10	10	xx	x	xx	x	xx	xx	x	xx
S6	0	0	1	0	x	xx	xx	xx	x	xx	x	xx	xx	0	01
S7A	0	0	0	0	x	xx	xx	xx	x	11	x	xx	xx	0	xx
S7B	0	0	0	1	x	11	10	xx	1	xx	x	00	01	x	xx
S8A	0	0	0	0	1	xx	xx	xx	x	10	x	xx	xx	x	xx
S8B	0	0	1	0	x	xx	xx	xx	1	xx	x	00	01	x	11
S9	1	0	0	0	0	xx	xx	0	x	xx	x	01	10	x	xx
S10	0	0	0	1	x	10	11	xx	x	00	x	xx	xx	x	xx
S11	1	0	0	0	x	xx	xx	0	x	xx	x	01	11	x	xx
S12	1	0	0	0	x	xx	xx	01	x	xx	x	xx	xx	x	xx
S13	1	0	0	0	0	xx	xx	0	x	xx	x	11	11	x	xx

Sf	1	0	0	0	0	xx	xx	0	x	xx	x	01	01	x	xx
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