Lab 5 - Pipelined Datapath

Introduction

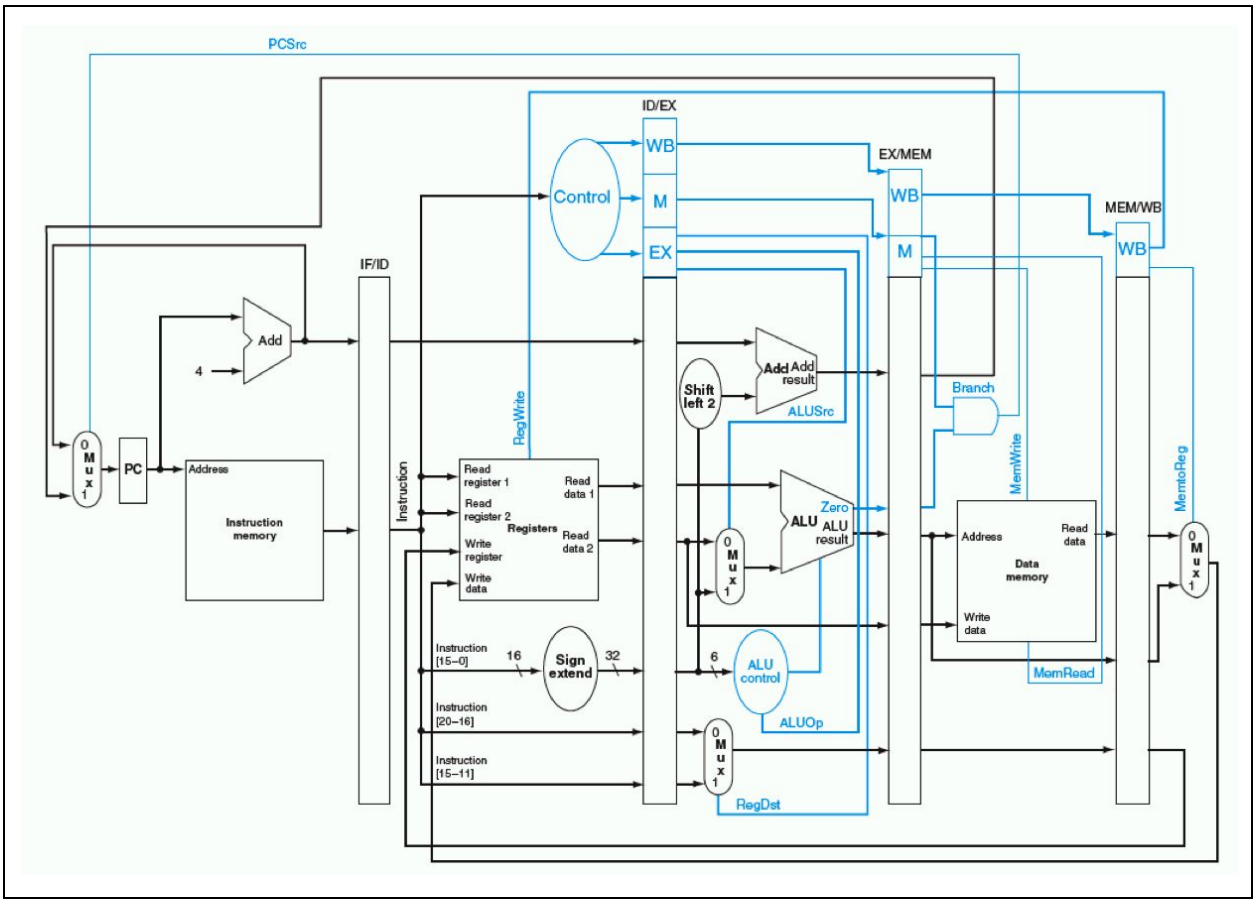
In the real world a signal must travel through the entire circuit from it's source to it's destination within one clock cycle. As the circuit's length increases so to does the time it takes for the signal to propagate. The longest path within a design is referred to as the critical path. Knowing the critical path's length allows us to determine the circuit's maximum clock frequency.

In the previous lab we designed a processor with the PC as the source and destination of all paths. This results in a processor with a low clock frequency. To improve this we can pipeline the processor. To do this we divide the datapath into stages, and at each stage we register the inputs and outputs. These registers act as new sources and destinations for the circuit's paths. This reduces the critical path of the circuit, allowing for an improved clock frequency.

Pipelining also has the benefit of processing multiple instructions concurrently. However, there are drawbacks. With multiple instructions executing data dependencies between them must be maintained. An instruction could read a register before the previous one has finished writing the new data back. There are a number of techniques to deal with these hazards that will be discussed in class, but for this lab you can assume pipeline stalls will be inserted by the compiler to ensure correct execution in the processor.

Deliverables

For this lab you are to extend your datapath from Lab 4 to a pipelined version. This is done by placing registers between each stage to hold the signals for one cycle. In this way each set of registers can hold one instruction. A pipelined version of the datapath can be found at Figure 4.51 in your textbook. I have also copied a version of it below.



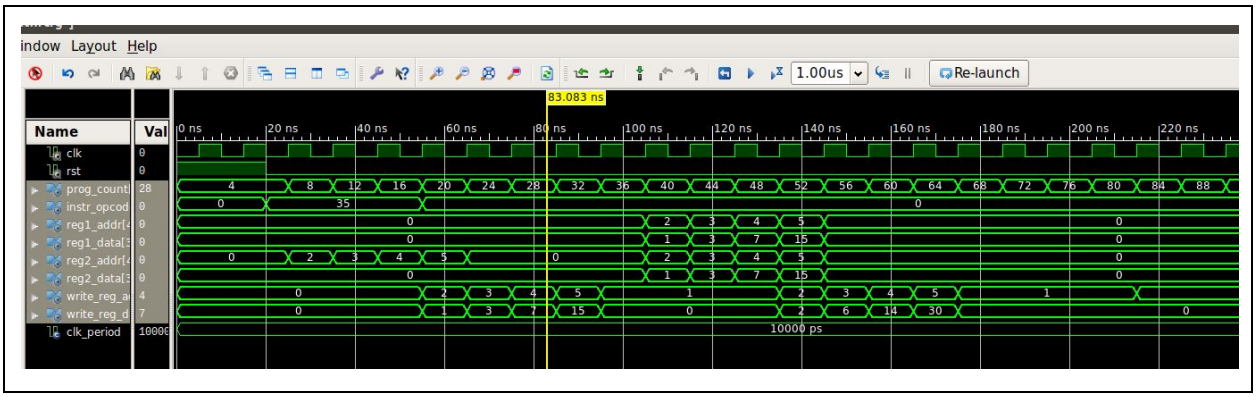
Turn in

Each group should turn in one tar file to iLearn. The contents of which should be:

- A README
- All Verilog files used in your design

Outputs

The expected waveform of the verilog simulation , for the input file, should be as shown next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