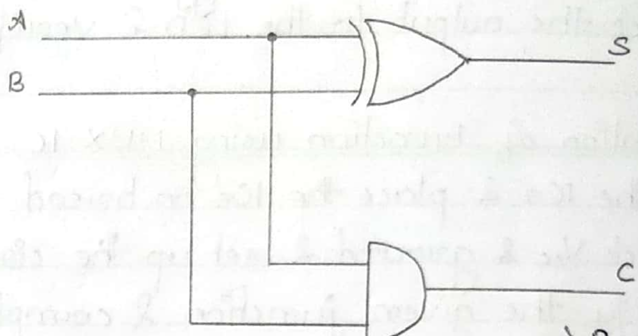
HALF ADDER

Truth Table

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Logic Circuit



Expression

$S = A\bar{B} + \bar{A}B = A \oplus B$

$C = AB$

A \ B	0	1
0	0	1
1	1	0

$S = A \oplus B$

A \ B	0	1
0	0	0
1	0	1

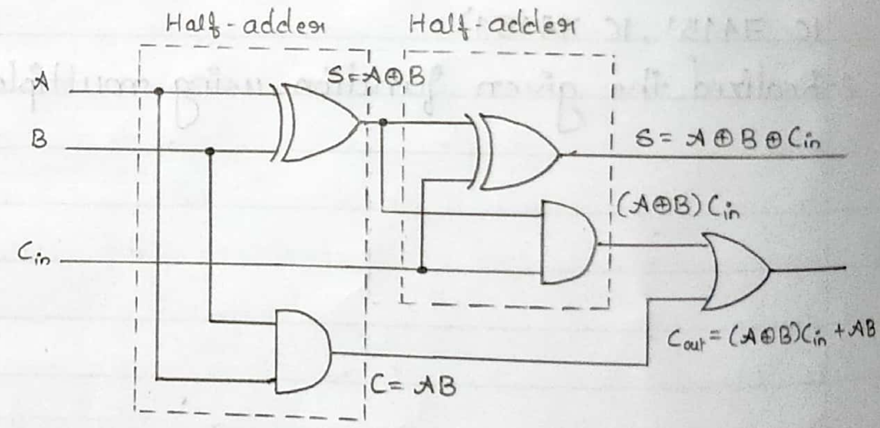
$C = AB$

FULL ADDER

Truth Table

Inputs			Sum	Carry
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logic Circuit



Expression

$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

$= (A\bar{B} + \bar{A}B)\bar{C}_{in} + (AB + \bar{A}\bar{B})C_{in}$

$= (A \oplus B)\bar{C}_{in} + (\overline{A \oplus B})C_{in} = A \oplus B \oplus C_{in}$

$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$

$= AB + (A \oplus B) C_{in}$

A \ BC_{in}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$S = A \oplus B \oplus C_{in}$

A \ BC_{in}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$C_{out} = AB + (A \oplus B)C_{in}$

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Aim

1. To implement half adder & full adder circuits using logic gates and realize full adder using NAND gates only.
2. To implement half subtractor & full subtractor circuits using logic gates and realize full subtractor using NOR gates only.

Components Required

IC 7400, IC 7402, IC 7404, IC 7408, IC 7432, IC 7486 and connecting wires

Theory

A half-adder is a combinational circuit with two binary inputs (augend and addend bits) and two binary outputs (sum and carry bits). It adds the two inputs (A and B) and produces the sum (S) and the carry (C) bits. It is an arithmetic circuit used to perform the arithmetic operation of addition of two single bit words.

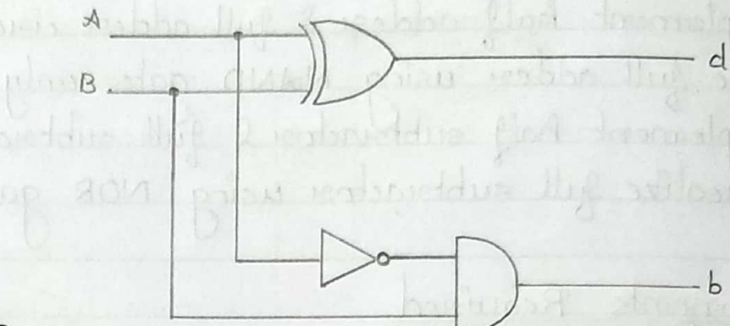
A full-adder is a combinational circuit that adds two bits and a carry and outputs a sum bit and a carry bit. The full-adder adds the bits A and B and the carry from the previous column called the carry-in C_{in} and outputs the sum bit S and the carry bit called the carry-out C_{out}. The variable S gives the value of the least significant bit of the sum. The variable C_{out} gives the output carry. When all the bits are 0s, the output is 0. The S output is equal to 1 when only 1 input is equal to 1 or when all the inputs are equal to 1. The C_{out} has a carry of 1 if two or three inputs are equal to 1.

HALF SUBTRACTOR

Truth Table

Inputs		Outputs	
A	B	d	b
0	0	0	0
1	0	1	0
1	1	0	0
0	1	1	1

Logic Circuit



Expression

$d = A\bar{B} + \bar{A}B$

$= A \oplus B$

$b = \bar{A}B$

A \ B	0	1
0	0	1
1	1	0

$d = A \oplus B$

A \ B	0	1
0	0	0
1	0	1

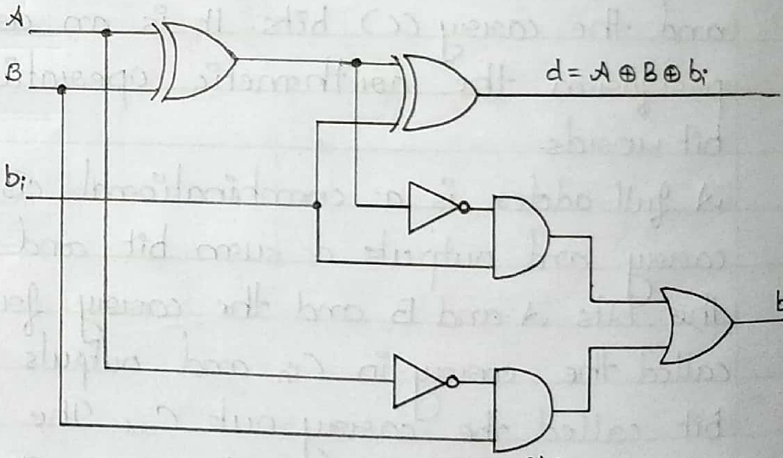
$b = \bar{A}B$

FULL SUBTRACTOR

Truth Table

Inputs			Difference	Borrow
A	B	b_i	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Logic Circuit



Expression

$d = \bar{A}\bar{B}b_i + \bar{A}B\bar{b_i} + A\bar{B}\bar{b_i} + ABb_i = b_i(AB + \bar{A}\bar{B}) + \bar{b_i}(A\bar{B} + \bar{A}B)$

$= b_i(\overline{A \oplus B}) + \bar{b_i}(A \oplus B) = A \oplus B \oplus b_i$

$b = \bar{A}\bar{B}b_i + \bar{A}B\bar{b_i} + \bar{A}Bb_i + ABb_i = \bar{A}B(b_i + \bar{b_i}) + (AB + \bar{A}\bar{B})b_i$

$= \bar{A}B + (\overline{A \oplus B})\, b_i$

A \ Bb_i	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$d = A \oplus B \oplus b_i$

A \ Bb_i	00	01	11	10
0	0	1	1	1
1	0	0	1	0

$b = \bar{A}B + (\overline{A \oplus B})\, b_i$

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A half-subtractor is a combinational circuit that subtracts one bit from the other and produces the difference. It also has an output to specify if a 1 has been borrowed. It is used to subtract the LSB of the subtrahend from the LSB of the minuend when one binary number is subtracted from the other. It has two inputs A and B and two outputs d and b. d indicates the difference and b is the output signal generated that informs the next stage that a 1 has been borrowed.

A full-subtractor subtracts one bit (B) from another bit (A), when already there is a borrow b_i from this column for the subtraction in the preceding column, and outputs the difference bit (d) and the borrow bit (b) required from the next column. So a full-subtractor is a combinational circuit with three inputs (A, B, b_i) and two outputs d and b. The two outputs present the difference and output borrow.

Procedure

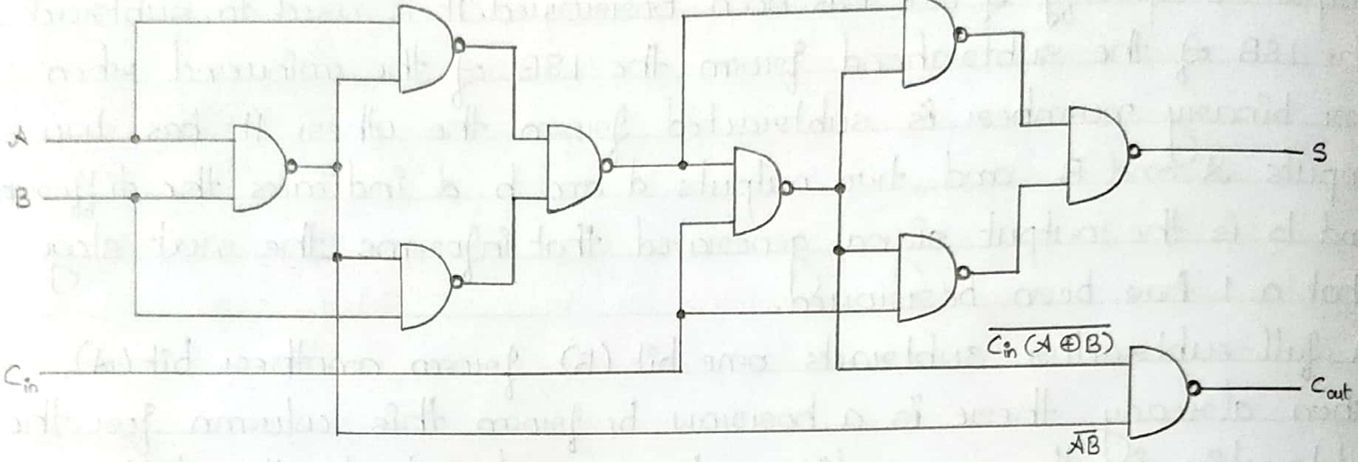
1. Place the ICs on the bread board.
2. Connect V_{cc} and ground (GND) to their respective pins.
3. Provide input from switch.
4. Connect the output of LED and verify the operation as per the truth table obtained.
5. Repeat these steps for different ICs taken.

Teacher's Signature : ____________

Realization of Full Adder Using NAND Gates

$$S = A \oplus B \oplus C_{in} = \overline{\overline{(A\oplus B)\cdot\overline{(A\oplus B)C_{in}}}\cdot\overline{C_{in}\cdot\overline{(A\oplus B)C_{in}}}}$$

$$C_{out} = C_{in}(A\oplus B) + AB = \overline{\overline{C_{in}(A\oplus B)}\cdot\overline{AB}}$$



Realization of Full Subtractor Using NOR Gates

$$d = A\oplus B\oplus b_i = (A\oplus B)\oplus b_i = \overline{(A\oplus B)}\,b_i + (A\oplus B)\overline{b_i}$$

$$= [(A\oplus B) + \overline{(A\oplus B)}\,\overline{b_i}][\,b_i + \overline{(A\oplus B)}\,\overline{b_i}]$$

$$= \overline{\overline{(A\oplus B) + \overline{(A\oplus B)+b_i}} + \overline{b_i + \overline{(A\oplus B)+b_i}}}$$

$$= \overline{\overline{\overline{(A\oplus B) + \overline{(A\oplus B)+b_i}} + \overline{b_i + \overline{(A\oplus B)+b_i}}}}$$

$$b = \bar{A}B + b_i\overline{(A\oplus B)} = \bar{A}(A+B) + \overline{(A\oplus B)}[(A\oplus B)+b_i]$$

$$= \overline{\overline{\overline{A} + \overline{(A+B)}} + \overline{(A\oplus B) + \overline{(A\oplus B)+b_i}}}$$