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FAMILIARIZATION OF DIGITAL IC TRAINER KIT

AIM :- To familiarize the digital IC trainer kit

Theory :- Digital IC trainer kit is an equipment used to test and setup digital circuits for lab experiments. Integrated circuits can be fitted in sockets on bread board provided in it. There is limit in voltage source and clock signals in it. The frequency of clock can be selected by turning knob at different positions in just mono power manually a switch is also provided. A set of select switches are also provided to select low and high state for digital inputs LED's are provided as digital

Technical Specification

1. 10 logic i/p switches providing high / low o/p
2. 10 logic o/p indicates with temperature.
3. 4 seven segment LED display with decorder drives and provision for BCD signal i/p.
4. a) fixed clock generator 1Hz, 10Hz, 100Hz, 1KHz, 10KHz, 1MHz
   b) Variable clock generator providing 1Hz – 1KHz

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5. Single pulse generator.
6. Experimental problem based comparing 1 no of IC sockets having 20 pins of IC sockets having 40 pins solder bread board with 1680 pins
7. PC regulated power supply
8. Input power supply 230V 50Hz AC.
9. Input signal are taken from output signals are given to spring type socket which provide selectable contacts.

System Description

1. logic switches,
   10 logic switches having 2 positions
   High position provides logic 1
   low position provides logic 0

2. Experimental problem based.
   a) IC socket
      It contain of 1 no. of IC 2if socket with 20 pins and 40 pins. A variable clock generator providing 1Hz - 1KHz output unaccilable.
   b) Solder less bread board
      1680 points are provided

3. 7 segment LED display
   - 4 number of 7 segment LED display
   - Each display is driven by a decoder IC 7487.

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- provision for BCD input.
- 4 socket marked as 1, 2, 4, 8 provided facilely for feeding in BCD input.

4. large monitor
- 10 No of LED logic lamp monitor
- make of 2 no. of drive IC 7406 10 inputs NOT gate with input on socket, LED will glow (logic 1) or does not glow (logic 0)

5. Clock generator
- Based on x-{2} of 4 MHz frequency
- provides a Clock output.
- Variable clock generator providing 1Hz - 1KHz output

6. Mono pulsar
- To get 2 pulse with in definite period
- achieved by a push button provides 2 pulse
- provides both +ve and -ve level which can be certified on a oscilloscope.

7. Power Supply
DC regulated supply using transformer rectifier, filter and Amp regulator circuit for +5V and 1-12 V/500 mA.

8. General
Ground and Vcc port (+5V) are available at different location of board for easy supply of power supply.

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Operation procedure

a. keep power ON / OFF switch in OFF position
b. Connect power to unit using 3 pin plug for 2 3pin socket with proper earth connection.
c. place the IC connection on IC to tested / connected for experiment on 21F packets.
d. Connect power to IC's using patch cords and complete circuit connection by giving inputs.
e. Switch ON power to unit and put power ON/OFF switch on trainer kit to ON position.
f. Check availability of power +5V, -12V.
g. Clock generation output can be tapped to seq port.
h) For having mono pulse output, connect from derived and control parts.

RESULT

Familiarized the digital IC trainer kit.

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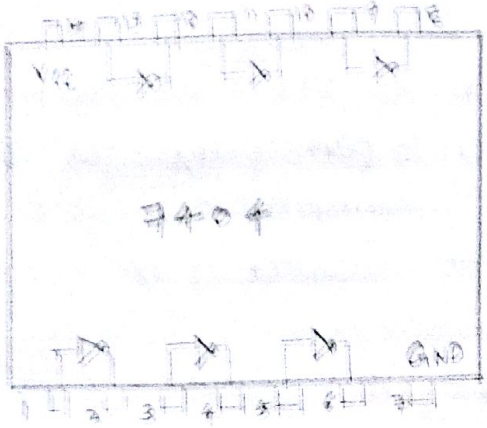
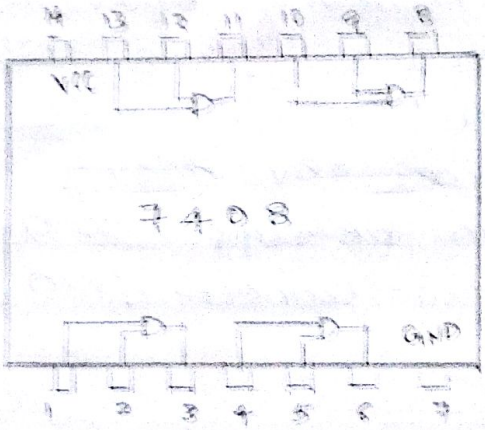
PIN DIAGRAM | GATE SYMBOL | TRUTH TABLE



NOT GATE

$Y = \bar{A}$

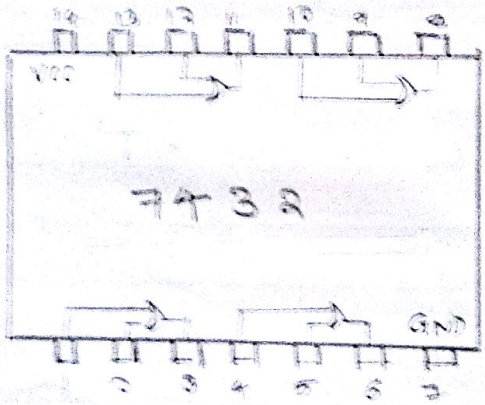
A	B
0	1
1	0



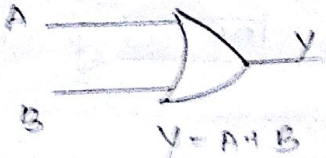
AND GATE

$Y = A \cdot B$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

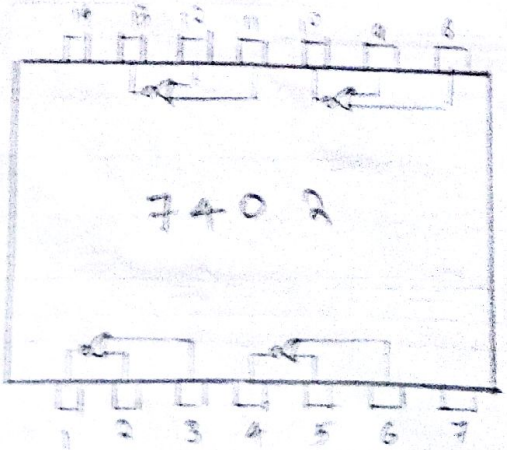


OR GATE

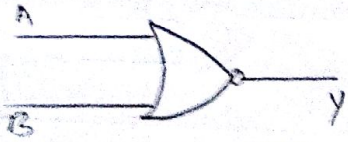


$Y = A + B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



NOR GATE



$Y = \overline{A + B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

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FAMILIARIZATION OF LOGIC GATES

Aim :- To verify truth table of NOT, AND, OR, NAND, NOR, XNOR gates, to verify relationship using truth table.

Components Required :-

IC's 7404, 7400, 7408, 7410, 7411, 7433, 7486

Principle :-

logic gates are basic elements that make up digital system may have one output with one or more input.

OR gate :- The o/p is high if any one of i/p is high 7432 is logical 2 i/p OR gate IC.

$Y = A+B$

NOT gate :- The gate acts as an inverter. The o/p is complement of i/p 7404 is single i/p NOT gate IC.

AND gate :- It give a high o/p when all its i/p are high 7408 is a quad 2 i/p AND gate IC.

$Y = A \cdot B$

NOR gate :- This is a combination of OR and NOT gate 7402 is a 2i/p NOR gate IC

$Y = \overline{A+B}$

NAND gate :- 7410 is a 3i/p NAND gate IC 7420 is

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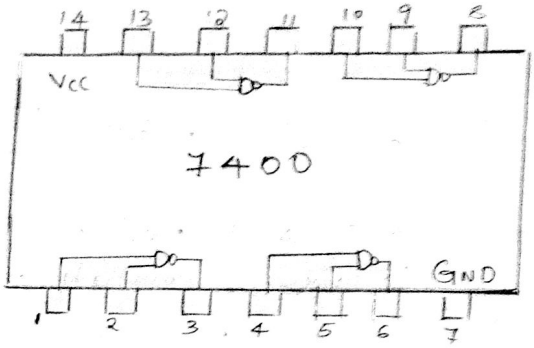
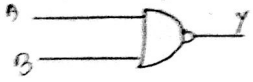
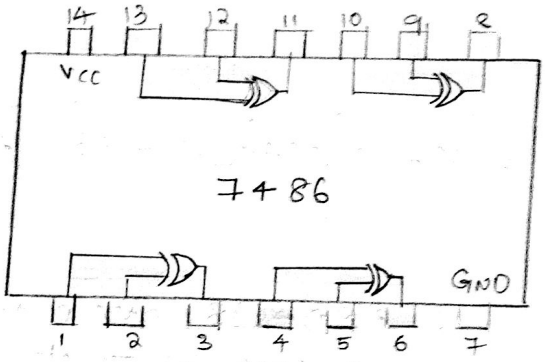
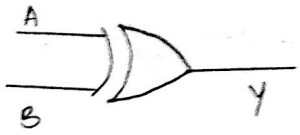




2 i/p NOR gate

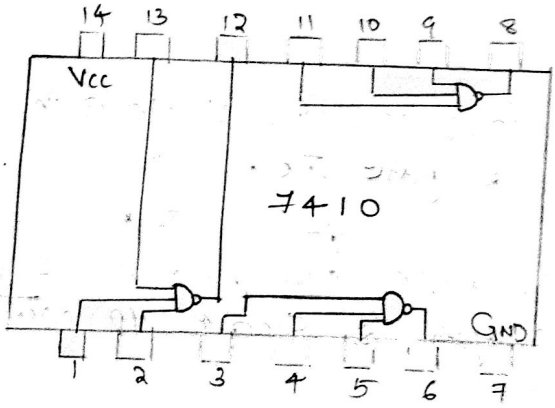
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

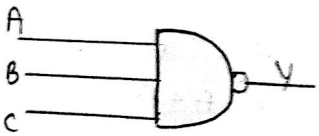




XOR gate

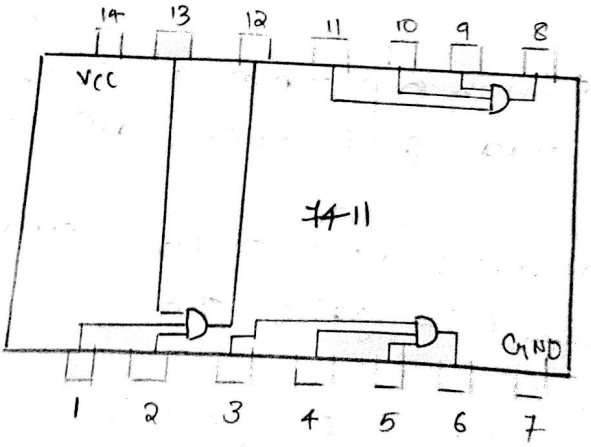
A	B	Y
0	0	0
0	1	1
1	1	0

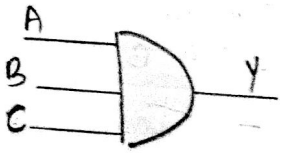




3 i/p NAND GATE

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0





3 i/p AND GATE

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

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a 4 i/p NAND gate Ic, 7400 is a 7 i/p Nand gate Ic

$Y = \overline{A \cdot B}$

XOR gate :- The o/p is high if odd no: of i/p is one high. 7486 is a XOR gate Ic.

$Y = A \oplus B$

Procedure :-

(1) place Ic's on bread board.
(2) Connect vcc and ground to respective pins.
(3) provide i/p from switch.
(4) Connect o/p of LED and verify operation as per given table.

RESULT :-

Familiarised with various logic gates and varified the truth table also verified given operation using truth table.

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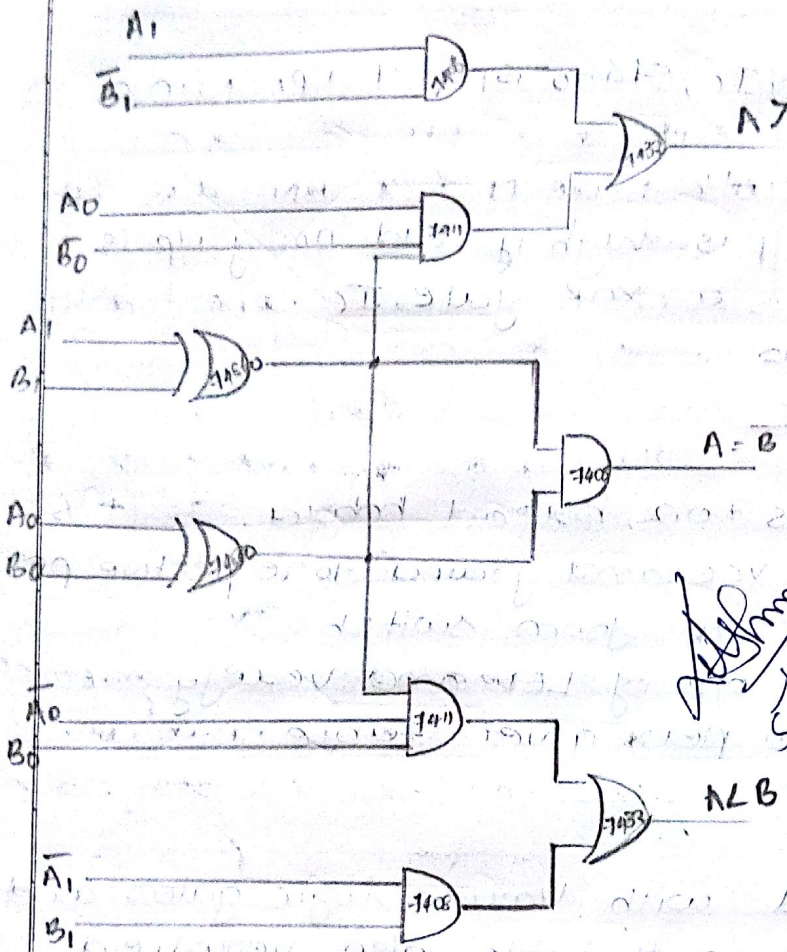
2 bit Comparator



Truth Table

Input				Output		
A_1	A_0	B_1	B_0	$A>B$	$A=B$	$A<B$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

5/5

K MAP

A > B

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

$A_1\bar{B}_1 + A_0\bar{B}_1\bar{B}_0 + A_1B_0\bar{B}_0$

A = B

A_1A_0 \ B_1B_0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

$\bar{A}_1\bar{A}_0\bar{B}_1\bar{B}_0 + \bar{A}_1A_0\bar{B}_1B_0 + A_1A_0B_1B_0 + A_1\bar{A}_0B_1\bar{B}_0$

A < B

A_1A_0 \ B_1B_0	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

$\bar{A}_1B_1 + \bar{A}_1\bar{A}_0B_0 + \bar{A}_0B_1B_0$

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2/3 BIT BINARY COMPARATORS

AIM :- To verify the truth table of two bit and three bit comparators using logic gates.

Apparatus Required :- IC7486, IC7404, IC7408 etc

Theory :- Digital or binary comparators are made up from standard AND, NOR and NOT gates that compare the digital signals at their input terminals and produces an output depending upon the condition of the inputs. For example, whether input A is greater than, smaller than or equal to input B etc.

Digital Comparators

They can compare a variable or unknown number for example A (A_1, A_2, A_3, A_n, etc) against that of a constant or known value such as B (B_1, B_2, B_3, B_n etc) and produces an output depending upon the result. For example, a comparator of 2 bit (A and B) would produce the following 3 output conditions $A>B$, $A=B$, $A<B$. This is useful if we want to compare two values and produces the following output from a counter when a certain count number is reached. Consider 2 bit and 3 bit comparator as below.

2-BIT MAGNITUDE COMPARATOR

A = A1A0

B = B1B0

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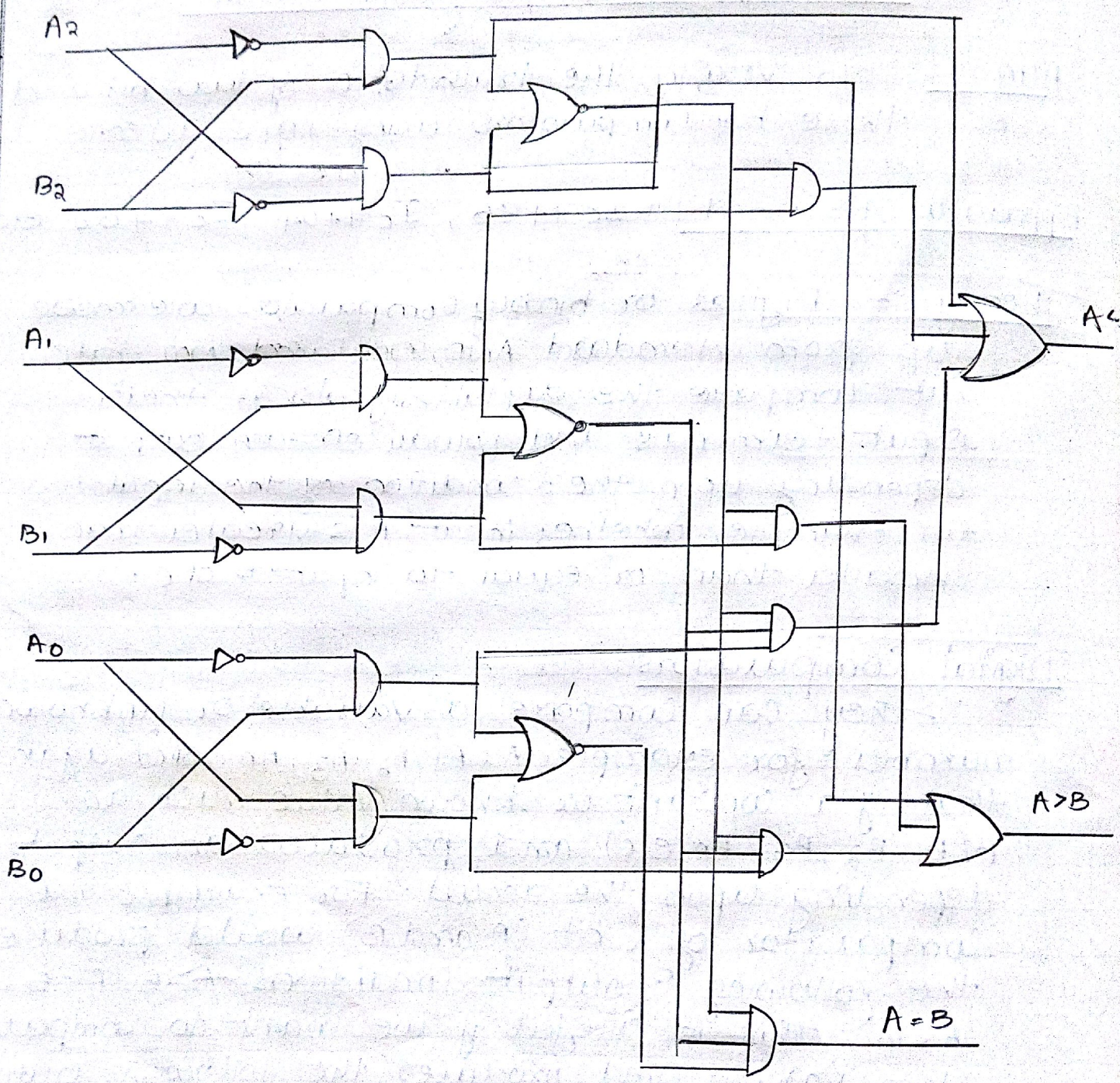
3 bit Comparator



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Here each subscript represents one of the give digits in the numbers equality.

The binary number A & B will be equal if all the pair of significant digits of both the numbers are equal.

ie $A_1 = B_1$ & $A_0 = B_0$ Since the number are binary the given digits are either 0 or 1 and the boolean function for equality of any two digits A_i and B_i can be expressed as 1 only if A_i and B_i are equal.

For the equality of A and B, all x_i variables (for $i = 0, 1$) must be 1. So the equality condition of A & B can be implemented using AND operation. as $(A=B) = x_1 x_0$. The binary variable $(A=B)$ is 1 only if all pair of the digits of the 2 numbers are equal.

In equality

In order to manually determine the greater of two binary number, we inspect the relative magnitude of pair of significant digit, starting from the most significant bit, gradually proceeding towards lower significant bit until an inequality is found. when an inequality is found if the correspond bit of A_1, 1 and that of B is 0 then we conclude that $A > B$. $(A > B)$ and $A < B)$ are output binary variable which are equal to 1 when $A > B$ or $A < B$ respectively. Similar procedure can be done for 8 bit Comparator.

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Procedure

ⓐ verify the gate
ⓑ make the connection as per the circuit diagram
ⓒ switch on Vcc
ⓓ Applying i/p and check for the outputs.
ⓔ The readings of output should be tabulated.

RESULT

verified the truth table of 2 bit comparator using logic gates.

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Truth Table

Input				Binary to grey					Grey to Binary				
I_3	I_2	I_1	I_0	M	D_3	D_2	D_1	D_0	M	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	1	0	0	0	0	1	1	0	0	0	1
0	0	1	0	0	0	0	1	1	1	0	0	1	1
0	0	1	1	0	0	0	1	0	1	0	0	1	0
0	1	0	0	0	0	1	1	0	1	0	1	1	1
0	1	0	1	0	0	1	1	1	1	0	1	1	0
0	1	1	0	0	0	1	0	1	1	0	1	0	0
0	1	1	1	0	0	1	0	0	1	0	1	0	1
1	0	0	0	0	1	1	0	0	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1	0
1	0	1	0	0	1	1	1	1	1	1	1	0	0
1	0	1	1	0	1	1	1	0	1	1	1	0	1
1	1	0	0	0	1	0	1	0	1	0	0	0	0
1	1	0	1	0	1	0	1	1	1	0	0	0	1
1	1	1	0	0	1	0	0	1	1	0	0	1	1
1	1	1	1	0	1	0	0	0	1	1	0	1	0

D_3 m=0

I_3I_2 \ I_1I_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$D_3 = I_3$

D_2 m=1

I_3I_2 \ I_1I_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$D_2 = I_3$

D_1 m=0

I_3I_2 \ I_1I_0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

$D_1 = I_3 \oplus I_2$

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CODE CONVERTER

AIM

To design and set up a 4-bit binary to grey and grey to binary code converter using mode control.

COMPONENTS REQUIRED

IC's 7486, 7408, trainer kit, connecting wires.

THEORY

To convert a binary code to grey code, following rules are applied:

1. MSB of gray is same as that of binary code.
2. From left to right each adjacent pair of binary digits are to get next gray digit. Carries are neglected.

To convert a gray code to binary code, following rules are applied:

1. The most significant bit in binary is same as corresponding digit in gray code.
2. Going from left to right, add each digit of binary generated with gray code bit of next adjacent position to get the next digit of binary. Discard carry.

To design a code converter, we use a code

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CODE CONVERTER CIRCUIT

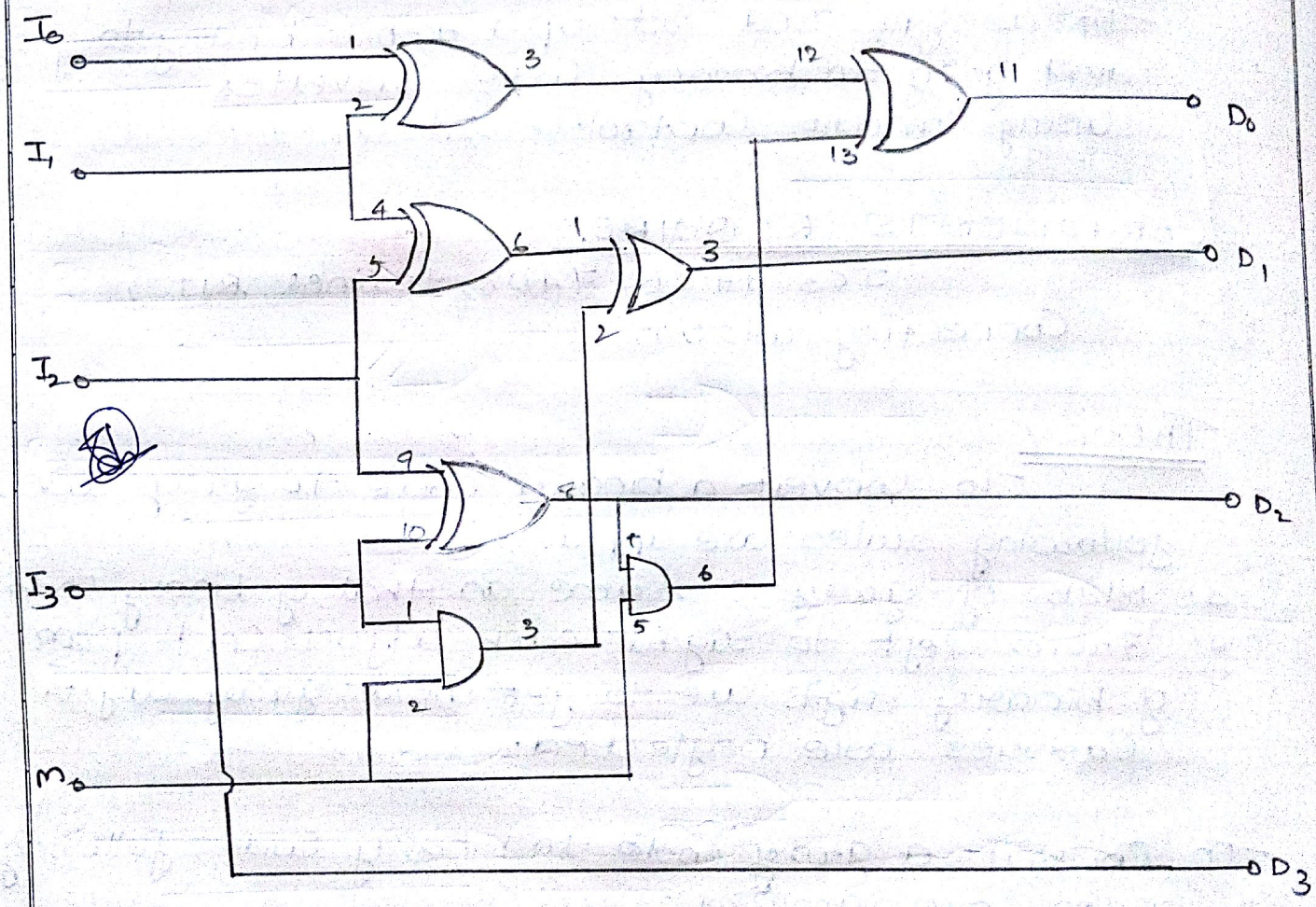

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table treating as a truth table to express each output as a Boolean algebraic function of all the inputs.

PROCEDURE

(i) place the IC's on the bread board.
(ii) Connect the Vcc and ground to the pins
(iii) provide i/p from the toggle switch
(iv) Connect the o/p to the LED and verify the operation as per truth table.

No Result

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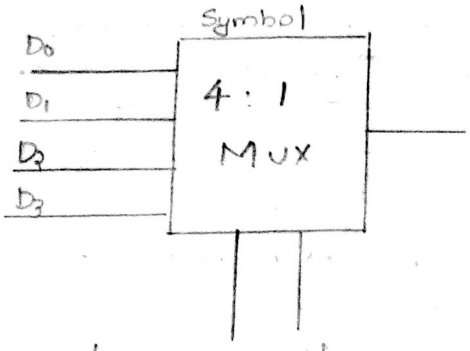
multiplexer

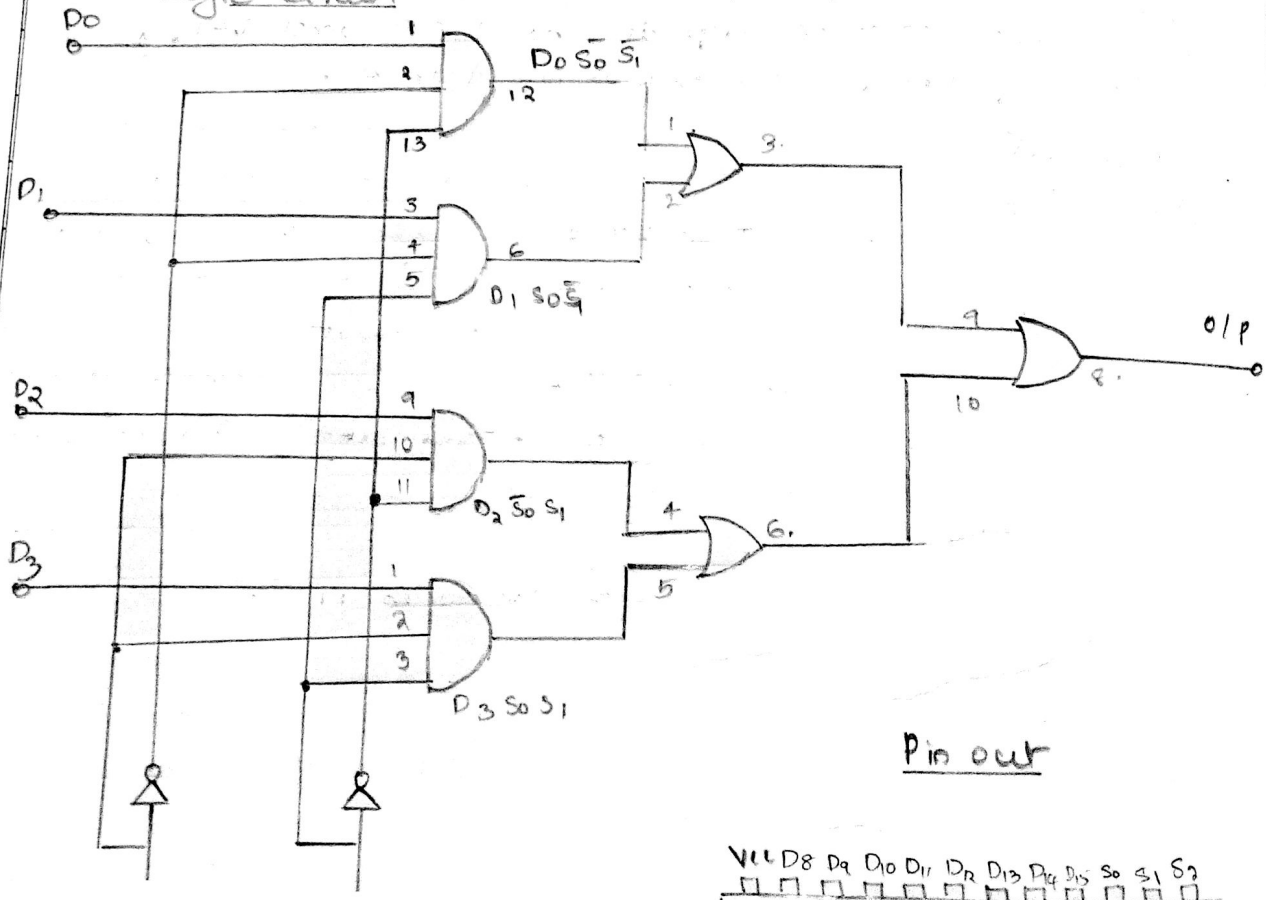
Symbol



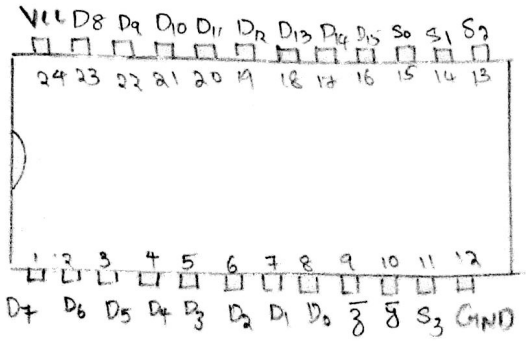
Truth Table

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Logic Circuit



Pin out



16 : 1
MUX

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MULTIPLEXER AND DEMULTIPLEXER

AIM

a) To design and setup a 4:1 multiplexer and 1:4 demultiplexer using discrete gates and familiarize the mux and demux IC's 74150, 74151, 16:1, 8:1 74154 1:16

b) Realization of the function using MUX ICs 74150, 74151, $F(A,B,C,D) = \Sigma m(1,5,7,9,10,11,12)$

PRINCIPLE

Multiplexer and demux is a special Combinational Circuit that is one of the most widely used standard circuits in digital design.

The multiplexer is a logic circuit that gates one out of several inputs to a single output. The input selected is Controlled by a set of select inputs. For selecting one out of N inputs for connection to the output, a set of M select inputs is required where $2M = N$.

The demux performs the reverse operation of a mux, It accepts a single input and distributes it over several outputs. The select input code determine to which output data input will be transmitted. The no: of output lines N and the select lines is M, where $N = 2M$

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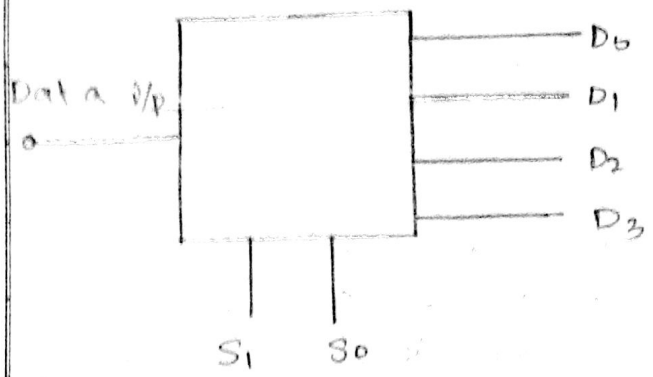
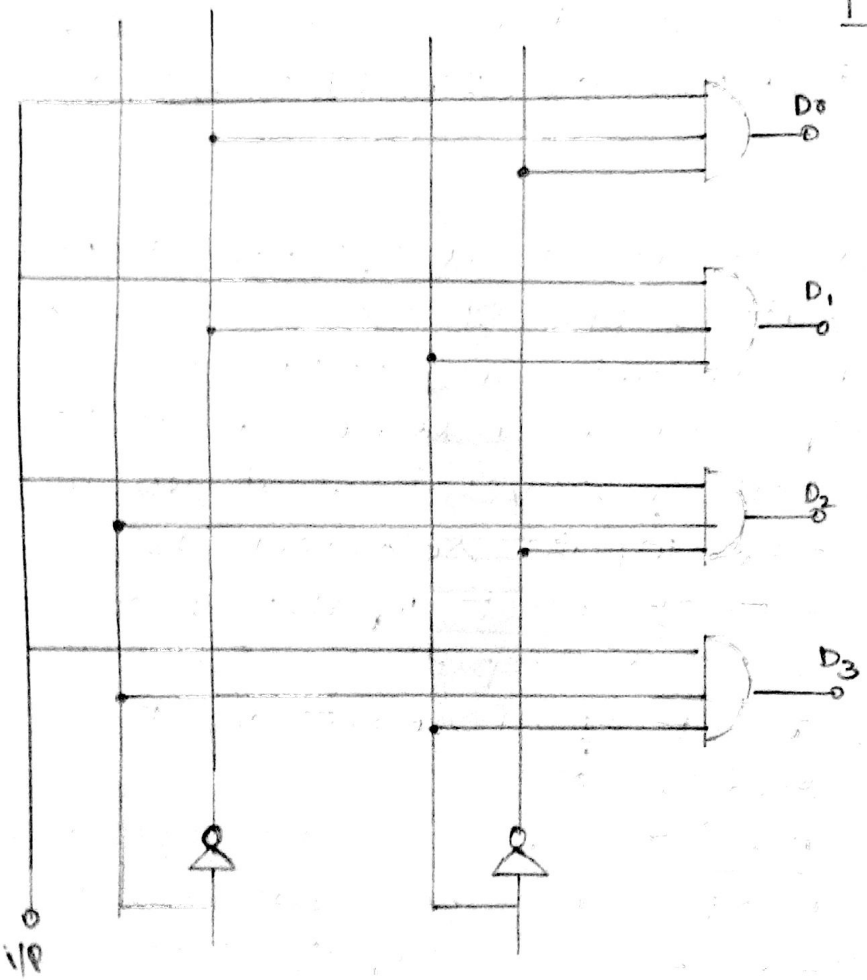
1:4 mux



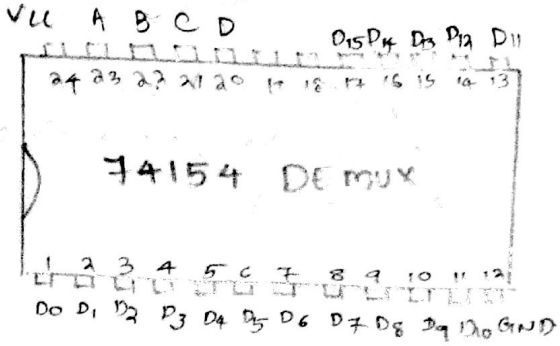
Truth Table

S_1	S_0	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Logic diagram



Pin out



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Standard MUX IC's are

4:1 - 74153

8:1 - 74151

Demux IC for 1:16 is 74154

PROCEDURE

(a) Place IC's on the bread board.

(b) Connect the Vcc and GND to resp pins.

(c) provide i/p from the toggle switch.

(d) Connect the o/p to the LED and verify the operation as per truth table.

APPLICATIONS

Binary / BCD conversions are most often encounted in connection with computer applications. Numerical data transmitted in BCD form from input devices must be converted to binary so that arthimetic operations can be peyormed on it. The binary results of the arithemetic operations must then be converted to BCD for transmission to output devices. Conversion tables may be stores in the ROM.

IC 74150 (16:1 mux)

The data selector contain full on chip decoding to select the desired data source IC 74150 selects one of the 16 data sources to enable the device. A higher level at the strobe forces the o/p to be high & its o/p is low.

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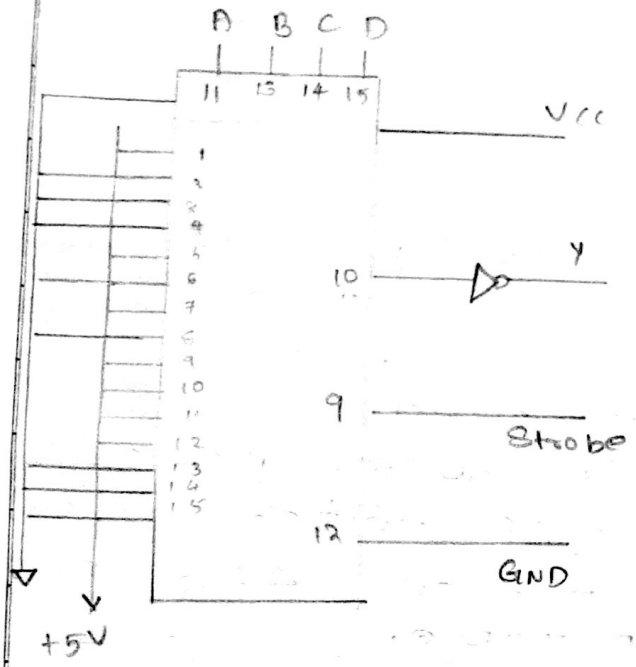
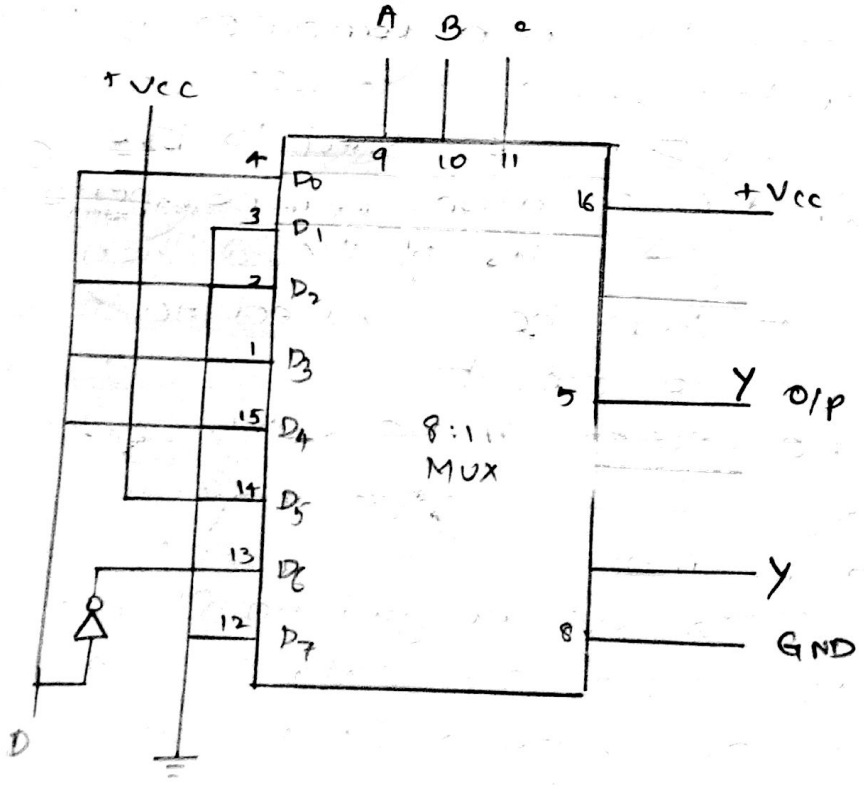
$Y = \Sigma m(1, 5, 7, 9, 10, 11, 12)$





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IC 74151

It is a popular 16 pin dual input IC that implements an 8:1 mux. Vcc is on pin 15 and GND is on pin 8 pins 5 and 6 are the output. On pin 6 is the inverted version of the output. The enable is on pin 7.

IC 74138

It is a high speed 1:8 DEMUX the multiple input enables allow parallel expansion to 1 of 24 decoder using IC.

PROCEDURE

(a) Check the IC's and place the IC's on bread board.
(b) Connect Vcc and ground and set up the circuit as per the given diagram
(c) Simplify the given function and complement the 16:1 mux and 8:1 mux using IC's 74150 and 74151.
(d) verify the function table.

RESULT

4:1 mux and 1:4 DEMUX were implemented using basic gates and mux IC's and outputs were verified.

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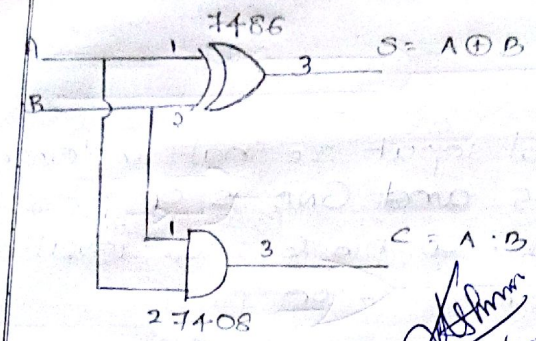
HALF ADDER



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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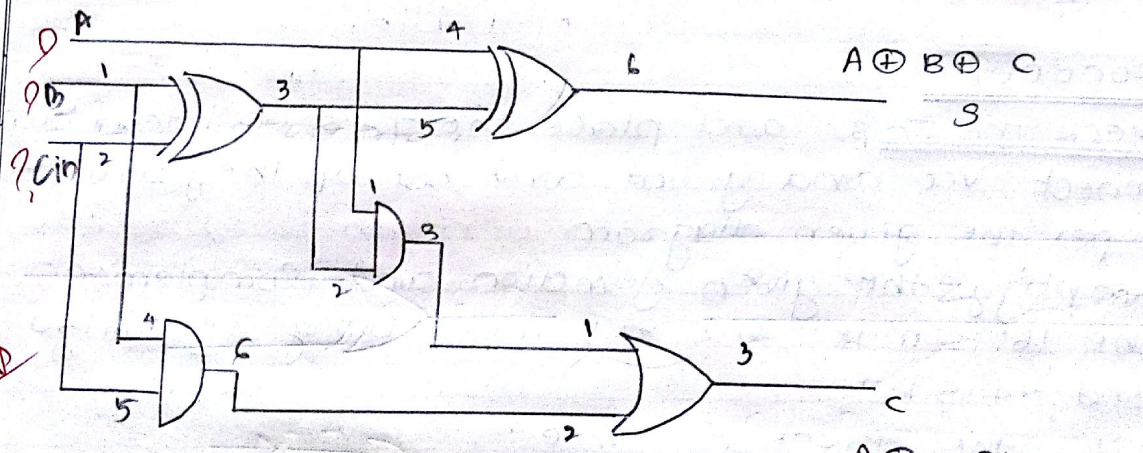
FULL ADDER



A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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ADDER AND SUBSTRACTOR USING BASIC AND UNIVERSAL GATES

AIM

Design and setup half adder, full adder, half substractor and full substractor using basic gates and universal gates.

COMPONENTS REQUIRED

Trainer kit, Ic's 7408, 7432, 7404, 7400, 7402, Connecting wires.

THEORY

A half adder is a logic circuit that adds two binary bits. The input to the circuits are two bits two augend (x) and addend (y) and the output of the circuit of the circuit are the sum (s) and the carry (c) The sum of the output is 1 when either x or y is 1 and Carry out is 1 when both x and y are one.

A full adder is a combinational circuit that performs the arithematic sum of three inputs bits - x, y, z and produce sum (s) and carry (c) output.

The logic circuit used for binary substractor are known as binary substractors. Here each subtrahend bit of the number is substracted from its corresponding significant minuend bit to form a difference bit.

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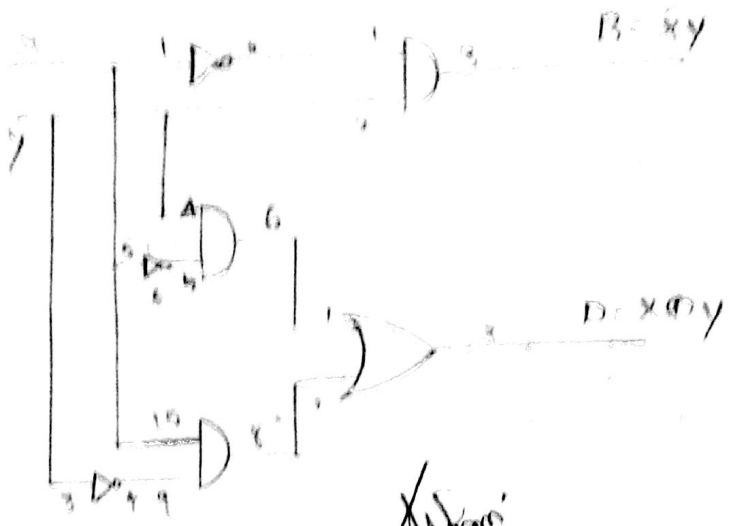
HALF SUBTRACTOR



X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$D = \overline{(\bar{x} + xy)(\bar{y} + xy)}$$

$$= \overline{(\bar{x} + xy)} + \overline{(\bar{y} + xy)}$$

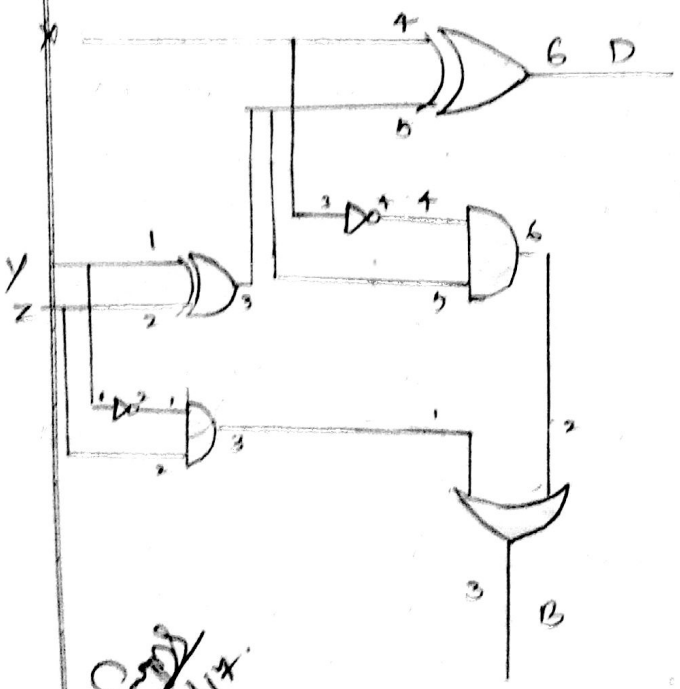
$$= x \cdot x\bar{y} + y \cdot \bar{x}y$$

$$= x\bar{y} + y\bar{x}$$

$$= \underline{x \oplus y}$$

5/5

FULL SUBTRACTOR



X	Y	Z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

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RESULT

Verified and studied all the adder and subtractor circuit.

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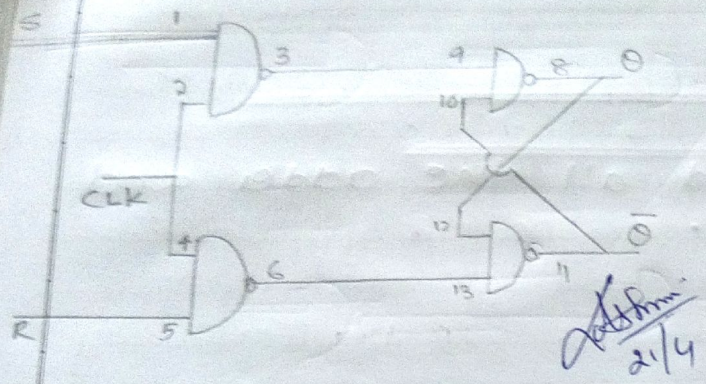
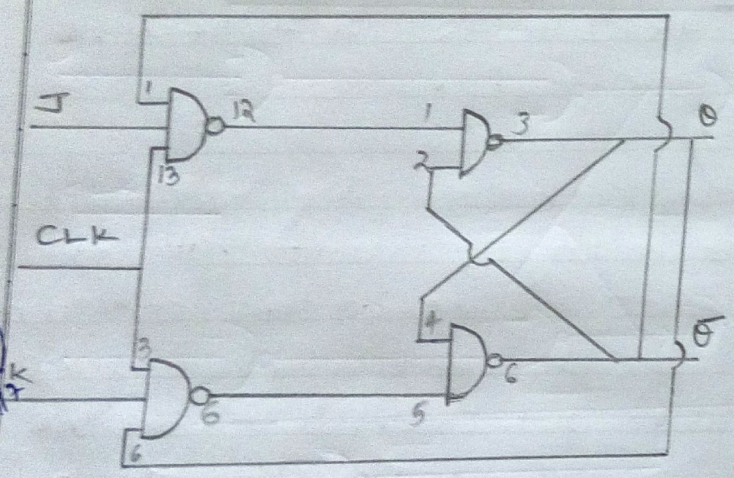
CLOCKED SR FLIP FLOP



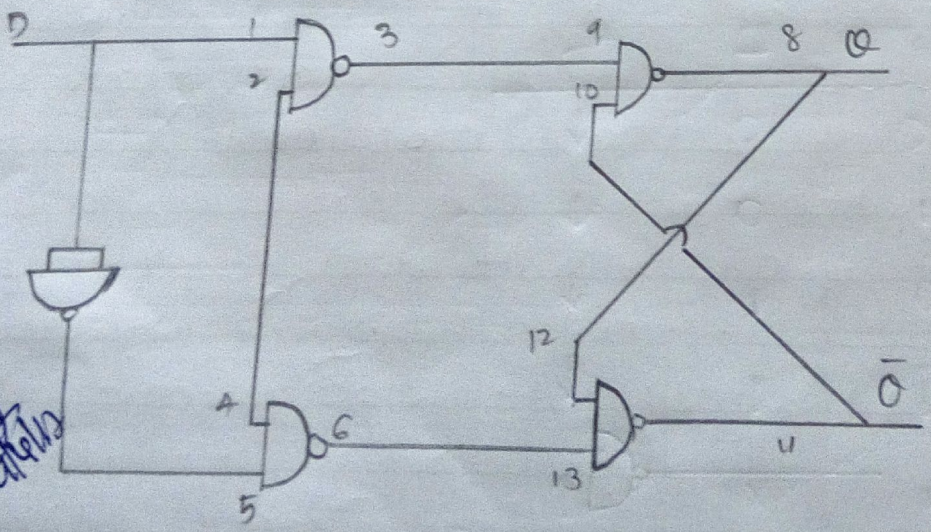
CLK	S	R	Q_n	Q_{n+1}	State
0	X	X	0	0	No Change
0	X	X	1	1	
1	0	0	0	0	No Change
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Forbidden
1	1	1	1	X	

CLOCKED JK FLIP FLOP



CLK	J	K	Q_{n+1}	State
0	X	X	Q_n	No Change
1	0	0	Q_n	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\bar{Q}_n$	Toggle

CLOCKED D FLIP FLOP



CLK	D	Q_n	Q_{n+1}	State
0	X	0	0	No Change
0	X	1	1	
1	0	0	0	Reset
1	0	1	0	
1	1	0	1	Set
1	1	1	1	

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STUDY OF FLIP-FLOPS

AIM

(a) To implement the following flip flops
1 Clocked SR, 2 Clocked D, 3 Clocked JK,
4 Clocked T, 5 master slave JK

(b) To familiarise with the flip flops ICs 7473, 7474.

COMPONENTS REQUIRED

ICs 7400, 7402, 7404, 7410, trainer kit.

THEORY

(1) flip flops are bistable electronic circuits than can be used to store 1 bit of signal information.

SR F/F - If the S and R i/p are low, output returns to the previsious state. If S is low and R is high, o/p returns to the previous state. If S is low and R is high, O/P is low and the flip-flop is said to be in reset condition. If S and R are high, Q and $\bar{Q}$ are forced to be same invalid condition.

D F/F - It is a modified SR flip flop. It has only one i/p. The clocked D flip-flop responds to the positive going edge of clock pulse Q_{n+1} follows D.

JK f/f - Similar to SR flip flop but the invalid condition is overcome. The data i/p J & K are connected to $\bar{Q}$ and Q to obtain S and R i/p respectively. When J=K=1, the O/P changes to the

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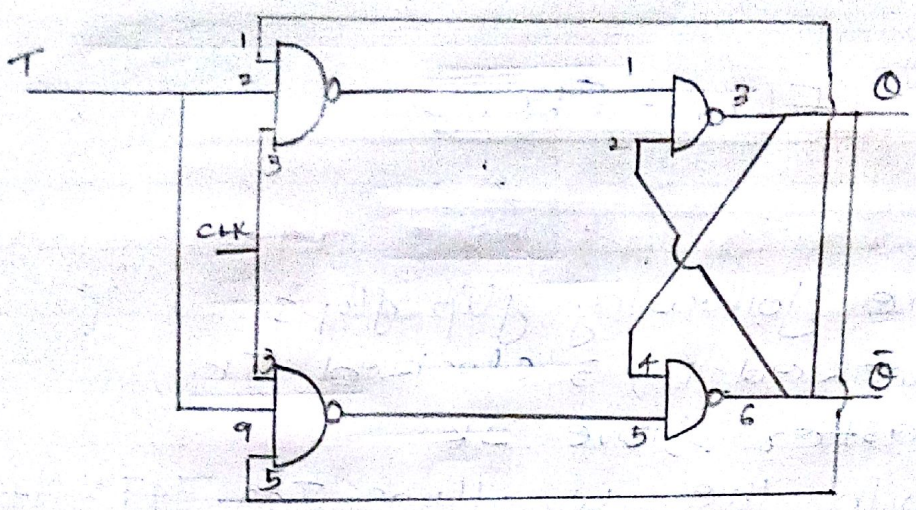
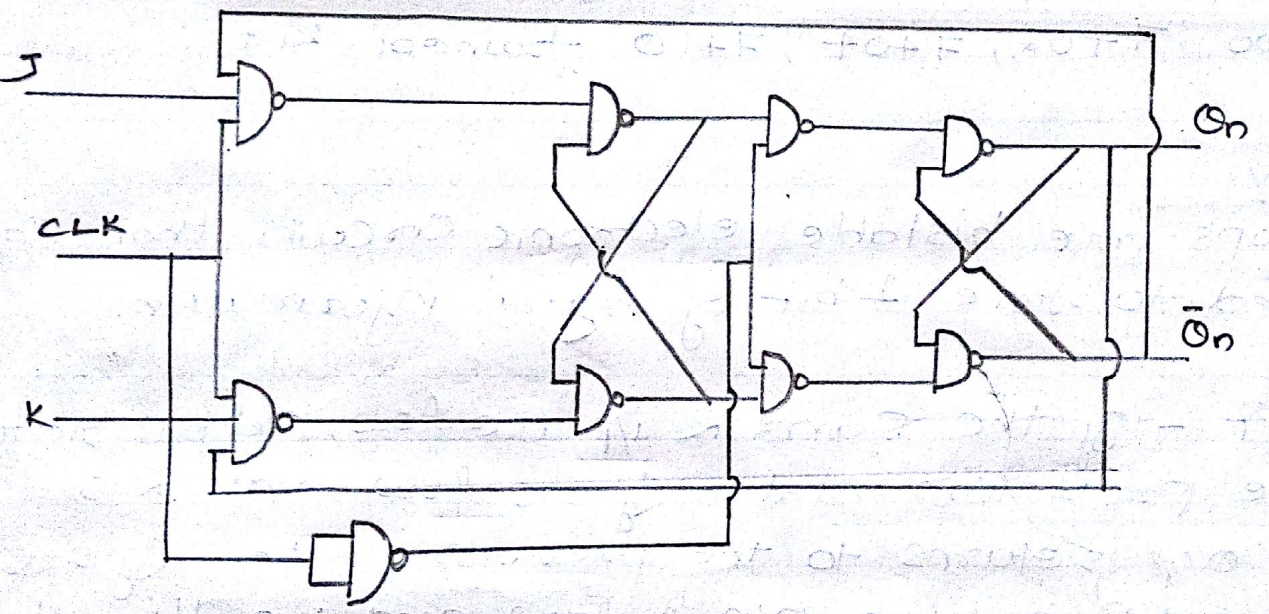
CLOCKED T FLIP FLOP



CLK	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	$\bar{Q}_n$

Master Slave JK FLIPFLOP



CLK	J	K	Q_{n+1}
↓	0	0	Q_n
↓	0	1	0
↓	1	0	1
↓	1	1	$\bar{Q}_n$
↑	X	X	Q_n

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Compliment of the last value.
master slave JK flip flop - It consists of a Clocked JK flip flop as a master and clocked SR f/f as a slave. signal is directly connected to the master slave and inverted through to the slave. Information present at the input is transfered to output of master f/f on the +ve clock pulse and it is held thus until -ve clock pulse occurs.

T f/f - Derived from master-slave JK flip flop by shorting JK inputs. when T=0, clock edge doesn't change the output. when T=1, it compliments the output.

(II) The most common flip flop IC's are 7474, 7476 and 7473. 7476 is a +ve edge triggered dual D flip flop with present and clear.

PROCEDURE

(1) Test the components
(2) set up the flip flop and verify the truth table.

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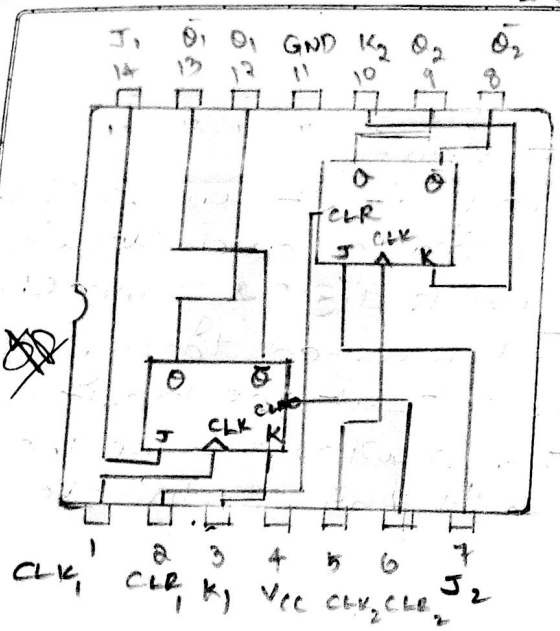
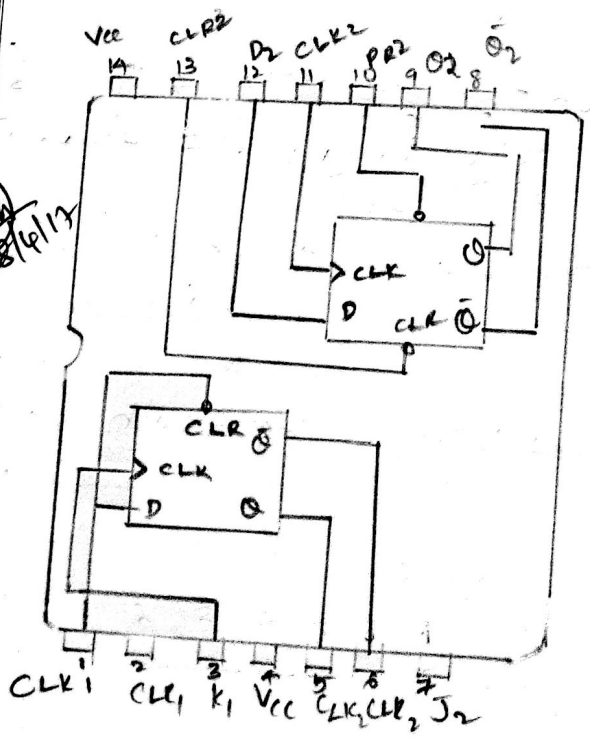
IC 7473



CLR	CLK	J	K	Q	Q̄
L	X	X	X	L	H
H	X	L	H	L	H
H	X	H	L	L	L
H	X	L	L	Previous state toggle	
H	X	H	H		

IC 7474



INPUTS				OUTPUTS	
Pr	Clr	clk	D	Q	Q̄
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	H	H
1	1	↑	↑	1	0
1	1	↑	0	0	1
1	1	0	X	Q_0	$\bar{Q}_0$

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RESULT

Verified and studied all types of flip flops

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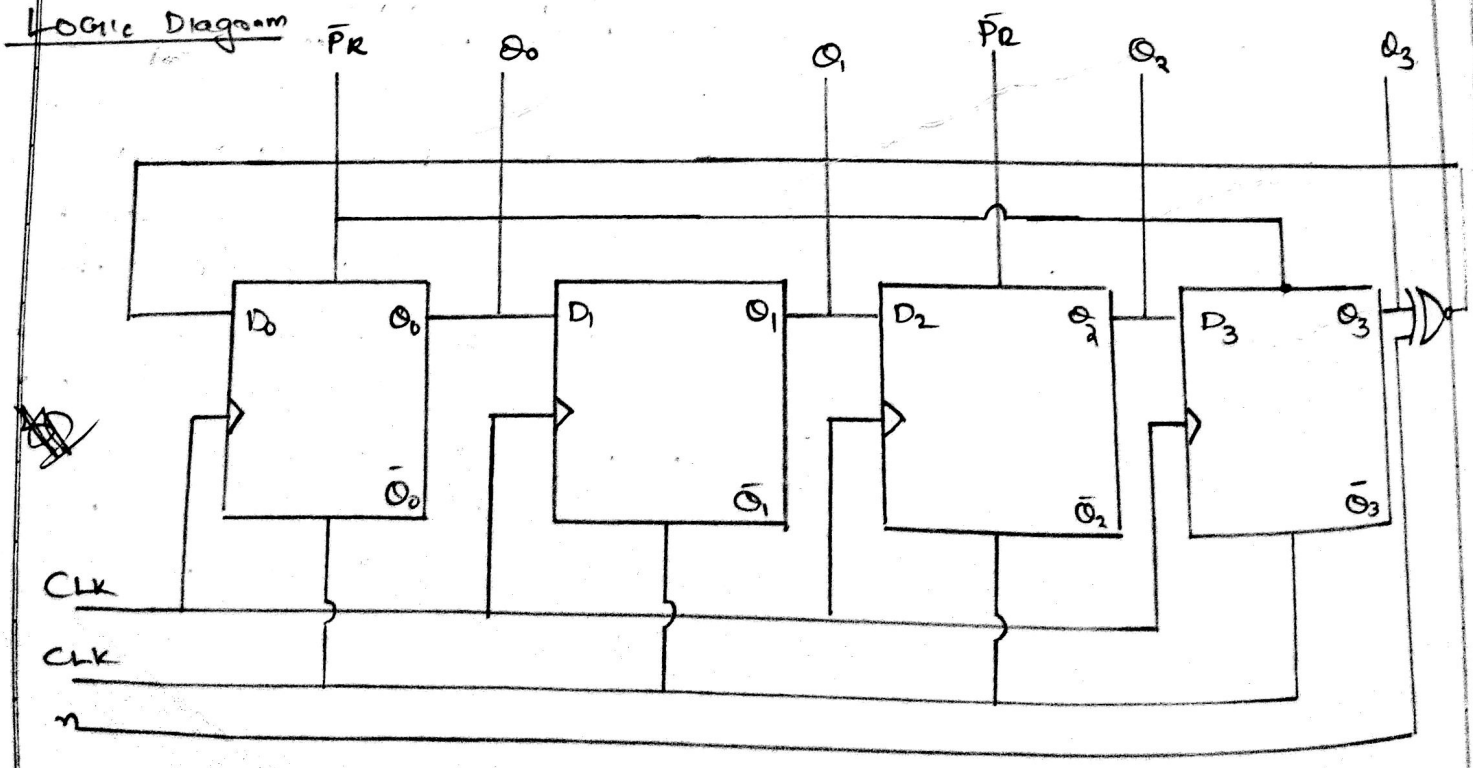
Truth Table

M	Q_3	Q_2	Q_1	Q_0
1	1	0	0	0
1	0	1	0	0
1	0	0	1	0
1	0	0	0	1
1	0	0	0	0
0	1	0	0	0
0	1	1	0	0
0	1	1	1	0
0	1	1	1	1
0	0	1	1	1
0	0	0	1	1
0	0	0	0	1

Logic Diagram



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RING / JOHNSON COUNTER USING FLIP FLOPS

AIM: To design and set up a 4 stage ring / Johnson counter using mode control.

COMPONENTS REQUIRED :- IC 7474 (2), IC 7486 (1), IC 7404 (1), digital trainer kit.

THEORY

Shift counters are basically shift registers in which the serial output is connected to the serial input to produce a special counting sequence. It is of 2 types ring counter and Johnson Counter.

In ring counter, the output of the last flip-flop is set connected to the first D flip flop. Initially all flip-flops are reset using clear pin and the first flip-flop is set using present pin.

In Johnson counter the $\bar{Q}$ of the flipflop is connected to the input of the 1st flip flop. It is also known as twisted ring counter. An N-state Johnson Counter will produce a mod-2N counter, when N is the number of states.

A ring / Johnson counter will work as a ring counter when m=1 and as a Johnson counter when m=0

Procedure :-

(a) Check the IC's

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(b) Set up the circuit on the bread board.
(c) Check the counting sequence and verify the output.

RESULT

Designed and set up a ring / Johson Counter with mode control using D flip-flops.

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PS			mode	NS			Required Excitations					
Q_3	Q_2	Q_1	M	Q_3	Q_2	Q_1	J_3	K_3	J_2	K_2	J_1	K_1
0	0	0	0	1	1	1	1	X	1	X	1	X
0	0	0	1	0	0	1	0	X	0	X	1	X
0	0	1	0	0	0	0	0	X	0	X	X	1
0	0	1	1	0	1	0	0	X	1	X	X	1
0	1	0	0	0	0	1	0	X	X	1	1	X
0	1	0	1	0	1	1	0	X	X	0	1	X
0	1	1	0	0	1	0	0	X	X	0	X	1
0	1	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	1	1	X	1	1	X	1	X
1	0	0	1	1	0	1	X	0	0	X	1	X
1	0	1	0	1	0	0	X	0	0	X	X	1
1	0	1	1	1	1	0	X	0	1	X	X	1
1	1	0	0	1	0	1	X	0	X	1	1	X
1	1	0	1	1	1	1	X	0	X	0	1	X
1	1	1	0	1	1	0	X	0	X	0	X	1
1	1	1	1	0	0	0	X	1	X	1	X	1

1	0	0	0
0	0	1	0
X	X	X	X
X	X	X	X

X	X	X	X
X	X	X	X
0	0	1	0
1	0	0	0

1	0	1	0
X	X	X	X
X	X	X	X
1	0	1	0

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SYNCHRONOUS UP/DOWN COUNTER

AIM

To design and set up a synchronous 3-bit up/down counter.

COMPONENTS REQUIRED

IC 7473 (2), IC 7404 (1), IC 7408 (1), IC 7432 (1)

THEORY

Synchronous counters are counters in which all the flip-flops are triggered simultaneously by the clock-input pulses. They have the advantages of high speed and less severe decoding problems, but the disadvantages of having more circuiting than that of asynchronous counters. Many synchronous counters have IC's that are designed to be presettable, ie they can be preset to any desired starting count either asynchronously or synchronously. Presetting is also called loading the counter.

A 3 bit counter requires 3 flip flops. It has 8 states and all states are valid. For selecting up and down modes a mode signal m is required. When m=1, it counts up and when m=0, it counts down. The corresponding excitation table is written and expressions are derived using K maps.

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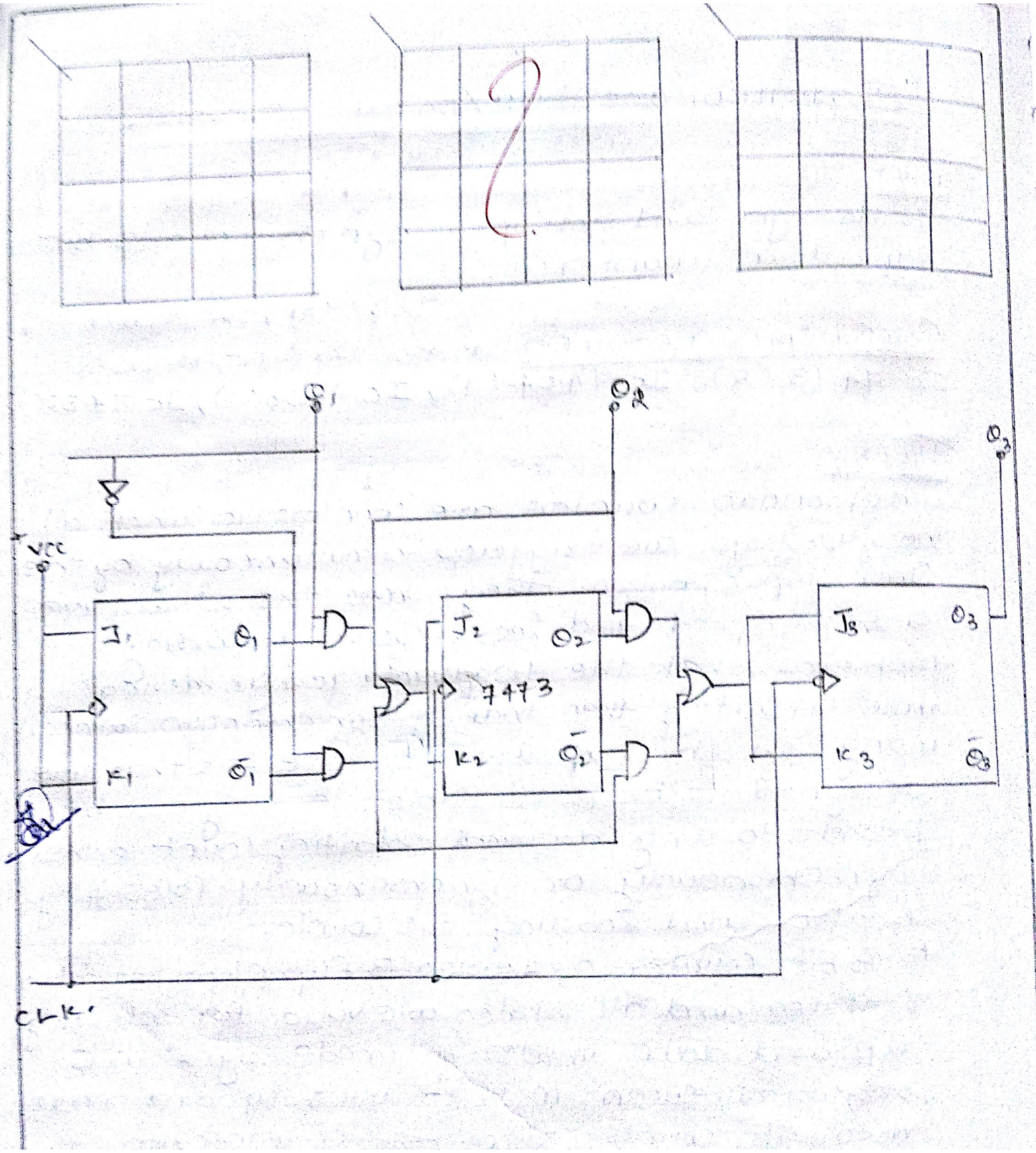

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PROCEDURE

ⓐ Test the components
ⓑ Set up the circuit on the bread board
ⓒ verify the excitation table

RESULT

Designed and set up a synchronous 3-bit up/down counter using JK flip flops.

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PS			NS			REQUIRED EXCITATION					
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	J_3	K_3	J_2	K_2	J_1	K_1
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X

K-MAP

Q_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_3$	0	0	1	0
Q_3	X	X	X	X

$J_3 = Q_2Q_1$

Q_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_3$	X	X	X	X
Q_3	1	X	X	X

Q_3				
$\bar{Q}_3$	0	1	X	X
Q_3	0	X	X	X

Q_3				
	X	X	1	0
	X	X	X	X

Q_3				
	1	X	X	1
	0	X	X	X

Q_3				
	X	1	1	X
	X	X	X	X

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SYNCHRONOUS MOD-5 COUNTER

Aim

To design and set up a synchronous mod-5 counter

COMPONENTS REQUIRED

IC 7473 (2), IC 7408 (1)

THEORY

The number of flip flops required for mod-5 counters is three. This is found from the equation

$$2^m \geq n \geq 2^{m-1}$$

where $n = 5$

Let us assume that mod 5 counter has 5 states. The number of states or counting sequences through which a particular counter advances before returning once again back to its original first state is called the modulus (MOD)

Modulus counters are defined based on the number of states that the counter will sequence through before returning back to the original value.

In general a mod-N counter will require N number of flip flops connected together to count a single data bit while providing 2^n different output states. N is always a whole integer value.

PROCEDURE

① Test the components

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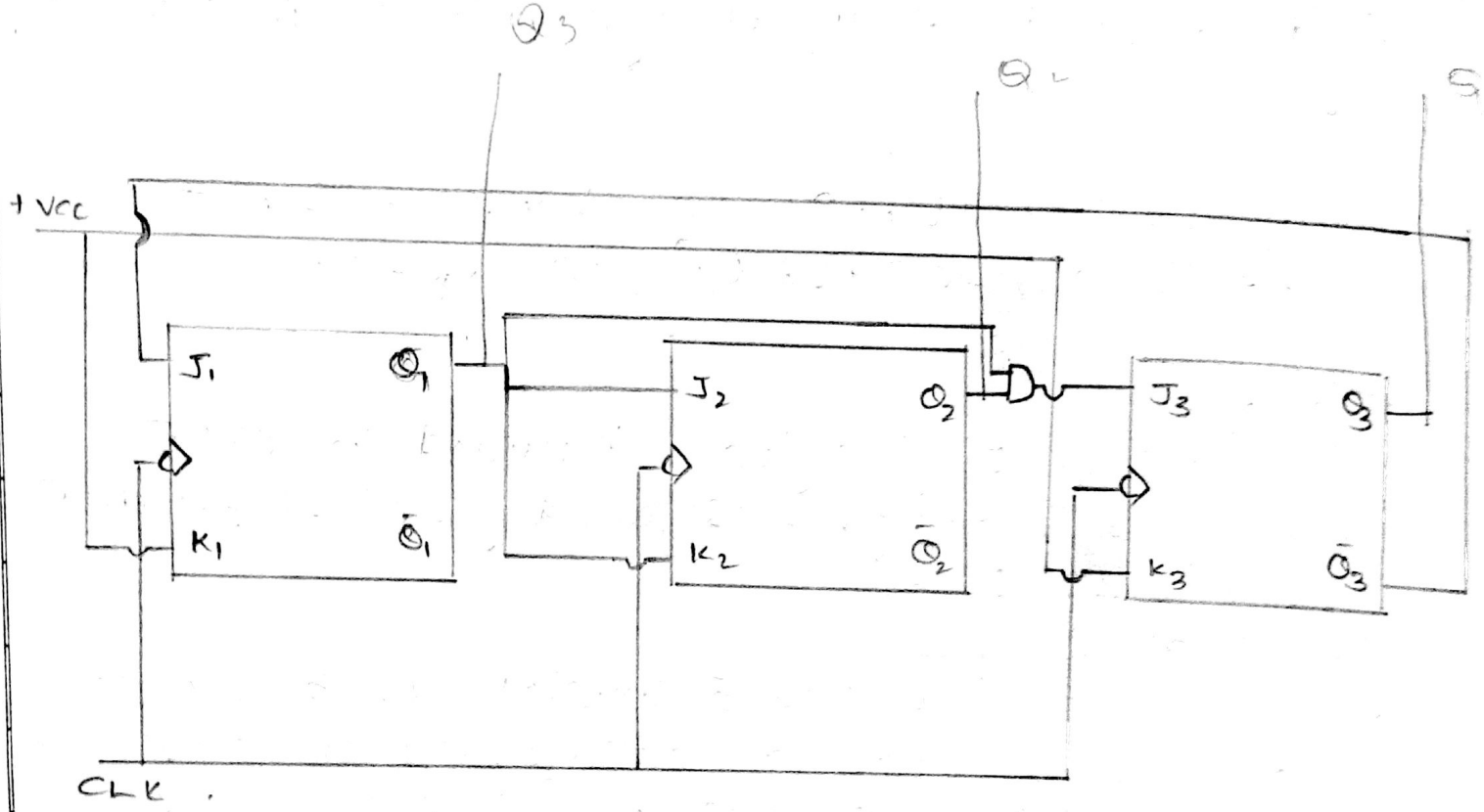

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(b) Set up the circuit on the bread board.
(c) Verify the excitation table.

RESULT

Designed and set up a mod-5 synchronous counter using JK flip flop.

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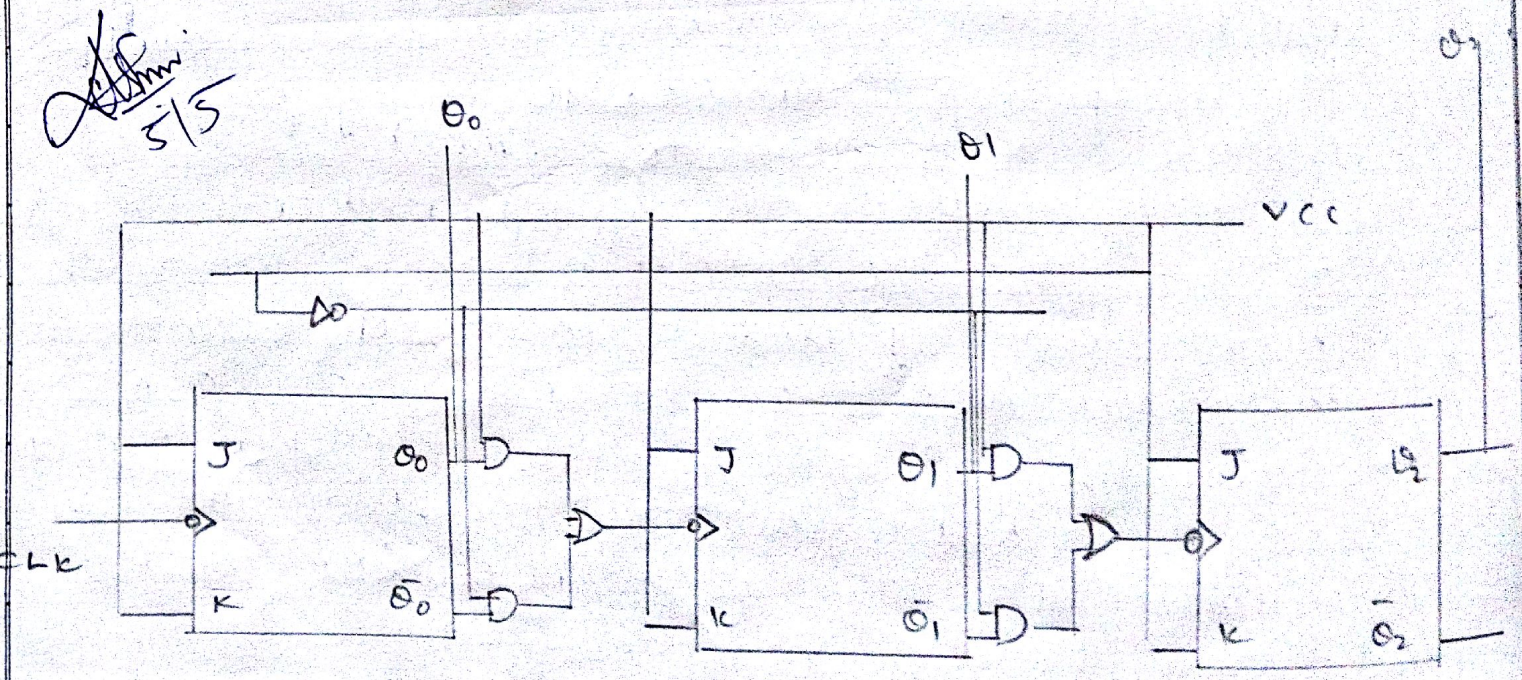
M	Q	$\bar{Q}$	Y
0	0	0	Ø
0	0	1	1
0	1	0	0
0	1	1	Ø
1	0	0	Ø
1	0	1	0
1	1	0	1
1	1	1	Ø

$y = \bar{m}\bar{Q} + mQ$

M \ Q	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{m}$	Ø	1	1	0
m	Ø	0	1	1

5/5



ASYNCHRONOUS UP/DOWN COUNTER

AIM

To design and set up a 3 bit asynchronous up-down counter using JK flip flop and mode control

COMPONENTS REQUIRED

Digital IC, trainer kit, IC 7408, 7404, 7432, 7473

THEORY

An asynchronous up counter is formed by connecting the outputs of one flip flop to the clock of the next flip flop. and an asynchronous down counter by connecting the $\bar{Q}$ output to the next flip flop clock. By adding the ideas of up counter and down counter, we can design an asynchronous up/down counter using a mode control line m.

The counter counts up for m=1 and counts down for m=0. When m=1 the NAND gates will pass the normal output of Q_A to clock of second flip flop and the output Q_B to clock of third flip flop. Now the counter counts upward. When m=0, the NAND gates will pass the inverted output $\bar{Q}_A$ to clock of second flip flop and $\bar{Q}_B$ to clock of third flip flop. Now the counter counts downward.

The up/down counter is slower than

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M = 0

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

M = 1

Q_2	Q_1	Q_0
0	0	0
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0

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up counter or a down counter due to additional propagation delay of NAND gates.

PROCEDURE

(a) Test the components
(b) Set up the circuit in a bread board as per the given circuit
(c) verify the output.

RESULT

A - 3 bit up/down asynchronous counter was designed and set up using IC 7473 JK flip flops.

Teacher's Sign

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Q_3	Q_2	Q_1	Reset
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
↓	↓	↓	
0	0	0	0
0	0	1	0

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ASYNCHRONOUS MOD-6 COUNTER

AIM

To design and verify an asynchronous mod 6 counter.

COMPONENTS REQUIRED

A digital trainer kit, IC 7573, IC 7410, bread board.

THEORY

A mod 6 asynchronous counter has 6 stable states; 000, 001, 010, 011, 100 and 101. When the 6th clock pulse is applied the counter temporarily goes to 110 state, but immediately resets to 000 because of the feedback.

It is a divide by 6 counter in the sense that it divides the input clock frequency by 6. It requires 3 flip flops. 3 flip flops can have 8 possible states out of which only 6 are used.

When the clock pulses are provided

$R = 0$ for 000 to 101

$R = 1$ for 110

$R = \phi$ for 111

$\therefore R = Q_3 Q_2$

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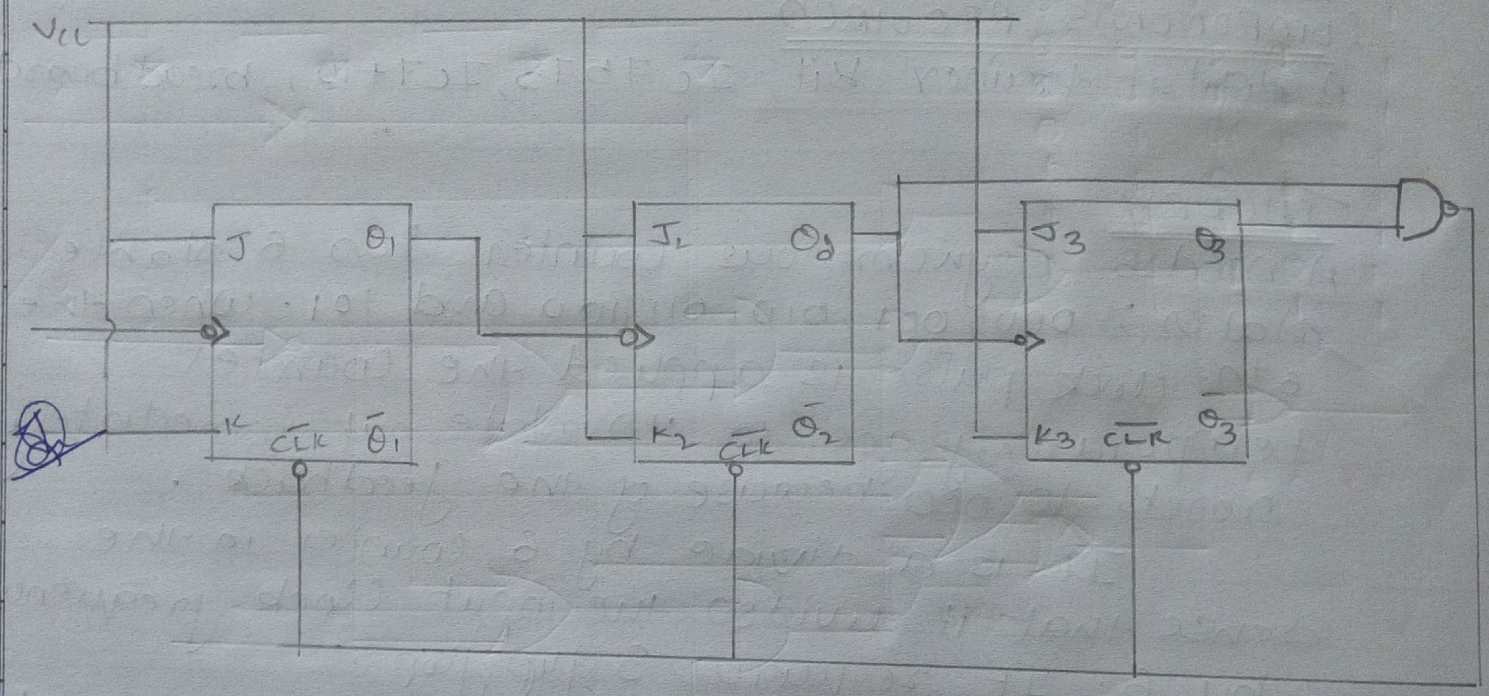
Q_3 \ Q_2Q_1	00	01	11	10
0	0	0	0	0
1	0	0	ϕ	1

$R = Q_3 Q_2$



R = 0 for 000 to 101

R = 1 for 110

R = ϕ for 111

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PROCEDURE

(a) Test the IC's
(b) Implement the circuit on bread board.
(c) Verify the output.

RESULT

Implemented and verified asynchronous mod 6 counter.

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1) $y = \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD + \bar{A}B\bar{C}D + \bar{A}BCD + AB\bar{C}\bar{D} + AB\bar{C}D + A$

AB \ CD				
	1	1	1	0
	1	1	1	0
	1	1	1	0
	0	0	0	0

SOP form

$Y = \bar{A}\bar{C} + \bar{A}D + \bar{C}B + DB$

POS form

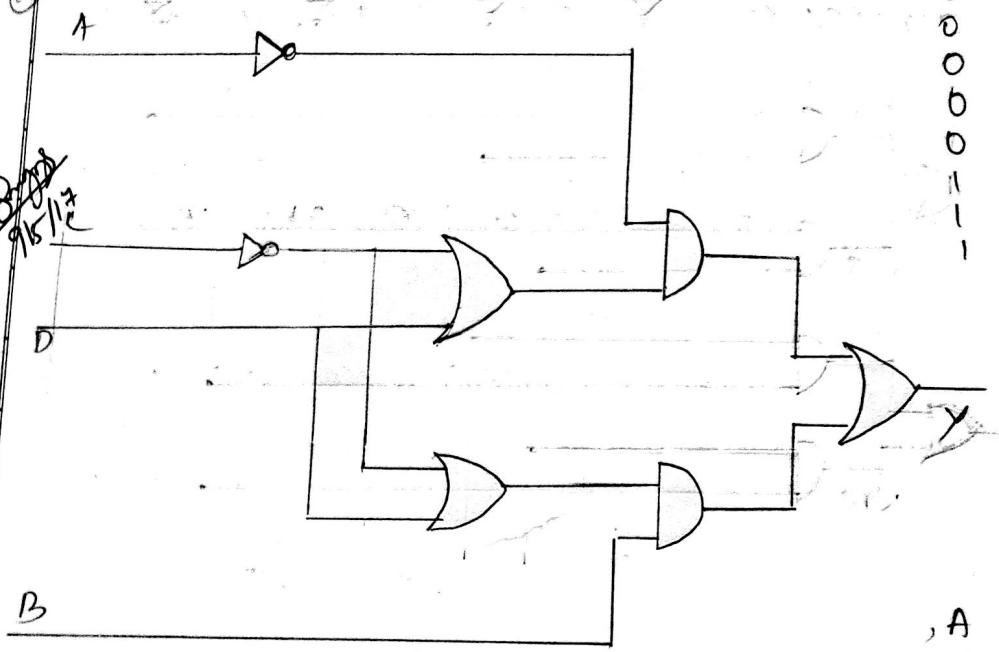
$\bar{Y} = D\bar{B} + C\bar{D}$

$Y = (\bar{A}+B)(C+D)$

1) $Y = \bar{A}\bar{C} + \bar{A}D + \bar{C}B + DB$

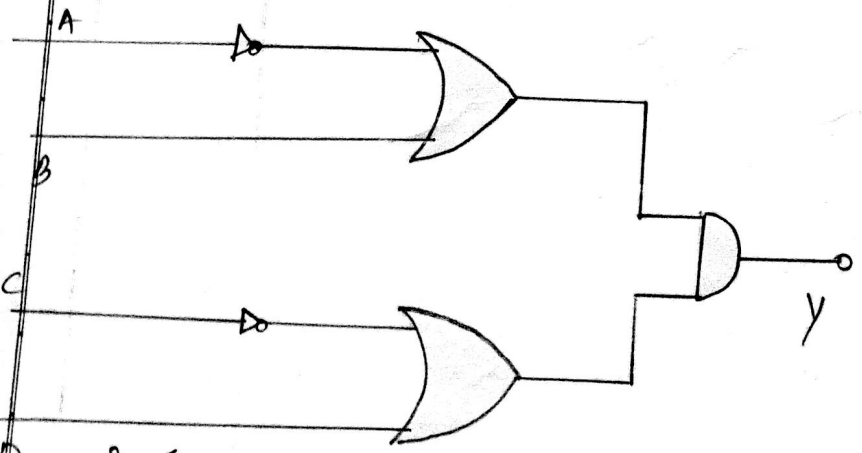
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0

1



2) Pos. $(\bar{A}+B)(\bar{C}+D)$

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



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REALISATION OF FUNCTION USIND SOP AND POS

AIM

(a) To realise the given function using logic gates and universal gates (in SOP and POS form).

(b) To implement the following functions and to compare them. $y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + AB\bar{C}\bar{D} + AB\bar{C}D + ABCD$ (ii) $Q = (A+B+C+\bar{D})(A+B+\bar{C}+D)(\bar{A}+B+C+D)(\bar{A}+\bar{B}+\bar{C}+D)(\bar{A}+B+\bar{C}+D)$

COMPONENTS REQUIRED

ICs of logic gates like 7408, 7432, 7400

THEORY

Any boolean expression can be expressed in a standard or canonical or expanded sum of products ic SOP form, or in standard or canonical or expanded product of sum ie POS form. A standard SOP form is one in which a number of product terms, each one of which contains all the variables of the function either in complemented or non complemented form are summed together. A standard POS form is one in which a number of sum terms, each one of which contains all the variables of function. Each of the product term in SOP form is called a minterm and each of sum terms is called maxterm. In a min term a variable takes the value '0' if it is

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is in complimented form and 1 in the normal form.
A standard SOP form can always be converted to a standard POS form by treating the missing minterms of the SOP form as the maxterm of POS form and vice-versa. Both SOP and POS can be simplified using K-map and can easily be implemented using logic gates.

PROCEDURE

(a) Simplify the given equation of the function to implement using K map.
(b) using digital IC trainer kit reproduce the circuit on the bread board.
(c) Connect vcc and GND to the circuit
(d) provide the different input and verify the function.

RESULT

Verified the various SOP and POS diagram.

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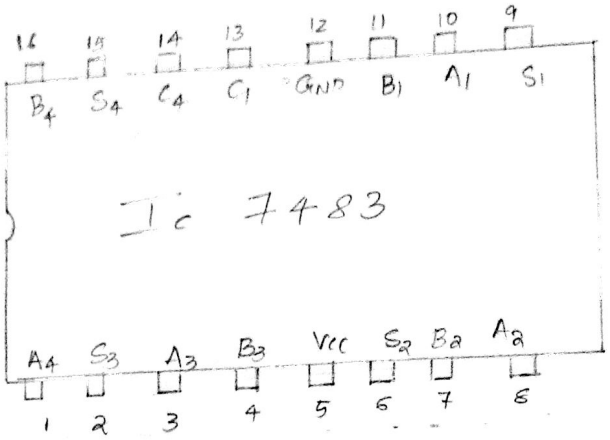
Pin diagram



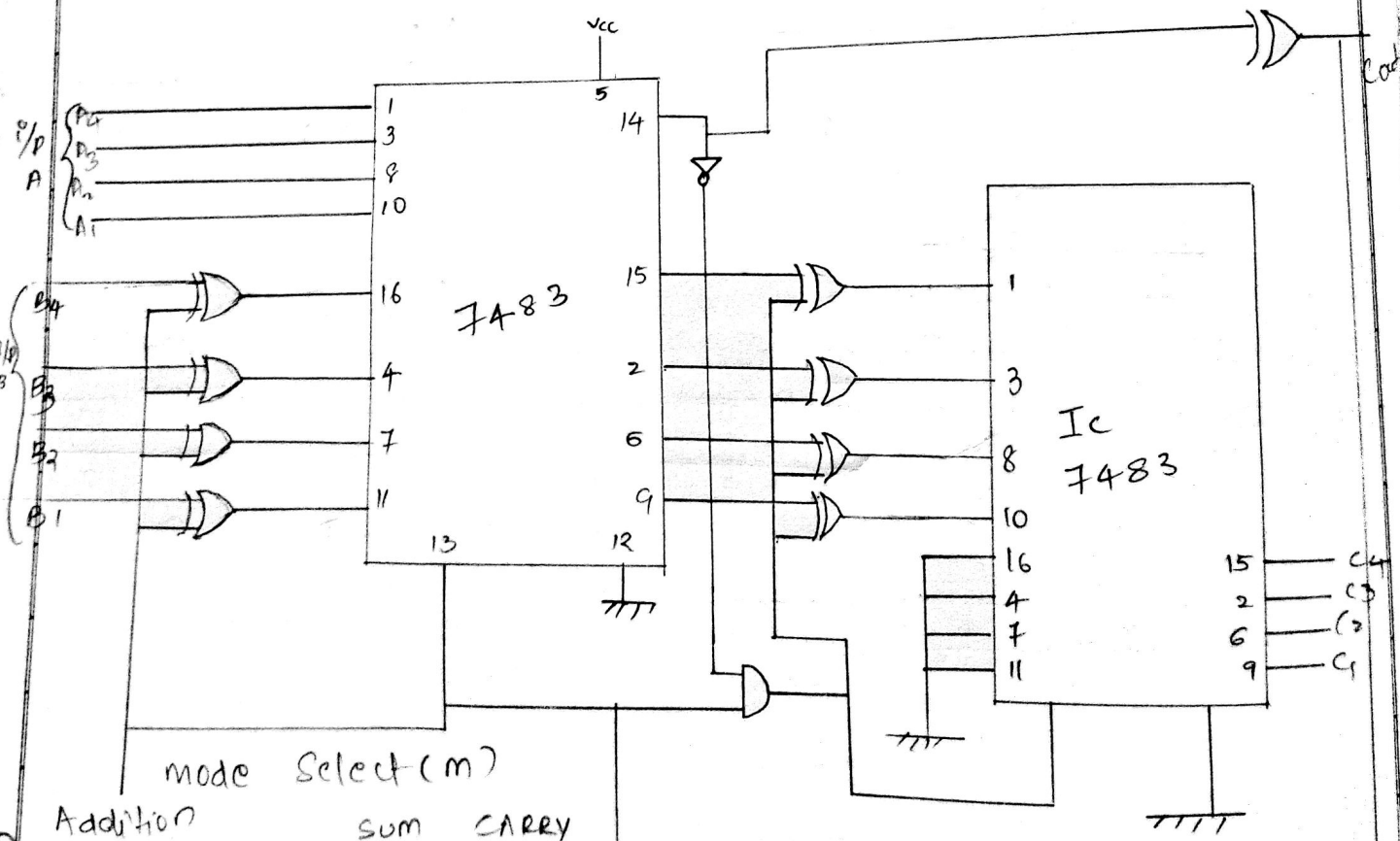
1, 3, 8, 10
16, 4, 7, 11 } i/p

M = 0 / 1

M = 0 addition

M = 1 Substraction

b) Adder / Subtractor



mode Select (m)

	Addition	sum	CARRY
a	0101 + 0101 =	1010	0
b	1010 + 0111 =	0001	1

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4- BIT ADDER / SUBTRACTOR BCD ADDER USING IC 7483

AIM

To design and set up a 4 bit adder / subtractor and BCD adder using IC 7483.

COMPONENTS REQUIRED

IC 7483, IC 7432, IC 7408, IC 7486

THEORY

A binary adder is a digital circuit that produces the arithematic sum of two 4 bit binary numbers. It can be constructed with full adder connected to the input carry from each full adder connected to the input carry of the next full adder in chain. The augend bit of A and the addend bits of B are designated by subscript numbers from right to left with subscript 0 denoting the least significant bits. The carries are connected in chain through the full adder. The input carry to the adder is C_0 and its ripples through the full adder to the output carry C_4.

Using a mod control line, it can act as both adder and subtractor. When m=0, the circuit works as an adder and when m=1, it acts as a subtractor. BCD adder follows BCD addition rule and thus requires an extra 6 for sum correction. This is

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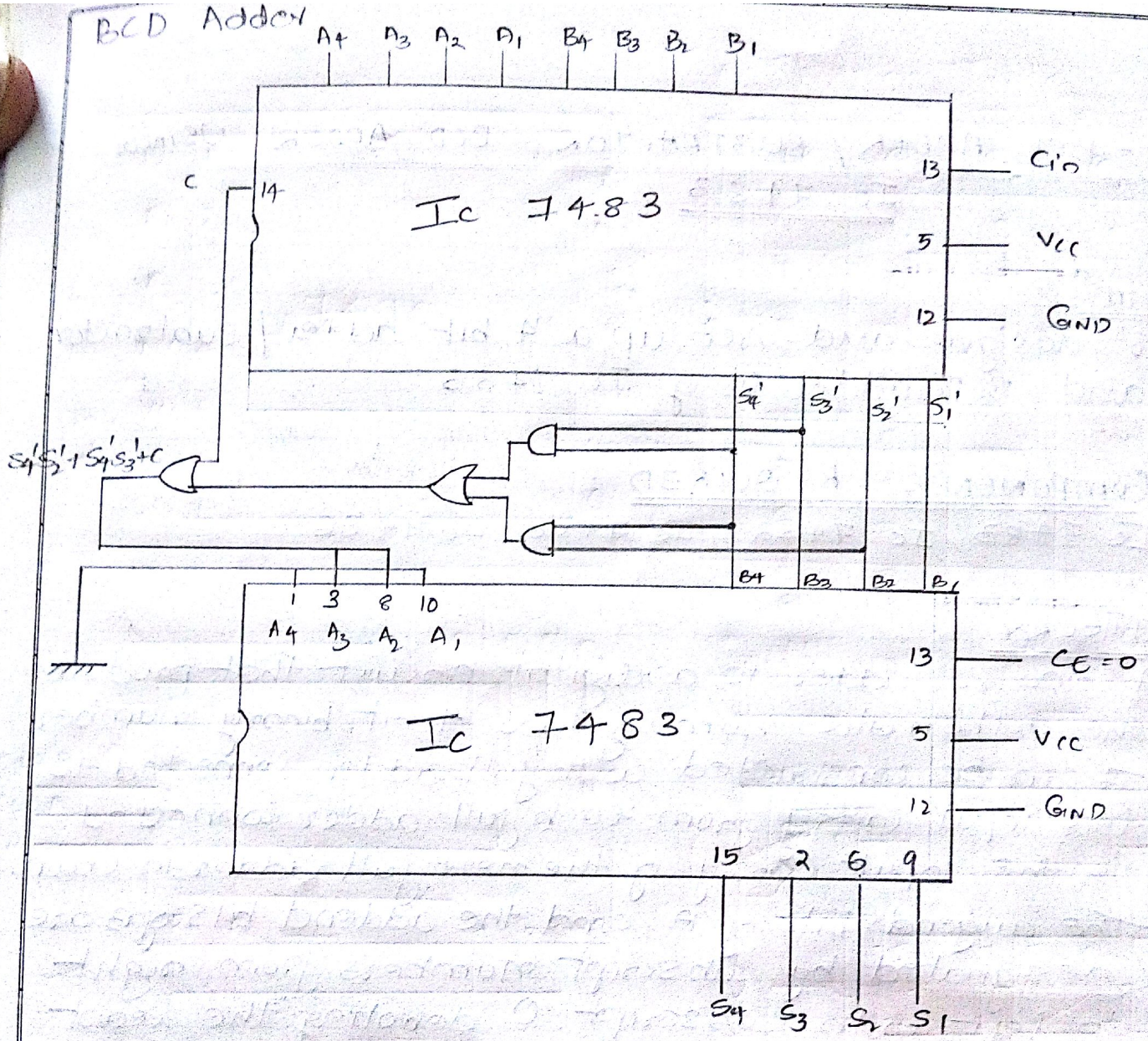
BCD Adder



4 bit adder

M	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_0	S_3	S_2	S_1	S_0
0	1	1	0	0	0	0	1	1	0	1	1	1	1
0	0	0	1	1	1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	1	0	1	0	1	0	1
1	1	0	0	1	1	0	1	0	1	0	0	0	1
1	1	1	1	0	1	1	1	1	1	0	0	0	1
0	1	0	1	0	1	0	1	1	1	0	1	0	1

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achieved using two 7483 IC's.

PROCEDURE

(a) place the IC's on the bread board of the digital trainer kit.
(b) make the suitable connections.
(c) Provide various inputs to the circuit and verify the output.

RESULT

Design and set up a 4 bit adder/Subtractor and BCD adder using IC 7483 was completed and output was verified.

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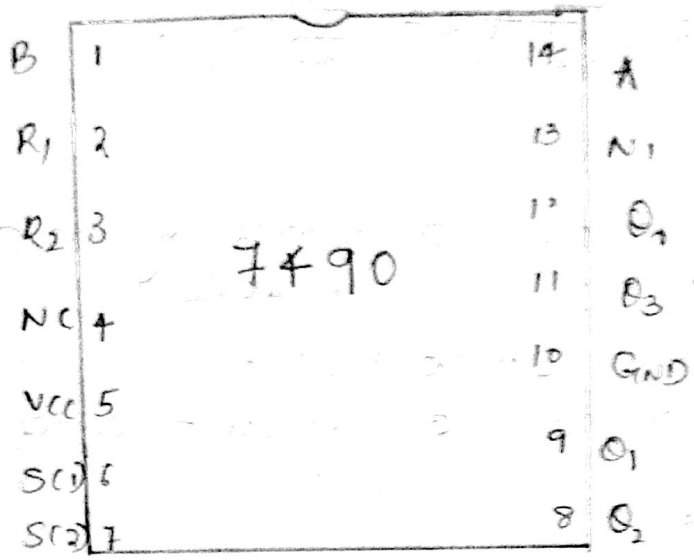
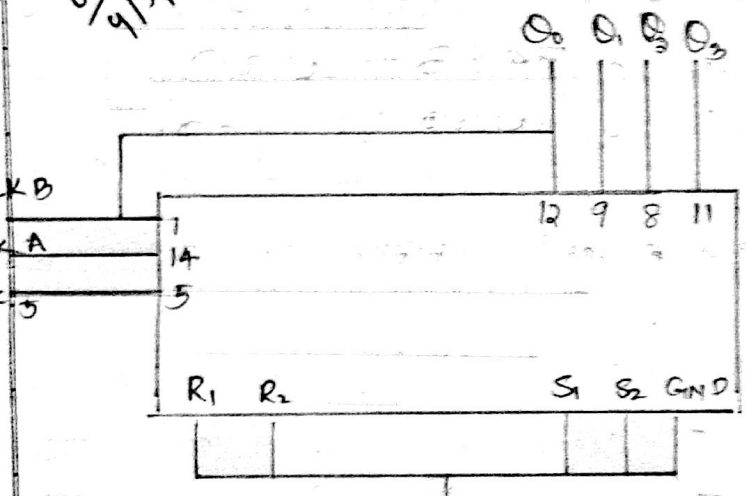
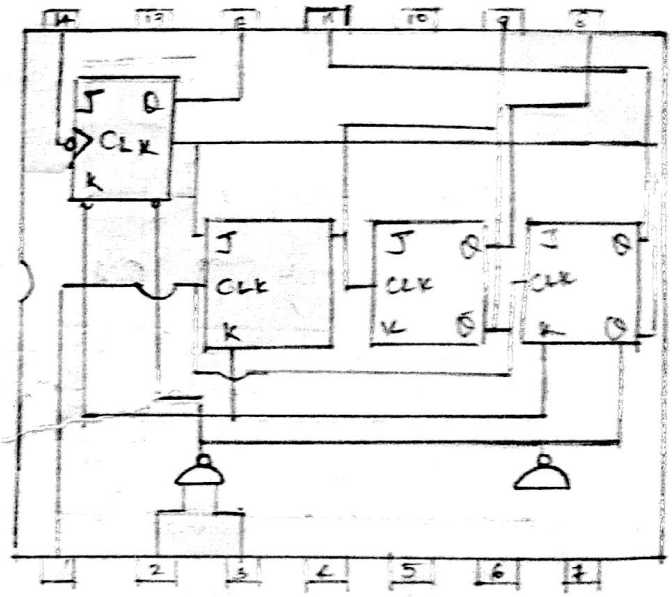
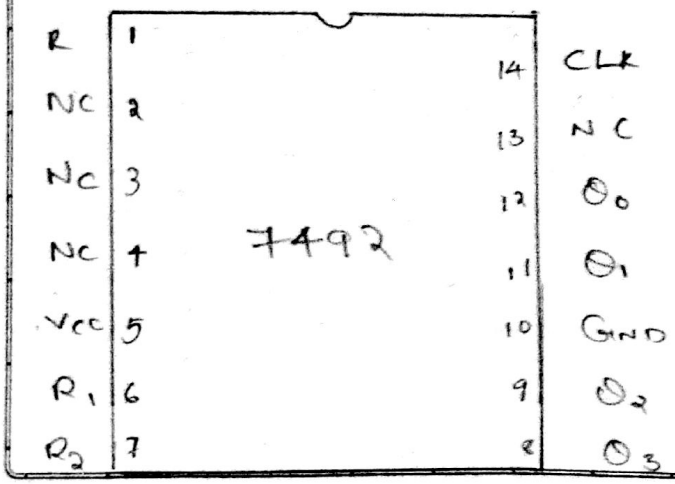
Truth Table

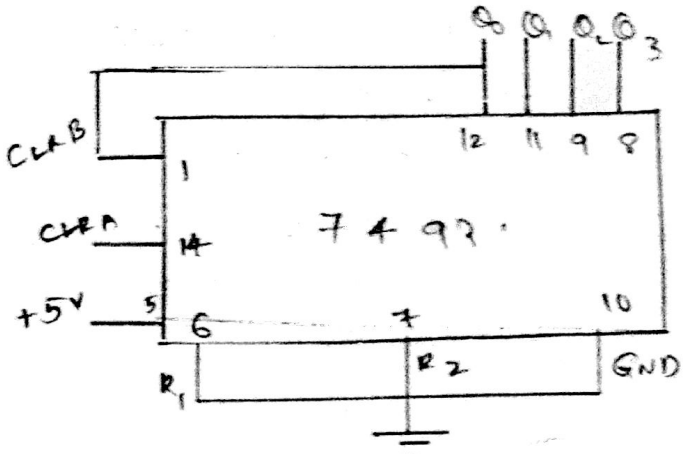
CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1











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COUNTER ICs

AIM

(a) To familiarise and study counter IC's 7490, 7492, 7493

(b) To realise a decade counter using IC 7490.

COMPONENTS REQUIRED

IC 7490, 7492, 7493, DIC trainer kit.

THEORY

(a) IC 7490

The synchronous decade counter has a MOD 2 counter and MOD 5 counter. If clock is applied at input B, MOD 5 counter output will appear at input $Q_3Q_2Q_1$. If clock is fed at A and Q_2 connected to B, $Q_3Q_2Q_1Q_0$ will provide BCD counter output.

(b) IC 7492

It is an asynchronous divide by 12 counter. If clock is applied at B, it will work as MOD 6 counter and MOD 12 when input applied at A and Q_0 connected to B.

(c) IC 7493

The 14 pin DIP, MSI chips is an asynchronous 4 bit binary counter which consists of 4 master slave JK flip flops. It consists of a MOD-2 counter followed by a MOD-6 counter.

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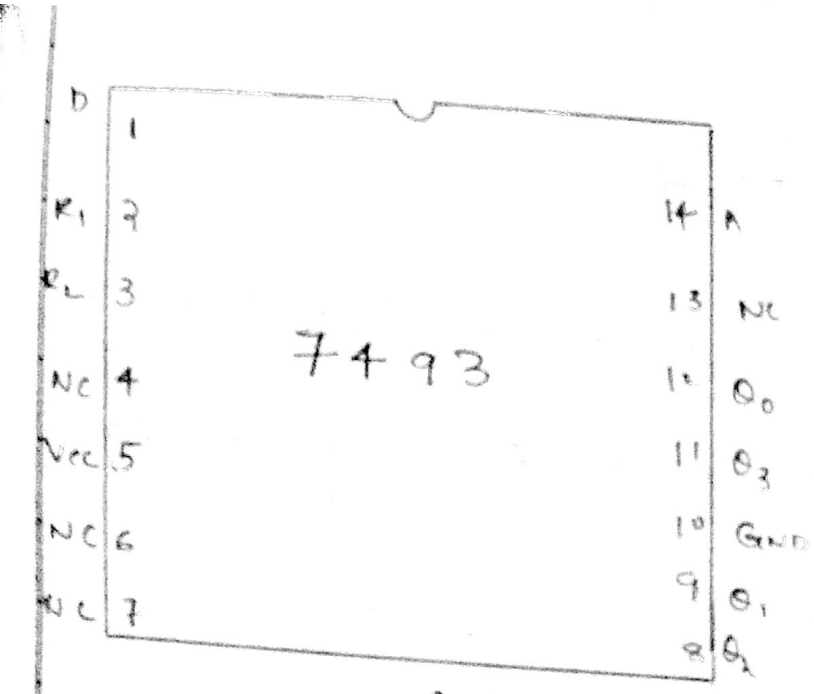

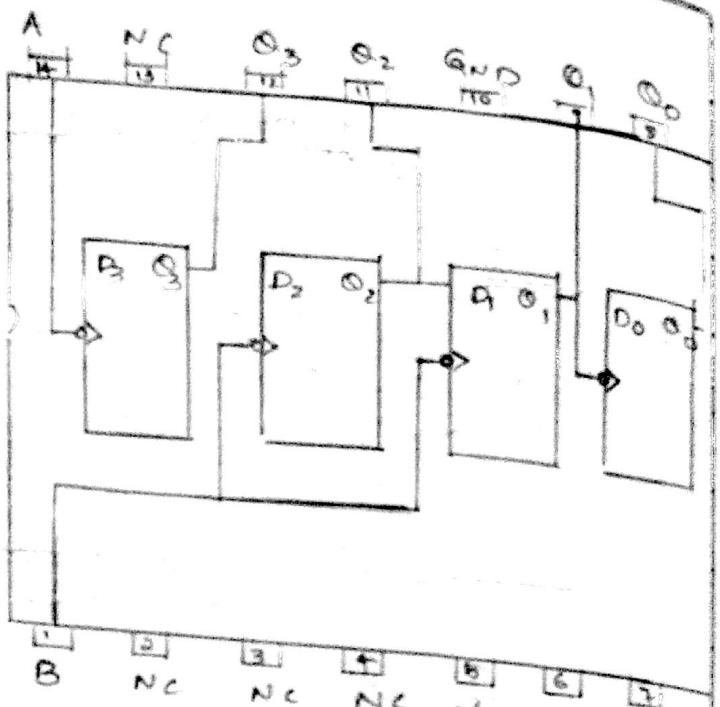

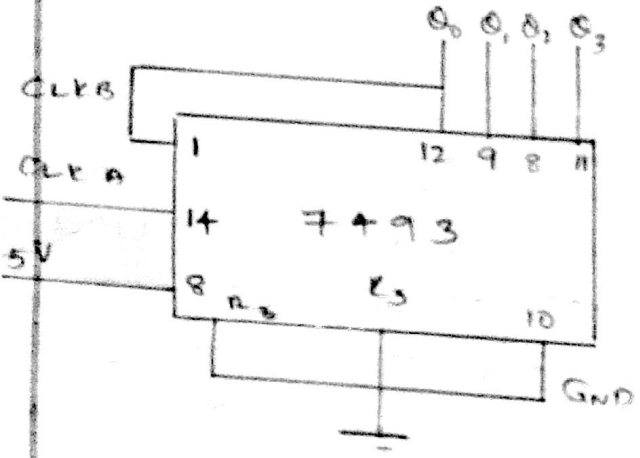

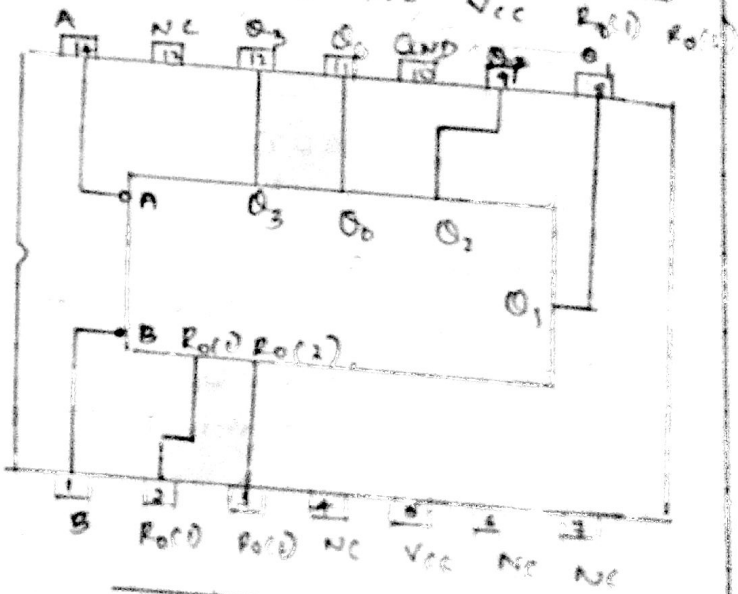

IC 7492 TRUTH TABLE

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

IC 7493 Truth Table

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A decade counter counts from 0000 to 1001. It is also called a MOD-10 counter divide by 10 counter or BCD counter. It is designed to generate a clear signal on receipt of 10th clock pulse (1010) and setting becomes 0000

PROCEDURE

(a) verify working of MOD-2, MOD-8, and MOD-16 counters of IC 7493.

(b) Verify working of MOD-2, MOD-5 and MOD-10 counter of IC 7490.

(c) Verify working of MOD-2, MOD-5 and MOD-12 counter of IC 7492.

RESULT

Familiarised with IC's 7490, 7492, 7493. Realised decade counter using IC 7490.

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