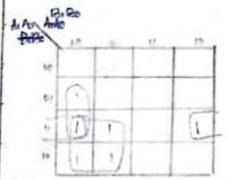
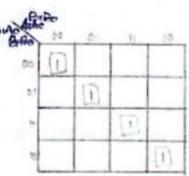
Imput.				Output		
Aı	Ao	В	Be	A>B	A = B	ALB
o	0	0	0	0	1	0
0	0	0	t	0	0	- 1
0	0	1	0	0	0	1
0	0	1	1	0	0	ı
0	1	0	0	1	0	0
0	ı	0	1	0	1.	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
t	0	0	1	1	0	0
ţ	0	1	0	0	ı	0
1	0	1	1	0	0	1
I	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	ı	1	0		0



61 = Ā,B, + Ā,Ā,Bo + Ā, BoB, = A,B, + Ā, B, (Ā,+B,) = A,B, + Ā,B, (A,B, + Ā,B, + B,Ā, + B,A,)

Gt = Ai Bi + Ao Bo (Ai @ Bi)



E = A, A B, B + A, A B, B L = A, E + A B, B +

+ A, A B, B + A, A B, B A

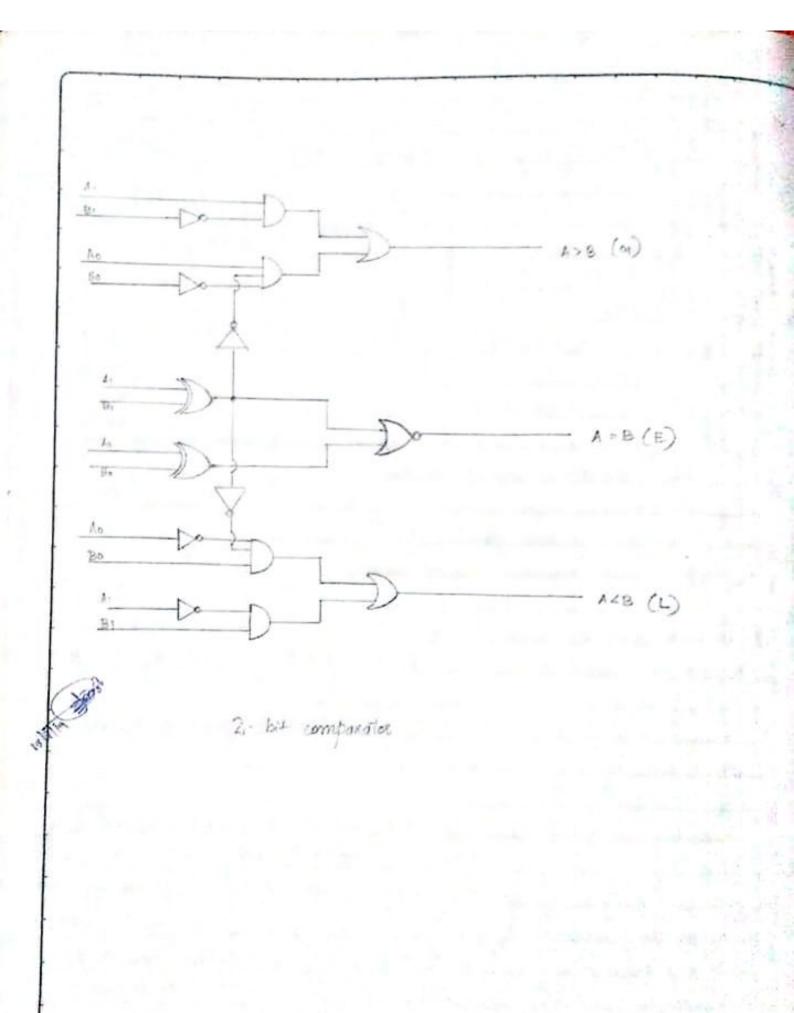
A, A B

A, B

E = (410B) (400B)

L= (A | A) + A B (A OR)

2 BIT BINARY COMPARATO	D.S. 13 1 2 1 19
	RS
And	110
MICH.	
To verify the druth table of two bit comparator in	suig legic gates.
COMPONENTS REGUIRED	
IC 7436, IC 7404, IC 7408 etc	
THEORY	
Digital buiary comparators are made up of AND	, NOR and NOT gates
that compare the digital signals at their input	terminals and suduces
an output depending upon the condition of the in	buts. It produces an
support depr one of three possible outputs based	on if the super is
less than greater than or equal - to each other	
A comparator compares a variable or unknown me known value and produces an amput dependence	uding upon the sesult.
the bicasy number A and D will be equal if a digits of both the numbers are equal.	all the pasts of significant
relative magnitude of pairs of 2 building mu	stasting som the me
selutive magnitude of pours of significant digits,	ver significant bits
significant bit gradually producing downsde low until an inequality is jound when it is jour bit of A is I and B is 0, we conclude A>B: It we conclude B>A.	nd . if the corresponding
bit of A is I and B is O, we conclude A>B. It	is the por opposite to
Te	ocher's Signature.



eriment Name / No.:		Camlin Page No.
		Date 1 1
PROCEDURE		
Very the gates		
2. Make the connections	as per excuit diagr	aur
3. Switch on Vec		1 2 3 3
4. Applying input check	k yes the autput	1 2 1 2
5. Tabulate the output	seadings	1 1 D V
	- J	
D-117		
RESULT		
Verified the hulb lable	of a bit comparates .	using logic gates.
*	Y 1 0 0 0	0 0
and the second	1 1 1	9 P E
		F 7 7 7
		13