Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS202

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each carries 3 marks.

1		Write the three-address, two-address and one-address representations of the operation below with relevant assumptions: $C \leftarrow [A] + [B]$	3
2		What is the use of linkage register in subroutine invocation?	3
3		Why is non-restoring division faster than restoring division?	3
4		Design and draw a 3X2 array multiplier.	3

PART B

Answer any two questions. Each carries 9 marks.

5		Illustrate various addressing modes with proper examples. Which is the default addressing mode selected by assemblers and compilers and why?	9
6		Give the flow chart for Booth's Algorithm. Illustrate using an example.	9
7	(a)	Assuming that stack grows towards lower address range write assembly code for the following (Without using PUSH and POP) : (i) Pushing elements stored at ITEM1, ITEM2 onto stack (ii) Popping an element onto address ITEM (iii) Copying value of top of stack to address TOP	4.5
7	(b)	Compare and contrast single bus and multiple bus organisation of CPU.	4.5

PART C

Answer all questions. Each carries 3 marks.

8		Compare the two main modes of DMA transfer.	3
9		Explain any two interrupt priority schemes.	3
10		What is MFC signal? How is it related to Memory Access Time?	3
11		Which design feature of SRAM cells helps in value retention without refresh?	3

PART D

Answer any two questions. Each carries 9 marks.

12 Illustrate with an example SCSI bus arbitration and selection. 9

13 With the help of a diagram examine the internal organisation of bit cells in a memory chip. 9

14 (a) Explain the architecture of USB with help of a diagram. 4.5

14 (b) Differentiate Direct and Associative mapped cache with examples. 4.5

PART E

Answer any four questions. Each carries 10 marks.

15 Give a simple design for generating status bits for a 8-bit ALU. 10

16 Draw a labelled block diagram of a processor unit with seven registers R1 to R7,a status register,ALU with 3-selection variables and C_{in}, and shifter with 3 selection variables. 10

17 With the help of a flowchart for sign-magnitude addition/subtraction, explain the steps involved in developing a hardwired control unit. 10

18 Using a block diagram analyse the design of a microprogram control for a processor unit.

19 What is a control word? With the help of proper illustrations and assumptions show how a designer would compose a control word for the processor unit. 10

20 With the help of a diagram establish the functioning of microprogram sequencer in a microprogram controlled processor. 10

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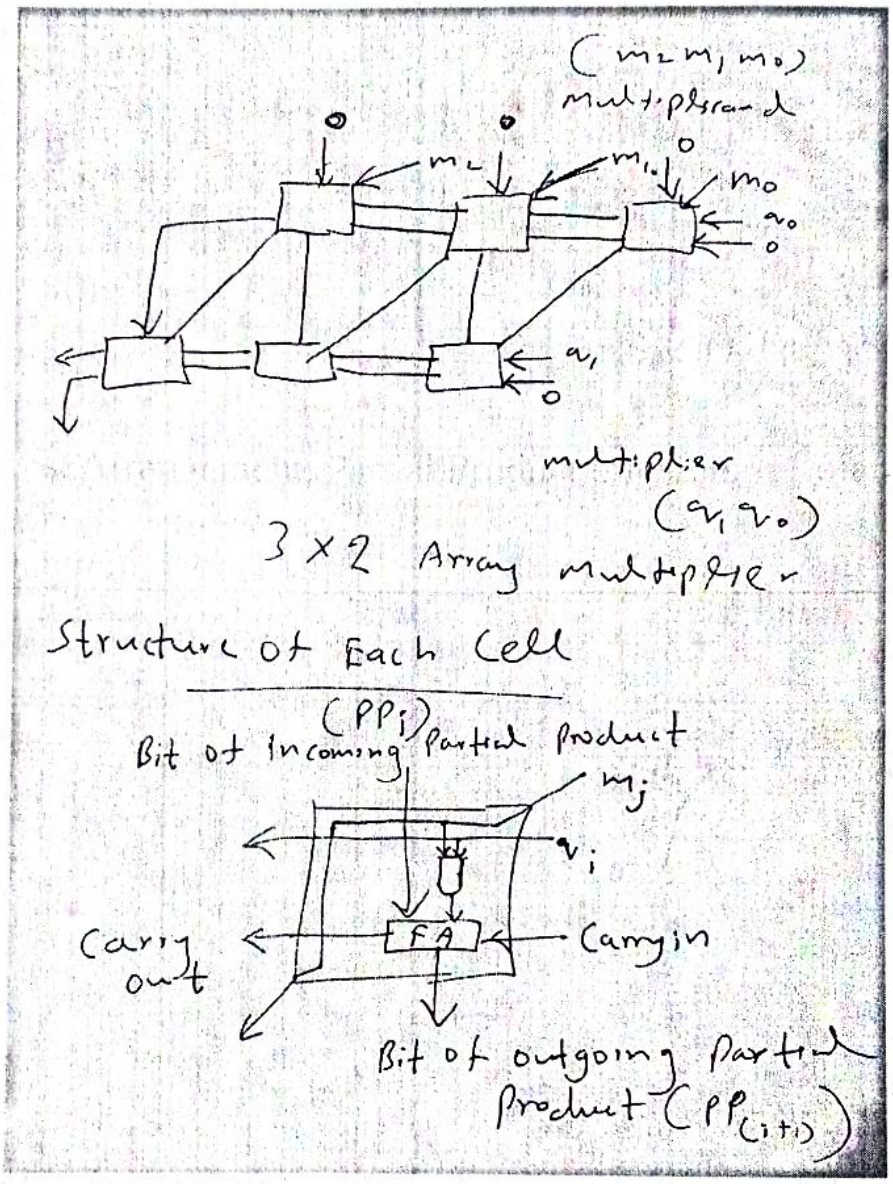
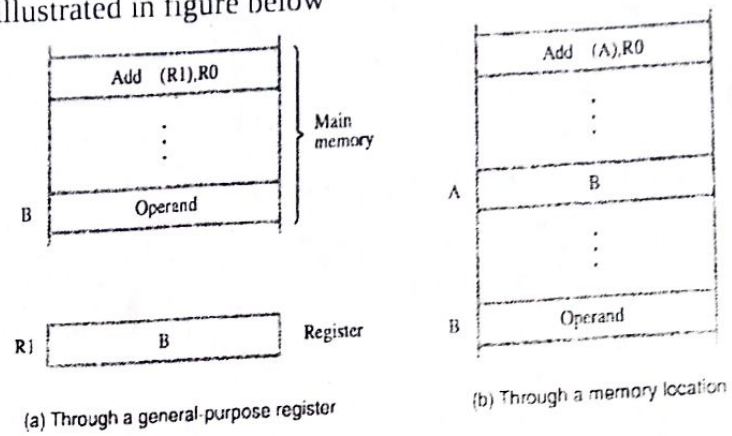
Part	Qn.No	CS202 COMPUTER ORGANISATION AND ARCHITECTURE	Marks
A	**Answer ALL Questions**		
	1	Write the three-address, two-address and one-address representations of the operation below with relevant assumptions: $C \leftarrow [A] + [B]$ Ans. **Three-address** **ADD A,B,C** **Two-Address** **ADD A, B** **MOVE B,C** **One-Address (Assuming Accumulator Register Is Implied Operand)** **LOAD A** **ADD B** **STORE C**	3
	2	What is the use of linkage register in subroutine invocation? Ans. To save return address before transferring control and to restore PC	3
	3	Why is non-restoring division faster than restoring division?	3

	Ans.If D is divisor, instead of doing D-D/2(2 steps) it does only +D/2(single step) Explanation—3 marks	
4	Design and draw a 3x2 array multiplier Ans.  Ans. Arrangement, Partial Product transfers—1 mark Diagram—2 marks	3

5	Illustrate various addressing modes with proper examples. Which is the default addressing mode selected by assemblers and compiler and why?	9

Ans. Indirect mode — The effective address of the operand is the contents of a register or memory location whose address appears in the instruction. We denote indirection by placing the name of the register or the memory address given in the instruction in parentheses as illustrated in figure below



(a) Through a general-purpose register

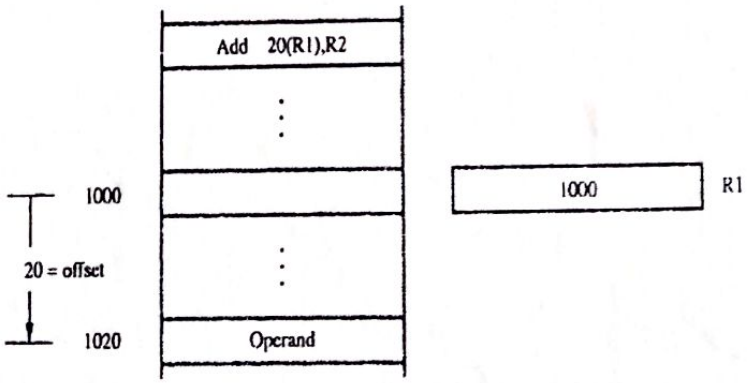
(b) Through a memory location

Explanation with figure—2 marks

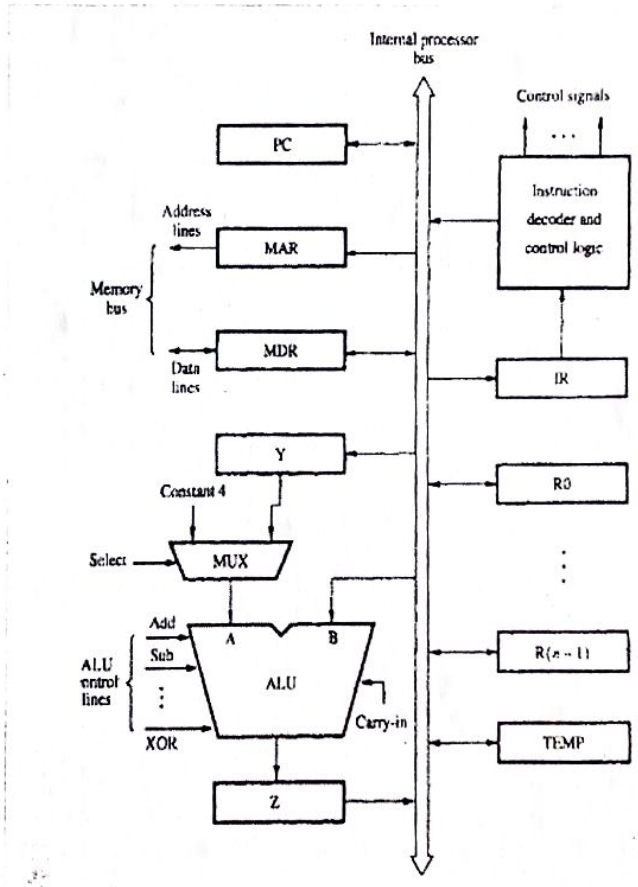
Index mode — The effective address of the operand is generated by adding a constant value to the contents of a register.
The register used may be either a special register provided for this purpose, or, more commonly, it may be any one of a set of general-purpose registers in the processor.

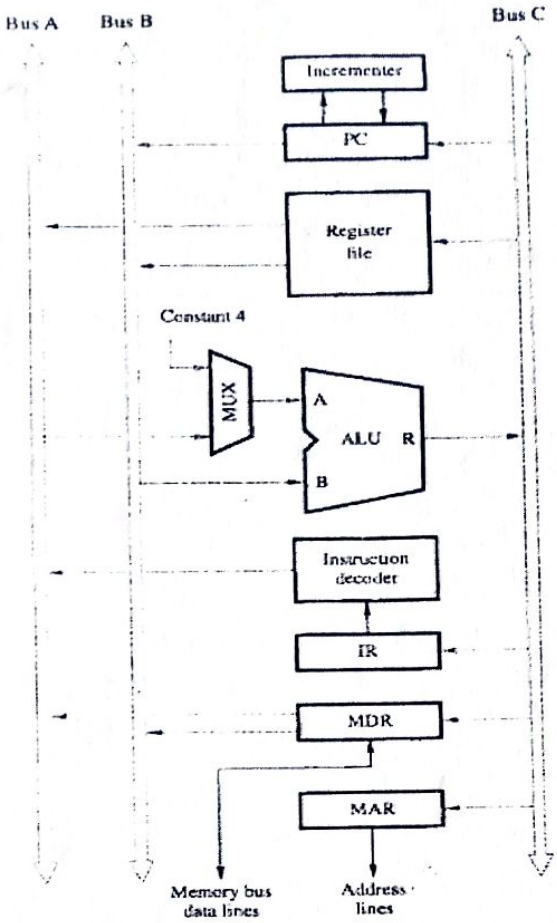
X--offset
EA = X + [Ri]

In the figure given below the index register, R1, contains the address of a memory location, and the value X defines an offset (also called a displacement) from this address to the location where the operand is found.



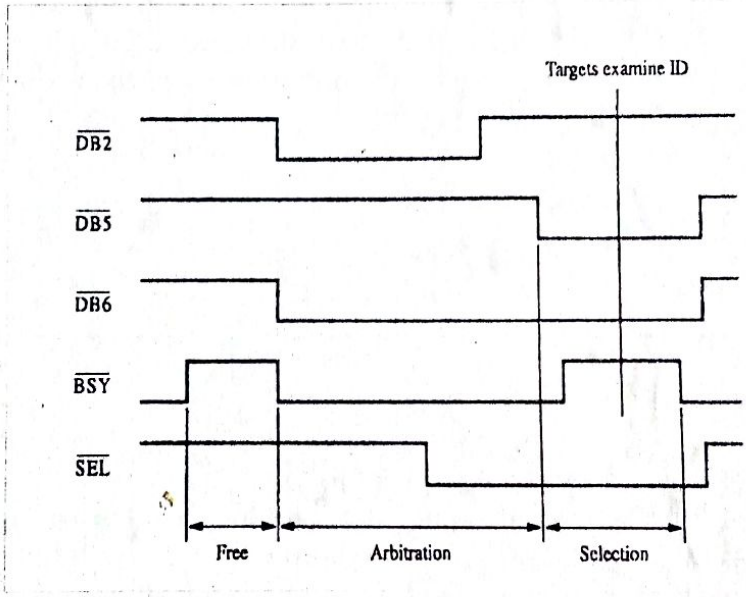
		Explanation with figure—2 marks Relative mode — The effective address is determined by the Index mode using the program counter in place of the general-purpose register R_i. X(PC) can be used to address a memory location that is X bytes away from the location presently pointed to by the program counter. Explanation with figure—2 marks Program counter relative addressing is used as default in compilers and assemblers as absolute address values to be stored by them are minimal---explanation—2 marks	
6		Example--Using Booth's Algorithm to multiply 3 by 4. For each step 1.5 marks. (4*1.5) A 0 0 1 1 3 X x 0 1 0 0 4 Y 1 -1 0 0 recoded multiplier --- Shift Only 0 0 0 0 0 Shift Only 0 0 0 0 0 0 Add -A +1 1 0 1 --- 1 1 0 1 0 0 Shift 1 1 1 0 1 0 0 Add A +0 0 1 1 --- 0 0 0 1 1 0 0 Shift 0 0 0 0 1 1 0 0 12 Flowchart—3 marks	9

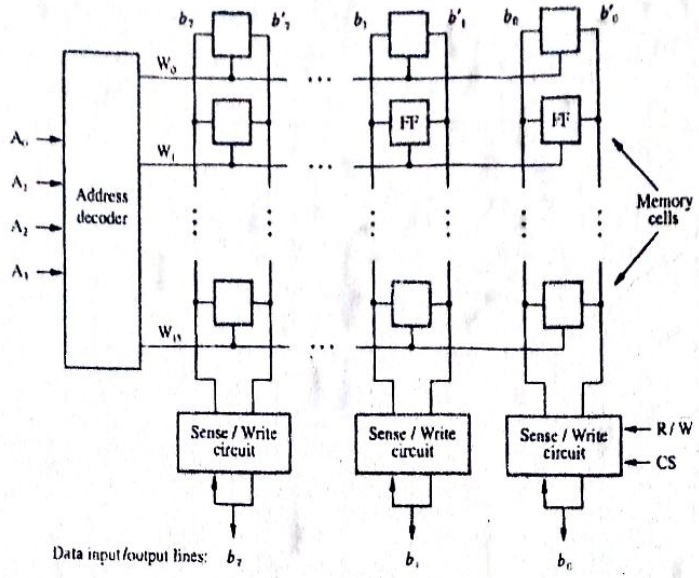
7(a)	Assuming that stack grows towards lower address range write assembly code for the following(Without using PUSH and POP) : (i)Pushing elements stored at ITEM1, ITEM2 onto stack Ans. **Subtract #4, SP** **Move ITEM1, (SP)** **Subtract #4,SP** **Move ITEM2, (SP)** ----2 marks (ii)Popping an element onto address ITEM Ans. **Move (SP), ITEM** **Add #4, SP** -----1.5 marks (iii)Copying value of top of stack to address TOP Ans. **Move (SP), TOP** ------1 marks	4.5
7(b)	Compare and contrast single bus and multiple bus organisation of CPU. Ans.  Single bus with diagram—2 marks	4.5

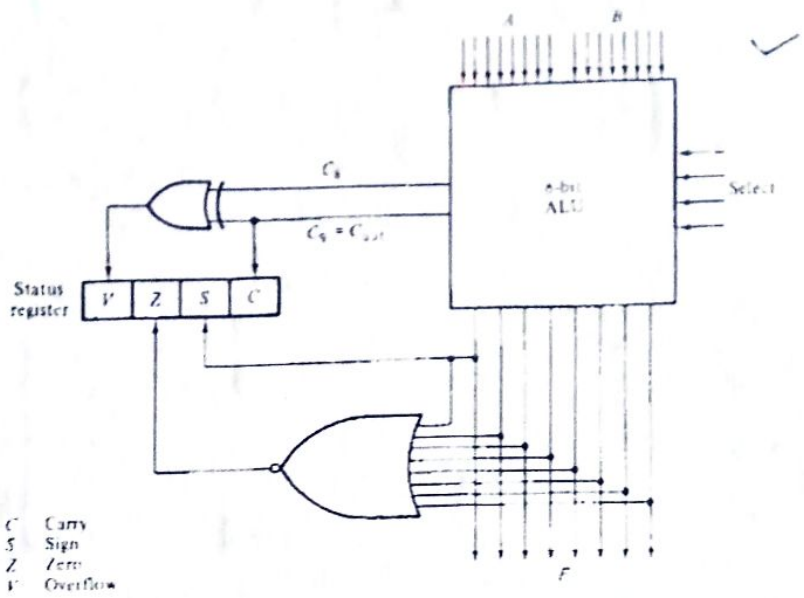


Mutliple bus with diagram—2.5 marks

8	Compare the two main modes of DMA transfer. Ans. Cycle stealing mode and burst mode. Explanation—3 marks.	3
9	Explain any two interrupt priority schemes Ans. (i)Arrangement of devices as per priority in a daisy chain (ii)Arranging devices in priority groups and each group arranged in a daisy chain	3

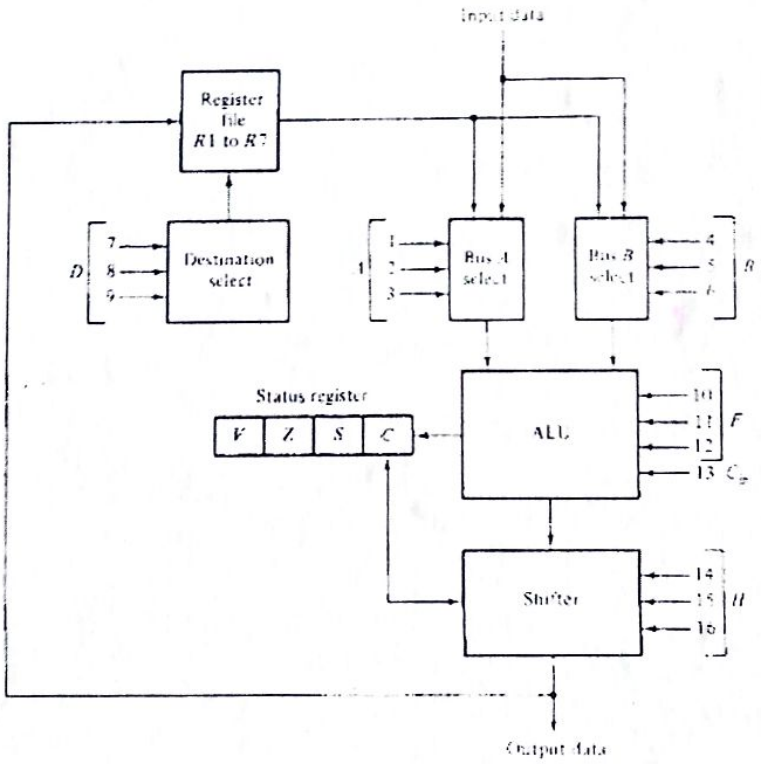
	Explanation with diagram—3marks	
10	What is MFC signal? How is it related to Memory Access Time? Ans. MFC—Memory Function Complete—1 mark Time between READ/WRITE signal and MFC is memory access time—2 marks	3
11	Which design feature of SRAM cells helps in value retention without refresh? Ans. Invertor elements connected back to back—explanation—3 marks	3
12	Illustrate with an example SCSI bus arbitration and selection. Ans.  Explanation of a sample use case DB6 wants to communicate with DB5 with timing diagram---9 marks	9
13	With the help of a diagram examine the internal organisation of bit cells in a memory chip. Ans.	9

	 Explanation with the above diagram---9 marks	
14(a)	Explain the architecture of USB with the help of diagram Ans. USB Serial Bus tree structure, split bus operation ,usb frame and packet formats with relevant explanations and diagrams—4.5 marks	4.5
14(b)	Differentiate Direct and Associative mapped cache with examples Ans. Direct mapped—Cache block can occur only one fixed position. Associative mapped—Cache block can occupy any of the slots of cache and searching for block are done parallelly. Explanation of above points—2.5 marks Diagrams—2 marks	4.5
15	Give a simple design for generating status bits for a 8-bit ALU. Ans.	10



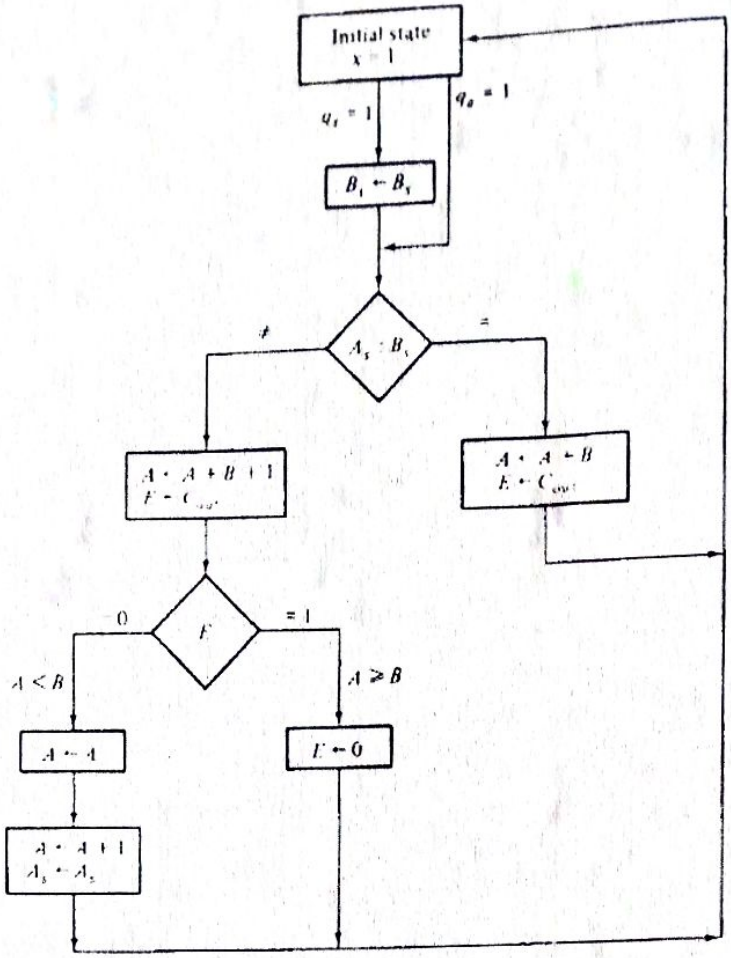
Explanation with diagram—10 marks

16	Draw a labelled block diagram of a processor unit with seven registers R1 to R7,a status register ,ALU with 3-selection variables and C_{in} and shifter with 3 selection variables. Ans.	10



Labelled diagram—10 marks

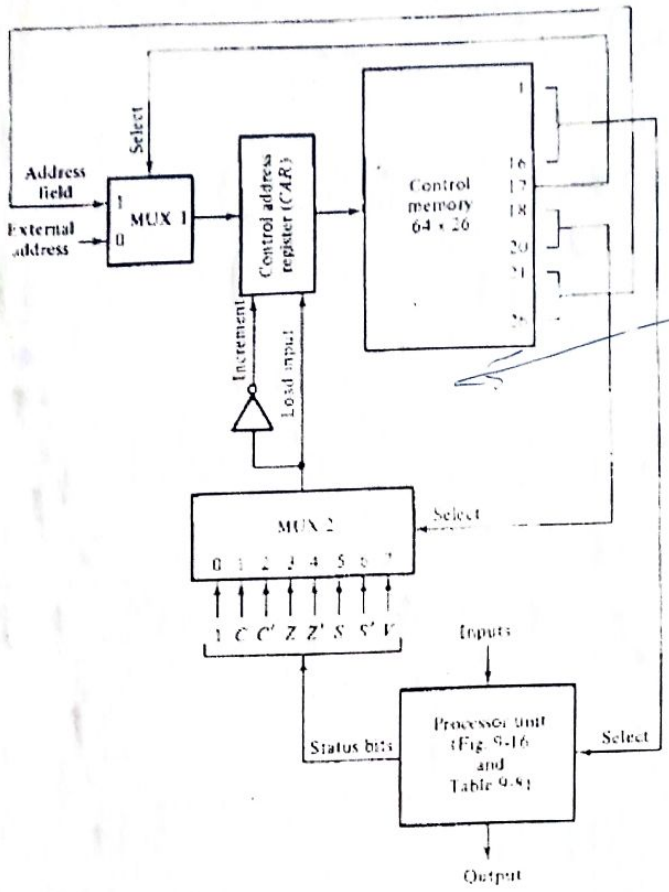
17	With the help of a flowchart explain the steps involved in sign-magnitude addition/subtraction, explain the steps involved in developing a hardwired control logic Ans.	10



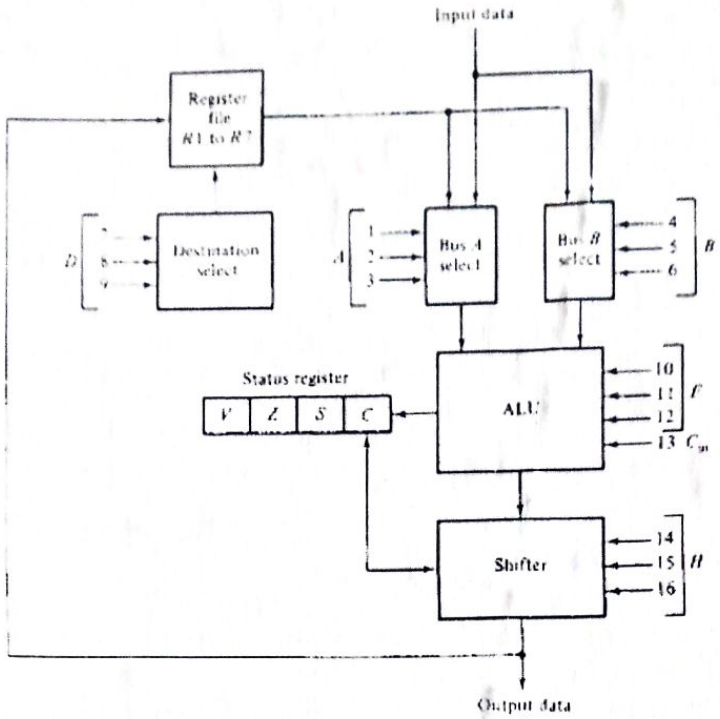
Flowchart—2.5 marks
Explanation—2.5 marks

Steps involved in design of any one approach of hardwired Control logic—5 marks

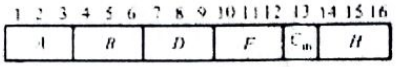
18	Using a block diagram analyse the design of a microprogram control for a processor unit. Ans. Explanation of components—5 marks Block-diagram—5 marks	10



19	What is a control word? With the help of proper illustrations and assumptions show how a designer would compose a control word for the processor unit. Ans. Control word—sequence of bits that triggers various operations In a processor Description of how bits for the control word are formed and grouped for the block diagram—5 marks Block diagram—5marks.	10

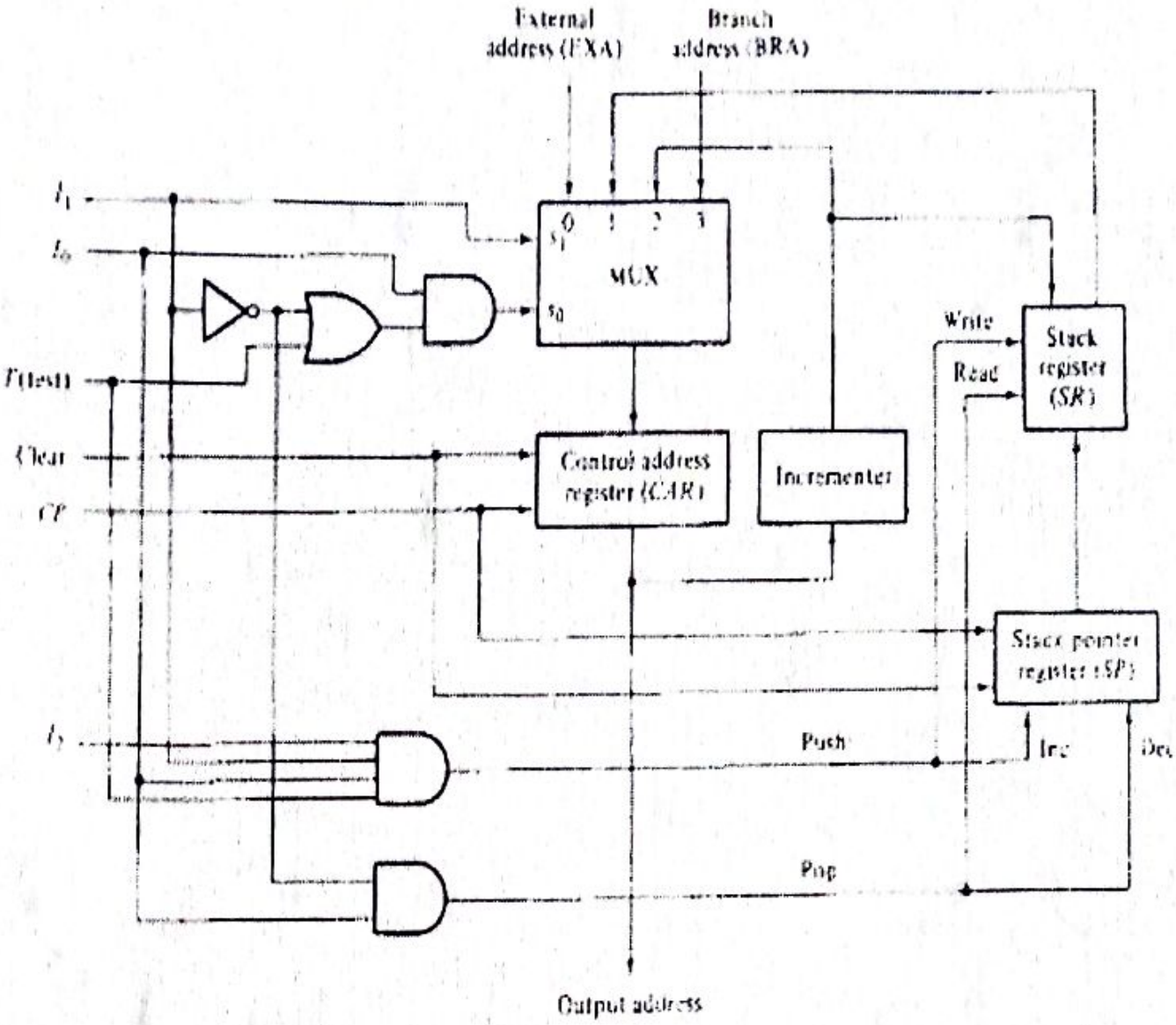


(a) Block diagram



(b) Control word

20	With the help of a diagram establish the requirement of microprogram sequencer in a microprogram controlled processor. Ans. Microprogram sequencer—used to generate address of microinstruction to be taken from control memory Explanation of block diagram—5 marks Block diagram—5 marks	10


External address (EXA)
Branch address (BRA)
MUX
Write
Read
Stack register (SR)
Clear
CP
Incrementer
Control address register (CAR)
Stack pointer register (SP)
Push
Pop
Output address