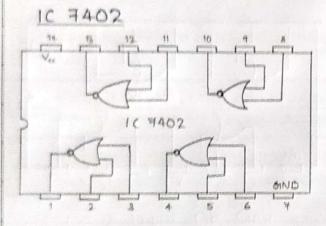
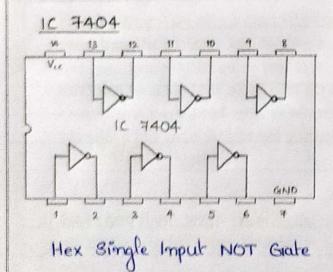


Inpula		Output
oΑ	13	
0	0	1
0	1	1
1	0	1
1	1	0



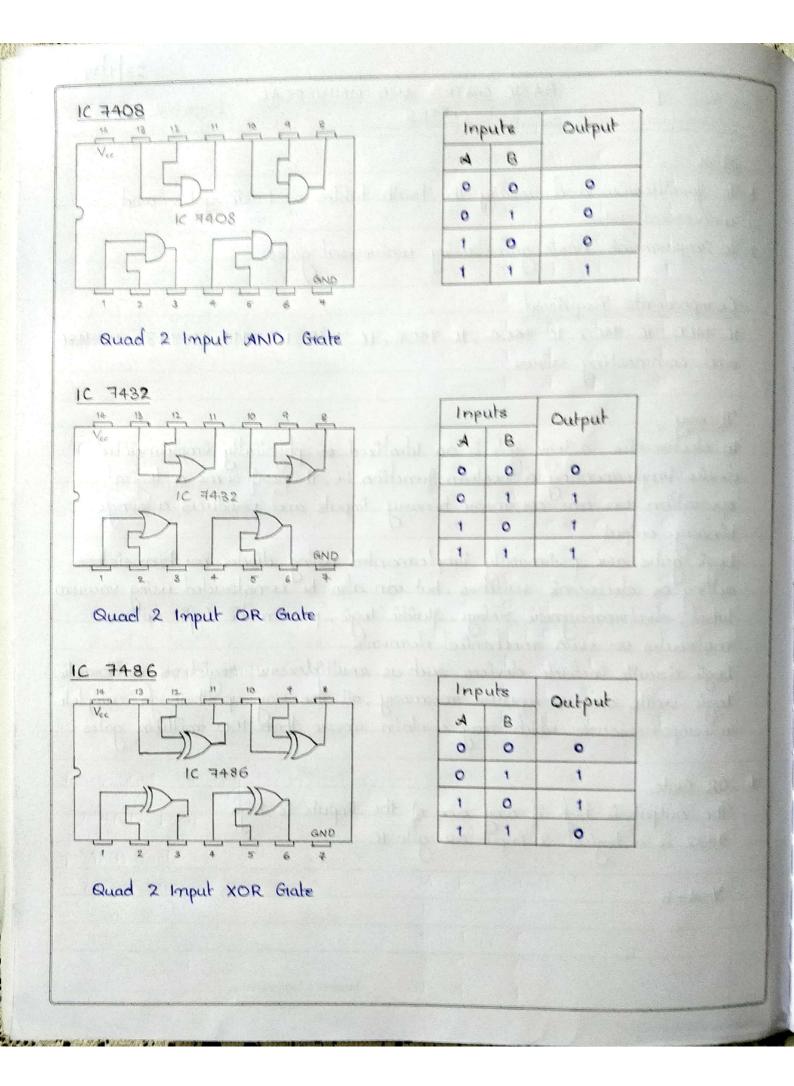
Inputs		Output
A	В	
0	0	1
0	1	0
1	0	0
1	1	0

Quad 2 Input NOR Grate

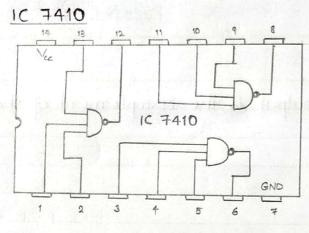


Input	Output
0	1
1	0

Date 28 1 19.
Expt. No. 1 BASIC GATES AND UNIVERSAL Page No. 3
Nim
1 To Jamilianize and venify the touth tables of basic gates and universal gates
2. To implement basic gates using universal gates
Components Required
IC 7400, IC 7402, IC 7404, IC 7408, IC 7410, IC 7411, IC 7432, IC 7486
and connecting wises.
Theosy
In electromics, a logic gate is an idealized on physically implemented
In electrionics, a logic gate is an idealized on physically implemented device implementing a boolean junction, i.e., it performs a logical
operation on one on more binary inputs and produces a single
binasy output
Logic gates are primarily implemented using diodes on transistors acting as electronic shifthes, but can also be constructed using vacuum
tubes, electromagnetic relays, fluidic logic, pneumatic logic, optics,
Logic ciacuits include devices such as multiplexess, registers, arithmetic
Logic units and computed memory, all the way up though complete microparocessous, which may contain mode than 100 million gates.
1. OR Grate
The output is high if any one of the inputs is high.  7432 is a logical 2 input OR gate IC.
Y= A+B
Teacher's Signature :



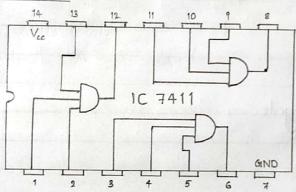
	Date 28/1/19
Expt. No 1	Page No 5
2. NOT Gale	
The gate acts like an invesites.	The output is the complement of the
impul	
7404 is a single imput NOT gate 10	
0, 1, 0	
Y=	
	Marie Children Shill and Market
3. AND Grate	
	Us imputs one Aish.
It gives a high output when all 17408 is a logical 2 imput AND	oate 10
0	
Y-A-B	
4 NOR Giole 0 01 0	
This is a combination of or and	NOT pate.
7402 is a 2 input NOR gate 10.	
Y = A + B	
Service Problems	
5. NAND Gate	
7410 is a 3 input NAND gate 10	
7420 is a 4 imput NAND gate 10	
7400 is a 4 imput NAND gate 10	A N
	A CONTRACTOR OF THE PARTY OF TH
Y= A.B	
Y= A.B	
Y= A.B	
	Teacher's Signature :



Touple	3	Imput	DUKN	Grate
		1 1 1 1 1 1 1 1 1		

Inputs		Output	
K	В	c	
0	0	0	1
0	٥	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0





Taiple 3 Imput AND Grate

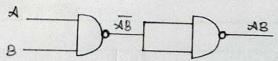
1,	nputs		Output %
K	В	C	
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Basic Gates Using Universal Gates

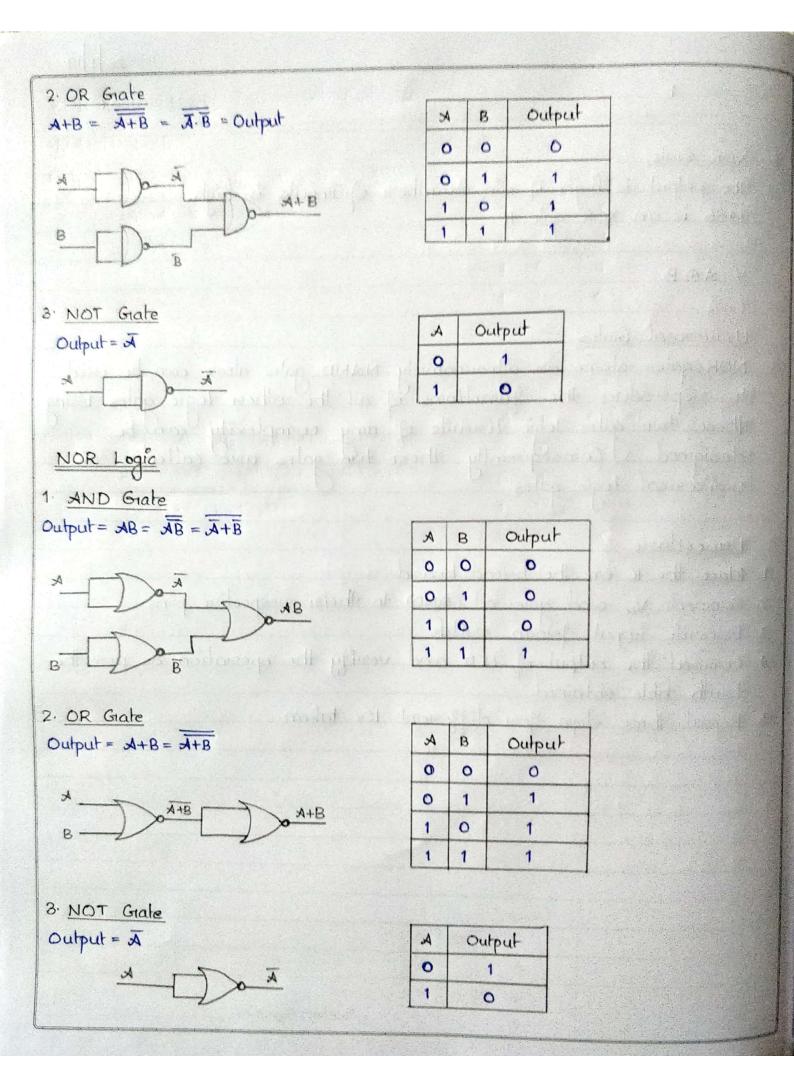
NAND Logic

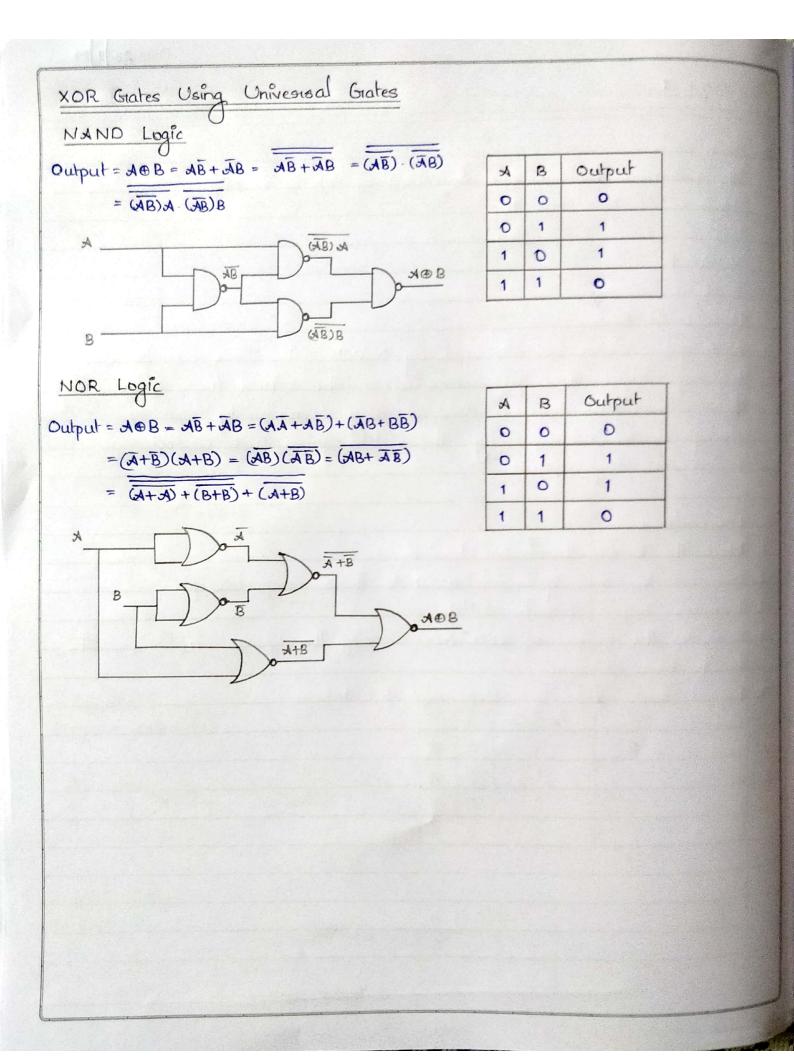
1 AND Grate

Output = AB = AB



K	В	Output
0	0	0
0	1	0
1	0	0
1	1	1





	Date 28 1 19
Expt. No1	Page No11
Result	
1 Familianized with and venified the touth universal gates. 2. Implemented basic gates using universal	tables of basic gates and
2) Implemented basis sales of	
pasic gales using universal	gates.
	<u> </u>
	/ /
Teacher's S	iignature :