

Total Pages: 2

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017

Course Code: CS202

Course Name: COMPUTER ORGANISATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions. Each carries 3 marks.

- | | | |
|---|--|-----|
| 1 | Differentiate between big-endian and little-endian byte assignments. | (3) |
| 2 | Design a 2x2 array multiplier. | (3) |
| 3 | Describe auto increment addressing mode with the help of an example. | (3) |
| 4 | Give the control sequence for execution of instruction Add[R2],R1 using a single bus organization. | (3) |

PART B

Answer any two questions. Each carries 9 marks.

- | | | |
|---|---|-----|
| 5 | a) Describe, with proper examples, the role of processor stack in subroutine call and return. | (5) |
| | b) Draw the flowchart for decimal multiplication. | (4) |
| 6 | a) Explain restoring method of division with the help of a flow chart. | (5) |
| | b) Write notes on three address, two address and one address instructions, giving example for each. | (4) |
| 7 | a) Explain single bus organization with the help of a diagram. Specify with examples, how memory operations are done in the given organization. | (5) |
| | b) Describe any 4 addressing modes with examples. | (4) |

PART C

Answer all questions. Each carries 3 marks.

- | | | |
|----|---|-----|
| 8 | What are vectored interrupts? | (3) |
| 9 | Write notes on flash memory. | (3) |
| 10 | Briefly explain the LRU cache replacement algorithm | (3) |
| 11 | Describe centralized bus arbitration. | (3) |

PART D

Answer any two questions. Each carries 9 marks.

- | | | |
|----|--|-----|
| 12 | a) Explain the architecture of USB with a diagram. What do you mean by split bus operation in USB? | (5) |
| | b) Write notes on static memories. | (4) |

- 13 a) Differentiate between associative and set associative cache mapping with examples. (5)
b) Write notes on interrupt nesting. Explain how simultaneous interrupt requests can be handled. (4)
- 14 a) Discuss about the different types of Read only memories. (4)
b) Explain with the help of timing diagrams, the input and output data transfers in an asynchronous bus. (5)

PART E

Answer any four questions. Each carries 10 marks.

- 15 a) Design a bus system for interconnecting four n bit registers (5)
b) Design a 4bit combinational logic shifter (5)
- 16 a) Briefly explain, with diagrams, the different methods for control organization (5)
b) Write notes on microprogrammed CPU organisation. (5)
- 17 a) Design an adder/subtractor circuit with one selection variable s and two inputs A and B. When s=0, the circuit performs A+B and when s=1 it performs A-B, by taking 2's complement of B. (5)
b) Write notes on status register. (5)
- 18 a) Describe the different ways in which a general-purpose processor unit can be organized. (6)
b) Write notes on conditional control statements. (4)
- 19 Explain with the help of a diagram, the working of microprogram sequencer. (10)
- 20 Describe the steps in control logic design with the help of an example. (10)
(Example can be realised using either hardwired or microprogrammed control organization.)
