| Course code | Course Name | L-T-P -Credits | Year of Introduction |
|---|---|---|---|
| CS404 | Embedded Systems | 3-0-0-3 | 2016 |

**Course Objectives:**

- To introduce the technologies behind embedded computing systems.
- To introduce and discuss various software components involved in embedded system design and development.
- To expose students to the recent trends in embedded system design.

**Syllabus:**

Introduction to embedded systems, basic components, its characteristics. Modelling embedded systems, firmware development. Integration and testing of embedded systems, development environment. Characteristics of RTOS, interrupt handling, creating tasks in a typical RTOS. Embedded product development life cycle.

**Expected Outcome**:

The Student will be able to :

i. demonstrate the role of individual components involved in a typical embedded system
ii. analyze the characteristics of different computing elements and select the most appropriate one for an embedded system
iii. model the operation of a given embedded system
iv. substantiate the role of different software modules in the development of an embedded system
v. develop simple tasks to run on an RTOS
*vi.* examine the latest trends prevalent in embedded system design

**References:**


1. J Staunstrup and Wayne Wolf, Hardware / Software Co-Design: Principles and Practice, Prentice Hall.
2. Jean J. Labrose, Micro C/OS II: The Real Time Kernel, 2e, CRC Press, 2002.
3. Raj Kamal, Embedded Systems: Architecture, Programming and Design, Third Edition, McGraw Hill Education (India), 2014.
4. Shibu K.V., Introduction to Embedded Systems, McGraw Hill Education (India), 2009.
5. Steave Heath, Embedded System Design, Second Edition, Elsevier.
6. Wayne Wolf , Computers as Components-Principles of Embedded Computer System Design, Morgan Kaufmann publishers, Third edition, 2012.


**Course Plan**

| Module | Contents | Hours | End Sem. Exam Marks |
|---|---|---|---|
| I | Fundamentals of Embedded Systems- complex systems and microprocessors- Embedded system design process .Specifications- architecture design of embedded system- design of hardware and software components- structural and behavioural description. | 6 | 15% |
| II | Hardware Software Co-Design and Program Modelling – Fundamental Issues, Computational Models- Data Flow Graph, Control Data Flow Graph, State Machine,. Sequential Model, Concurrent Model, Object oriented model, UML | 9 | 15% |

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|---|---|---|---|
| **FIRST INTERNAL EXAMINATION** | | | |
| **III** | Design and Development of Embedded Product – Firmware Design and Development – Design Approaches, Firmware Development Languages. | 6 | 15% |
| **IV** | Integration and Testing of Embedded Hardware and Firmware- Integration of Hardware and Firmware. Embedded System Development Environment – IDEs, Cross Compilers, Disassemblers, Decompilers, Simulators, Emulators and Debuggers. | 6 | 15% |
| **SECOND INTERNAL EXAMINATION** | | | |
| **V** | RTOS based Design – Basic operating system services. Interrupt handling in RTOS environment. Design Principles. Task scheduling models. How to Choose an RTOS. Case Study – MicroC/OS-II. | 9 | 20% |
| **VI** | Networks – Distributed Embedded Architectures, Networks for embedded systems, Network based design, Internet enabled systems. Embedded Product Development Life Cycle – Description – Objectives -Phases – Approaches1. Recent Trends in Embedded Computing. | 6 | 20% |
| **END SEMESTER EXAM** | | | |

**Question Paper Pattern**

1. There will be ***FOUR*** parts in the question paper – **A, B, C, D**
2. **Part A**
   a. **Total marks : 40**
   b. ***TEN*** questions, each have **4 marks**, covering **all the SIX modules** (***THREE*** questions from **modules I & II**; ***THREE*** questions from **modules III & IV**; ***FOUR*** questions from **modules V & VI**). ***All*** questions have to be answered.
3. **Part B**
   a. **Total marks : 18**
   b. ***THREE*** questions, each having **9 marks**. One question is from **module I**; one question is from **module II**; one question ***uniformly*** covers **modules I & II**.
   c. ***Any TWO*** questions have to be answered.
   d. Each question can have ***maximum THREE*** subparts.
4. **Part C**
   a. **Total marks : 18**
   b. ***THREE*** questions, each having **9 marks**. One question is from **module III**; one question is from **module IV**; one question ***uniformly*** covers **modules III & IV**.
   c. ***Any TWO*** questions have to be answered.
   d. Each question can have ***maximum THREE*** subparts.
5. **Part D**
   a. **Total marks : 24**
   b. ***THREE*** questions, each having **12 marks**. One question is from **module V**; one question is from **module VI**; one question ***uniformly*** covers **modules V & VI**.
   c. ***Any TWO*** questions have to be answered.
   d. Each question can have ***maximum THREE*** subparts.
6. There will be ***AT LEAST* 50%** analytical/numerical questions in all possible combinations of question choices.