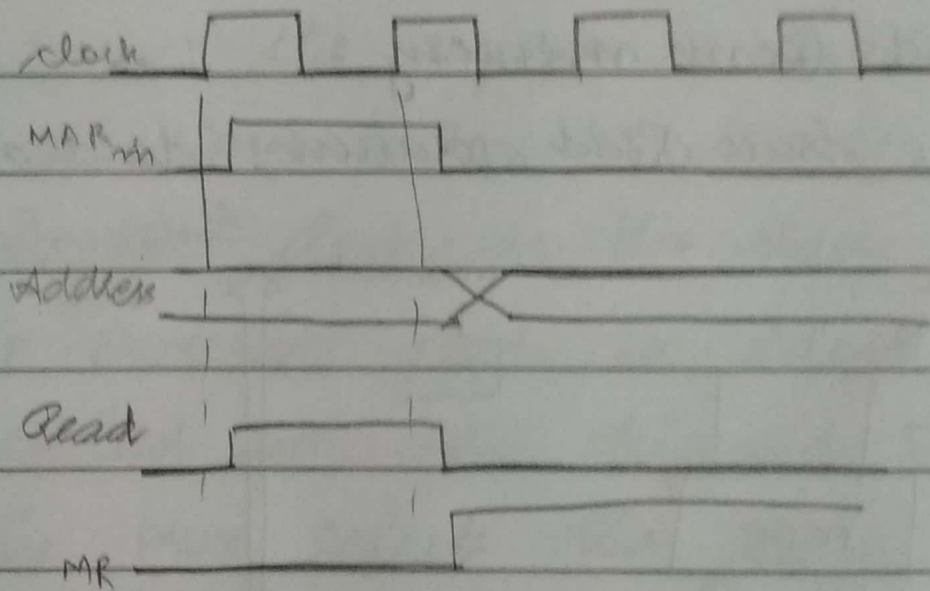


21.02.2019 \*  
MAP

Timing :



\* **mfc**: It is a control sig that indicates the <sup>requested</sup> read operation from MAR has been completed. When mfc sig has been set to 1 it indicates the contents of specified location has been read into the data lines of the mem. bus.

mfc is used to accommodate the variability in response time to access the memory.

4) **Storing of a word in memory:**

Address is loaded into MAR

Data to be written loaded into MDR

Write command is issued.

Example: Move R2, (R1)

R2 contents should be moved to the address of R1.

R1 out, MAR in

R2 out, MDR in, Write

MDR out, WMFC wait

→ processor waits until the write operation has been completed.

\* **Execution of a complete instruction:**

(i) Add (R3), R1

(ii) Fetch the instr<sup>n</sup>.

(iii) Fetch the first operand (the contents of the memory loc<sup>n</sup> pointed to by R3).

(iv) Perform the add<sup>n</sup>.

(v) Load the result into R1.



Execution of a complete instruction:

Add (R3), R1

Step Action

- Common
1. PC<sub>out</sub>, MAR<sub>in</sub>, Read, Select 4, Add, Z<sub>in</sub>
  2. Z<sub>out</sub>, PC<sub>in</sub>, Y<sub>in</sub>, WMFC <sup>(checks if instruction reached MDR)</sup>
  3. MDR<sub>out</sub>, IR<sub>in</sub> <sup>instruction</sup>
  4. R3<sub>out</sub>, MAR<sub>in</sub>, Read <sup>contains address</sup>
  5. R1<sub>out</sub>, Y<sub>in</sub>, WMFC
  6. MDR<sub>out</sub>, Select Y, Add, Z<sub>in</sub>
  7. Z<sub>out</sub>, R1<sub>in</sub>, End

\* Execution of branch instructions:

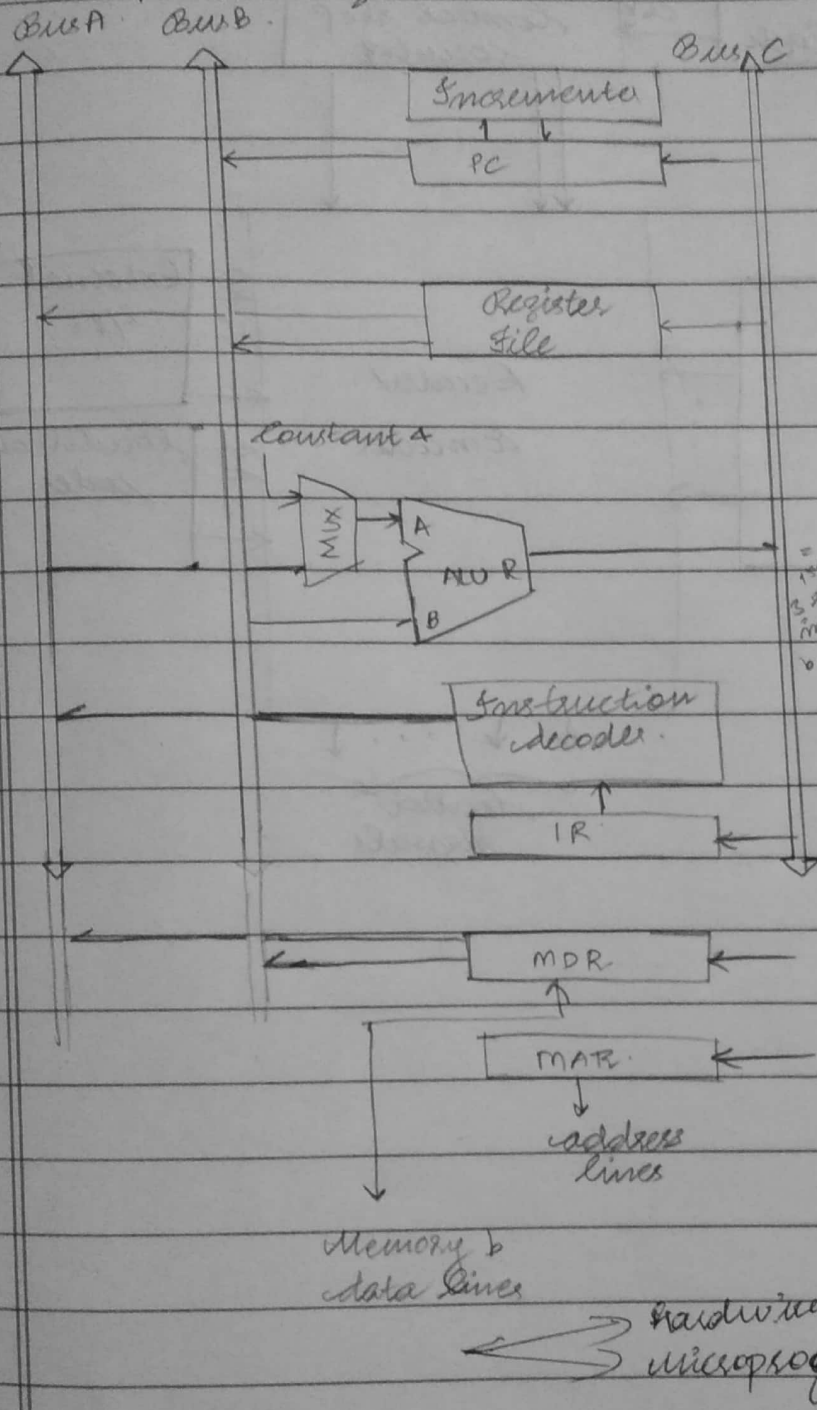
(i) \* branch instruction replaces the contents of PC with the 'branch target address', which is usually obtained by adding an offset X given in the branch instruction.

(ii) The offset X is usually the diff. b/w IR & PC

1. PC<sub>out</sub>, MAR<sub>in</sub>, Read, Select 4, Add, Z<sub>in</sub>
2. Z<sub>out</sub>, PC<sub>in</sub>, Y<sub>in</sub>, WMFC
3. MDR<sub>out</sub>, IR<sub>in</sub>
4. Offset-field of IR<sub>out</sub>, Add, Z<sub>in</sub>
5. Z<sub>out</sub>, PC<sub>in</sub>, End

Date \_\_\_\_ / \_\_\_\_ / \_\_\_\_

## \* Multiple bus organisation :



Constant 4 can be used to increment other address such as load multiple & store multiple.

Add R4, R5, R6.

1. PC<sub>out</sub>, R = B, MAR<sub>in</sub>, Read, IncPC.

2. WMFC.

3. MDR<sub>out</sub> B, R = B, IR<sub>in</sub>.

4. R4<sub>out</sub> A, R5<sub>out</sub> B, Select A, Add, R6<sub>in</sub>, End.

## \* Hardwired Control:

Bring changes to hardware, - speed ↑, flexibility ↓  
no change can be made to the code.

