Date __/__/____

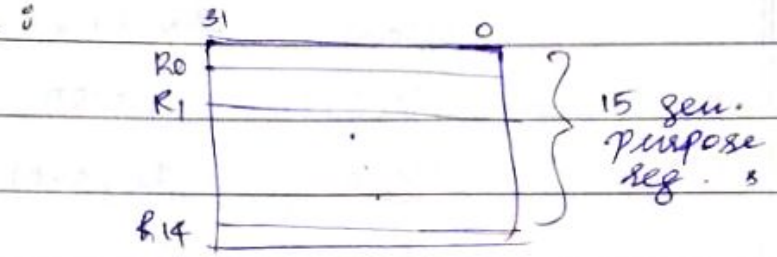
Saathi

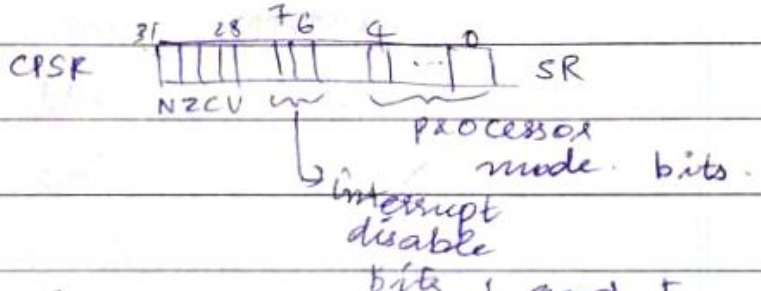
★ ARM:

o Memory:

1. Byte addressable.
2. 32 bit in a word.
3. words addresses aligned
4. Little + Big - endian supported.
5. accessed by load & store instruc^{n}'s

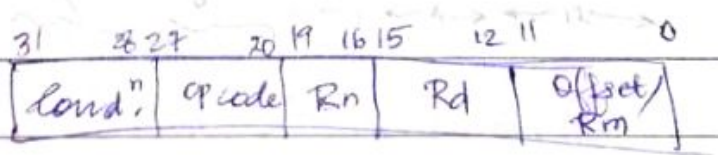
o Register structure:





★ Mem. access instruc^{n}s:

Format —



Load - LDR / LDRB mem → reg.

Store - STR / STRB reg → mem.

Before execu^{n}. check cond^{n}

Load / Store multiple operands: LDM1A R101, {R0, R1, R6}

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- Addressing mode :

1) Pre-indexed mode :

EA = [Base reg.] + Offset

2) Pre-indexed with write back

[EA] → Base reg

3) Post indexed :

EA = [Base reg.]

&Base reg ← [Base reg.] + Offset

4) Relative :

EA = [PC] + offset.

offset → immediate
→ stored in reg.

* Reg. move instruc" :

MOV R1 ← R0

R1 ← [R0]

MOV R0, #76

R0 ← 76

AND
ORR
EOR
BIC.

arithmetic → shifting
→ rotation

Branch instruc"s → <cond"> <opcode> <offset>