COA ASSIGNMENT

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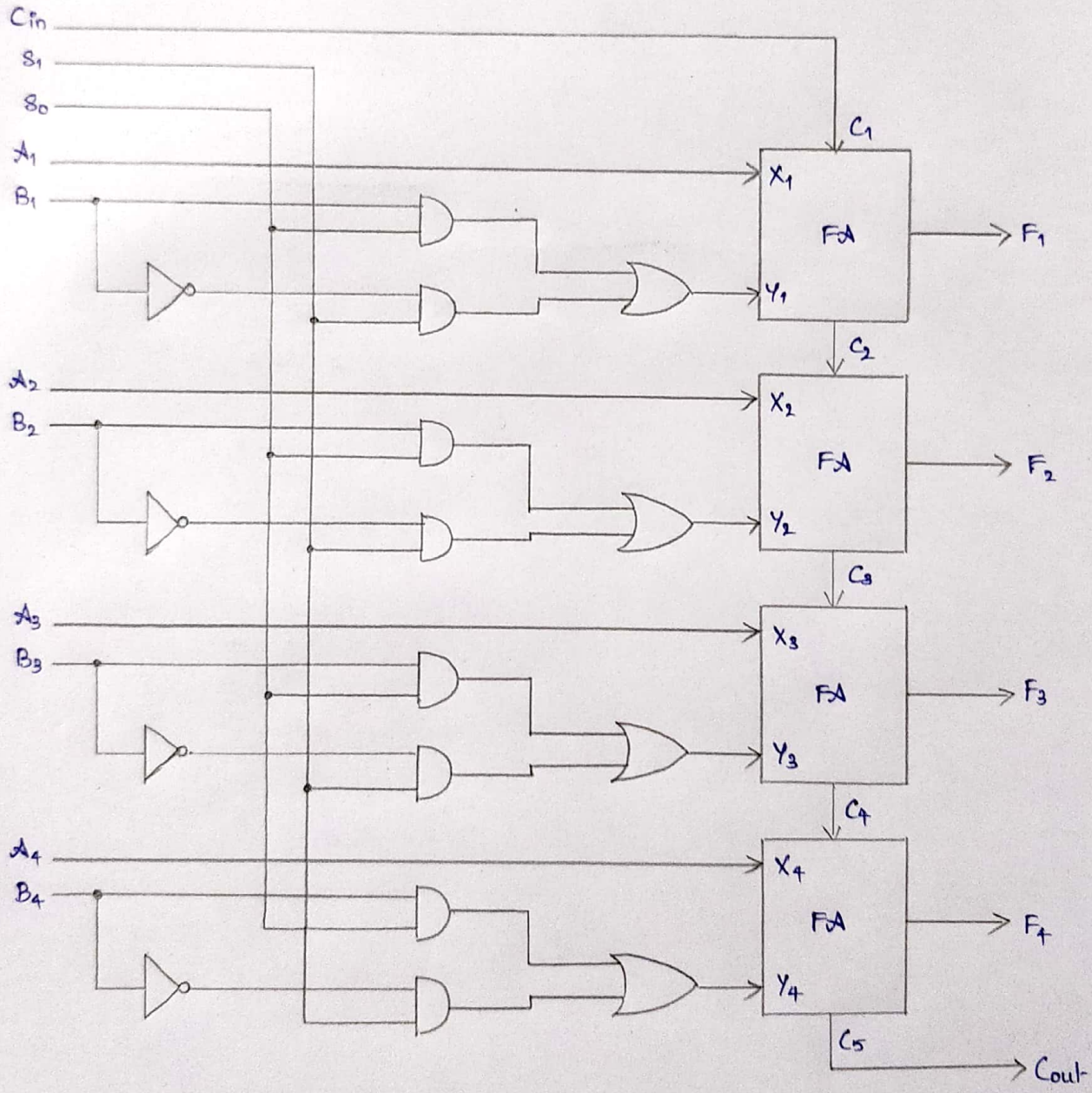
QUESTION 1

Design a 4-bit arithmetic unit which performs the following operations.

S_1	S_0	$C_{in}=0$	$C_{in}=1$
0	0	$F=A$	$F=A+1$
0	1	$F=A+B$	$F=A+B+1$
1	0	$F=A+B'$	$F=A+B'+1$
1	1	$F=A-1$	$F=A$

ANSWER



QUESTION 2

Distinguish horizontal & vertical microinstructions.

ANSWER

Microinstruction is normally structured as assign one bit position to each control signal. Microinstructions can be organized in two different ways named as Horizontal & Vertical microinstructions.

Horizontal Microinstructions

The below represented scheme of micro instruction by assigning 1 bit position to each control signal is known as horizontal microinstruction.

Example

0111000101100101

Drawback of this Scheme

Assigning individual bits to each control signal results in long micro instructions because the no. of required signals is usually large. For any given micro instruction, only few bits are set to 1.

For a total of 42 control signals, 42 bits would be needed for each micro instruction.

Vertical Microinstructions

In all cases, most signals are not needed simultaneously & many signals are mutually exclusive.

For example, only 1 function of the ALU can be activated at a time. Signals can be grouped so that all mutually exclusive signals are placed in the same group. A binary coding scheme can be used to represent the signals within a group. This type of highly encoded scheme which uses compact codes to specify control functions in each micro instruction is referred to as vertical micro instruction.

Comparison of Horizontal & Vertical Micro Instructions

The horizontal approach is useful when a higher operating speed is desired & when the machine structure allows parallel use of resources. But in vertical micro instruction, grouping control signals into fields requires a little more hardware because decoding circuits must be used to decode the bit patterns of each field into individual control signals. The cost of this additional hardware is more. The vertical approach results in considerably slower operating speeds because more micro instructions are needed to perform the desired control functions. To handle the execution of micro instructions only less hardware is needed.

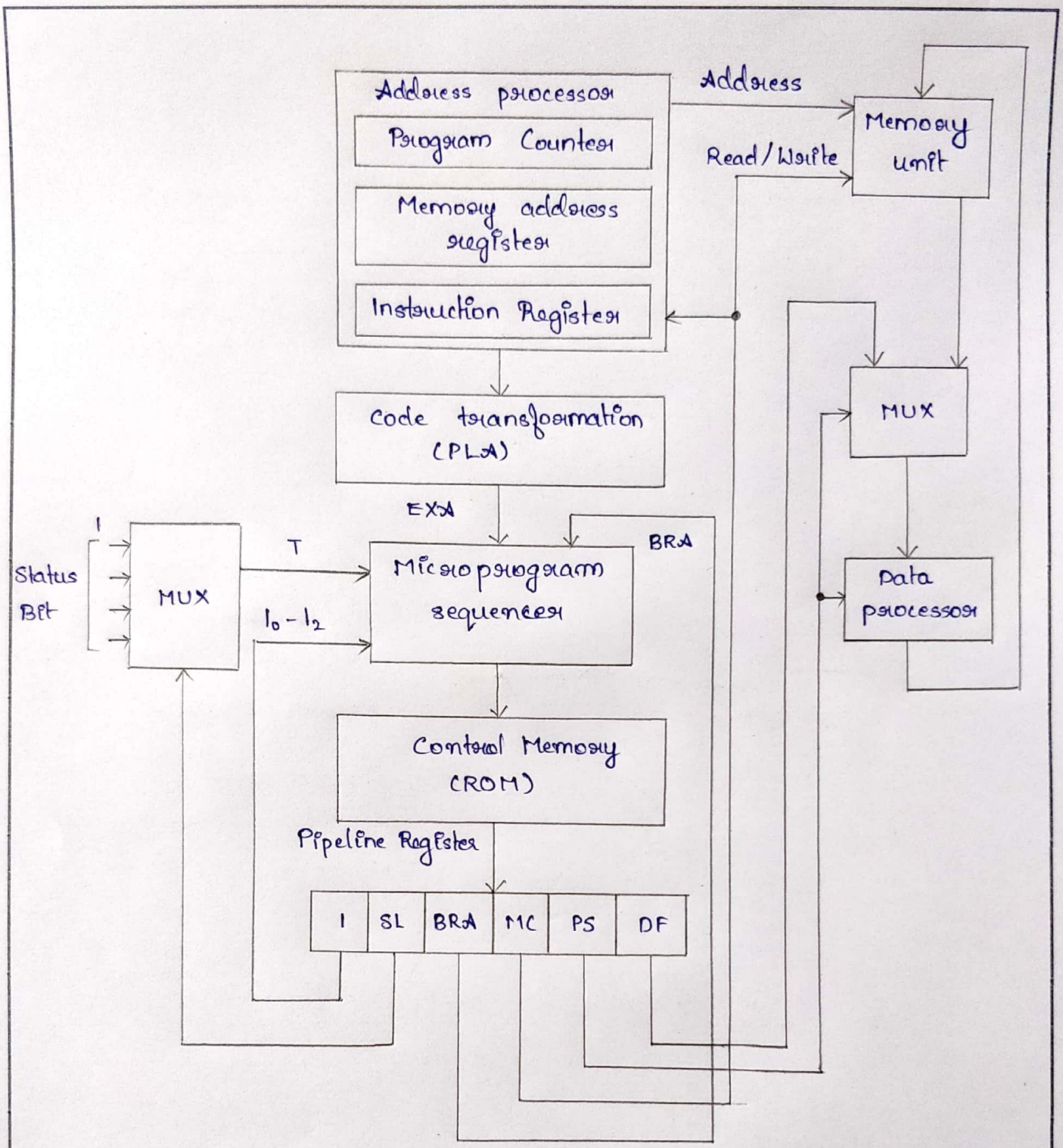
QUESTION 3

Explain microprogrammed CPU organization with the help of diagram.

ANSWER

A digital computer consists of a Central Processor Unit (CPU), a memory unit & input-output devices. CPU is classified into control section & processing section. Microprogram sequencer is the basic element of micro-programmed control for a CPU.

It consists of a memory unit, 2 processor units, a microprogram sequencer, a control memory & other digital functions. The memory unit stores the instructions & data supplied by the user through an input device. The data processor manipulates the data & address processor manipulates the address information received from memory. These 2 units can also be combined into 1. The instruction extracted from memory goes into instruction register. The instruction-code bits in instruction register specify a macrooperation for control memory. Operation code bits of instruction are converted into starting address for control memory using ROM or PLA. The address generated from PLA is applied to the External Address (EXA) input of sequencer. Control Unit contains a control memory, a MUX & a pipeline register. MUX selects status bits & applies it to test input of sequencer. Pipeline register may speed up control operation. I field (3 bits) supplies input information to sequencer. SL bits are status bits for MUX. BRA field supplies branch address to sequencer. MC [Memory Control) bits control address processor & read & write operations in memory. PS (Processor Select) bits control operation in data processor. DF (Data Field) bits are used to introduce constants into processor. Data field counts the no. of times a microprogram loop is traversed. Data field outputs set up control registers & introduce data in processor registers.



I → Sequence selector

SL → MUX selector

BRA → Branch address

MC → Memory control

PS → Processor selector

DF → Data field

QUESTION 4

Design a 4-bit combinational logic shifter.

ANSWER

H_1	H_0	Operation	Function
0	0	$S \leftarrow F$	Transfer F to S (No shift)
0	1	$S \leftarrow shr\ F$	Shift-right F into S
1	0	$S \leftarrow shl\ F$	Shift-left F into S
1	1	$S \leftarrow 0$	Transfer 0's into S