DATA SHEET

GPCM1F Series

ARM® Cortex®-M0 32-bit Sound Controller

Aug. 26, 2022

Version 1.5

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4-BIT SPEECH WITH SPU

1 GPCM1F SERIES

The primary differences in features between GPCM1FxxA and GPCM1FxxB series are listed in the following table.

Item	GPCM1F064A	GPCM1F064A_0001	GPCM1F064B	GPCM1F064B_0001	GPCM1FV000A
Microprocessor	ARM Cortex-M0	ARM Cortex-M0	ARM Cortex-M0	ARM Cortex-M0	ARM Cortex-M0
System Clock	Max. 81.92MHz	Max. 81.92MHz	Max. 81.92MHz	Max. 81.92MHz	Max. 81.92MHz
Operating Voltage	2.2V - 5.5V	2.2V - 5.5V	2.2V - 5.5V	2.2V - 5.5V	2.2V - 5.5V
Regulator Out (Body Option)	2.7~3.6V, ~30mA	2.7~3.6V, ~30mA	2.7~3.6V, ~30mA	2.7~3.6V,~30mA	2.7~3.6V, ~30mA
Internal RAM Size	13KB+ 2KB cache	13KB+ 2KB cache	8KB + 2KB cache	8KB + 2KB cache	13KB+ 2KB cache
GPIO Numbers	31	31	29 (Without IOA22,IOA23)	29 (Without IOA22,IOA23)	31
ADC LIN-IN	8 Channels	8 Channels	6 Channels	6 Channels	8 Channels
Execute External Program	V	V	X	X	V
Voice Recognition	X	V	X	V	X
ICE/ Writer Read Protect (Body Option)	V	V	V	V	V

2 GENERAL DESCRIPTION

The GPCM1F microcontroller equips an ARM® Cortex®-M0 processor core which is capable of operating at a speed up to 81.92MHz. The GPCM1F series is applicable for applications such as digital sound process, voice recognition, etc.

3 FEATURE

- **CPU**
  - CPU Core
    - ARM® Cortex®-M0 32-bit CPU (81.92MHz max) with Code Fetch Accelerator
    - Nested Vectored Interrupt Controller (NVIC) with 30 interrupt sources
    - 24-bit SysTick timer
    - Single cycle 32-bit multiplier instruction
- **Memory**
  - 13K-byte SRAM and 2K-byte RAM Cache
  - Up to (64K-64B) Bytes (max) Program Memory
- **Clock Management**
  - Internal oscillator: 8.192MHz
  - Phase Lock Loop with configurable output frequency: 81.92MHz (max.)
  - Internal 32768Hz oscillator and XTAL 32768Hz crystal
- **Power Management**
  - Sleep mode: Only CPU clock is off.
  - Deep Sleep mode: CPU clock is off; system enters deep sleep mode and all clocks are off.
  - Halt mode: CPU clock is off; system enters deep sleep mode and only 32768Hz clock remains on.
  - Regulator with configurable output SPI Voltage and Codec voltage
  - Low Voltage Detection
- **Reset Management**
  - Power On Reset
  - Low Voltage Reset
  - Watchdog Timeout Reset
  - PAD(H/W Key)Reset
  - S/W Reset
- **Analog peripherals**
  - 16-bit Audio PWM
  - 12-bit DAC with two 16-bit software channels featuring noise filter mixer and scalar for high-quality sound playback
  - 16-bit Sigma Delta Codec ADC(MIC ADC)
  - 12-bit SAR ADC and 8 x line PADs(GPCM1FxxB only has 6 x line PADs)
  - CTS(Capacitor sensing touch) supporting 10 x Touch IO PAD
- **I/O Ports**
  - Up to 31 multifunction and bi-direction I/Os

- I/O port options include pull-up resistor, pull-down resistor, output high, output low or floating input, and 4mA/ 8mA/ 12mA/ 16mA source-current/sink-current depending on the configurations set in the corresponding registers
- Each IO can be set as an external key to wake CPU up

■ **System Control**
- Three-channel DMA controller
- System Management Unit (SMU) for system configuration and control
- 16x16 MAC function
- Two quadrature decoders

■ **Timer**
- Three 16-bit general-purpose timers/counters
- Two 16-bit touch-sensing timers for CTS
- Two 16-bit CCP timers (Capture/Compare/PWM) and 8 PWMIOs

  All timers can be used as general-purpose timers.

■ **Communication peripherals**
- One I2C hardware
- One I2S input (Slave mode) and output(Master mode) hardware
- One SPIFC (SPI controller for FLASH device access) and two SPI serial interface I/Os
- One UART hardware
- One IR TX hardware

■ **SAR ADC Controller**
- 12-bit resolution SAR ADC and 10-channel selection (8*LINE-IN, V15_AD,and VSS_ADC)
- Supporting single, regular and regular scan conversion mode
- Data alignment: left and right
- External trigger option for injected conversion
- Analog detection watchdog
- DMA request generation during channel conversion

■ **SDM ADC Controller(MIC ADC)**
- 16-bit resolution Sigma-Delta Modulation ADC (SDM ADC) with Digital Audio Gain Control(DAGC)
- Generating acknowledgement for DMA after ADC data conversion completed

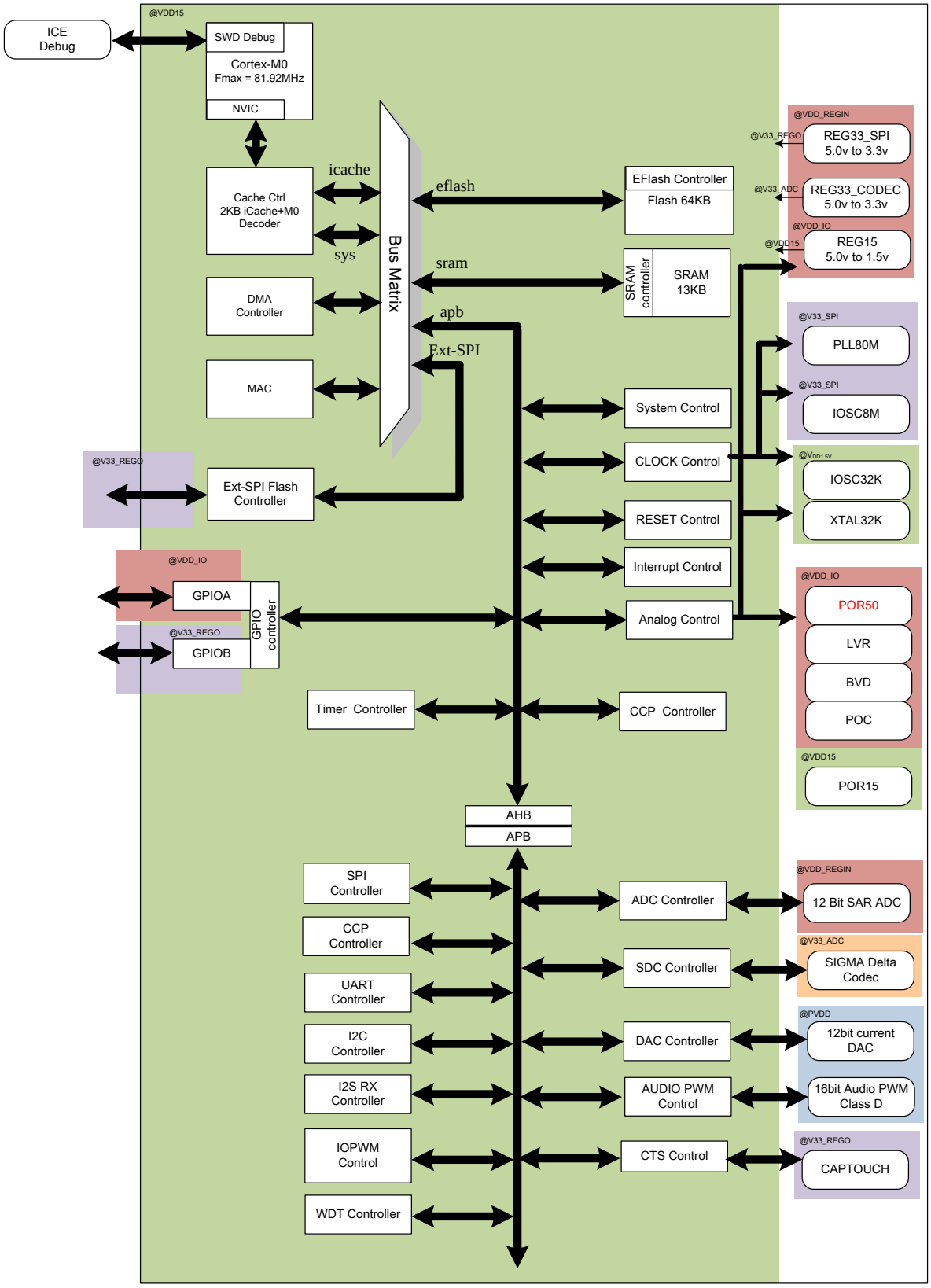
■ **DAC Controller**
- Supporting two input channel and 4x up-sampling
- Supporting scale/truncation mode when data saturation
- Generating acknowledgement for DMA after DAC data conversion completed.
- Output to 16-bit Audio PWM or 12-bit DAC
- Audio PWM supporting digital gain control and auto mute control

■ **Debug System**
- ARM serial-wire debug (SWD)
- Supporting up to three hardware breakpoints

■ **Operation Temperature**
- -40°C to 85°C

■ **Package**
- LQFP48

4 BLOCK DIAGRAM



5 SIGNAL DESCRIPTION

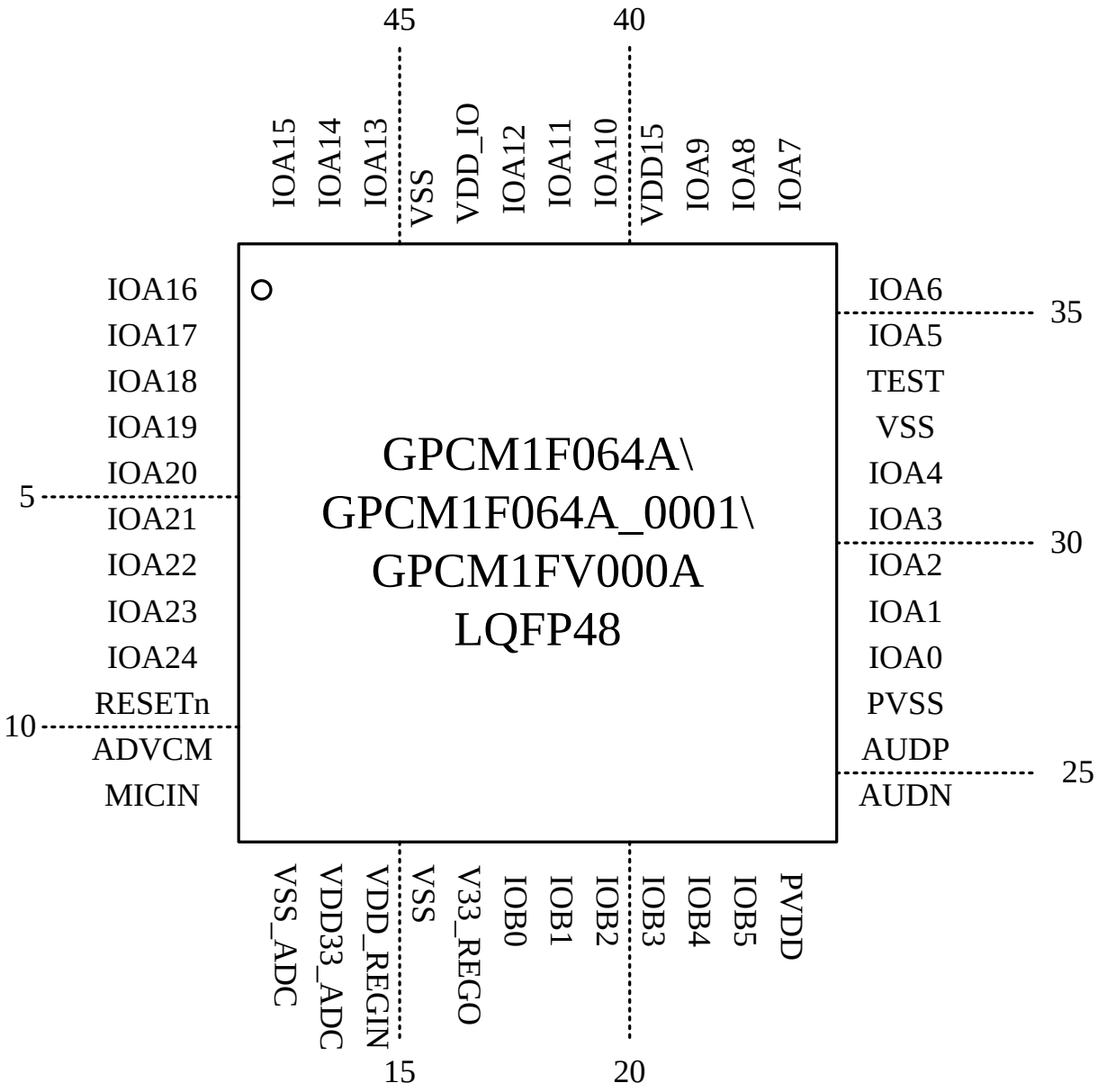
P = Power Pin, G = Ground Pin, A = Analog Pin

I/O = Bidirectional Pin, I = Input, O= Output

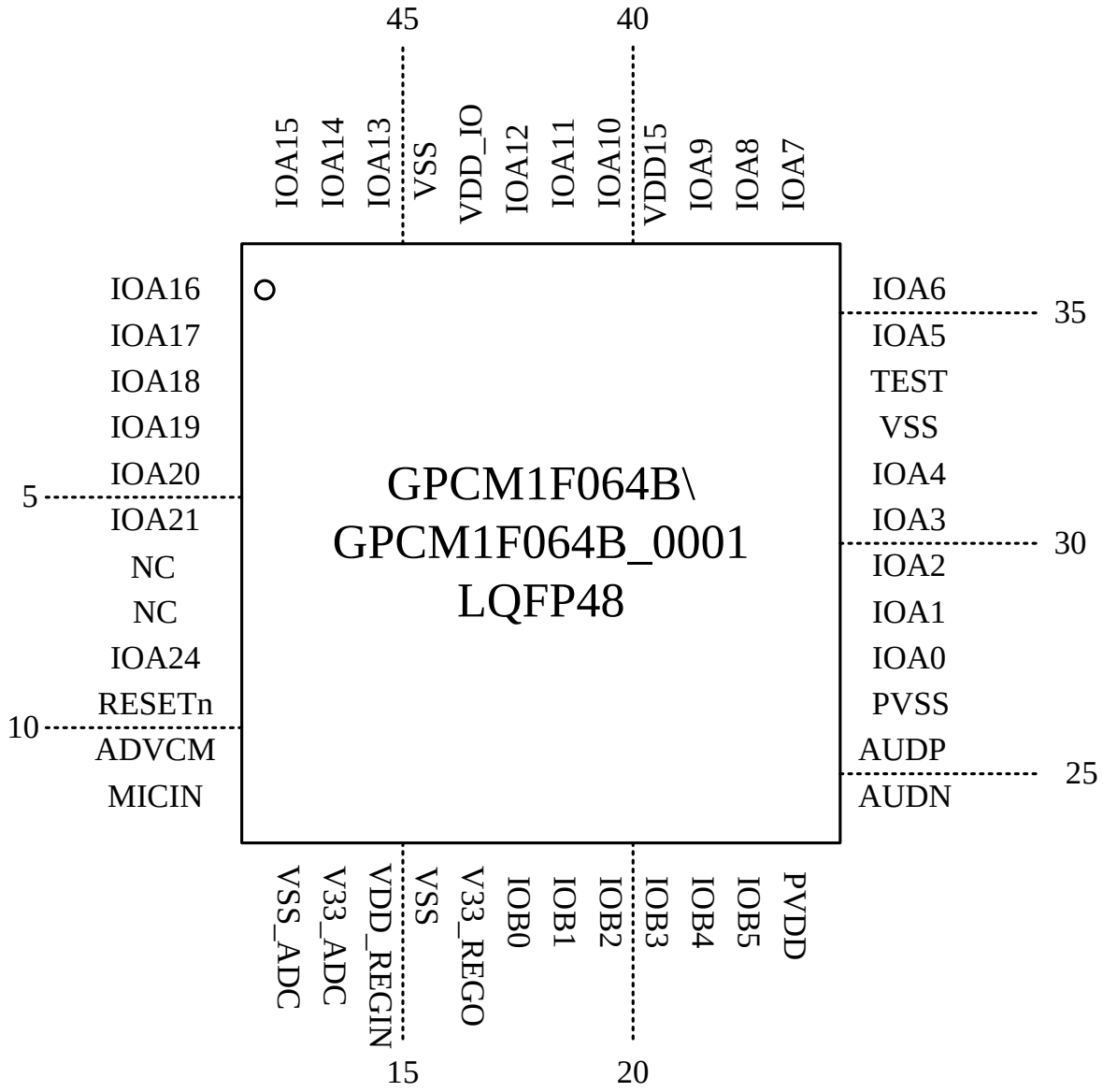
Num	PAD	Pin Name	Type	GROUP	Description
1	46	IOA13	AI/IO	X32KI	General purpose I/O Port IOA13 or Crystal 32K PAD In
2	47	IOA14	AO/IO	X32KO	General purpose I/O Port IOA14 or Crystal 32K PAD In
3	48	IOA15	I/O	IOA	General purpose I/O Port IOA15
4	1	IOA16	I/O	IOA	General purpose I/O Port IOA16
5	2	IOA17	I/O	IOA	General purpose I/O Port IOA17 or SAR ADC line In PAD
6	3	IOA18	I/O	IOA	General purpose I/O Port IOA18 or SAR ADC line In PAD
7	4	IOA19	I/O	IOA	General purpose I/O Port IOA19 or SAR ADC line In PAD
8	5	IOA20	I/O	IOA	General purpose I/O Port IOA20 or SAR ADC line In PAD
9	6	IOA21	I/O	IOA	General purpose I/O Port IOA21 or SAR ADC line In PAD
10	7	IOA22	I/O	IOA	General purpose I/O Port IOA22 or SAR ADC line In PAD
11	8	IOA23	I/O	IOA	General purpose I/O Port IOA23 or SAR ADC line In PAD
12	9	IOA24	I/O	ICE	General purpose I/O Port IOA24, ICE and Power writer SDA pin, or SAR ADC Line In PAD
13	10	RESETn	I	ICE	Reset pin(Low active) or ICE and Power writer SCK pin function
14	NC	VSS	G	GND	Ground
15	11	ADVCM	AO	ADC	Common voltage(1/2*VDD) for amplifier and ADC
16	12	MICIN	AI	ADC	Microphone input
17	13	VSS_ADC	G	ADC	CODEC ADC Ground
18	14	V33_ADC	P	ADC	CODEC ADC VDD 3.3V power. Connect a 2.2uF capacitor to VSS_ADC.
19	15	VDD_REGIN	P	VDD_REGIN	VDD_REGIN is formed by V33_REGIN and ADC_REGIN power input pins
20	16	VSS	G	GND	Ground
21	17	V33_REGO	P	V33_REGO	V33_REG output pin supplies 2.7V~3.6V and output current up up 30mA
22	18	IOB0	I/O	IOB/SPI FC	General purpose I/O Port IOB0 and SPIFC HOLDB/ SIO3 pin
23	19	IOB1	I/O	IOB/SPI FC	General purpose I/O Port IOB1 and SPIFC SCK pin
24	20	IOB2	I/O	IOB/SPI FC	General purpose I/O Port IOB2 and SPIFC MOSI/ SIO0 pin
25	21	IOB3	I/O	IOB/SPI FC	General purpose I/O Port IOB3 and SPIFC CS pin
26	22	IOB4	I/O	IOB/SPI FC	General purpose I/O Port IOB4 and SPIFC MISO/ SIO1 pin
27	23	IOB5	I/O	IOB/SPI FC	General purpose I/O Port IOB5 and SPIFC WPB/ SIO2 pin
28	24	PVDD	P	Audio_PWM	Audio PWM VDD 5V power input pin
29	24	PVDD	P	Audio_PWM	Audio PWM VDD 5V power input pin
30	25	AUDN	AO	Audio_PWM	Audio PWM AUDN output
31	25	AUDN	AO	Audio_PWM	Audio PWM AUDN output
32	26	AUDP/DACO	AO	Audio_PWM	Audio PWM AUDP & DAC output
33	26	AUDP/DACO	AO	Audio_PWM	Audio PWM AUDP & DAC output
34	27	PVSS	G	Audio_PWM	Audio PWM Ground More than 3 PVSS pads are suggested to be bounded.
35	27	PVSS	G	Audio_PWM	
36	27	PVSS	G	Audio_PWM	
37	NC	PVSS	G	Audio_PWM	
38	NC	VSS	G	GND	Ground. This pin is not necessarily bounded out because all VSS PADs are connected in IC.

Num	PAD	Pin Name	Type	GROUP	Description
39	28	IOA0	I/O	IOA	General purpose I/O Port IOA0
40	29	IOA1	I/O	IOA	General purpose I/O Port IOA1
41	30	IOA2	I/O	IOA	General purpose I/O Port IOA2
42	31	IOA3	I/O	IOA	General purpose I/O Port IOA3
43	32	IOA4	I/O	IOA	General purpose I/O Port IOA4
44	33	VSS	G	GND	Ground
45	34	TEST	I	TEST	Test PIN
46	35	IOA5	I/O	IOA	General purpose I/O Port IOA5
47	36	IOA6	I/O	IOA	General purpose I/O Port IOA6
48	37	IOA7	I/O	IOA	General purpose I/O Port IOA7
49	38	IOA8	I/O	IOA	General purpose I/O Port IOA8
50	39	IOA9	I/O	IOA	General purpose I/O Port IOA9
51	NC	VNN	AI	EFLASH	EFLASH Test Pin (for internal use only)
52	NC	VPP	AI	EFALSH	EFLASH Test Pin (for internal use only)
53	40	VDD15	P	VDD15	Core Power
54	41	IOA10	I/O	IOA	General purpose I/O Port IOA10
55	42	IOA11	I/O	IOA	General purpose I/O Port IOA11
56	43	IOA12	I/O	IOA	General purpose I/O Port IOA12
57	44	VDD_IO	P	VDD_IO	VDD50 is formed by Core power's REG_IN and VDD_IOA power input pins)
58	45	VSS	G	GND	Ground

5.1 GPCM1F064A\GPCM1F064A_0001\GPCM1FV000A LQFP48 Package



5.2 GPCM1F064B\GPCM1F064B_0001 LQFP48 Package



6 FUNCTION DESCRIPTION

6.1 CPU

GPCM1F is equipped with a Cortex®-M0 32-bit processor, which is especially designed for a broad range of embedded applications. The significant benefits of this core processor include:

• Simple, easy-to-use programming model
• Highly efficient ultra-low power operation
• Excellent code density
• Deterministic high-performance interrupt handling
• Upward compatibility with the rest of the Cortex-M processor family. The processor also supports a 24-bit system timer and 32-bit single cycle multiplier instruction. Interrupts include 30 IRQs (Interrupt Request) and NMI (Non-Maskable Interrupt).

6.2 Memory

6.2.1. SRAM

The 13K-byte working SRAM is ranged from 0x2000_0000 through 0x2000_33FF, and a 2K-byte dedicated RAM cache.

6.2.2. Embedded FLASH

GPCM1F supports a high-speed 64K-byte embedded FLASH memory in which access time is determined by CPU clock. CPU to read EFLASH memory needs four CPU clock cycles when CPU runs at 81.92MHz (maximum speed).

6.3 Clock Management

6.3.1. IOSC 8.192MHz

When GPCM1F powers up, the 8.192MHz Internal Oscillator(IOSC) is used for system clock as well as PLL input frequency. The 8.182MHz IOSC is enabled in default.

6.3.2. PLL(Phase Lock Loop)

The purpose of PLL is to pump frequency up from 24.576MHz to 81.92MHz for system clock. PLL has eight types of clock outputs available. The PLL frequency is 81.92MHz in default.

6.3.3. IOSC 32768 Hz and XTAL 32768 Hz

GPCM1F can choose one of IOSC 32768(default enabled) or XTAL 32768Hz for the source of 32KHz system clock (IOSC32768 in default). The 32KHz system clock in normal mode is the clock source for CTS, timer, and watchdog. In halt mode, only 32KHz system clock remains working for power saving purpose.

6.4 Power management

GPCM1F supports three low power modes: Sleep mode, Deep Sleep mode, and Halt mode. The detail description is as follows:

Mode	Entry	Wakeup	Clocks	Regulator Voltage	I/O State
Sleep	WFI	Any interrupt	CPU clock is OFF	Output voltage in normal mode voltage	Keep in the setting before entering low power modes.
	WFE	Any event			
Deep Sleep	WFI+SLEEPDEEP=1	External input +interrupt	All clocks are OFF, All Macro go Sleep	Output voltage changes to Deep Sleep mode voltage.	
	WFE+SLEEPDEEP=1	External input +event			
Halt	WFI+SLEEPDEEP=1	External input + interrupt + CTS+ MIC+ RTC	Only 32K ON, All Macro go Sleep		
	WFE+SLEEPDEEP=1	External input + interrupt + CTS+ MIC+RTC			

6.5 Reset Management

6.5.1. Power-On Reset

When IC is powered ON, power-on reset (PORB) will be triggered by which all registers are reset.

6.5.2. Low Voltage Reset

When operating voltage drops below Low Voltage Reset (LVR) level, it will generate LVR signal to reset system. GPCM1F has only 1.9V LVR level available. LVR is able to keep IC operating normally at low voltage condition.

6.5.3. PAD(H/W KEY) Reset

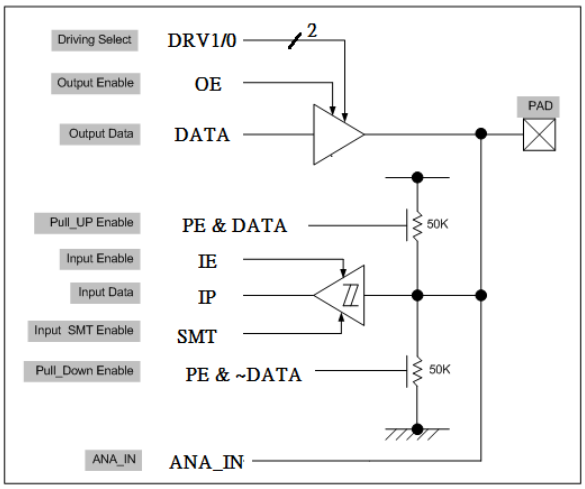
Pad RESETn has a denounce function so that it must be kept low at least for 50us in order to trigger Pad RESETn and reset system.

6.5.4. Watchdog timeout Reset

If watchdog function is enabled, a reset signal is generated to reset system when watchdog counter is overflow.

6.6 I/O port

GPCM1F has up to 31 IOs, where 25 IOs in Port IOA and 6 IOs in Port IOB. All I/Os have options such as pull-up resistor, pull-down resistor, output high, output low or floating input, 4mA/ 8mA/ 12mA/ 16mA source-current/ sink-current, all depending on the configurations set in the corresponding registers. All IOs can be programed as external keys in bit-operation for wakeup purpose. In addition to ordinary I/O function, all ports also have special functions in certain pins. The following diagram demonstrates the I/O schematics.



6.7 System Control

6.7.1. DMA

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU action. The DMA controllers have three channels, each dedicated to managing memory access requests from one or more peripherals. It has an arbiter for handling the priority between DMA requests.

6.7.2. MAC

The MAC controller is designed to accelerate the audio MAC process of 16-bit system. It supports up to 16x16 MAC function, 40-bit accumulator, 8/16/32-bit saturation detection, and output auto-shift function.

6.7.3. Quadrature decoder

The purpose of quadrature decoder (QD) is to detect the phase differences between two square waves, normally used for rotating devices to detect the rotation velocity and position, etc. There are two sets of quadrature decoders, each comprising of two data inputs, control bits, counter and a clear port to reset the counter. User only needs to input two square waves into quadrature decoder through two input pins and starts running function.

6.8 Timers

GPCM1F is designed having seven 16-bit timers to meet various application needs.

6.8.1. General-purpose timers

GPCM1F provides three timers with counter mode and capture mode function. It supports as ADC/DAC trigger source, external clock source from GPIO, and capture mode with debounce filter.

6.8.2. Touch sensing timers

GPCM1F provides two timers with pre-loaded function. It can be dedicated for CTS or general timer.

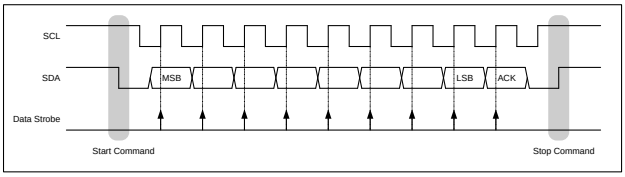
6.8.3. CCP timers

GPCM1F features two timers with Compare, Capture, PWM (or abbreviated as CCP), and Counter functions. It supports eight-channel PWM output and ADC trigger source.

6.9 Communication Peripherals

6.9.1. I2C

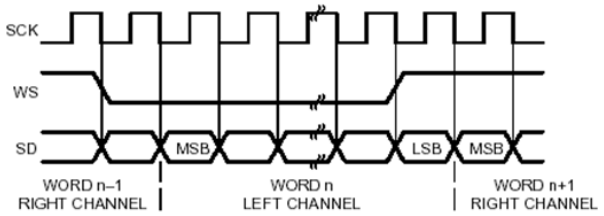
The I2C is mainly for communicating the lower-speed peripheral to processor or microcontroller in short-distance. Depending on the device chosen, 7-bit or 10-bit address mode can be selected. The I2C protocol only requires two wires (SCK and SDA) to implement. I2C controller supports four transferring modes: master transmitting, master receiving, slave transmitting, and slave receiving modes. The format of I2C frame is depicted as follows:



It also supports multi-master capability, option clock, and DMA capability.

6.9.2. I2S

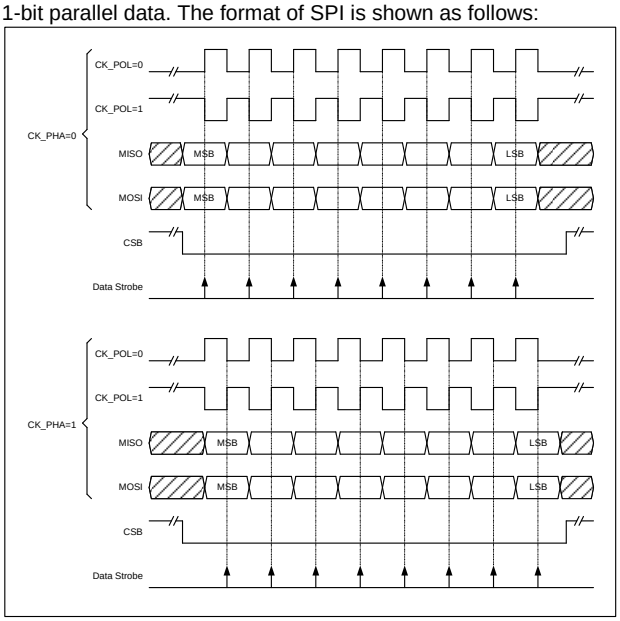
The I2S bus is a 3-line serial bus, which consists of a line for two time-multiplexed data channels (SD), a word selection line (WS) and a clock line (SCK). Since the transmitter and receiver are having the same clock signal for data transmission, the transmitter, as a master, has to generate the bit clock, word-selection signal and data. The format of I2S is as follows:



It also supports configurable settings of each RX channel for different frame size, word length, frame synchronization mode, data alignment, MSB/LSB first send mode, rising/falling sending edge mode, frame polarity, and the polarity of first transmitted frame.

6.9.3. SPI

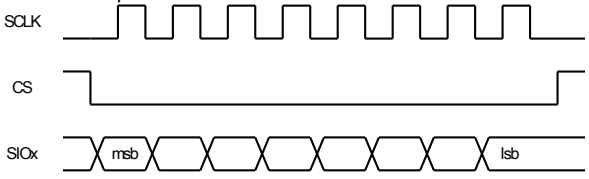
The GPCM1F incorporates two Serial Peripheral Interfaces (SPI). The SPI is a synchronous serial communication interface specification used for short distance communication. It allows half/ full-duplex serial communication with external devices and only 1-bit parallel data. The format of SPI is shown as follows:



It also supports master or slave operation, multi-master mode, programmable clock polarity and phase, and 1-byte transmission and reception with DMA.

6.9.4. SPI FC

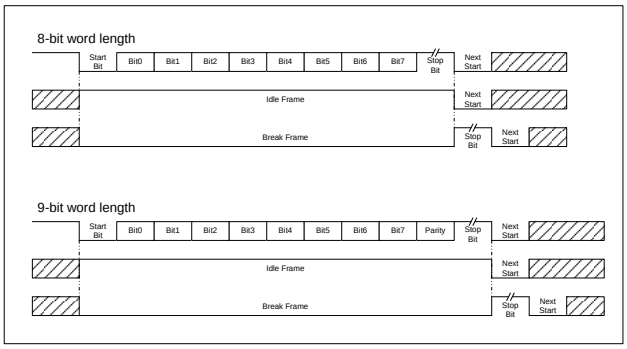
GCM1F has an enhanced SPI controller for FLASH device (SPIFC) in which the interface involves a clock (SCLK), chip selection (CS), and at most 4-bit parallel data pin. SPIFC supports 1-bit, 2-bit and 4-bit data bus, configurable received data timing and variable package type. It features a 32-bit width and 8-depth of FIFO for speeding up SPI signal processing. The format of SPIFC is depicted as follows:



SIOx: x= 1,2,4 IO

6.9.5. UART

The universal asynchronous receiver transmitter (UART) supports half-duplex, asynchronous communication, and wide range of baud rates determined by baud rate generator. User can program the word length of data (8 or 9 bits), and configure the stop bits (1 or 2 stop bits) as well as control parity. The format of UART frame is shown as follows:

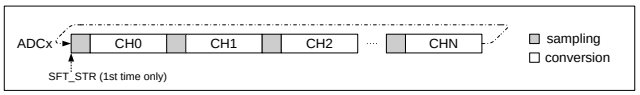


6.9.6. IR TX

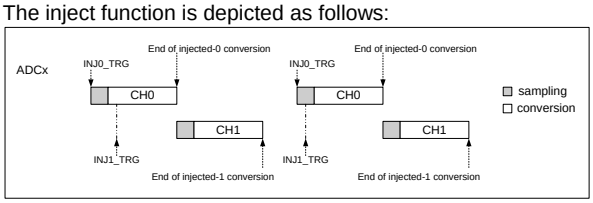
The IR TX function supports seven trigger sources for IR clock, configurable mask, pole, and duty control.

6.10 SAR ADC Controller

The 12-bit SAR ADC has up to 10 multiplexed channels, allowing it to measure signals from eight external and two internal sources (V15 or VSS_ADC). The functionally of A/D conversion can be performed in single, regular, regular scan, and injected conversion mode. The result of the conversion data is stored in a data register and can trigger DMA function. The regular scan function is as follows:



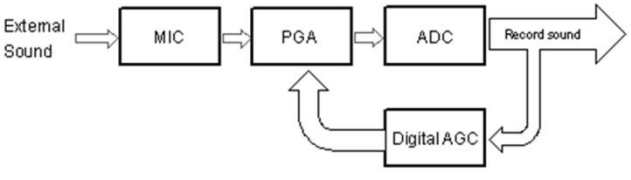
The inject function is depicted as follows:



User can also set data with left or right alignment. SAR ADC controller supports analog watchdog function. It allows the application to detect whether the input-voltage is beyond the user-defined range. If it is determined out of user-defined range, an interrupt will be generated for CPU.

6.11 SDM ADC Controller

A 16-bit resolution SDM ADC (Sigma-Delta Modulation ADC) with DAGC (Digital Audio Gain Control) is embedded in GPCM1F. When peak or RMS of record sound is larger than the threshold value, the digital AGC will start activating followed by lower down PGA gain. The block diagram is shown as follows:



The SDM ADC supports auto-mute and MIC wakeup function. The MIC wakeup function is to detect MIC IN voltage and accumulate MIC IN value in deep-sleep mode. When the accumulated value exceeds the value of threshold, SDM ADC controller will issue a wakeup IRQ to wake CPU up. When the ADC data conversion is finished, it will be stored in data register and acknowledge DMA to obtain the data.

6.12 DAC Controller

GPCM1F audio can be exported to the 12-bit DAC or 16-bit AUDPWM. DAC Controller supports two input channels data port, new 4 x up-sampling function, and DMA data. User is allowed sending the various data into different channels and thus, IC will perform the mix operation before DAC conversion. Audio PWM can support digital gain control and auto-mute function.

7 ELECTRICAL SPECIFICATION

7.1 Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	VDD_REGIN/VDD_IO	<= 5.5V	V
VREG_OUT 0	VDD15	<=1.75V	V
VREG_OUT 1	V33_ADC	<=3.6V	V
VREG_OUT 2	V33_REGO	<=3.6V	V
Input Voltage For IOA	VDD_IO	<=5.5V	V
Input Voltage For IOB	VDD_REGO	<=3.6V	V
Operating Temperature	T_A	-40~85	℃

7.2 DC Characteristics (VDD_REGIN/VDD_IO = 3.3V, VDD_REGO= 3.3V, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REGIN/ VDD_IO	2.2	-	5.5	V	-
Operating Current	I_{OP}	-	13	15	mA	F_{OSC} = 81.92MHz, AD and DAC are disabled, without loading.
Standby Current	I_{STB}	-	10	12	μA	In deep-sleep mode, all clocks are off.
			13	15	μA	In halt mode, 32KHz is enabled and PLL (F_{OSC}) is disabled.
Input High Level	V_{IH}	$0.7VDD_{IOA}$ $0.7VDD_{IOB}$	-	-	V	-
Input Low Level	V_{IL}	-	-	$0.3VDD_{IOA}$ $0.3VDD_{IOB}$	V	-
PAD IOA GROUP						
Output High Current	I_{OH}	8	-	32	mA	V_{OH} =0.7VDD_IO
Output Low Current	I_{OL}	8	-	32	mA	V_{OL} =0.3VDD_IO
Input Pull-Low Register	R_{PL}	30	50	70	KΩ	V_{IN} =VDD_IO
Input Pull-High Register	R_{PH}	30	50	70	KΩ	V_{IN} =VSS
PAD IOB GROUP						
Output High Current	I_{OH}	4	-	16	mA	V_{OH} =0.7V33_REGO
Output Low Current	I_{OL}	4	-	16	mA	V_{OL} =0.3V33_REGO
Input Pull-Low Register	R_{PL}	30	50	70	KΩ	V_{IN} =V33_REGO
Input Pull-High Register	R_{PH}	30	50	70	KΩ	V_{IN} =VSS
Internal ROSC frequency deviation	⊿F/F	-2%	8.192M	+2%	HZ	-

7.3 DC Characteristics (VDD_REGIN/VDD_IO = 4.5V, VDD_REGO= 3.3V, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REGIN/ VDD_IO	2.2	-	5.5	V	-

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{OP}	-	15	-	mA	F_{OSC} = 81.92MHz, AD and DAC are disabled. without loading.
Standby Current	I_{STB}	-	12	-	μA	In Deep-Sleep mode, All clock OFF
			15	-	μA	In Halt mode, 32KHz is enabled and PLL(F_{OSC}) is disabled.
Input High Level	V_{IH}	$0.7VDD_{IOA}$ $0.7VDD_{IOB}$	-	-	V	-
Input Low Level	V_{IL}	-	-	$0.3VDD_{IOA}$ $0.3VDD_{IOB}$	V	-
PAD IOA GROUP						
Output High Current	I_{OH}	4	-	16	mA	V_{OH} =0.7VDD_IO
Output Low Current	I_{OL}	4	-	16	mA	V_{OL} =0.3VDD_IO
Input Pull-Low Register	R_{PL}	30	50	70	KΩ	V_{IN} =VDD_IO
Input Pull-High Register	R_{PH}	30	50	70	KΩ	V_{IN} =VSS
PAD IOB GROUP						
Output High Current	I_{OH}	4	-	16	mA	V_{OH} =0.7V33_REGO
Output Low Current	I_{OL}	4	-	16	mA	V_{OL} =0.3V33_REGO
Input Pull-Low Register	R_{PL}	30	50	70	KΩ	V_{IN} =V33_REGO
Input Pull-High Register	R_{PH}	30	50	70	KΩ	V_{IN} =VSS
Internal ROSC frequency deviation	⊿F/F	-2%	8.192M	+2%	HZ	-

7.4 Regulator Characteristics

REG15_LVR_BVD

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Input Voltage	VDD_IO	2.2	-	5.5	V
Maximum Current Output	Ivdd15	-	-	20	mA
Output Voltage	VDD15	1.38	1.55	1.65	V

Note: For IC use only. Users are not allowed using it.

REG33_ADC_SPI

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Input Voltage	VDD_REGIN	2.5	-	5.5	V
V33_ADC					
Maximum Current Output for V33_ADC	Iv33_adc	-	-	10	mA
Output Voltage	V33_ADC	2.5	3.3	3.6	V
V33_REGO					
Maximum Current Output for V33_REGO	V33_REGO	-	-	30	mA
Output Voltage		2.5	3.3	3.6	V

7.5 16-Bit CODEC ADC Characteristics (V33_ADC = 3.0V, TA = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
ADC Microphone Input Voltage Range	VINMIC	VSS	-	V33_ADC	V
Resolution of ADC	RESO	-	-	16	bits
Signal to noise ratio(SNR) Boost gain = 0dB, PGA = 0 dB	SINAD	-	81	-	dB
Dynamic range Boost gain = 0 dB, PGA = 0 dB	DR	-	80	-	dB
Total harmonic distortion + noise Boost gain = 0 dB, PGA = 0 dB	THD+N	-	-76	-	dB
Total harmonic distortion + noise Boost gain = 21 dB, PGA = 0 dB	THD+N	-	-65	-	dB

7.6 12-Bit SAR ADC Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SAR ADC Input Voltage Range from IOA[24 :17]	VINIOAx	0	-	VDD_IO	V
Resolution of ADC	RESO	-	-	12-	bits
Integral Non-Linearity of ADC	INL	±5	±3	-	LSB
Differential Non-Linearity of ADC	DNL	±2	±1	-	LSB
ENOB	ENOB	9	9.3	-	bits
No Missing Code		9	10	-	Bits
AD Conversion Rate=ADCCLK/16	F_{CONV}	-	-	200K	Hz

7.7 Audio PWM Characteristics (PVDD =4.5V, R_L=8Ω, f=1KHz, TA=25℃)

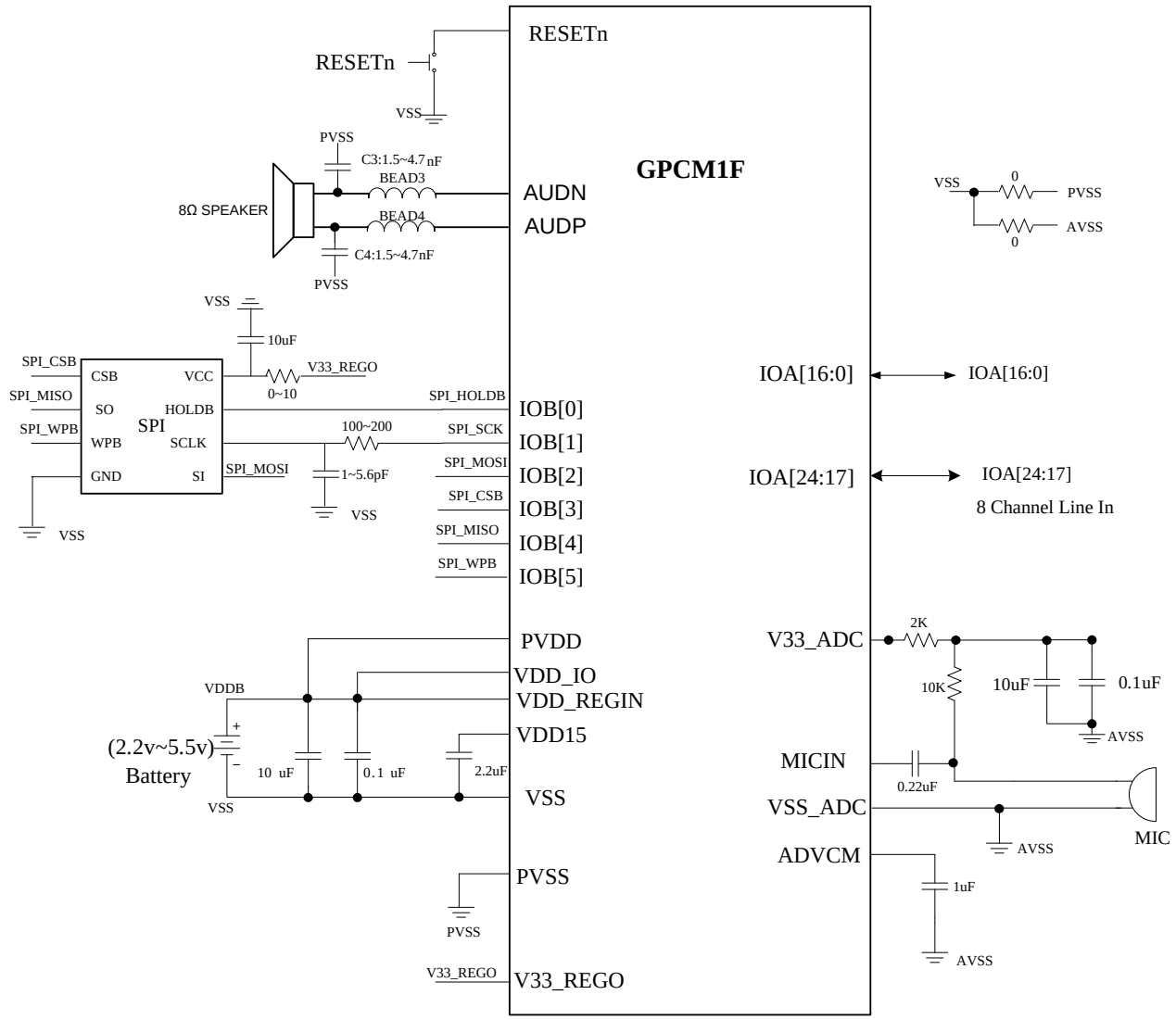
Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	16	bit
THD+n(4.5V@0.4W)	-	-	1	-	%
Noise at No Signal	-	-	-100	-	dBr A
Dynamic Range (-60dB)	-	-	-80	-	dBr A

7.8 Current DAC Characteristics(PVDD =4.5V, R_L=8Ω, f=1KHz, TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Operating Voltage	V50	2.5V	-	5.5V	V
Resolution		-	-	12	bit
Sample frequency		-	-	400	KHz
THD＋N		-	-58	-	dB
INL		-	±5	-	dB
Dynamic range		-	70	-	dB
Noise at no signal		-	-70	-	dB

8 APPLICATION CIRCUITS

8.1 Application Circuit with Internal 8.192MHz Oscillator and Internal 32768Hz Oscillator

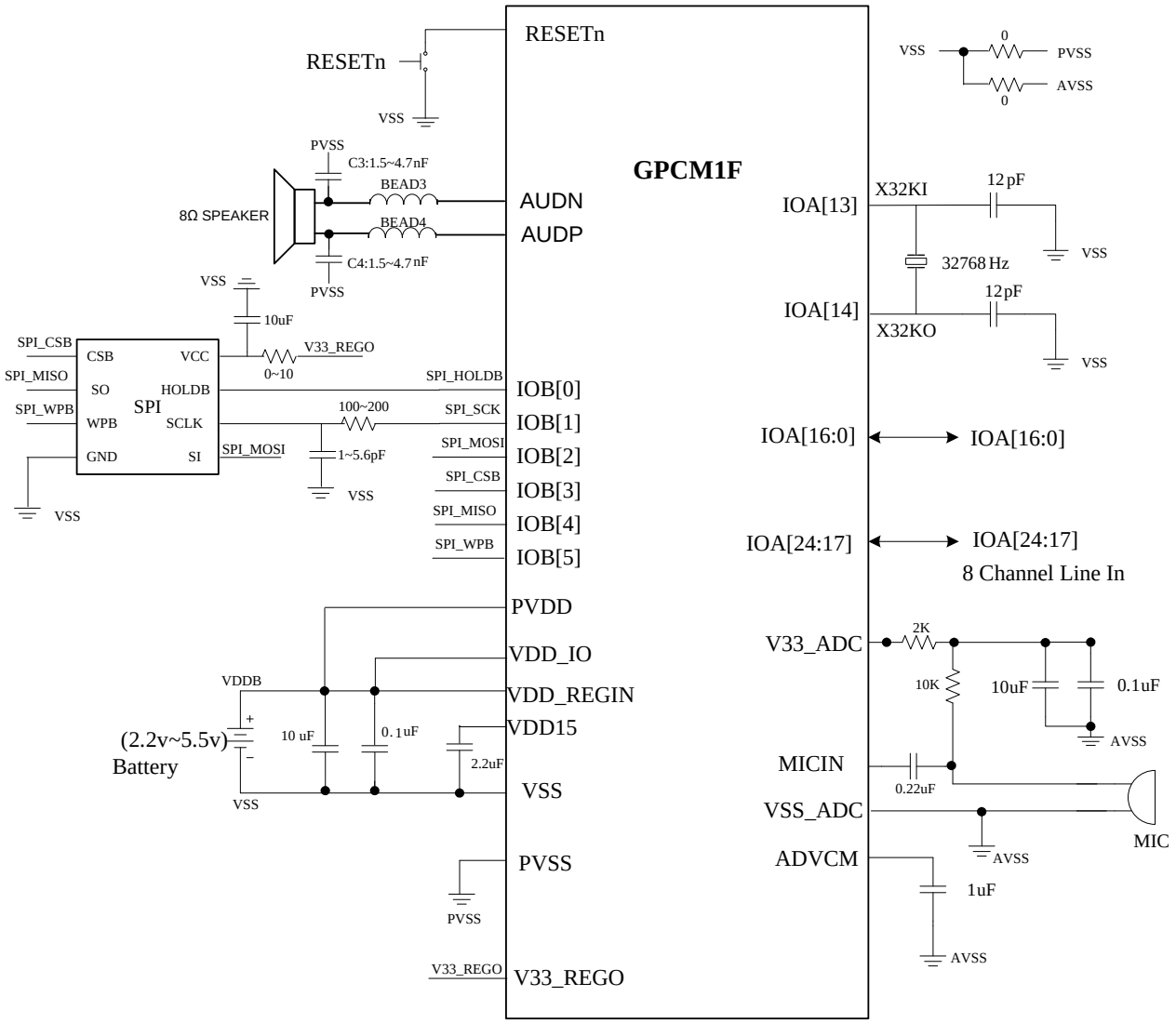


Note*1: Bead3/4 are optional for EMI sensitive application.—Bead3/4 should be located as close as possible to AUDP/AUDN/PVSS.

Note*2: The typical value of C3/4 is 1.5nF, and could be modified in different loadings. C4/5 should be located as close as possible to AUDP/AUDN/PVSS.

Note*3: To obtain a clearer sound quality for MIC ADC, the power source VSS (e.g. battery) is recommended being an independent path connecting with AVSS (VSS_ADC). This PCB layout approach is capable of reducing MIC's background noise significantly.

8.2 Application Circuit with Internal 8.192MHz Oscillator and External 32768Hz Crystal

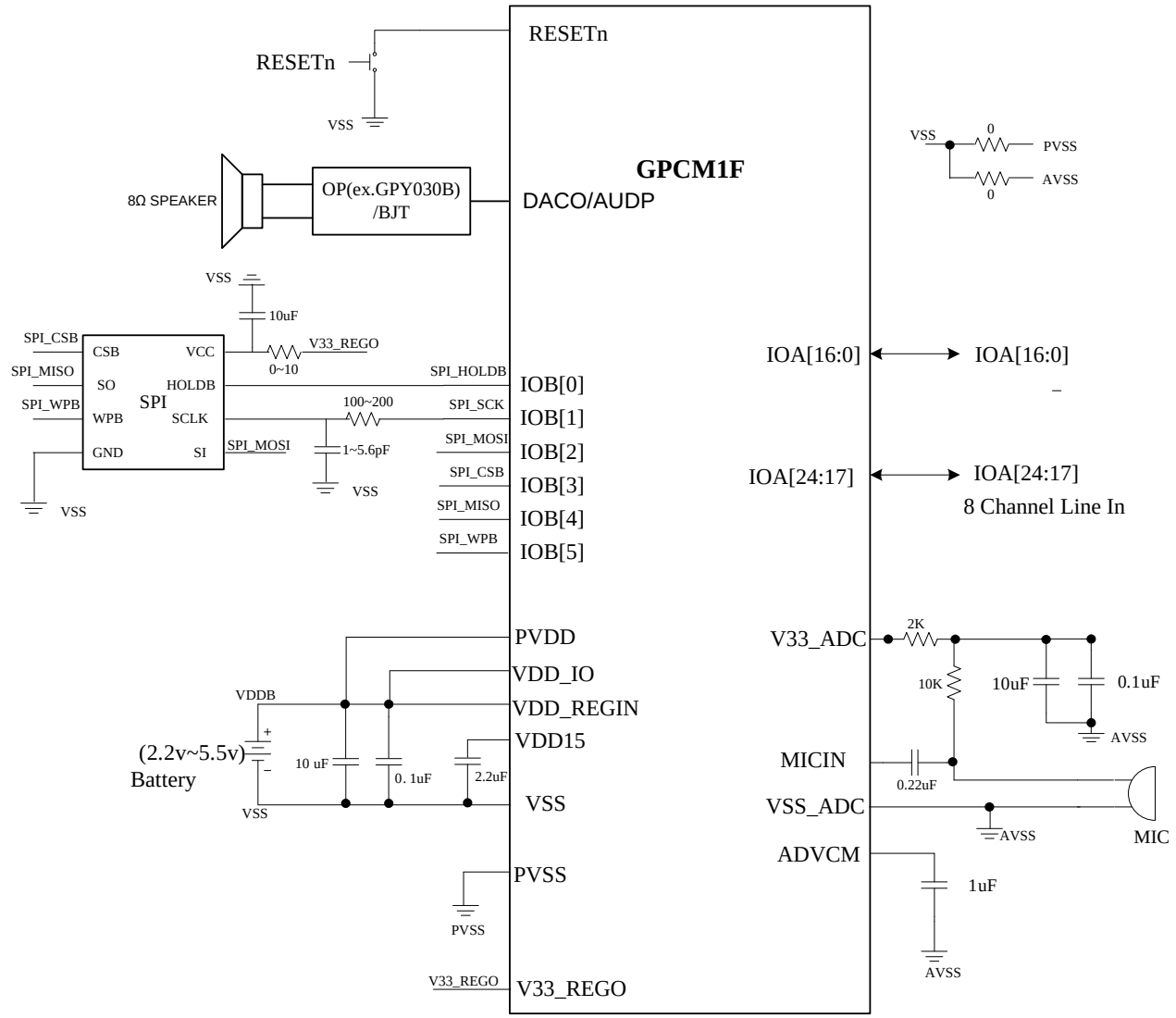


Note*1: Bead3/4 are optional for EMI sensitive application. Bead3/4 should be located as close as possible to AUDP/AUDN/PVSS.

Note*2: The typical value of C3/4 is 1.5nF, and could be modified in different loadings. **C4/5 should be located as close as possible to AUDP/AUDN/PVSS.**

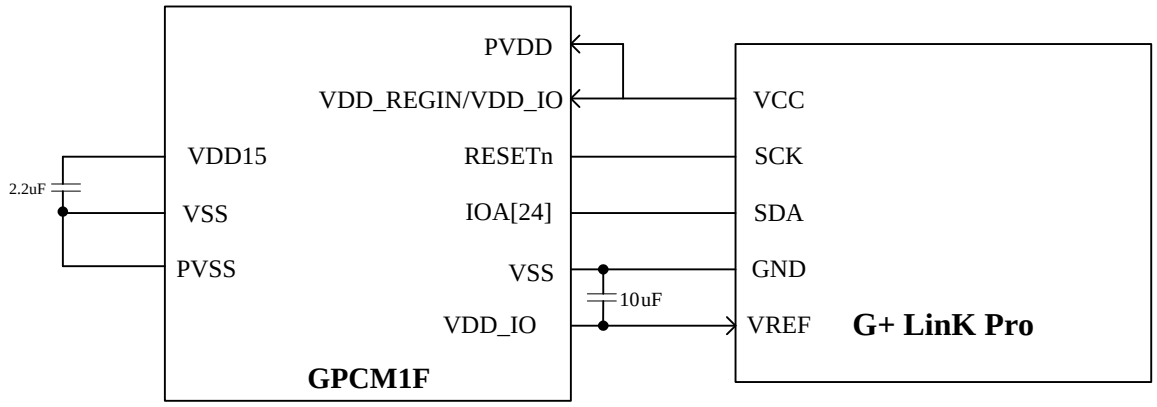
Note*3: To obtain a clearer sound quality for MIC ADC, the power source VSS (e.g. battery) is recommended being an independent path connecting with AVSS (VSS_ADC). This PCB layout approach is capable of reducing MIC's background noise significantly.

8.3 Application Circuit with Internal 8.192MHz Oscillator and Current DAC

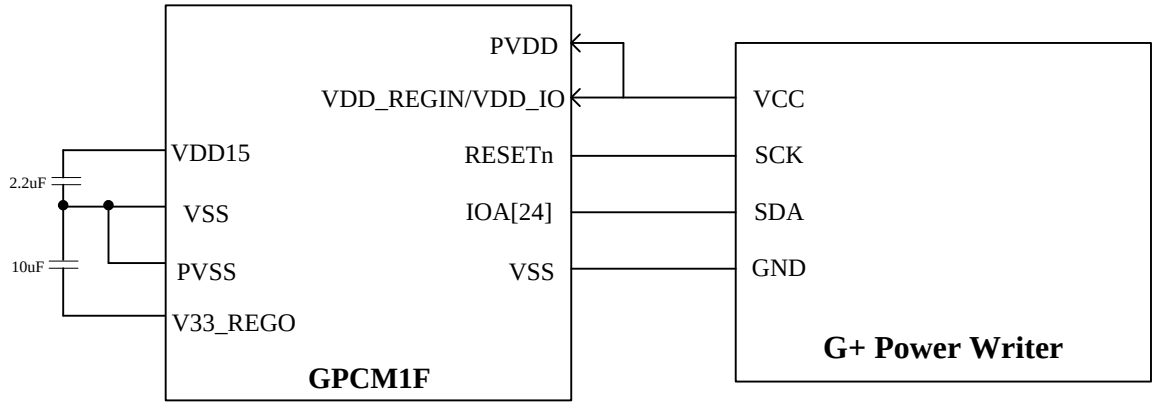


Note*1: To obtain a clearer sound quality for MIC ADC, the power source VSS (e.g. battery) is recommended being an independent path connecting with AVSS (VSS_ADC). This PCB layout approach is capable of reducing MIC's background noise significantly.

8.4 Embedded FLASH write with G+ Link



8.5 Embedded FLASH write with G+ Power Writer



9 PACKAGE/PAD LOCATION

9.1 Ordering Information

Body	Product Number	Package Type
GPCM1F064A	GPCM1F064A-NnnV-C	Chip form
	GPCM1F064A-NnnV-QL231	Green Package – LQFP48
GPCM1F064B	GPCM1F064B-NnnV-C	Chip form
	GPCM1F064B-NnnV-QL231	Green Package – LQFP48
GPCM1F064A_0001	GPCM1F064A_0001-NnnV-C	Chip form
	GPCM1F064A_0001-NnnV-QL231	Green Package – LQFP48
GPCM1F064B_0001	GPCM1F064B_0001-NnnV-C	Chip form
	GPCM1F064B_0001-NnnV-QL231	Green Package – LQFP48
GPCM1FV000A	GPCM1FV000A-NnnV-C	Chip form
	GPCM1FV000A-NnnV-QL231	Green Package – LQFP48

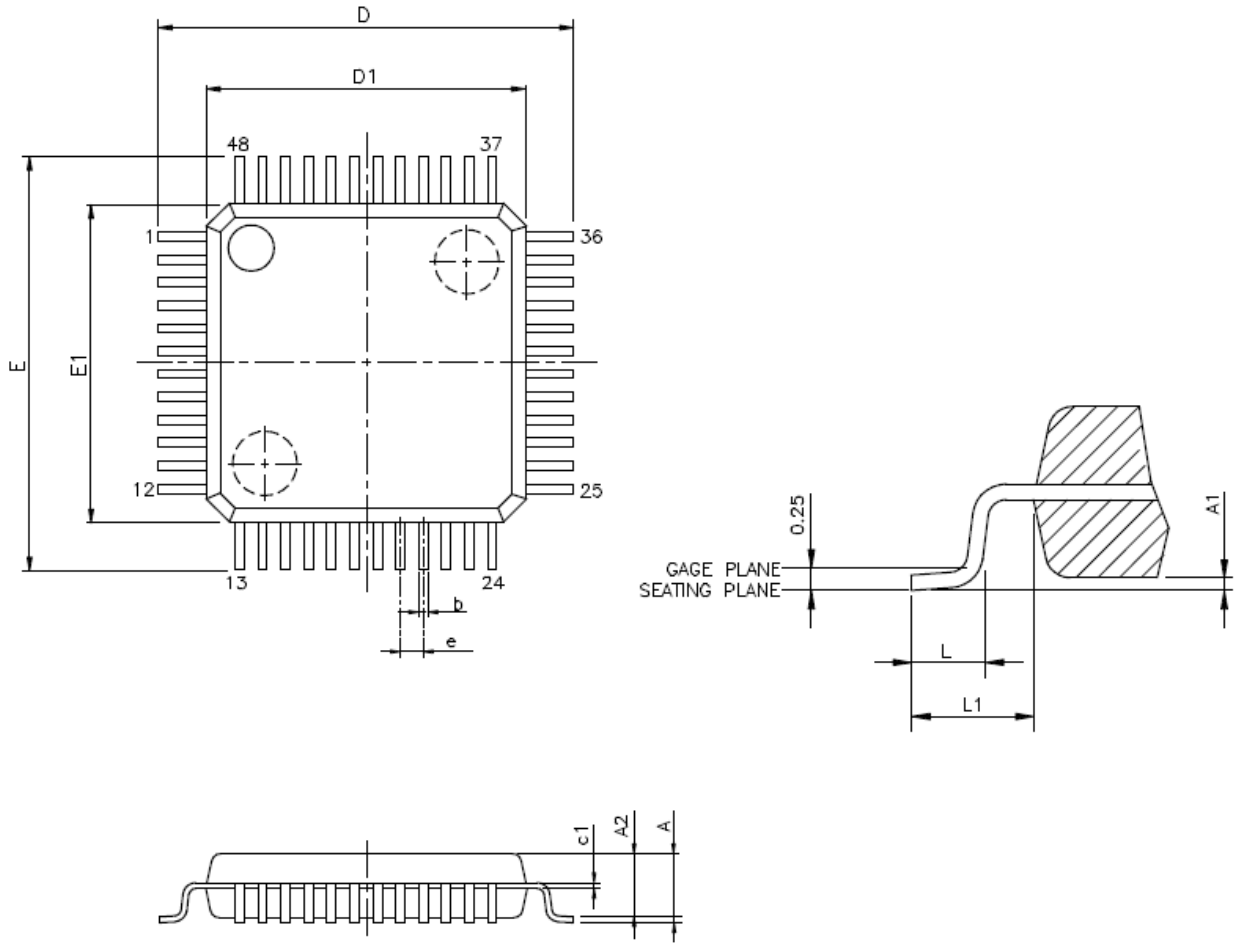
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2 Package Information

LQFP48 Outline Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1.JEDEC OUTLINE:MS-026 BBC

2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

10 DISCLAIMER

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11 REVISION HISTORY

Date	Revision #	Description	Page
Aug. 26, 2022	1.5	1. REG15_LVR_BVD Characteristic correct 2. Add SPI application circuit and AUDP/AUDN application circuit correct	16 18,19,20
Sep. 10, 2021	1.4	1. Analog peripherals description 2. Signal description 3. I/O Port description 4. 7.2/7.3 DC Characteristics description 5. Application Circuits correct 6. Ordering Information correct	4 7,8 11 15,16 18,19,20 22
Oct.06, 2020	1.3	1. GPCM1F is only 1.9V LVR levels available. 2. VDD15 Max/TYP/MIN Value	11 16
Apr. 17, 2020	1.2	1. IOA22--> NC ,NC--> IOA24 2. OP Current / Standby Current 3. Application Circuit Reset Pin not connect Cap 4. Ordering Information	10 15 18-20 22
Feb. 14, 2020	1.1	1. REG15 Out 2. Application Circuit add Bead 1/2/3/4 For EMI	
Dec. 30, 2019	1.0	1. Redefine IO Name 2. Correct electric space error	
Oct. 04, 2019	0.1	Original	24