DATA SHEET

GPCM3 Series

ARM® Cortex®-M0 32-bit Sound Controller

Feb. 06, 2025

Version 1.4

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32-BIT SOUND CONTROLLER

1 GPCM3 SERIES

The following table briefly introduces GPCM3's basic features.

Item	GPCM300A	GPCM300B
Microprocessor	ARM Cortex-M0	ARM Cortex-M0
System Clock	Max. 122.88MHz	Max. 122.88MHz
Operating Voltage	2.0V - 5.5V	2.0V - 5.5V
Regulator Out (Body Option)	3.0~3.3V, ~30mA	3.0~3.3V, ~30mA
Internal RAM Size	32KB+ 8KB cache	16KB+ 8KB cache
GPIO Numbers	37+6*[1]	21+6*[1]
ADC LINE-IN	8 Channels	8 Channels
Execute External Program	V	V
SPU	32-CH	--
DAC/PWM	DACx2 or PWM	DACx2 or PWM
USB1.1 / USB2.0 Full Speed	V	--
ICE/ Writer IF	V	V

Note1：IOB[5:0], total of six IOs can be connected to SPIFC I/F.

2 GENERAL DESCRIPTION

The industrial microcontroller of GPCM3 series equips ARM® Cortex®-M0 processor core and 32-channel sound process unit (SPU), operating at a frequency of up to 122.88MHz. The GPCM3 series is applicable for the applications of digital sound processing and voice recognition, etc.

3 FEATURE

- **CPU**
  - CPU Core
    - ARM® Cortex®-M0 32-bit CPU (122.88MHz max) with Code Fetch Accelerator
    - Nested Vectored Interrupt Controller (NVIC) with 32 interrupt sources
    - 24-bit SysTick timer
    - Single cycle 32-bit multiplier instruction
- **32-channel SPU**
- **Memory**
  - Max. 32K-byte SRAM and 8K-byte Cache RAM
  - running SPI external code and data in auto mode
- **Clock Management**
  - Internal 12.288MHz oscillator and XTAL 12M crystal
  - Phase Lock Loop with configurable output frequency: 122.88M Hz (max)
  - Internal 32768Hz oscillator and XTAL 32768Hz crystal
- **Power Management**
  - In Shutdown mode: Core power and all clocks are stopped
  - In Deep Sleep mode: CPU clocks off, system entering deep sleep mode ,and all clock off
  - In Halt mode: CPU clocks off, system entering deep sleep mode, and only 32768Hz clock on.
  - In Sleep mode: Only CPU Clock off
  - Regulator with configurable output SPI Voltage and Codec voltage
  - Battery Voltage Detection
- **Reset Management**
  - Power On Reset
  - Low Voltage Reset
  - Watchdog Timeout Reset
  - PAD(H/W Key)Reset
  - S/W Reset
- **Analog peripherals**
  - 16-bit Audio PWM
  - 16-bit DAC x 2
  - 16-bit Sigma Delta Codec ADC(MIC ADC)
  - 12-bit SAR ADC and 8 x line-in PADs
  - CTS(Capacitor sensing touch) supporting 32 x Touch IO PADs
- **I/O Ports**

- Max. 43 (include SPIFC) multifunction and bi-direction I/Os
  - I/O ports with pull-up resistor, pull-down resistor, output high, output low or floating input, and configurable source/sink current depending on programmer's settings on the corresponding registers
- IOA can be set External Key for CPU wakeup.

■ **System Control**
- Five-channel DMA controller
- System Management Unit (SMU) for system configuration and control
- HW 16x16 MAC for accumulator
- HW 32x16 MAC function
- HW 32/32 Divider function
- Two quadrature decoders

■ **Timer**
- Three general-purpose 16-bit timers/counters
- Two 16-bit touch sensing timers for CTS
- Two 16-bit CCP timers(Capture/Compare/PWM) Units and 16 PWMIOs
  All of them can be used as general- purpose timers.

■ **Communication peripherals**
- One I2C hardware
- One I2S TX and I2S RX.
- One SPIFC (SPI controller for FLASH device access) and two SPI serial interface I/Os
- Two UART hardware
- One IR TX hardware

■ **SAR ADC Controller**
- 12-bit resolution SAR ADC and 10-channel selection (8*LINE-IN, VDD12 and VDD_IO/4)
- Supporting single, regular and regular scan conversion mode
- Data alignment with left-aligned and right-aligned
- External trigger option for injected conversion
- Analog detection watchdog
- DMA request generation during channel conversion

■ **PDM**
- Pulse-density modulation MES MIC

■ **SDM ADC Controller(MIC ADC)**
- 16-bit resolution Sigma-Delta Modulation ADC (SDM ADC) with Digital Audio gain control(DAGC)
- DMA request generation during ADC conversion

■ **DAC Controller**
- Supporting two input channel and 4x Up-Sampling
- Supporting scale/truncation mode when data saturation
- DMA request generation during DAC data done
- Output to 16-bit Audio PWM or 16-bit DAC
- Audio PWM support digital gain control and auto mute control

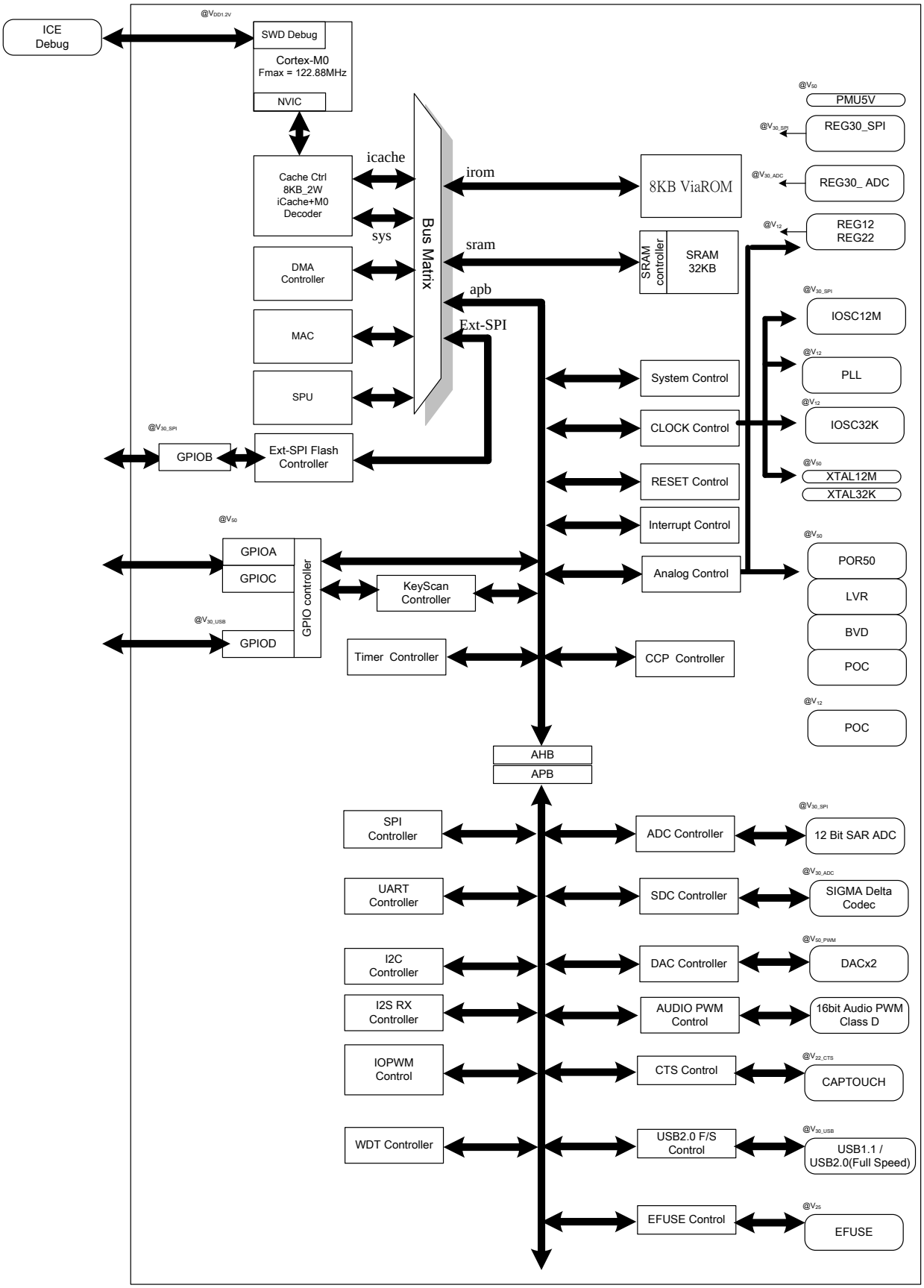
■ **USB Device Controller**
- Supports USB1.1 / USB2.0(full speed) compliant device with built-in transceiver

■ **Debug System**
- ARM serial wire debug (SWD)
- Supporting up to three hardware breakpoints

■ **Operation Temperature**
- -40°C to 85°C

■ **Package**
- LQFP64

4 BLOCK DIAGRAM



5 SIGNAL DESCRIPTION

5.1 GPCM300A pin description

P = Power Pin, G = Ground Pin, A = Analog Pin

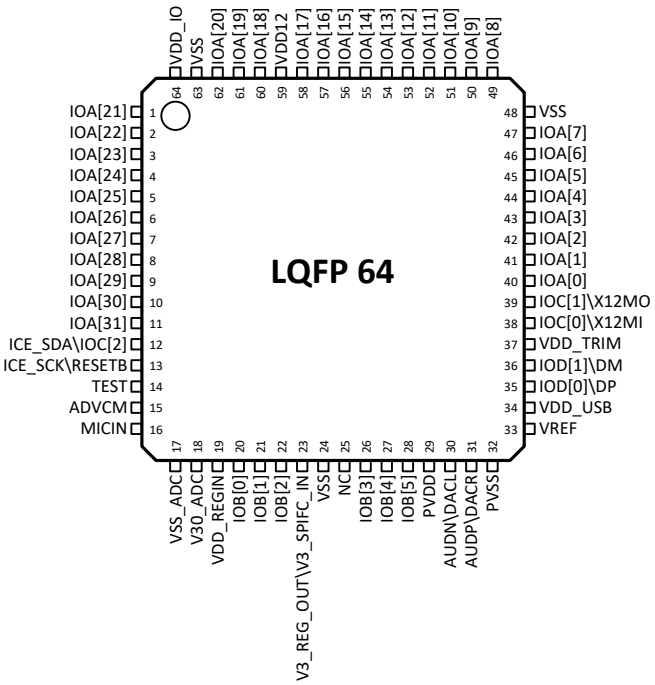
I/O = Bidirectional Pin, I = Input, O= Output

Pin Name	Type	GROUP	Description
IOA[25]	I/O	IOA	General purpose I/O Port IOA25 or SAR ADC Line In PAD
IOA[26]	I/O	IOA	General purpose I/O Port IOA26 or SAR ADC Line In PAD
IOA[27]	I/O	IOA	General purpose I/O Port IOA27 or SAR ADC Line In PAD
IOA[28]	I/O	IOA	General purpose I/O Port IOA28 or SAR ADC Line In PAD
IOA[29]	I/O	IOA	General purpose I/O Port IOA29 or SAR ADC Line In PAD
IOA[30]	I/O	IOA	General purpose I/O Port IOA30 or SAR ADC Line In PAD
IOA[31]	I/O	IOA	General purpose I/O Port IOA31 or SAR ADC Line In PAD
VSS	G	GND	Ground
IOC[2] / ICE_SDA	I/O	ICE	General purpose I/O Port IOC2 or ICE and Power writer SDA pin
RESETB / ICE_SCK	I	ICE	Reset pin(Low active) or ICE and Power writer SCK pin function
TEST	I	TEST	Test PIN
ADVCM	AO	ADC	Common voltage(1/2*VDD) for amplifier and ADC
MICIN	AI	ADC	Microphone input
VSS_ADC	G	ADC	CODEC ADC Ground
V3_ADC	P	ADC	V3_ADC can supply 3.0V or 3.3V power output. Connect 2.2uF capacitance to VSS_ADC. Power for CODEC ADC.
VDD_REGIN2	P	VDD_REGIN	VDD5 Power as Internal CODEC ADC regulators power input pin
VDD_REGIN1	P	VDD_REGIN	VDD5 Power as Internal V3_REG regulators power input pin
IOB[0]	I/O	IOB/SPI FC	General purpose I/O Port IOB0 & SPIFC pin
IOB[1]	I/O	IOB/SPI FC	General purpose I/O Port IOB1 & SPIFC SCK pin
IOB[2]	I/O	IOB/SPI FC	General purpose I/O Port IOB2 & SPIFC pin
V3_REG_OUT	P	V3_REGO	V3_REG output pin can supply 3.0V or 3.3V and max output current 30mA Power for SAR ADC and IOSC12M
V3_SPIFC_IN	P	V3_REGO	V3 power in, connect to V3_REG_OUT Power for SPIFC IO
VSS	G	GND	Ground
IOB[3]	I/O	IOB/SPI FC	General purpose I/O Port IOB3 & SPIFC pin
IOB[4]	I/O	IOB/SPI FC	General purpose I/O Port IOB4 & SPIFC pin
IOB[5]	I/O	IOB/SPI FC	General purpose I/O Port IOB5 & SPIFC pin
VSS_SPI	G	GND	Ground
PVDD	P	DAC_PWM	DAC_PWM VDD 5V power input pin
AUDN / DACL	AO	DAC_PWM	Audio PWM AUDN or DACL output
AUDP / DACR	AO	DAC_PWM	Audio PWM AUDP or DACR output
PVSS	G	DAC_PWM	Audio PWM Ground
PVSS	G	DAC_PWM	Audio PWM Ground
VREF	CAP	DAC_PWM	Connect external cap for DAC
VDD_USB	P	USB	USB power input
DP / IOD[0]	I/O	USB	General purpose I/O Port IOD0 share with USB DP
DUMMY	PAD	DUMMY	DUMMY pad

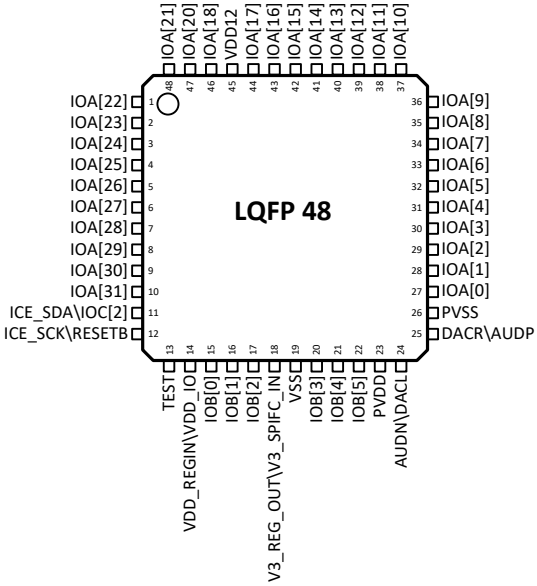
Pin Name	Type	GROUP	Description
DM / IOD[1]	I/O	USB	General purpose I/O Port IOD1 share with USB DM
VSS_USB	G	USB	USB ground
VDD_TRIM	N/C	EFUSE	Pad for efuse trimming (for internal use only)
VSS	G	GND	Ground
X12MI / IOC[0]	AI/IO	X12M	General purpose I/O Port IOC0 share with X12MI
X12MO / IOC[1]	AO/IO	X12M	General purpose I/O Port IOC0 share with X12MO
IOA[0]	I/O	IOA	General purpose I/O Port IOA0
IOA[1]	I/O	IOA	General purpose I/O Port IOA1
IOA[2]	I/O	IOA	General purpose I/O Port IOA2
IOA[3]	I/O	IOA	General purpose I/O Port IOA3
IOA[4]	I/O	IOA	General purpose I/O Port IOA4
IOA[5]	I/O	IOA	General purpose I/O Port IOA5
IOA[6]	I/O	IOA	General purpose I/O Port IOA6
IOA[7]	AI/IO	X32KI	General purpose I/O Port IOA7 or Crystal 32K PAD In
VSS	G	GND	Ground
IOA[8]	AO/IO	X32KO	General purpose I/O Port IOA8 or Crystal 32K PAD Out
IOA[9]	I/O	IOA	General purpose I/O Port IOA9
IOA[10]	I/O	IOA	General purpose I/O Port IOA10
IOA[11]	I/O	IOA	General purpose I/O Port IOA11
IOA[12]	I/O	IOA	General purpose I/O Port IOA12
IOA[13]	AI/IO	IOA	General purpose I/O Port IOA13
IOA[14]	AO/IO	IOA	General purpose I/O Port IOA14
IOA[15]	I/O	IOA	General purpose I/O Port IOA15
IOA[16]	I/O	IOA	General purpose I/O Port IOA16
IOA[17]	I/O	IOA	General purpose I/O Port IOA17
VDD12	P	VDD12	Core Power
IOA[18]	I/O	IOA	General purpose I/O Port IOA18
IOA[19]	I/O	IOA	General purpose I/O Port IOA19
IOA[20]	I/O	IOA	General purpose I/O Port IOA20
VSS	G	GND	Ground
VDD_IO	P	VDD_IO	VDD5 Power as Core REG_IN & VDDIOA power input pin
IOA[21]	I/O	IOA	General purpose I/O Port IOA21
IOA[22]	I/O	IOA	General purpose I/O Port IOA22
IOA[23]	I/O	IOA	General purpose I/O Port IOA23
IOA[24]	I/O	IOA	General purpose I/O Port IOA24 or SAR ADC Line In PAD

Note1: Please DON'T bond DUMMY, TEST and NC pin.

5.1.1 GPCM300A LQFP64 Package



5.1.2 GPCM300A LQFP48 Package



5.2 GPCM300B pin description

P = Power Pin, G = Ground Pin, A = Analog Pin

I/O = Bidirectional Pin, I = Input, O= Output

Pin Name	Type	GROUP	Description
IOA[25]	I/O	IOA	General purpose I/O Port IOA25 or SAR ADC Line In PAD
IOA[27]	I/O	IOA	General purpose I/O Port IOA27 or SAR ADC Line In PAD
IOA[30]	I/O	IOA	General purpose I/O Port IOA30 or SAR ADC Line In PAD
IOA[31]	I/O	IOA	General purpose I/O Port IOA31 or SAR ADC Line In PAD
VSS	G	GND	Ground
IOC[2] / ICE_SDA	I/O	ICE	General purpose I/O Port IOC2 or ICE and Power writer SDA pin
RESETB / ICE_SCK	I	ICE	Reset pin(Low active) or ICE and Power writer SCK pin function
TEST	I	TEST	Test PIN
ADVCM	AO	ADC	Common voltage(1/2*VDD) for amplifier and ADC
MICIN	AI	ADC	Microphone input
VSS_ADC	G	ADC	CODEC ADC Ground
V3_ADC	P	ADC	V3_ADC can supply 3.0V or 3.3V power output. Connect 2.2uF capacitance to VSS_ADC. Power for CODEC ADC.
VDD_REGIN2	P	VDD_REGIN	VDD5 Power as Internal CODEC ADC regulators power input pin
VDD_REGIN1	P	VDD_REGIN	VDD5 Power as Internal V3_REG regulators power input pin
IOB[0]	I/O	IOB/SPI FC	General purpose I/O Port IOB0 & SPIFC pin
IOB[1]	I/O	IOB/SPI FC	General purpose I/O Port IOB1 & SPIFC SCK pin
IOB[2]	I/O	IOB/SPI FC	General purpose I/O Port IOB2 & SPIFC pin
V3_REG_OUT	P	V3_REGO	V3_REG output pin can supply 3.0V or 3.3V and max output current 30mA Power for SAR ADC and IOSC12M
V3_SPIFC_IN	P	V3_REGO	V3 power in, connect to V3_REG_OUT Power for SPIFC IO
VSS	G	GND	Ground
IOB[3]	I/O	IOB/SPI FC	General purpose I/O Port IOB3 & SPIFC pin
IOB[4]	I/O	IOB/SPI FC	General purpose I/O Port IOB4 & SPIFC pin
IOB[5]	I/O	IOB/SPI FC	General purpose I/O Port IOB5 & SPIFC pin
VSS_SPI	G	GND	Ground
PVDD	P	DAC_PWM	DAC_PWM VDD 5V power input pin
AUDN / DACL	AO	DAC_PWM	Audio PWM AUDN or DACL output
AUDP / DACR	AO	DAC_PWM	Audio PWM AUDP or DACR output
PVSS	G	DAC_PWM	Audio PWM Ground
PVSS	G	DAC_PWM	Audio PWM Ground
VSS	G	GND	Ground
DUMMY	PAD	DUMMY	DUMMY pad
VSS	G	GND	Ground
X12MI / IOC[0]	AI/IO	X12M	General purpose I/O Port IOC0 share with X12MI
X12MO / IOC[1]	AO/IO	X12M	General purpose I/O Port IOC0 share with X12MO
IOA[0]	I/O	IOA	General purpose I/O Port IOA0
IOA[3]	I/O	IOA	General purpose I/O Port IOA3
IOA[4]	I/O	IOA	General purpose I/O Port IOA4

Pin Name	Type	GROUP	Description
IOA[5]	I/O	IOA	General purpose I/O Port IOA5
IOA[6]	I/O	IOA	General purpose I/O Port IOA6
IOA[7]	I/O	IOA	General purpose I/O Port IOA7
VSS	G	GND	Ground
IOA[8]	I/O	IOA	General purpose I/O Port IOA8
IOA[10]	I/O	IOA	General purpose I/O Port IOA10
IOA[13]	AI/IO	X32KI	General purpose I/O Port IOA13 or Crystal 32K PAD In
VDD12	P	VDD12	Core Power
IOA[20]	I/O	IOA	General purpose I/O Port IOA20
VSS	G	GND	Ground
VDD_IO	P	VDD_IO	VDD5 Power as Core REG_IN & VDDIOA power input pin
IOA[21]	I/O	IOA	General purpose I/O Port IOA21
IOA[22]	I/O	IOA	General purpose I/O Port IOA22
IOA[23]	I/O	IOA	General purpose I/O Port IOA23
IOA[24]	I/O	IOA	General purpose I/O Port IOA24 or SAR ADC Line In PAD

Note1: Please DON'T bond DUMMY, TEST and NC pins.

6 FUNCTION DESCRIPTION

6.1 CPU

GPCM3 is equipped with a Cortex®-M0 processor, which is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

• Simple, easy-to-use program model
• Highly efficient ultra-low power operation
• Excellent code density
• Deterministic, high-performance interrupt handling
• Upward compatibility with the rest of the Cortex-M processor family.

The processor also supports a 24-bit system timer and Single cycle 32bit multiplier instruction. The interrupt include 32 IRQs (Interrupt Request) and NMI (Non-Maskable Interrupt).

6.2 Memory

6.2.1 SRAM

There is a maximum of 32K-byte working SRAM available, ranged from 0x2000_0000 through 0x2000_7FFF, and an 8K-byte dedicated cache RAM.

6.3 Clock Management

6.3.1 IOSC 12.288MHz and XTAL 12MHz

When GPCM3 powers up, Internal Oscillator(IOSC) 12.288M is the system clock. That is also used as PLL input frequency. The IOSC 12.288MHz is enabled in default. C12M clock switch to XTAL12M after boot code loaded if XTAL12M is selected as C12M clock source.

6.3.2 PLL (Phase Lock Loop)

The purpose of PLL is to pump the frequency from 12.288MHz to 122.88MHz for system clock. PLL has eight types of clock outputs available. The PLL's default frequency is 98.304MHz.

6.3.3 IOSC 32768 Hz and XTAL 32768 Hz

GPCM3 can choose one of IOSC 32768(default enable) or XTAL 32768Hz (by body) as System 32K Clock source (default IOSC32768). System 32K Clock in normal mode is the clock source for CTS, timer, and watchdog. In halt mode, only system 32K is working for power saving purpose.

6.4 Power management

GPCM3 supports three low power modes: Sleep mode, Deep Sleep mode, Halt mode, Shutdown mode. The detail description is as follows:

Mode	Entry	Wakeup	Clocks	Regulator voltage	I/O state
Sleep	WFI	Any interrupt	CPU clock off	Output voltage in normal voltage	Keep in the setting before entering low power modes
	WFE	Any event			
Deep Sleep	WFI+SLEEPDEEP=1	External input + interrupt	All clocks off All macro sleep	Output voltage to deep sleep mode voltage	
	WFE+SLEEPDEEP=1	External input + event			
Halt	WFI+SLEEPDEEP=1	External input + interrupt + RTC	Only 32K ON All macro sleep		
	WFE+SLEEPDEEP=1	External input + interrupt + RTC			
Shut down	SLEEPDEEP=1	Key Reset IOA[31:24]+IOA[7:0] | 16K TimeOut	All clocks off	Core power regulator shut off	

6.5 Reset Management

6.5.1 Power-On Reset

When IC powered ON, power on reset (PORB) will be triggered, and reset all registers.

6.5.2 Low Voltage Reset

When operation voltage drops below Low Voltage Reset (LVR) level, it will generate LVR signal to reset system. GPCM3 has 1.9V LVR level available. LVR is able to keep IC operating in normal at low voltage.

6.5.3 PAD (H/W KEY) Reset

Pad RESETn has a denounce function so that it must be kept low at least more than 200us in order to trigger Pad RESETn and reset system.

6.5.4 Watchdog timeout Reset

If watchdog function is enabled, a reset signal is generated to reset system when watchdog counter is overflow.

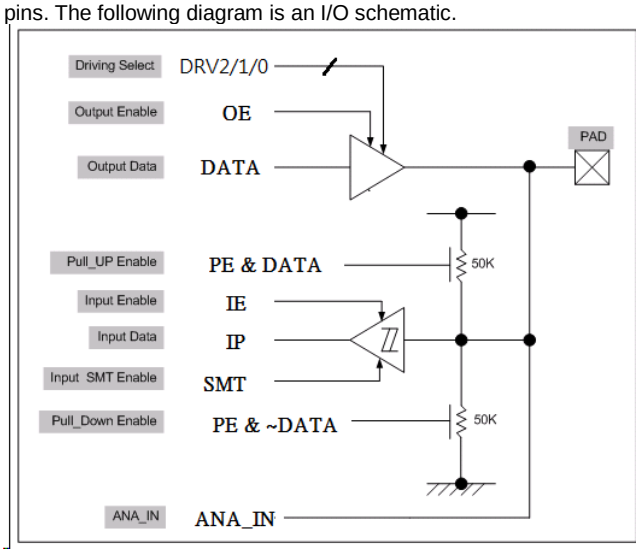
6.6 I/O port

GPCM3 provides 43x max IOs (32xIO in Port IOA, 6xIO in Port IOB, 3xIO in Port IOC and 2xIO in Port IOD). All I/Os support pull-up resistor, pull-down resistor, output high, output low or floating input, and with configurable source/sink current

IOA and IOC：8mA/16mA

IOB and IOD：2mA/4mA/6mA/8mA/10mA/12mA/14mA/16mA

determined by settings in the corresponding registers. IOA can be programed external KEY for wakeup function. IOA and IOB can be programed for bit operation. In addition to regular I/O function, all ports also provide some special functions in certain pins. The following diagram is an I/O schematic.



6.7 USB Device Function (by body)

GPCM3 series (by body) provides device function compatible with USB1.1 / USB2.0(full speed) standard. An USB transceiver is also built-in.

6.8 System Control

6.8.1 DMA

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU action. The DMA controllers have five channels, each dedicated to managing memory access requests from one or more peripherals. It has an arbiter for handling the priority between DMA requests.

6.8.2 MAC

The MAC controller is designed for accelerate the audio MAC process of 16-bit system. It supports max 16x16 MAC function, 40-bit accumulator, 8/16/32-bit saturation detection, and output auto shift function. It also supports two sets of 32x16 MAC function.

6.8.3 Divider

The divider with 32/32 is equipped to assist user get more flexible calculation.

6.8.4 Quadrature decoder

The purpose of quadrature decoder (QD) is to detect the phase differences between two square waves, normally used for rotating devices to detect the rotation velocity and position, etc. There are two sets of quadrature decoders, each comprising of two data inputs, control bits, counter and a clear port to reset the counter. User only needs to input two square waves into quadrature decoder through two input pins and starts running function.

6.9 Timers

GPCM3 is designed with seven 16-bit timers to satisfy various application needs.

6.9.1 General-purpose timers

GPCM3 provides three timers with counter mode and capture mode function. It supports as ADC/DAC trigger source, external clock source from GPIO, and capture mode with debounce filter.

6.9.2 Touch sensing timers

GPCM3 provides two timers with pre-loaded function. It can be dedicated for CTS or general timer.

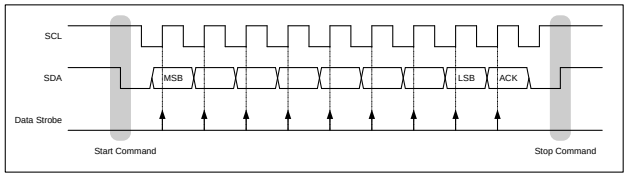
6.9.3 CCP timers

GPCM3 provides two timers with Compare, Counter, Capture and PWM Function (CCP). It supports eight-channel PWM output and ADC trigger source.

6.10 Communication Peripherals

6.10.1 I2C

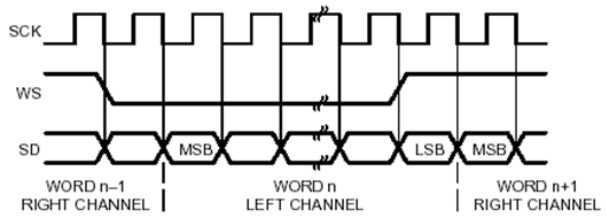
The I2C is used for attaching lower-speed peripheral ICs to processors and microcontrollers in short-distance. It supports 7-bit or 10-bit (depending on the device used) address space. Only two wires (SCK and SDA) are needed to implement the protocol. I2C controller supports four transfer modes. Four transfer modes is master transmit, master receive, slave transmit, and slave receiver. The format of I2C Frame as follows:



It also supports multi-master capability, option clock, and DMA capability.

6.10.2 I2S

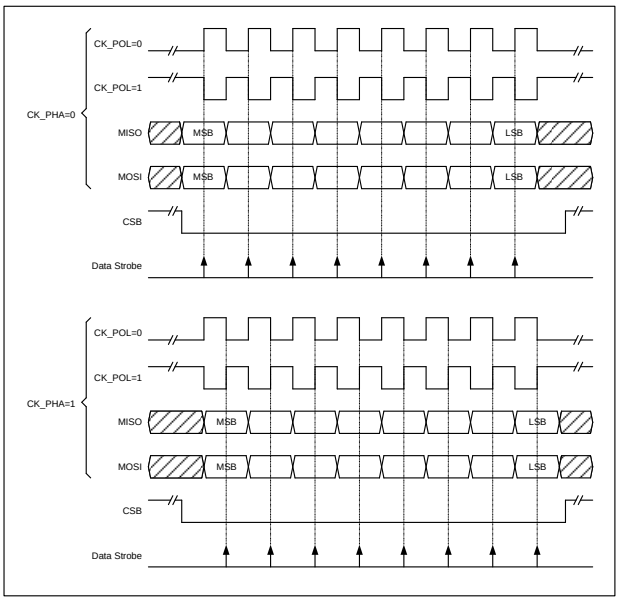
The I2S bus is a 3-line serial bus is used, consisting of a line for two time-multiplexed data channels (SD), a word selection line(WS) and a clock line(SCK). Since the transmitter and receiver have the same clock signal for data transmission, the transmitter, as a master, has to generate the bit clock, word-select signal and data. The typical format of I2S as follows:



It also supports configurable settings of each TX/RX channel for different frame sizes, word length, frame synchronization mode, data alignment, MSB/LSB first send mode, rising/falling sending edge mode, frame polarity, and the polarity of first transmitted frame.

6.10.3 SPI

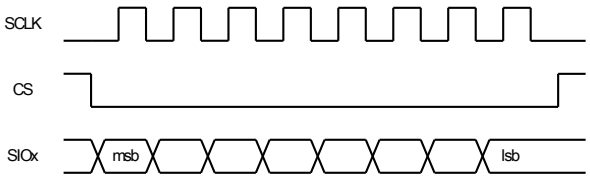
GPCM3 incorporates two Serial Peripheral Interfaces (SPI). The SPI is a synchronous serial communication interface specification used for short distance communication. It allows half/ full-duplex serial communication with external devices and only 1-bit parallel data. The format of SPI as follows:



It also supports master or slave operation, multi-master mode, programmable clock polarity and phase, and 1 byte transmission and reception with DMA.

6.10.4 SPI FC

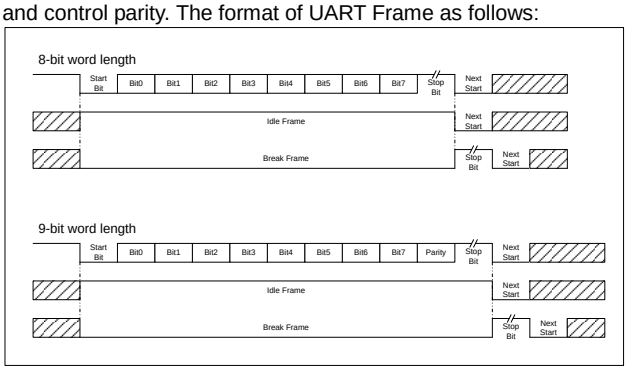
GPCM3 provides an enhanced SPI controller for FLASH device access(SPIFC). The interface includes a clock (SCLK), chip select (CS), and at most 4-bit parallel data pin. SPIFC support 1-bit, 2-bit and 4-bit data bus, configurable received data timing, and configurable variable package type. It provides with 32-bit width and 8-depth of FIFO for speeding up SPI signal processing. The format of SPIFC is depicted as follows:



SIOx: x= 1, 2, 4 IO

6.10.5 UART

The universal asynchronous receiver transmitter (UART) supports half-duplex, asynchronous communications, and wide range of baud rates by baud rate generator. User can programmable data word length (8 or 9 bits), configurable stop bits (1 or 2 stop bits), and control parity. The format of UART Frame as follows:



6.10.6 IR TX

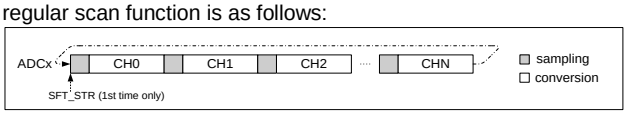
GPCM3 supports IR TX Function. It supports 7 trigger sources as IR clock, configurable mask, polarity and duty control.

6.10.7 Sound Processing Unit

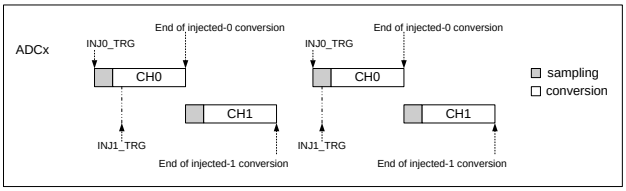
The SPU (Sound Process Unit) inside the GPCM3 series is designed to emulate various types of musical instruments via programming its tone ROM and controlling the envelope slope for each channel. Each channel can further be defined as a speech channel to produce PCM-format sound effects, e.g. percussion, animal sounds, gun, explosions accompanied with main music rhythm.

6.11 SAR ADC Controller

GPCM3 supports 12-bit SAR ADC. ADC has up to 10 multiplexed channels allowing it measure signals from 8 external and 2 internal sources (VDD12 or VDD_IO/4). The functionally of A/D conversion can be performed in single, regular, regular scan, and injected conversation mode. The result of the conversion data is stored in a data register and can trigger DMA function. The regular scan function is as follows:



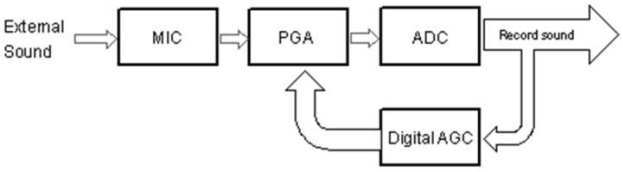
the inject function as follows:



User also can set data alignment with left-aligned or right- aligned. SAR ADC controller supports analog watchdog function. It allows the application to detect input-voltage. It is used to detect whether the input voltage is out of user-defined range. If out of range is detected, it will generate an interrupt to CPU.

6.12 SDM ADC Controller

A 16-bit resolution SDM ADC (Sigma-Delta Modulation ADC) with DAGC (Digital Audio Gain Control) is embedded in GPCM3. When peak or RMS of record sound is larger than the threshold value, the digital AGC will start to activate then lower down the PGA gain. The block diagram as follows:



The SDM ADC supports auto-mute. When the ADC conversation finish, it will store in data register and can trigger DMA function.

6.13 DAC Controller

GPCM3 audio can be exported to 2-channel 16-bit DAC or 16-bit AUDPWM. DAC Controller supports two input channels data port, new 4x up-sampling function, and DMA data in. User is allowed to send the various data into different channels and thus, IC will perform the mix operation before DAC conversion. Audio PWM can support digital gain control and auto mute function.

7 ELECTRICAL SPECIFICATION

7.1 Absolute Maximum Rating

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 5.5V
PortA/C Pad Supply Voltage	V_{IO}	< 5.5V
PortB/D Pad Supply Voltage	V_{IO}	< 3.6V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	-40℃ to +85℃
Storage Temperature	T_{STO}	-50℃ to +150℃

7.2 DC Characteristics (V5 = 3.0V, V3= 3.0V, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REGIN/ VDD_IO	2.0	-	5.5	V	-
Operating Current	I_{OP}	-	27	35	mA	F_{OSC} = 122.88MHz, AD and DAC are disabled, without loading.
Halt Current	I_{halt}	-	1	2	mA	In halt mode, 32KHz is enabled and PLL (F_{OSC}) is disabled.
Shutdown Current	I_{SD}	-	3	6	μA	Shutdown mode current with V3 and V12 off
Input High Level	V_{IH}	0.7VDD	-	-	V	SMT Enabled for IOA, IOC, IOB, IOD
Input Low Level	V_{IL}	-	-	0.3VDD	V	SMT Enabled for IOA, IOC, IOB, IOD
PAD IOA and IOC GROUP						
Output High Current	I_{OH}	4	8	12	mA	V_{OH} =0.7VDD_IO for IOA and IOC with DRV=0
		8	16	24	mA	V_{OH} =0.7VDD_IO for IOA and IOC with DRV=1
Output Low Current	I_{OL}	4	8	12	mA	V_{OL} =0.3VDD_IO for IOA and IOC with DRV=0
		8	16	24	mA	V_{OL} =0.3VDD_IO for IOA and IOC with DRV=1
Input Pull-Low Register	R_{PL}	30	50	70	KΩ	V_{IN} =VDD_IO
Input Pull-High Register	R_{PH}	30	50	70	KΩ	V_{IN} =VSS
PAD IOB and IOD GROUP						
Output High Current	I_{OH}	1	2	3	mA	V_{OH} =0.7VDD_IO for IOB and IOD with DRV=000
		2	4	6	mA	V_{OH} =0.7VDD_IO for IOB and IOD with DRV=001
		3	6	9	mA	V_{OH} =0.7VDD_IO for IOB and IOD with DRV=010
		4	8	12	mA	V_{OH} =0.7VDD_IO for IOB and IOD with DRV=011
		5	10	15	mA	V_{OH} =0.7VDD_IO for IOB and IOD with DRV=100

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
		6	12	18	mA	V_{OH} =0.7VDD_IO for IOB and IOD with DRV=101
		7	14	21	mA	V_{OH} =0.7VDD_IO for IOB and IOD with DRV=110
		8	16	24	mA	V_{OH} =0.7VDD_IO for IOB and IOD with DRV=111
Output Low Current	I_{OL}	1	2	3	mA	V_{OL} =0.3VDD_IO for IOB and IOD with DRV=000
		1.5	3	4.5	mA	V_{OL} =0.3VDD_IO for IOB and IOD with DRV=001
		3	6	9	mA	V_{OL} =0.3VDD_IO for IOB and IOD with DRV=010
		4	8	12	mA	V_{OL} =0.3VDD_IO for IOB and IOD with DRV=011
		5	10	15	mA	V_{OL} =0.3VDD_IO for IOB and IOD with DRV=100
		6	12	18	mA	V_{OL} =0.3VDD_IO for IOB and IOD with DRV=101
		8.5	17	25.5	mA	V_{OL} =0.3VDD_IO for IOB and IOD with DRV=110
		9.5	19	28.5	mA	V_{OL} =0.3VDD_IO for IOB and IOD with DRV=111
Input Pull-Low Register	R_{PL}	30	50	70	KΩ	V_{IN} =V3
Input Pull-High Register	R_{PH}	30	50	70	KΩ	V_{IN} =VSS
Internal ROSC frequency deviation	⊿F/F	-2%	12.288M	+2%	HZ	-

Note: V5 → VDD_IO, VDD_REGIN, PVDD
V3 → V3_REG_OUT, V3_SPIFC_IN, V3_ADC, VDD_USB

7.3 DC Characteristics (V5 = 4.5V, V3= 3.0V, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REGIN/ VDD_IO	2.0	-	5.5	V	-
Operating Current	I_{OP}	-	27	35	mA	F_{OSC} = 122.88MHz, AD and DAC are disabled, without loading.
Halt Current	I_{halt}	-	1	2	mA	In halt mode, 32KHz is enabled and PLL (F_{OSC}) is disabled.
Shutdown Current	I_{SD}	-	5	7	μA	Shutdown mode current with V3 and V12 off
Input High Level	V_{IH}	0.7VDD	-	-	V	SMT Enabled for IOA, IOC, IOB, IOD
Input Low Level	V_{IL}	-	-	0.3VDD	V	SMT Enabled for IOA, IOC, IOB, IOD

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
PAD IOA and IOC GROUP						
Output High Current	I_{OH}	7	14	21	mA	V_{OH} =0.7VDD_IO for IOA and IOC with DRV=0
		13	26	39	mA	V_{OH} =0.7VDD_IO for IOA and IOC with DRV=1
Output Low Current	I_{OL}	7	14	21	mA	V_{OL} =0.3VDD_IO for IOA and IOC with DRV=0
		13	26	39	mA	V_{OL} =0.3VDD_IO for IOA and IOC with DRV=1
Input Pull-Low Register	R_{PL}	30	50	70	KΩ	V_{IN} =VDD_IO
Input Pull-High Register	R_{PH}	30	50	70	KΩ	V_{IN} =VSS
Internal ROSC frequency deviation	⊿F/F	-2%	12.288M	+2%	HZ	-

Note: V5 → VDD_IO, VDD_REGIN, PVDD
V3 → V3_REG_OUT, V3_SPIFC_IN, V3_ADC, VDD_USB

7.4 Regulator Characteristics

LDO12

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Input Voltage	VDD_IO	2.0	-	5.5	V
Maximum Current Output	Ivdd12	-	-	20	mA
Output Voltage	VDD12	1.0	1.2	1.4	V

Note: For IC use only. Users are not allowed using it.

LDO30

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Input Voltage	VDD_REGIN	2.0	-	5.5	V
V3_ADC					
Maximum Current Output for V3_ADC	Iv3_adc	-	-	10	mA
Output Voltage @ VIN=4.5V, Iout=5mA	V3_ADC	2.85	3.0	3.15	V
Output Voltage @ VIN=2.0V, Iout=5mA	V3_ADC	1.8	1.92	2.0	V
V3_REG_OUT					
Maximum Current Output for V3_REG_OUT	Iv3_reg_out	-	-	30	mA
Output Voltage @ VIN=4.5V, Iout=5mA	V3_REG_OUT	2.85	3.0	3.15	V
Output Voltage @ VIN=2.0V, Iout=5mA	V3_REG_OUT	1.8	1.93	2.0	V

7.5 16-Bit CODEC ADC Characteristics (V3_ADC = 3.0V, TA = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
ADC Microphone Input Voltage Range	VINMIC	VSS	-	V3_ADC	V
Resolution of ADC	RESO	-	-	16	bits

7.6 12-Bit SAR ADC Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SAR ADC Input Voltage Range from IOA[31 :24]	VINIOAx	0	-	VDD_IO	V
Resolution of ADC	RESO	-	-	12	bits
Integral Non-Linearity of ADC	INL	-6	-	+3	LSB
Differential Non-Linearity of ADC	DNL	-1	-	+6	LSB
ENOB	ENOB	8.4	8.6	-	bits
No Missing Code		9	10	-	Bits
AD Conversion Rate=ADCCLK/16	F_{CONV}	-	-	200K	Hz

7.7 Audio PWM Characteristics (PVDD =4.5V, R_L=8Ω, f=1KHz, TA=25℃)

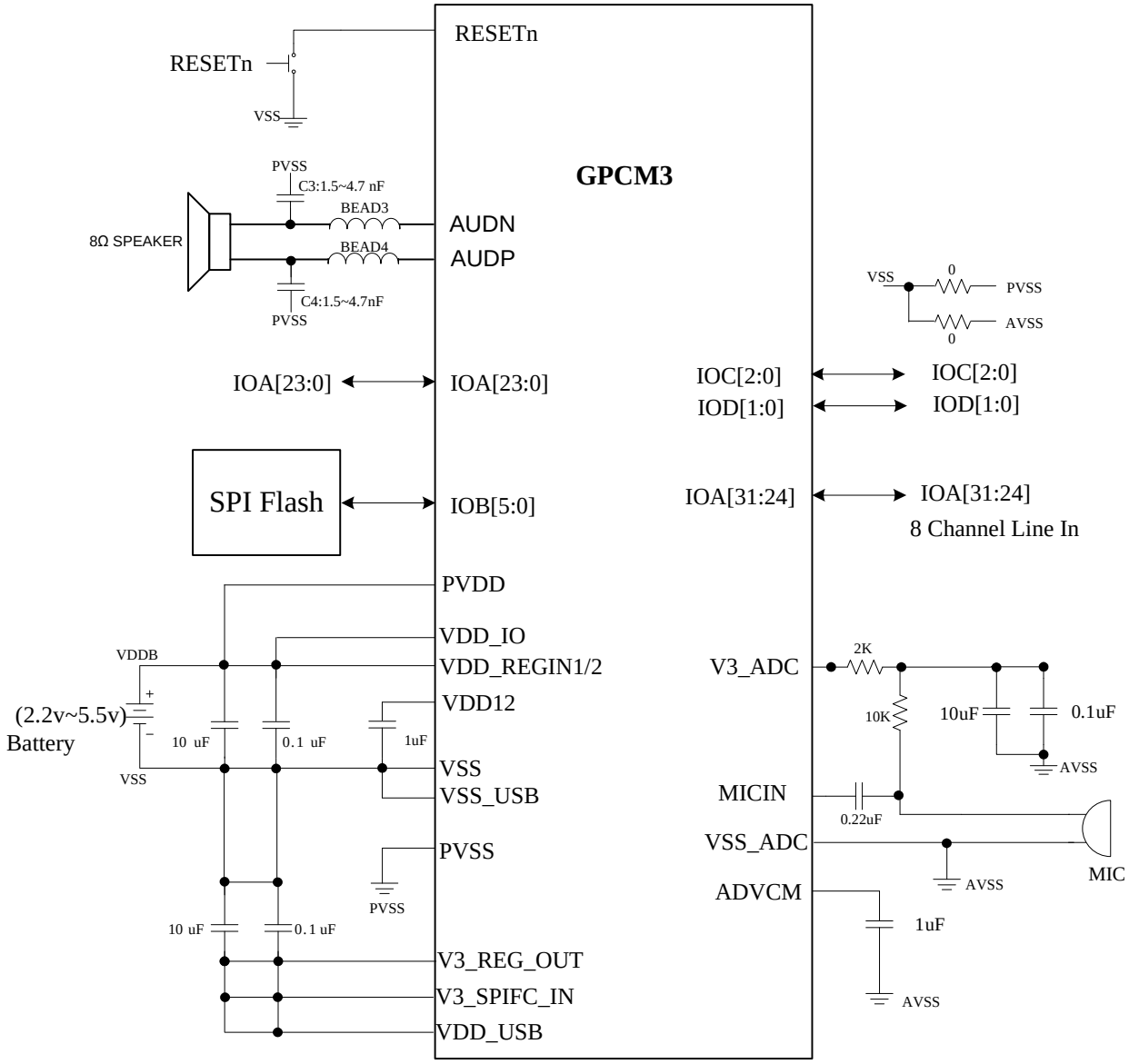
Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Resolution	RESO	-	-	16	bit
THD+n(4.5V@0.4W)	THD+n	-	1	-	%
Noise at No Signal (SNR)	SNR	-	-100	-	dBr A
Dynamic Range (-60dB)	DR	-	-80	-	dBr A

7.8 Voltage DAC Characteristics (PVDD =3.0V, R_L=8Ω, f=1KHz, TA=25℃with GPY0030C)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Resolution	RESO	-	-	16	bit
THD+n(4.5V@0.4W)	THD+n	-	1	-	%
Noise at No Signal (SNR)	SNR	-	-90	-	dBr A
Dynamic Range (-60dB)	DR	-	-70	-	dBr A

8 APPLICATION CIRCUITS

8.1 Application Circuit with Internal 12.288MHz Oscillator and Internal 32768Hz Oscillator

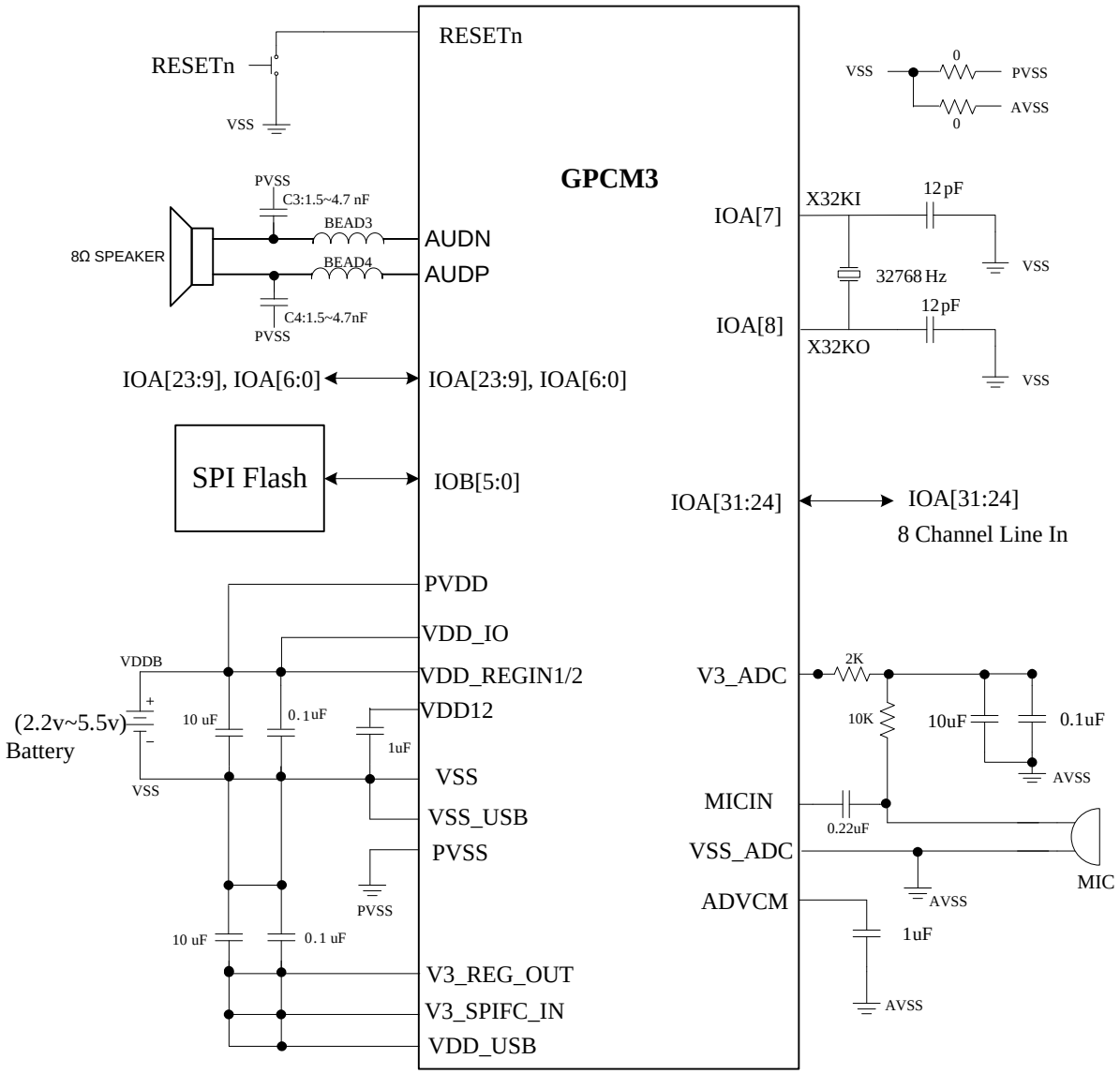


Note*1: Bead3/4 are optional for EMI sensitive application. Bead3/4 should be located as close as possible to AUDP/AUDN/PVSS.

Note*2: The typical value of C3/4 is 1.5nF, and could be modified in different loading. C4/5 should be located as close as possible to AUDP/AUDN/PVSS.

Note*3: Stand-alone PCB ground line from battery to VSS_ADC is suggested for better quality on ADC MIC.

8.2 Application Circuit with Internal 12.288MHz Oscillator and External 32768Hz Crystal

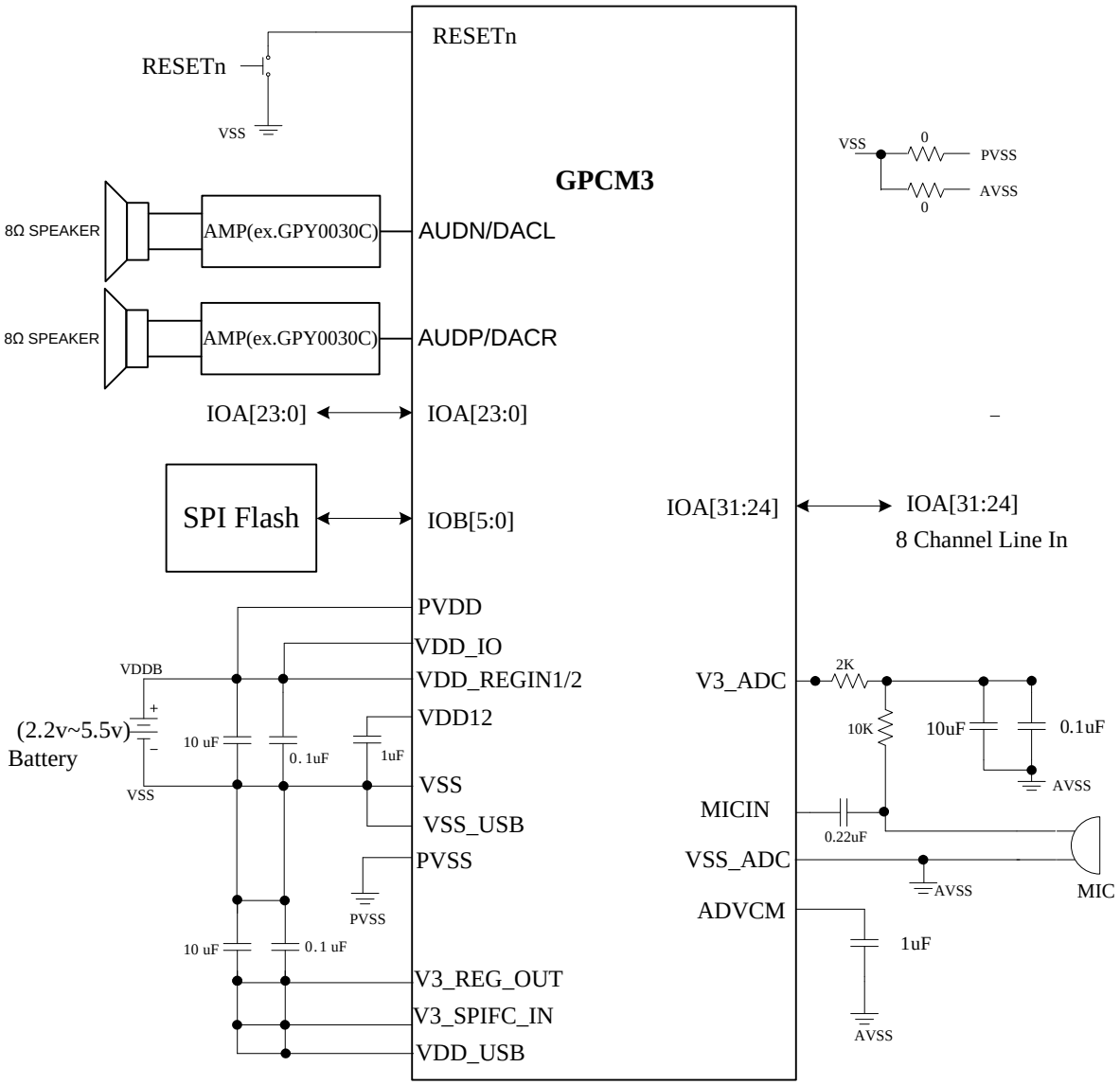


Note*1: Bead3/4 are optional for EMI sensitive application. Bead3/4 should be located as close as possible to AUDP/AUDN/PVSS.

Note*2: The typical value of C3/4 is 1.5nF, and could be modified in different loadings. C4/5 should be located as close as possible to AUDP/AUDN/PVSS.

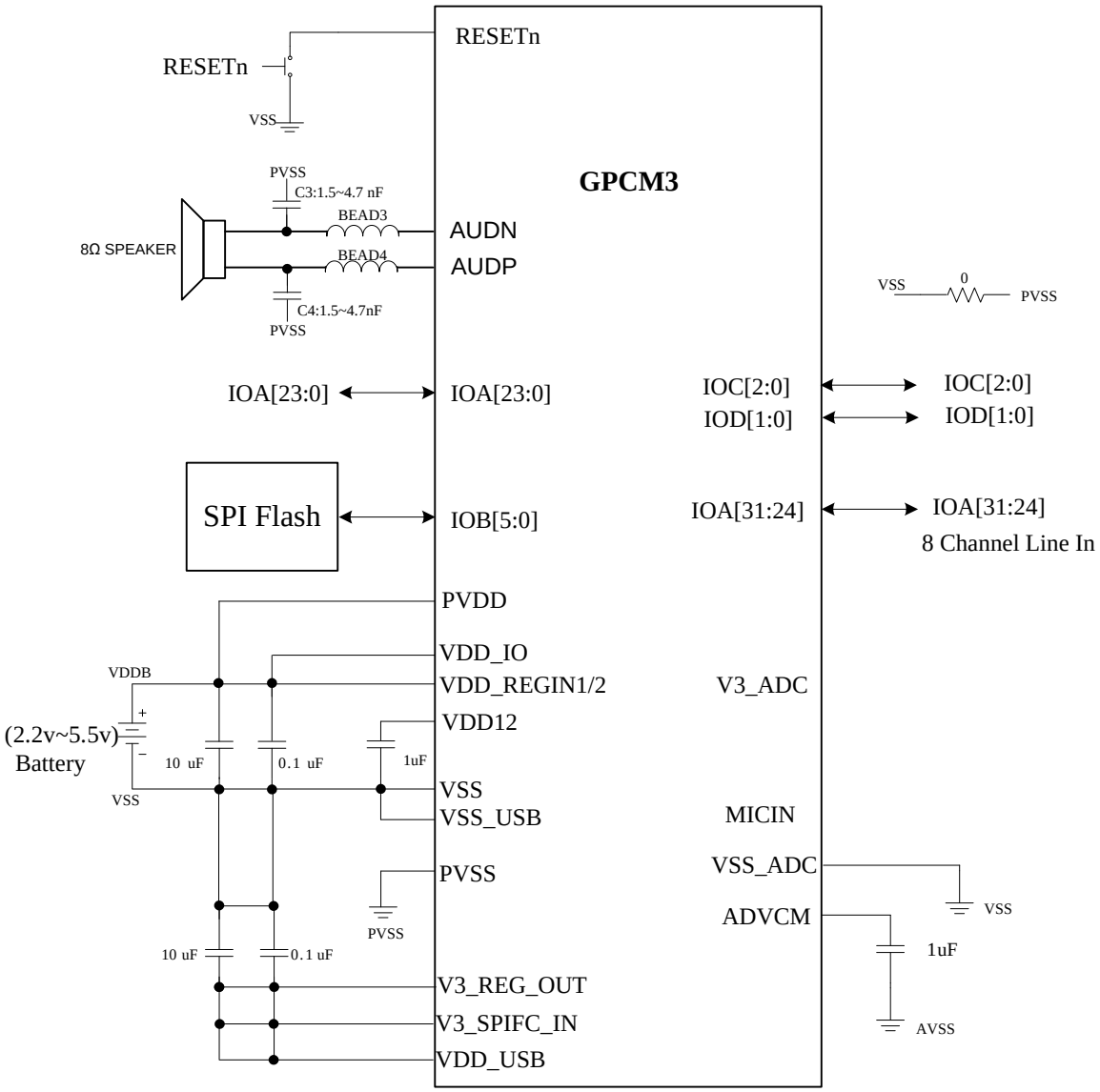
Note*3: To obtain a clearer sound quality for MIC ADC, the power source VSS (e.g. battery) is recommended being an independent path connecting with AVSS (VSS_ADC). This PCB layout approach is capable of reducing MIC's background noise significantly.

8.3 Application Circuit with Internal Oscillator and Voltage DAC



Note*1: To obtain a clearer sound quality for MIC ADC, the power source VSS (e.g. battery) is recommended being an independent path connecting with AVSS (VSS_ADC). This PCB layout approach is capable of reducing MIC's background noise significantly.

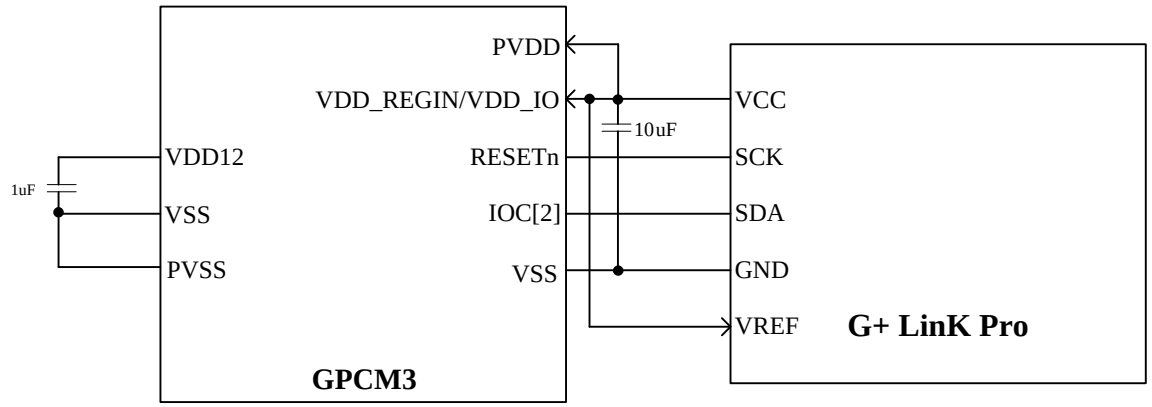
8.4 Application Circuit with Internal 12.288MHz Oscillator and Internal 32768Hz Oscillator and without MIC



Note*1: Bead3/4 are optional for EMI sensitive application. Bead3/4 should be located as close as possible to AUDP/AUDN/PVSS.

Note*2: The typical value of C3/4 is 1.5nF, and could be modified in different loading. C4/5 should be located as close as possible to AUDP/AUDN/PVSS.

8.5 Connect with G+ Link



Note: Connection above is applied for VREF=VCC. Check application notice for more detail information

9 PACKAGE/PAD LOCATION

9.1 Ordering Information

Body	Product Number	Package Type
GPCM300A	GPCM300A-NnnV-C	Chip form
	GPCM300A-NnnV-QL24x	Green Package – LQFP64_7x7x1.4
	GPCM300A-NnnV-QL23x	Green Package – LQFP48_7x7x1.4
GPCM300B	GPCM300B-NnnV-C	Chip form

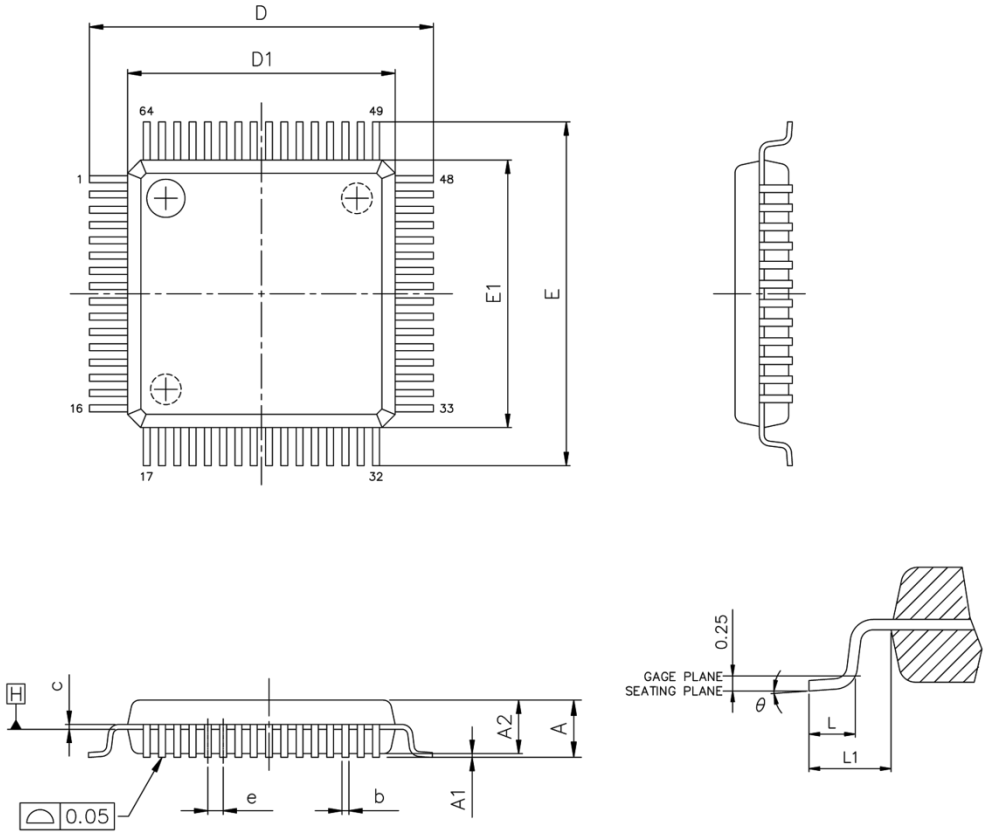
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2 Package Information

9.2.1 LQFP 64_7x7x1.4 Outline Dimensions

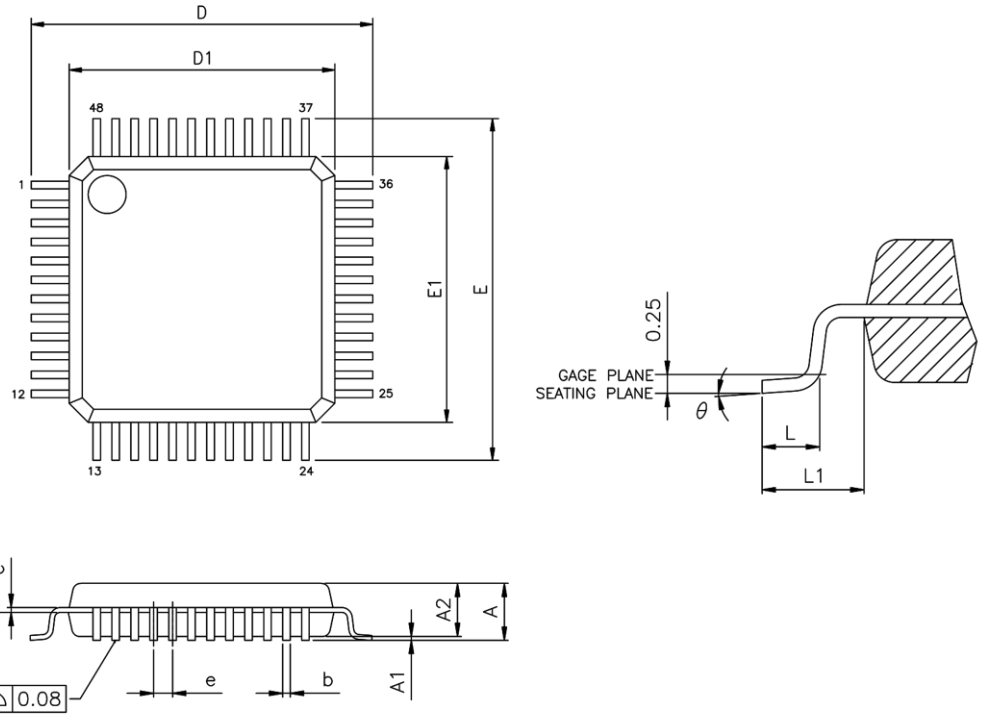


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:
1. JEDEC OUTLINE : MS-026 BBD
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM. PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBER PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO . EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

9.2.2 LQFP 48_7x7x1.4 Outline Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:
1. JEDEC OUTLINE : MS-026 BBC
2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H] .
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

10 DISCLAIMER

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11 REVISION HISTORY

Date	Revision #	Description	Page
Feb. 06, 2025	1.4	1. typo revise	9, 16, 17, 20, 21, 22
		2. LDO30 min. voltage spec modify to 2.0V	18
Aug. 28, 2024	1.3	1. Power pin name and description modify	7,9~10,16~18 ,20~22
		2. Add application circuits without MIC	23
Oct. 17, 2023	1.2	1. Remove Idsp and correct Isd max. to 7uA	16,17
		2. Typo revise	22
		3. Correct Iop max. to 35mA	16,17
		4. Add LQFP48 information	9,25,27
Jun. 06, 2023	1.1	1. Typo revise	4~7,10
		2. LQFP64 pin23~25 revise	9
		3. Remove LQFP64_10x10 information	
Feb. 03, 2023	1.0	1. Wake source modify	12
		2. Add new body GPCM300B description	4
		3. Modify Max. frequency to 122.88MHz	4
		4. Typo revise	7,14
Nov. 25, 2022	0.1	Preliminary version	29