

N32G401F8S7-1

Datasheet

N32G401F8S7-1 series based on 32-bit ARM Cortex-M4F kernel, run up to 72MHz, support floating-point unit and DSP instructions, up to 64KB embedded flash, 8KB SRAM, integrated high-performance analog interface, built-in 1x12bit 4.2Mps ADC, Integrated multi-channel U(S)ART, I2C, SPI and other digital communication interfaces.

Key features

- **CPU core**
 - 32-bit ARM Cortex-M4 + FPU, DSP instruction
 - Built-in 1KB instruction Cache, which support Flash acceleration unit to execute program 0 wait
 - Run up to 72MHz, 90DMIPS
- **Encrypted memory**
 - Up to 64KByte of embedded Flash memory, supporting encrypted storage , 10,000 cycling and 10 years data retention.
 - 8KByte of SRAM, retention in Stop2 mode, configurable in Standby mode
- **Power consumption mode**
 - Support Run, Sleep, Stop0, Stop2, Standby mode
- **High-performance analog interface**
 - 1x 12bit 4.2Mps ADC, 12/10/8/6 bits configurable, up to 9 external single-ended input channels, 3 internal single-ended input channels, support differential mode
- **Clock**
 - HSE: 4MHz~32MHz external high-speed crystal
 - HSI: Internal high-speed RC 8MHz
 - LSI: Internal low speed RC 40KHz
 - Built-in high speed PLL
 - MCO: Support 1-way clock output, configurable SYSCLK, HSI, HSE, LSI, and PLL clock output that can be divided
- **Reset**
 - Supports power-on/power-off/external pin reset
 - Support watchdog reset, software reset
 - Support programmable low voltage detection and reset
- **Up to 15+1 GPIOs are supported**
- **Communication interface**
 - 1x U(S)ART interface, 2x UART interfaces, and USART interface (supporting 1xISO7816, 1xIrDA, LIN)
 - 2x SPI interfaces, master mode and slave mode up to 18Mbps, support I²S
 - 2x I2C interfaces with a rate up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
- **1x DMA controller, supports 8 channels, channel source address and destination address can be arbitrarily configurable**
- **1x RTC real-time clock, support leap year perpetual calendar, alarm clock event, periodic wake up, support internal and external clock calibration**

- **1x Beeper, support complementary output, 12mA output drive capability**
- **Timing counter**
 - 2x 16-bit advanced timer counters, support input capture, complementary output, orthogonal encoding input, maximum control accuracy 7.8ns; Each timer has four independent channels, Timer1 support 2 complementary PWM output , Timer8 support 2 complementary PWM output
 - 4x 16-bit general purpose timer counters, TIM2 and TIM3 have 3 independent channels, TIM4 and TIM5 have 4 independent channels, support input capture/output comparison /PWM output
 - 1x 16-bit basic timer counter
 - 1x 16-bit low power timer counter, support double pulse counting function, can work in STOP2 mode
 - 1x 24-bit SysTick
 - 1x 14-bit Window Watchdog (WWDG)
 - 1x 12-bit Independent Watchdog (IWDG)
- **Programming mode**
 - Support SWD online debugging interface
- **Security features**
 - Flash Storage encryption
 - CRC16/32
 - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
 - Support safe start, program encryption download, security updates
 - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
 - Operating voltage range: 2.4V~3.6V
 - Operating temperature range: -40℃ ~ 105℃
 - ESD: ±4KV (HBM model), ±2KV (CDM model)
- **Encapsulation**
 - TSSOP20(6.5mm x 4.4mm)
- **Ordering information**

Series	Part Number
N32G401x8	N32G401F8S7-1

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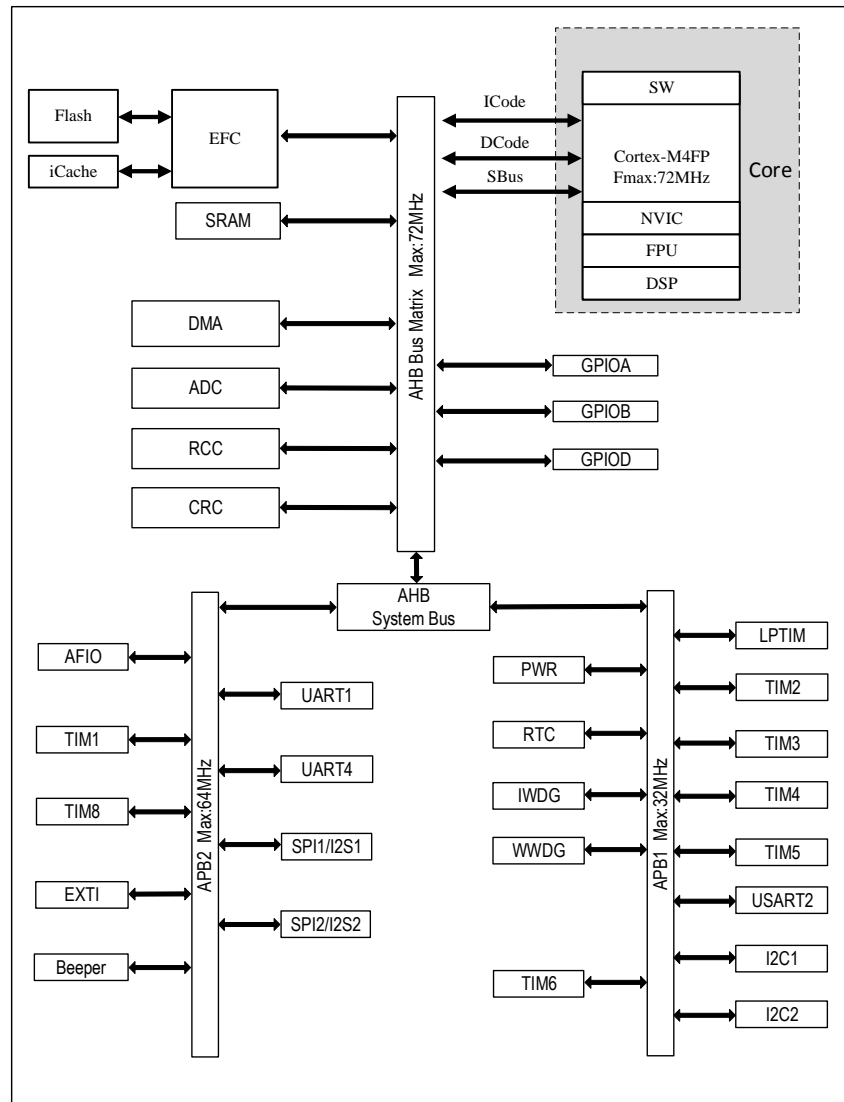
1 Product introduction

N32G401F8S7-1 family of microcontrollers features a high-performance 32-bit ARM Cortex™-M4F core, integrated floating point operation unit (FPU) and digital Signal processing (DSP), and supports parallel computing instructions. Maximum operating main frequency 72MHz, integrated up to 64KB of in-chip encrypted storage Flash, supports multi-user partition permission management, maximum 8KB of embedded SRAM. It has an internal high speed AHB bus, two low speed peripherals clock bus APB and bus matrix. It supports up to 16 reusable I/Os and provides a rich array of high performance analog interfaces, including 1x 12-bit 4.2Mps ADC, up to 16 external input channels and 3 internal channels. At the same time, it provides a variety of digital communication interfaces, including 3x U(S)ART, 2x I2C, 2x SPI/ I2S communication interface.

N32G401F8S7-1 series products can work stably in the temperature range of -40 ℃ to +105 ℃, supply voltage from 2.4V to 3.6V, provide a variety of power modes for users to choose, refer to the requirements of low-power applications. This series of products are available in 20 pin package.

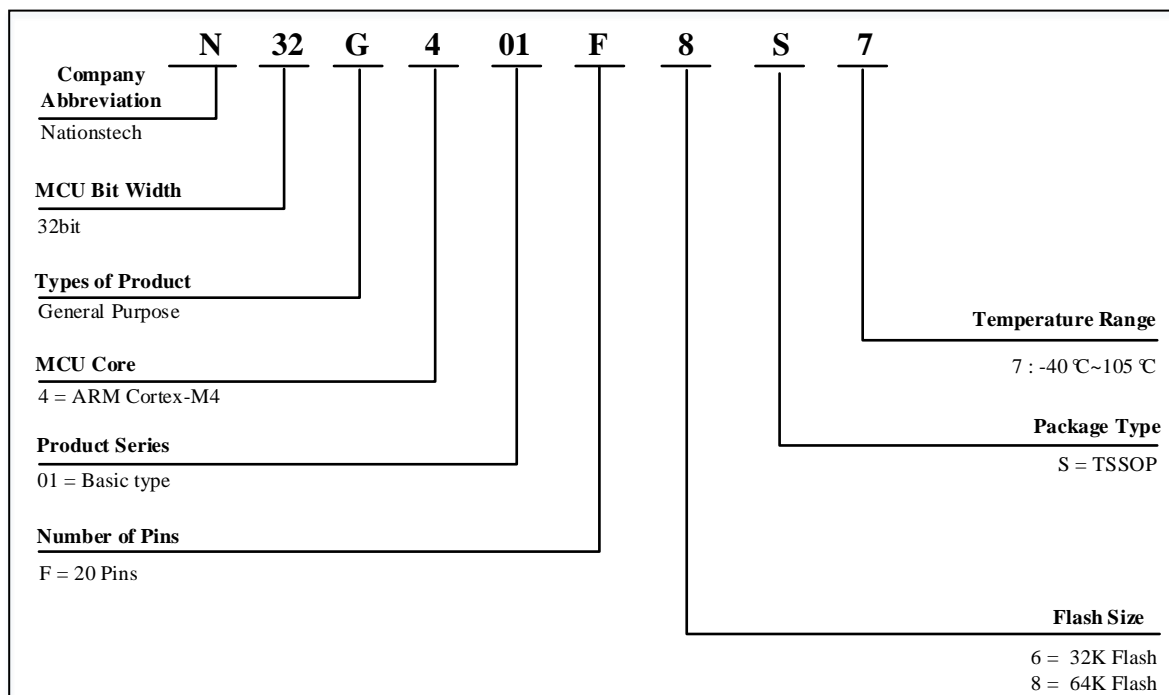
Figure 1-1 N32G401F8S7-1 Series Block Diagram

Figure 1-1 N32G401F8S7-1 Series Block Diagram



1.1 Part number information

Figure 1-2 N32G401F8S7-1 Series Part Number Information



1.2 List of devices

Table 1-1 N32G401F8S7-1 Series Resource Configuration

Part Number		N32G401F8S7-1
Flash capacity (KB)		64
SRAM capacity (KB)		8
CPU frequency		ARM Cortex-M4F@72MHz, 90DMIPS
Working environment		2.4~3.6V/-40~105℃
Timer	General	4 (TIM2 and TIM3 support 3 channels, TIM4 and TIM5 support 4 channels)
	Advanced	2 (TIM1 supports 4 channels and 3 complementary PWM output, TIM8 supports 4 channels and 2 complementary PWM output)
	Basic	1
	LPTIM	1
Communication interface	SPI	2
	I2S	2
	I2C	2
	UART	2
	USART	1
BEEPER		1
GPIO		16
DMA		1
Number of Channels		8 Channel
12bit ADC		1
Number of channels		9Channel
security protection		Read and write protection (RDP/WRP), storage encryption
Package		TSSOP20

2 Function Introduction

2.1 Processor core

The N32G401F8S7-1 family integrates the latest generation of embedded ARM Cortex™-M4F processors, enhanced computing power based on the Cortex™-M3 core, new floating point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 1.25DMIPS/MHz. Its efficient signal processing capabilities are combined with the advantages of low power consumption, low cost, and ease of use of the Cortex-M family of processors to meet the requirements of a mixture of control and signal processing capabilities and easy to use applications.

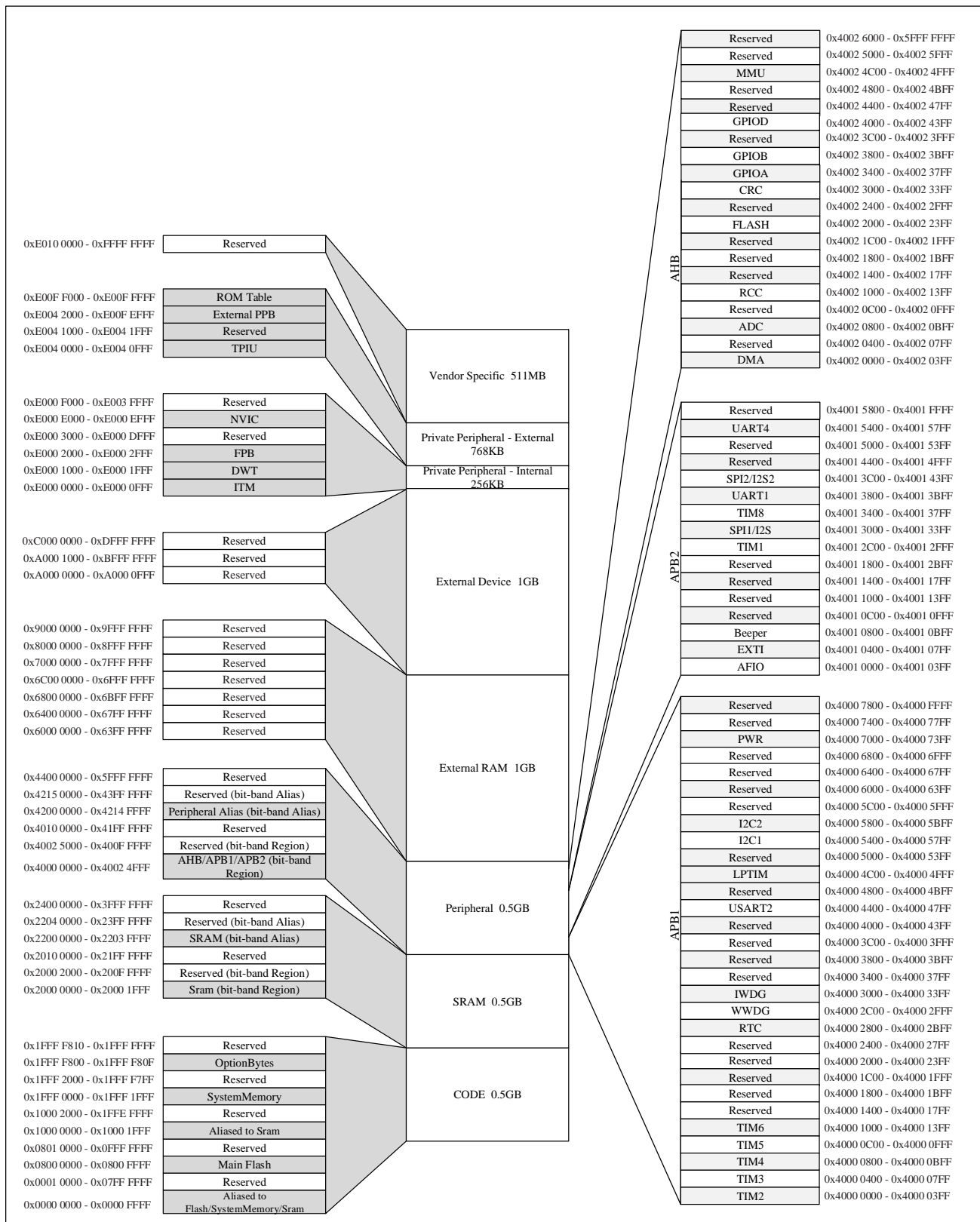
The ARM Cortex™-M4F 32-bit compact instruction set processor provides excellent code efficiency.

Note: Cortex-M4F is backward compatible with Cortex-M3 code.

2.2 Storage

N32G401F8S7-1 series devices include embedded encrypted Flash memory and embedded SRAM.

Figure 2-1 Memory map



2.2.1 Embedded FLASH memory

Integrated 64K bytes embedded encryption FLASH (FLASH), used to store programs and data, page size of 2Kbyte, supporting page erasing, word writing, word reading, half word reading, byte reading operations.

Support storage encryption protection, write automatic encryption, read automatic decryption (including program execution operation).

Support user partition management, can be divided into a maximum of two user partitions, different users cannot access each other's data (only executable code).

2.2.2 Embedded SRAM

The chip integrates a built-in SRAM of up to 8K bytes. In RUN、SLEEP、STOP0、STOP2 and STANDBY mode, SRAM data can be retained.

2.2.3 Nested vector interrupt controller (NVIC)

Built-in nested vector interrupt controller, capable of handling up to 48 maskable interrupt channels (not including the 16 Cortex™-M4F interrupts) and 16 priorities.

- ◆ Tightly coupled NVIC enables low latency interrupt response processing
- ◆ Interrupt vector entry address directly into the kernel
- ◆ Tightly coupled NVIC interface
- ◆ Allows early handling of interrupts
- ◆ Handles late arriving higher-priority interrupts
- ◆ Support interrupt tail link function
- ◆ Automatically saves processor state
- ◆ Automatically resumes when the interrupt returns with no additional instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.3 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 24 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its triggering event (rising edge or falling edge or bilateral edge) and can be individually shielded. There is a suspended register that maintains the state of all interrupt requests. EXTI can detect clock cycles with pulse widths smaller than internal APB2. Up to 16 universal I/O ports are connected to 16 external interrupts.

2.4 Clock system

The device provides a variety of clocks for users to choose from, including internal high speed RC oscillator HSI (8MHz), internal low speed clock LSI (40KHz), external high speed clock HSE (4MHz~32MHz), PLL.

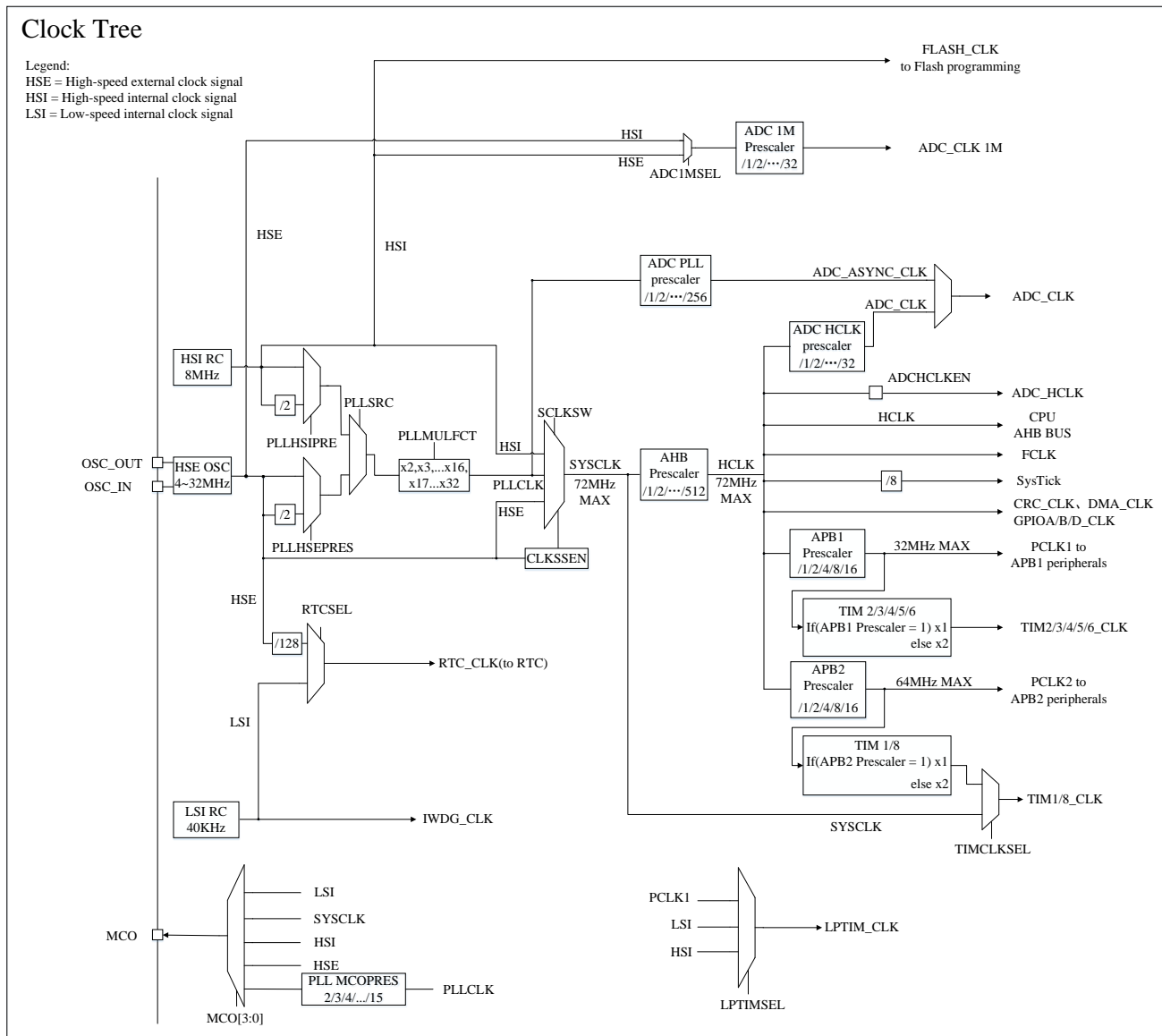
During reset, the internal HSI clock is set as the default CPU clock, and then the user can choose the external HSE clock with failure monitoring function. When an external clock failure is detected, it will be isolated, the system will automatically switch to HSI, and if interrupts are enabled, the software can receive the corresponding interrupt. Also, complete interrupt management of the PLL clock can be adopted when needed (such as when an indirectly used external oscillator fails).

The built-in clock security system detects whether the external HSE fails in real time. If the external clock fails, HSE will automatically switches to internal clock and generates an interrupt alarm.

Multiple prescalers are used to configure the AHB frequency, high speed APB(APB2) and low speed APB(APB1) regions. AHB has a maximum frequency of 72MHz, APB2 has a maximum frequency of 64MHz and APB1 has a maximum frequency of 32MHz.

Note: If APB1 and APB2 are running at the highest frequency, the system clock needs to be reduced to 64MHz.

Figure 2-2 Clock Tree



2.5 Boot mode

At BOOT time, the BOOT mode after reset can be selected with the option byte BOOT configuration (USER2).

- Boot from program FLASH Memory
- Boot from System Memory
- Boot from internal SRAM

The Bootloader is stored in the system memory and can be programmed to FLASH Memory through UART1.

2.6 Power supply scheme

- $V_{DD} = 2.4 \sim 3.6V$: The V_{DD} pin supplies power to the I/O pin and the internal voltage regulator.
- $V_{SSA}, V_{DDA} = 2.4V \sim 3.6V$: provides power supply for ADC. V_{DDA} must be connected to V_{DD} , and V_{SSA} is connected to V_{SS} inside the chip.

2.7 Reset

POR circuit is integrated inside the device. This part of the circuit is always in working state to ensure that the system works stably when the power supply exceeds 2.4V. When V_{DD} falls below a set threshold ($V_{POR/PDR}$), place the device in the reset state without using an external reset circuit.

2.8 Programmable voltage detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD} and compares it with the threshold V_{PVD} . When V_{DD} is lower or higher than the threshold V_{PVD} , an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be started through the program. See Table 4-6 for values of $V_{POR/PDR}$ and V_{PVD} .

2.9 Voltage regulator

The voltage regulator has three control modes:

- Master mode, MCU run in RUN, SLEEP, STOP0 modes
- Low power mode, MCU run in STOP0 mode
- Turn off mode, MCU run in STOP2, STANDBY modes

The voltage regulator is always in the master mode after the MCU reset.

2.10 Low power mode

The N32G401F8S7-1 series supports four low-power modes.

- SLEEP mode

In SLEEP mode, only the CPU stops and all peripherals are active and can wake up the CPU when an interrupt/event occurs.

- STOP0 mode

STOP0 mode is based on Cortex®-M4F deep sleep mode, combined with peripheral clock control mechanism. The voltage regulator can be configured in normal or low power mode. In STOP0 mode, most clock sources in the core domain are disabled, such as PLL, HSI and HSE. But SRAM and all register contents retention.

In STOP0 mode, all I/O pins remain in the same state as in run mode.

- STOP2 mode

STOP2 mode is based on the Cortex®-M4F deep sleep mode, and all the core digital logic areas are powered off. Main voltage regulator (MR) is off, HSE/HSI/PLL is off. CPU register retention, LSI optional work, RCC retention, all GPIO retention, SRAM retention, 80 byte backup register retention, RET domain and Backup domain work normally.

Wake up: The microcontroller can be woken up from STOP2 mode by any signal configured as EXTI, which can be 16 external EXTI signals (I/O related), WKUP pins wakeup, RTC periodic wake up, RTC alarm, RTC tamper, RTC timestamp, NRST reset, IWDG reset.

- STANDBY mode

In STANDBY mode, the current consumption is low. Internal voltage regulator is turned off, PLL, HSI RC oscillator and HSE crystal oscillator are also turned off, only LSI work; After entering STANDBY mode, IO output states are maintained, main domain register contents will be lost, SRAM is optional, and the STANDBY circuit still works.

Before entering the STANDBY mode, if pins PA13 and PA14 are used as non-debug pins, and configured as input mode, it is necessary to add strong pull-down resistance on pins PA13 and PA14. The pull-down resistance is recommended to be within 10KΩ.

An external reset signal on the NRST, an IWDG reset, a rising/falling edge on three WKUP pins, a RTC periodic wake up, a RTC alarm, a RTC timestamp and a RTC tamper can wake up the microcontroller from STANDBY mode.

Note: RTC, IWDG and corresponding clock can not be stopped when entering standby mode.

2.11 Direct memory access (DMA)

The device integrates a flexible general-purpose DMA controller that supports eight DMA channels to manage data transfers from memory to memory, peripherals to memory, and memory to peripherals. The DMA controller supports the management of ring buffers, avoiding interruptions when controller transfers reach the end of the buffer.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The transmission length, source address and destination address of each channel can be set separately by software.

DMA can be used with major peripherals: SPI, I2C, USART, general, basic and advanced timers TIMx, I2S, ADC.

2.12 Real time clock (RTC)

RTC is a set of continuously running counters with a built-in calendar clock module that provides a perpetual calendar function, as well as alarm interrupt and periodic interrupt (minimum 2 clock cycles) functions. The RTC will not be reset by the system reset, nor will it be reset when wake up from STANDBY mode. The RTC can be driven by an internal low-power 40KHz RC oscillator, or a high-speed external clock with 128 frequency divisions. The RTC has a 22-bit predivider for a time-based clock, which will produce a 1-second long time reference at 40kHz by default. In addition, RTC can be used to trigger wake up in low-power mode.

2.13 Timer and watchdog

Up to 2 advanced control timers, 4 general-purpose timers and 1 basic timers, 1 low power timer, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 2-1 Comparison of Timer functions

Timer	Counter resolution	Counter type	Prescaler factor	Generate DMA requests	Capture/compare channels	Complementary output
TIM1 TIM8	16	Up, down, up/down	Any integer between 1 and 65536	Y	3	Y
TIM2 TIM3	16	Up, down, up/down	Any integer between 1 and 65536	Y	3	N
TIM4 TIM5	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	N
TIM6	16	upward	Any integer between 1 and 65536	Y	0	N

2.13.1 Low power timer LPTIM

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes except for Standby mode. LPTIM can run without internal clock source, it can be used as a “Pulse Counter”. Also, the LPTIM can wake up the system from low-power modes, to realize “Timeout functions” with extreme low power consumption.

The main functions of the low-power timer are as follows:

- 16-bit upcounter
- Clock prescaler with 3-bit to provide 8 dividing factors (1,2,4,8,16,32,64,128)
- Multiple clock sources
 - Internal : LSI, HSI or APB1 clock
 - External : LPTIM Input1 (working with no LP oscillator running used by Pulse Counter application)
- 16-bit auto-reload register
- 16-bit compare register
- Continuous or One-shot counting mode
- Programmable software or hardware input trigger
- Programmable digital filter for filtering glitch
- Configurable output: Pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting (orthogonal and non-orthogonal)

2.13.2 Basic timer (TIM6)

The basic timer contains a 16-bit counter.

The basic timer has the following functions:

- 16-bit auto-reload up-counting counters.
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- The events that generate the interrupt/DMA are as follows:
 - ◆ Update event

2.13.3 General-purpose timer (TIMx)

The general-purpose timers (TIM2, TIM3, TIM4 and TIM5) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

The main functions of the universal timer include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- TIM2 and TIM3 support 3 channels, TIM4 and TIM5 support 4 channels.
- Channel's working modes: PWM output, output compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
 - ◆ Update event
 - ◆ Trigger event
 - ◆ Input capture
 - ◆ Output compare
- TIM can be controlled by external signal

- TIM can be linked internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;

2.13.4 Advanced control timer (TIM1 and TIM8)

The advanced control timers (TIM1 and TIM8) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc. Advanced timers have complementary output function with dead-time insertion and break function. Suitable for motor control.

The main functions of the advanced timer include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting). TIM1 support center-aligned asymmetric mode.
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 up to 9 channels, TIM8 up to 6 channels.
- 4 capture/compare channels, the working modes are PWM output, output compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
 - ◆ Update event
 - ◆ Trigger event
 - ◆ Input capture
 - ◆ Output compare
 - ◆ Break input
- Complementary outputs with adjustable dead-time.
 - For TIM1, channel 1,2,3 support this feature.
 - For TIM8, channel 1,3 support this feature
- TIM can be controlled by external signal
- TIM can be linked internally for TIM synchronization or chaining
- For TIM1, the pulse signal output by channel 4/7/8/9 is configured as the rising and falling edges to trigger the ADC.
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;

2.13.5 SysTick timer (SysTick)

This timer is dedicated to real-time operating systems and can also be used as a standard decrement counter.

It has the following characteristics:

- ◆ 24 bit decrement counter
- ◆ Automatic reloading function
- ◆ A maskable system interrupt is generated when the counter is 0
- ◆ Programmable clock source

2.13.6 Watchdog (WDG)

Support for two watchdog independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit decrepit counter and a 3-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP and STANDBY modes. Once activated, if the dog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. The option byte can be configured to start the watchdog software or hardware. Reset and low power wake up are available.

Window Watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the decline counter value is flushed before the T6 bit becomes zero, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 14-bit decrement counter value (in the control register) is flushed before the decrement counter reaches the window register value, then an MCU reset will also occur. This indicates that the decrement counter needs to be refreshed in a finite time window.

Main features:

- ◆ WWDG is driven by the clock generated after the APB1 clock is divided.
- ◆ Programmable free-running decrement counter;
- ◆ Reset condition:
 - ◆ When the decrement counter is less than 0x40, a reset occurs (if the watchdog is started);
 - ◆ A reset occurs when the decrement counter is reloaded outside the window (if the watchdog is started);
 - ◆ If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWINT) occurs when the decrement counter equals 0x40, which can be used to reload the counter to avoid WWDG reset.

2.14 I²C bus interface

The device integrates up to two independent I2C bus interfaces, which provide multi-host function and control all I2C bus-specific timing, protocol, arbitration and timeout. Supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, System Management Bus(SMBus), and Power Management Bus(PMBus).

The functions of the I2C interface are described as follows:

- ◆ Multi-master function: this module can be used as master device or slave device;
- ◆ I2C master device function;
 - Generate a clock;
 - Generate start and stop signals;
- ◆ Function of I2C slave device
 - Programmable address detection;
 - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode.
 - Stop bit detection;
- ◆ Generate and detect 7-bit / 10-bit addresses and broadcast calls;

- ◆ Support different communication speeds;
 - Standard speed (up to 100 kHz);
 - Fast (up to 400 kHz);
 - Fast + (up to 1MHz);
- ◆ Status flags:
 - Transmitter/receiver mode flag;
 - Byte transfer complete flag;
 - I2C bus busy flag;
- ◆ Error flags:
 - Arbitration is missing in Master mode
 - Acknowledge (ACK) error after address/data transfer;
 - Error start or stop condition detected
 - Overrun or underrun when clock extending is disable;
- ◆ Two interrupt vectors:
 - 1 interrupt for address/data communication success;
 - 1 interrupt for an error;
- ◆ Optional extend clock function
- ◆ DMA of single-byte buffers;
- ◆ Generation or verification of configurable PEC(Packet error detection)
- ◆ In transmit mode, the PEC value can be transmitted as the last byte
- ◆ PEC error check for the last received byte
- ◆ SMBus 2.0 compatible
 - Timeout delay for 25ms clock low
 - 10 ms accumulates low clock extension time of master device
 - 25 ms accumulates low clock extension time of slave device
 - PEC generation/verification of hardware with ACK control
 - Support address resolution protocol (ARP)
- ◆ Compatible with the PMBus

2.15 Universal synchronous/asynchronous transceiver (USART)

N32G401F8S7-1 series products integrate up to 3 serial transceiver interfaces, including 1 universal synchronous/asynchronous transceivers (USART2) and 2 universal asynchronous transceivers (UART1 and UART4). These 3 interfaces provide asynchronous communication, support for IrDA SIR ENDEC transmission codec, multi-processor communication mode, single-line half-duplex communication mode, and LIN master/slave function.

The USART2 interfaces has hardware CTS and RTS signal management, ISO7816-compatible smart card mode, and SPI-like communication mode, all of which can use DMA operations.

Main features of USART are as follows:

- ◆ Full duplex, asynchronous communication;
- ◆ NRZ standard format;
- ◆ Fractional baud rate generator system, baud rate programmable, used for sending and receiving

- ◆ Programmable data word length (8 or 9 bits)
- ◆ Configurable stop bit, supporting 1 or 2 stop bits;
- ◆ LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates 13 bit interrupters and detects 10/11 bit interrupters
- ◆ Output sending clock for synchronous transmission;
- ◆ IRDA SIR encoder decoder, supports 3/16 bit duration in normal mode;
- ◆ Smart card simulation function;
 - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3.
 - 0.5 and 1.5 stop bits for smart cards;
- ◆ Single-wire half duplex communication;
- ◆ Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer;
- ◆ Independent transmitter and receiver enable bits;
- ◆ Test flag
 - Receive buffer is full
 - Send buffer empty
 - End of transmission flag
- ◆ Parity control
 - Send parity bit
 - Verify the received data
- ◆ Four error detection flags;
 - Overflow error
 - Noise error
 - Frame error
 - Parity error
- ◆ 10 USART interrupt sources with flags
 - CTS change
 - LIN disconnect detection
 - Send data register is empty
 - Send complete
 - Received data register is full
 - Bus was detected to be idle
 - Overflow error
 - Frame error
 - Noise error
 - Parity the error
- ◆ Multi-processor communication, if the address does not match, then enter the silent mode;

- ◆ Wake up from silent mode (via idle bus detection or address flag detection)
- ◆ There are two ways to wake up the receiver: address bit (MSB, bit 9), bus idle
- ◆ Mode configuration:

USART modes	USART2	UART1	UART4
Asynchronous mode	support	support	support
Hardware flow control	support	Does not support	Does not support
Multiple Cache communication (DMA)	support	support	support
Multiprocessor communication	support	support	support
Synchronous mode	support	Does not support	Does not support
The smart card	support	Does not support	Does not support
Half Duplex (Single wire mode)	support	support	support
IrDA	support	support	support
LIN	support	support	support

2.16 Serial peripheral interface (SPI)

The device integrates two SPI interfaces, reusable as an I2S interface, SPI shares resources with I2S.

SPI allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner. This interface can be configured in master mode and provides a communication clock (SCK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-line simplex synchronous transmission using a two-way data line, and reliable communication using CRC checks.

The main functions of SPI interfaces are as follows:

- ◆ 3-wire full-duplex synchronous transmission;
- ◆ Two-wire simplex synchronous transmission with or without a third bidirectional data line;
- ◆ 8 or 16 bit transmission frame format selection;
- ◆ Master or slave operations;
- ◆ Support multi-master mode;
- ◆ 8 master mode baud rate predivision frequency coefficient (maximum $f_{PCLK}/2$);
- ◆ Slave mode frequency (maximum $f_{PCLK}/2$);
- ◆ Fast communication between master mode and slave mode;
- ◆ NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes;
- ◆ Programmable clock polarity and phase;
- ◆ Programmable data order, MSB before or LSB before;
- ◆ Dedicated send and receive flags that trigger interrupts;
- ◆ SPI bus busy flag;
- ◆ Hardware CRC for reliable communication;
 - In send mode, the CRC value can be sent as the last byte;
 - In full-duplex mode, CRC is automatically performed on the last byte received.
- ◆ Master mode failures, overloads, and CRC error flags that trigger interrupts
- ◆ Single-byte send and receive buffer with DMA capability: generates send and receive requests
- ◆ Maximum interface speed: 18Mbps

2.17 Serial audio interface (I²S)

I²S is a 3-pin synchronous serial interface communication protocol. The device integrates two standard I²S interfaces (multiplexed with SPI) and can operate in master or slave mode. The two interfaces can be configured for 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8KHz to 96KHz. It supports four audio standards, including Philips I²S, MSB and LSB alignment, and PCM.

It can work in master and slave mode in half duplex communication. When it acts as a master device, it provides clock signals to external slave devices through an interface.

The main functions of I²S interface are as follows;

- ◆ Simplex communication (send or receive only);
- ◆ Master or slave operations;
- ◆ 8-bit linear programmable prescaler for accurate audio sampling frequencies (8 KHZ to 96KHz);
- ◆ The data format can be 16, 24, or 32 bits;
- ◆ Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame);
- ◆ Programmable clock polarity (steady state);
- ◆ The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode;
- ◆ 16-bit data registers are used for sending and receiving, with one register at each end of the channel;
- ◆ Supported I²S protocols:
 - I²S Philips standard;
 - MSB alignment standard (left aligned);
 - LSB alignment standard (right aligned);
 - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame);
- ◆ The data direction is always MSB first;
- ◆ Both send and receive have DMA capability;
- ◆ The master clock can be output to external audio devices at a fixed rate of 256xFs(Fs is the audio sampling frequency)

2.18 General purpose input/output interface (GPIO)

Up to 16 GPIO, which can be divided into four groups (GPIOA/GPIOB/GPIOD). Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up/pull-down), or multiplexing peripheral function port. Most GPIO pins are shared with digital or analog multiplexing peripherals, and some I/O pins are multiplexed with clock pins. All GPIO pins except ports with analog input capability have high current passing capability.

GPIO features are described as follows:

- ◆ Each bit of the GPIO port can be configured separately by the software into multiple modes:
 - Input floating;
 - Input pull up (weak pull up);
 - Input pull down (weak pull down);
 - Analog input;
 - Open drain output;

- Push-pull output;
- Push-pull multiplexing function;
- Open drain multiplexing function.
- ◆ General I/O (GPIO)
 - During and just after reset, the alternate functions are not enabled, except for NRST pin, the I/O port is configured to analog input mode.
 - After reset, the default state of pins associated with the debug system is enable SWD, the SWD pin is placed in input pull-up or pull-down mode:
 - ✓ SWCLK in pull-down mode;
 - ✓ SWDIO in pull-up mode;
 - When configured as output, values written to the output data registers are output to the appropriate I/O pins. Can be output in push pull mode or open drain mode
- ◆ Combined I/O(GPIO)
 - There are two groups of combination IO, namely the 13th PIN and the 14th PIN. The 13th PIN is the combination of PB3 and PB5, and the 14th PIN is the combination of PA9, PA15 and PB10. When the combined IO is used, only the functions of one IO can be used at the same time. The other IO's on the same pin must be configured as input floating mode to avoid affecting the functions of the IO's in use.
- ◆ Separate bit setting or bit clearing functions;
- ◆ External interrupt/wake up: All ports have external interrupt capability. In order to use external interrupts, ports must be configured in input mode.
- ◆ Alternate function :(port bit configuration register must be programmed before using default alternate function)
- ◆ GPIO lock mechanism, which freezes I/O configurations. When a LOCK is performed on a port bit, the configuration of the port bit cannot be changed until the next reset.
- ◆ Precautions for using GPIO
 - When VDD and VDDA are not powered on, the voltage applied on GPIO shall not exceed 3.6V;
 - VDD and VDDA shall not be lower than 2.4V when the voltage applied on GPIO is 5.5V;
 - If you don't want leakage in the MCU, need to ensure that the voltage applied on GPIO is less than or equal to VDD and VDDA;
 - When the voltage applied on GPIO is greater than VDD and VDDA, series resistance on GPIO is required if the MCU leakage current is expected to be reduced;

2.19 Analog/digital converter (ADC)

The device supports a 12-bit 4.2MSPS sequential comparison ADC with a sampling rate of single-ended and differential inputs, measuring 16 external and 3 internal sources.

The main features of ADC are described as follows:

- ◆ Support 12/10/8/6 - bit resolution configurable

- The highest sampling rate at 12bit resolution is 4.2MSPS
- The maximum sampling rate at 10bit resolution is 5.5MSPS
- The maximum sampling rate at 8bit resolution is 6.5MSPS
- The maximum sampling rate at 6bit resolution is 8MSPS
- ◆ ADC clock source is divided into working clock source, sampling clock source and timing clock source
 - AHB_CLK can be configured as the working clock source, up to 72MHz
 - PLL can be configured as a sampling clock source, up to 72MHZ, support 1,2,4,6,8,10,12,16,32, 64,128,256 frequency division
 - The AHB_CLK can be configured as the sampling clock source, up to 72MHz, and supports frequency 1,2,4,6,8,10,12,16,32
 - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- ◆ Supports timer trigger ADC sampling
- ◆ Interrupts when conversion ends, injection conversion ends, and analog watchdog events occur
- ◆ Single and continuous conversion modes
- ◆ Automatic scan mode from channel 1 to channel N
- ◆ Support for self-calibration
- ◆ Data alignment with embedded data consistency
- ◆ Sampling intervals can be programmed separately by channel
- ◆ Both regular conversions and injection conversions have external triggering options
- ◆ Continuous mode
- ◆ ADC power supply requirements: 2.4V to 3.6V
- ◆ ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
- ◆ ADC can use DMA operations, and DMA requests are generated during regular channel conversion.
- ◆ Analog watchdog function can monitor one, multiple, or all selected channels with great precision. When the monitored signal exceeds the preset threshold, an interruption will occur.

2.20 Temperature sensor (TS)

The temperature sensor generates a voltage that varies linearly with temperature in the range of $2.4V < V < 3.6V$. The temperature sensor is internally connected to the ADC_IN17 input channel for converting the output of the temperature sensor to digital values.

2.21 Beeper

The beeper module supports complementary outputs and can generate periodic signals to drive external passive buzzers. Used to generate a beep or the alarm to sound.

2.22 Cyclic redundancy check calculation unit (CRC)

Integrated CRC32 and CRC16 functions, the cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain any CRC calculation results. In many applications, CRC-based techniques are used

to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting flash memory errors, CRC cells can be used to calculate signatures of software in real time and compare them with signatures generated when linking and generating the software.

The CRC has the following features:

- ◆ CRC16: supports polynomials $X^{16} + X^{15} + X^2 + X^0$
- ◆ CRC32: supports polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- ◆ CRC16 calculation time: 1 AHB clock cycle (HCLK)
- ◆ CRC32 calculation time: 1 AHB clock cycle (HCLK)
- ◆ The initial value for cyclic redundancy computing is configurable
- ◆ Support DMA mode

2.23 Unique device serial number (UID)

N32G401F8S7-1 series products have two built-in unique device serial numbers of different lengths, which are 96-bit Unique Device ID (UID) and 128-bit Unique Customer ID (UCID). These two device serial numbers are stored in the system configuration block of flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32G401F8S7-1 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in flash memory.

UCID is 128-bit, which complies with the definition of national technology chip serial number. It contains the information related to chip production and version.

2.24 Serial wire debug port (SW-DP)

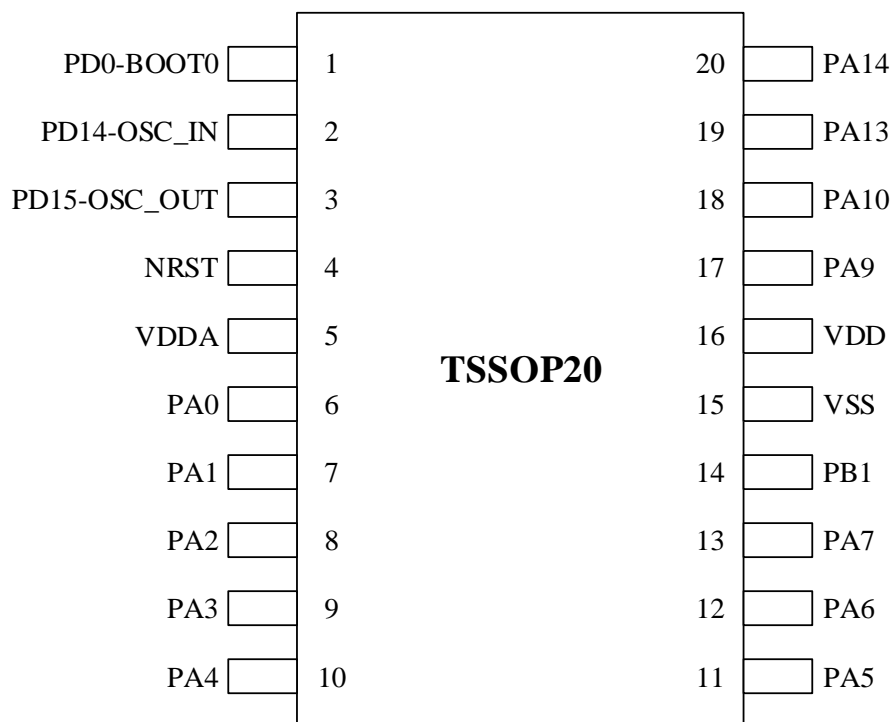
Embedded ARM SW-DP interface, which is serial single-line debugging interface, can achieve serial single-line debugging interface.

3 Pin and description

3.1 Pinouts

3.1.1 TSSOP20

Figure 3-1 N32G401F8S7-1 Series TSSOP20 pinout



3.2 Pin definition

Table 3-1 Pin Definitions

TSSOP20	Pin name (function after reset)	Type ⁽¹⁾	I/O ⁽²⁾	Fail-safe ⁽⁴⁾	Alternate functions ⁽³⁾	Additional functions
2	PD14-OSC_IN	I/O	FTa	Y	-	OSC_IN
3	PD15-OSC_OUT	I/O	FTa	Y	-	OSC_OUT
4	NRST	I	-	-	-	-
5	VDDA/VREF+	S	-	-	-	-
6	PA0	I/O	FTa	Y	USART2_CTS TIM2_CH1 TIMER2_ETR TIM5_CH1 TIM8_ETR SPI1_MISO I2S1_MCK EVENTOUT TIM1_CH1 UART4_TX	ADC_IN1 ⁽⁵⁾ WKUP2 RTC-TAMP2
7	PA1	I/O	FTa	Y	USART2_RTS TIM5_CH2 TIM2_CH2 EVENTOUT SPI1_NSS TIM1_CH1N	ADC1_IN2 ⁽⁵⁾
8	PA2	I/O	FTa	Y	USART2_TX TIM5_CH3 TIM2_CH3 I2C2_SDA EVENTOUT TIM8_BKIN TIM8_CH1	ADC_IN3 ⁽⁵⁾
9	PA3	I/O	FTa	Y	USART2_RX TIM5_CH4 I2C2_SCL EVENTOUT TIM8_CH2	ADC_IN4 ⁽⁵⁾
10	PA4	I/O	FTa	Y	USART2_CK I2C1_SCL SPI1_NSS I2S1_WS UART1_TX EVENTOUT LPTIM_OUT SPI2_NSS TIM8_CH3 I2S2_WS TIM4_CH3	ADC_IN5 ⁽⁵⁾

11	PA5	I/O	FTa	Y	SPI1_SCK I2C1_SDA I2S1_CK UART1_RX EVENTOUT LPTIM_IN1 TIM8_CH4 TIM4_CH4	ADC_IN6 ⁽⁶⁾
12	PA6	I/O	FTa	Y	SPI1_MISO I2S1_MCK TIM8_BKIN TIM3_CH1 TIM1_BKIN EVENTOUT BEEPER_OUT_P TIM8_CH3 USART2_TX TIM1_CH2N	ADC_IN7 ⁽⁶⁾
13	PA7	I/O	FTa	Y	SPI1_MOSI I2S1_SD TIM1_CH1N TIM8_CH1N TIM3_CH2 EVENTOUT USART2_RX BEEPER_OUT_N TIM1_CH4 TIM4_CH1	ADC_IN8 ⁽⁶⁾
14	PB1	I/O	FTa	Y	TIM1_CH3N TIM3_CH4 TIM8_CH3N UART4_RX EVENTOUT SPI1_SCK SPI2_MOSI I2S2_SD TIM4_CH2	ADC_IN10 ⁽⁶⁾
15	VSS	S	-	-	-	-
16	VDD	S	-	-	-	-
17	PA9	I/O	FT	Y	UART1_TX I2C2_SCL TIM1_CH2 EVENTOUT TIM8_BKIN SPI2_MISO I2S2_MCK	LPTIM_IN2

					MCO TIM1_CH3N	
18	PA10	I/O	FT	Y	UART1_RX I2C2_SDA SPI1_SCK SPI2_SCK I2S1_CK I2S2_CK TIM1_CH3 EVENTOUT TIM1_BKIN	LPTIM_ETR RTC_REFIN
19	PA13 ⁽⁷⁾	I/O	FT	Y	SWDIO SPI2_NSS I2S2_WS EVENTOUT SPI2_MISO	-
20	PA14 ⁽⁷⁾	I/O	FT	Y	SWCLK USART2_CK I2C1_SDA EVENTOUT SPI2_MOSI I2S2_SD	-
1	BOOT0/PD0	I/O	FT	Y	-	-

1. I = input, O = output, S = power supply
2. FT: 5V tolerant, FTa: 5V tolerant, with Analog function
3. This alternate function can be configured by the software to other pins (if the corresponding package model has such pins). For details, refer to the I/O and debugging Settings sections of the alternate function in the N32G401F8S7-1 user manual.
4. Fail-safe indicates that when the chip has no power input, a high input level is added to the IO. The high input level does not flood into the chip, resulting in a certain voltage on the power supply and current consumption.
5. The corresponding ADC channel is a fast channel and supports a maximum sampling rate of 4.2MSPS(12Bit).
6. The corresponding ADC channel is a slow channel, supporting a maximum sampling rate of 3.6MSPS(12Bit).
7. If MCU will enter STANDBY mode, before entering the STANDBY mode, if pins PA13 and PA14 are used as non-debug pins, and configured as input mode, it is necessary to add strong pull-down resistance on pins PA13 and PA14. The pull-down resistance is recommended to be within 10KΩ.

For the FT and FTa ports in the table, it is necessary to ensure that the voltage difference between the IO voltage and the power supply voltage is less than 3.6V

4 Electrical Characteristics

4.1 Parameter conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and maximum values

Unless otherwise specified, all minimums and maximums will be guaranteed under the worst ambient temperature, supply voltage and clock frequency conditions by performing tests on 100% of the product on the production line at ambient temperatures $T_A=25\text{ }^{\circ}\text{C}$.

Note at the bottom of each form that data obtained through characterization results, design simulation and/or process characteristics will not be tested on the production; Base on characterization, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean $\pm 3\Sigma$).

4.1.2 Typical numerical values

Unless otherwise specified, typical data are based on $T_A=25\text{ }^{\circ}\text{C}$ and $V_{DD}=3.3\text{V}$ ($2.4\text{V} \leq V_{DD} \leq 3.6\text{V}$ voltage range). These data are for design guidance only and not tested.

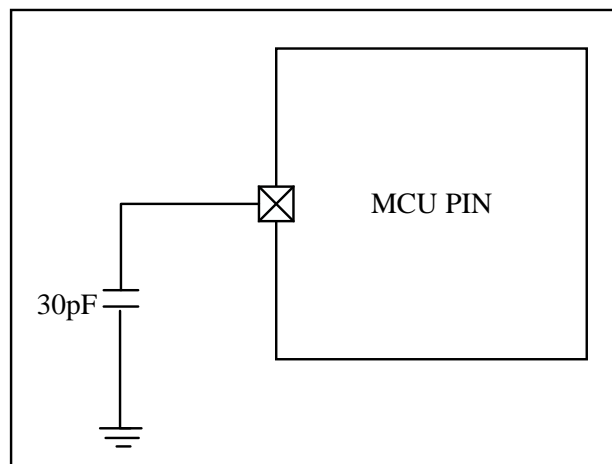
4.1.3 Typical curve

Unless otherwise specified, typical curves are for design guidance only and not tested.

4.1.4 Loading capacitor

The load conditions for measuring pin parameters are shown in Figure 4-1.

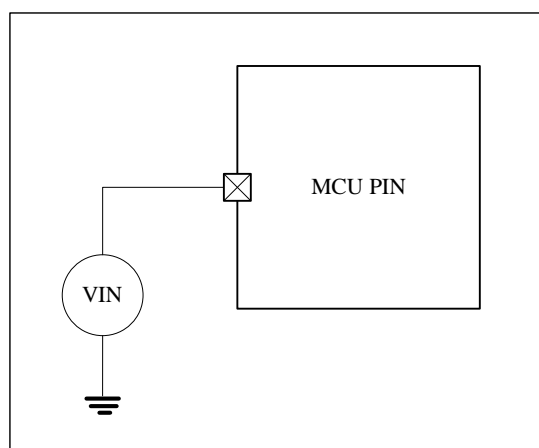
Figure 4-1 Pin loading conditions



4.1.5 Pin input voltage

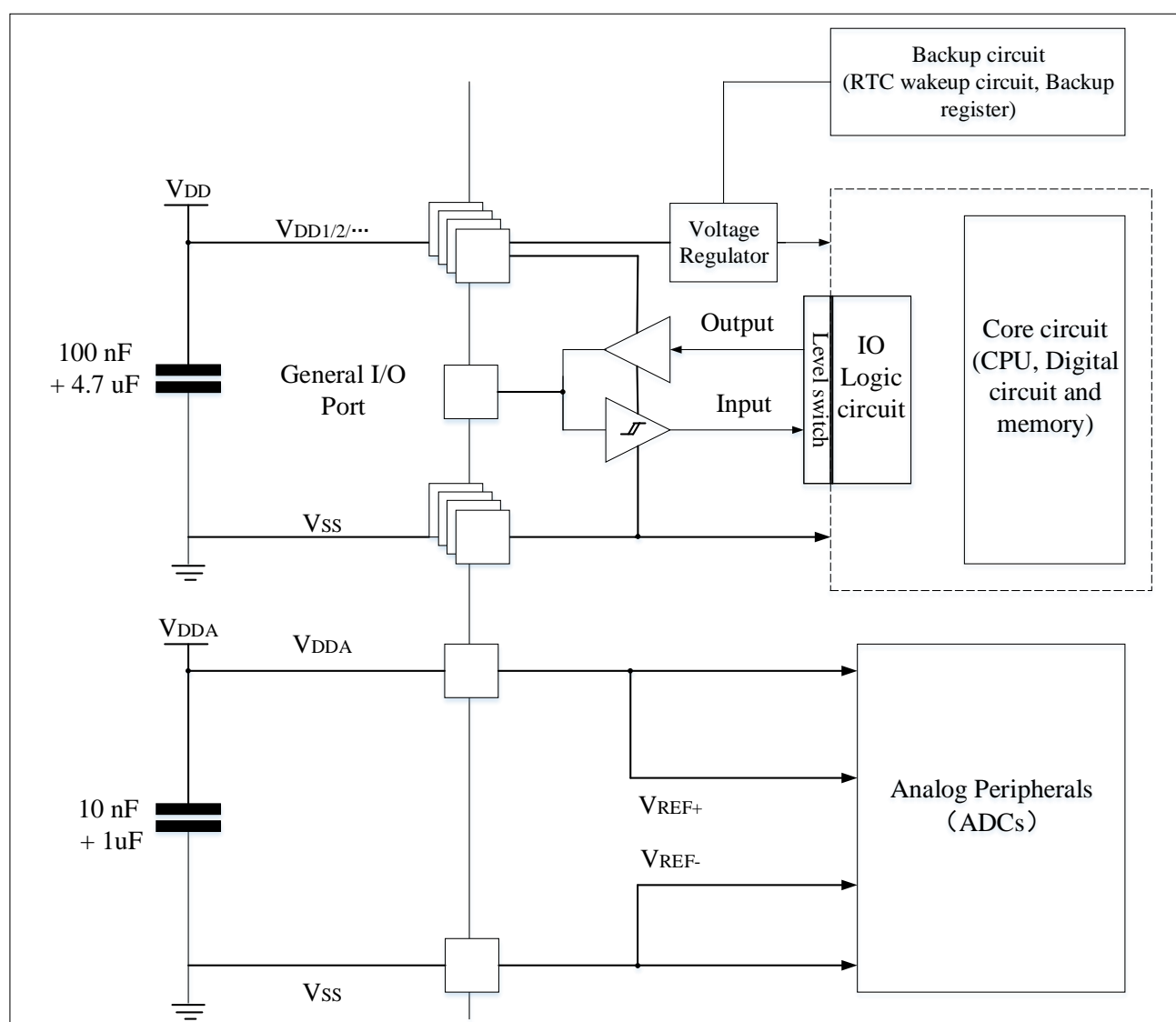
The measurement of the input voltage on the pin is shown in Figure 4-2.

Figure 4-2 Pin input voltage



4.1.6 Power supply scheme

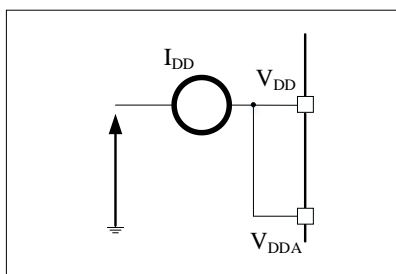
Figure 4-3 Power supply scheme



Note: Please refer to the hardware design guide for the capacitor connection method.

4.1.7 Current consumption measurement

Figure 4-4 Current consumption measurement scheme



4.2 Absolute maximum rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1, Table 4-2, Table 4-3). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage characteristics

Symbol	Describe	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DD} and V_{DDA}) ⁽¹⁾	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins ⁽³⁾	$V_{SS} - 0.3$	5.5	
	Input voltage on other pins ⁽²⁾	$V_{SS} - 0.3$	$V_{DD} + 0.3$	
$ \Delta V_{DDx} $	Voltage difference between different supply pins	-	50	mV
$ V_{SSx} - V_{SS} $	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD Electrostatic discharge voltage (human body model)	See section 4.3.11		

1. All power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply system within permissible limits.
2. V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.
3. When 5.5V is applied to the 5V tolerant pin, V_{DD} cannot be less than 2.25V.

Table 4-2 Current characteristics

Symbol	Describe	Max ⁽¹⁾	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) ⁽¹⁾⁽⁴⁾	150	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) ⁽¹⁾⁽⁴⁾	150	
I_{IO}	Output current sunk by I/O and control pin	12	
	Output current source by I/O and control pin	-12	
$I_{INJ(PIN)}^{(2)(3)}$	Injection current on NRST pin	-5/0	
	Injection current on other pins	±5	

1. All power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply system within permissible limits.
2. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current. $I_{INJ(PIN)}$ should not exceed its maximum value. Voltage characteristics refer to Table 4-1.
3. Reverse injection current can interfere with the analog performance of the device. See section 4.3.17.
4. When the maximum current occurs, the maximum allowable voltage drop of V_{DD} is $0.1V_{DD}$.

Table 4-3 Temperature Characteristics

Symbol	Describe	Value	Unit
T_{STG}	Storage temperature range	- 40 ~ + 150	°C
T_J	Maximum junction temperature	125	°C

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-4 General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32 ⁽²⁾	
f_{PCLK2}	Internal APB2 clock frequency	-	0	64 ⁽²⁾	
V_{DD}	Standard operating voltage	-	2.4	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD} ⁽¹⁾	2.4	3.6	V
T_A	Ambient temperature(temperature number 7)	7 suffix version	- 40	105	°C
T_J	Junction temperature range	7 suffix version	- 40	125	°C

1. It is recommended that the same power supply be used to power the V_{DD} and V_{DDA} . During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA} .
2. If APB1 and APB2 are running at the highest frequency, the system clock needs to be reduced to 64MHz.

4.3.2 Operating conditions at power-on and power-off

The parameters given in the following table are based on the ambient temperatures listed in Table 4-4.

Table 4-5 Operating conditions at power-on and power-off

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Supply voltage goes from 0 to V_{DD}	20	∞	$\mu s/V$
	V_{DD} fall time rate	Supply voltage drops from V_{DD} to 0	80	∞	

4.3.3 Embedded reset and power control module characteristics

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-6 Features of embedded reset and power control modules

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (PWR_CTRL.MSB = 0)	PLS[2:0]=011 (rising)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising)	2.76	2.88	3	V
		PLS[2:0]=111 (falling)	2.66	2.78	2.9	V
	Programmable voltage detector level selection (PWR_CTRL.MSB = 1)	PLS[2:0]=100 (rising)	3.15	3.28	3.41	V
		PLS[2:0]=100 (falling)	3.05	3.18	3.31	V
		PLS[2:0]=101 (rising)	3.24	3.38	3.52	V
		PLS[2:0]=101 (falling)	3.15	3.28	3.41	V
		PLS[2:0]=110 (rising)	3.34	3.48	3.62	V
		PLS[2:0]=110 (falling)	3.24	3.38	3.52	V
		PLS[2:0]=111 (rising)	3.44	3.58	3.72	V
		PLS[2:0]=111 (falling)	3.34	3.48	3.62	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PVDhyst}^{(1)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	VDD Power on/down Reset threshold	Falling edge	1.625	1.856	2.179	V
		Rising edge	1.648	1.893	2.236	
$V_{PDRhyst}^{(1)}$	PDR hysteresis	-	22	36	58	mV
$T_{RSTTEMPO}^{(1)}$	Reset temporization	-	-	0.8	4	ms

1. Guaranteed by design, not tested in production.

4.3.4 Embedded reference voltage

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-7 Built-in reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.164	1.2	1.236	V
$T_{S_vrefint}^{(1)}$	The sampling time of the ADC when reading the internal reference voltage	-	-	5	17 ⁽²⁾	μs
$V_{RERINT}^{(2)}$	Internal reference voltage spread over the temperature range	$V_{DD}=3.3\text{V} \pm 10\text{mV}$	-	-	10	mV
$T_{Coeff}^{(2)}$	Temperature coefficient	-	-	-	48	ppm/ $^{\circ}\text{C}$

1. The shortest sampling time is obtained through multiple loops in the application.

2. Guaranteed by design, not tested in production.

4.3.5 Power supply current characteristics

Current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, I/O pin flip rate, program location in memory, and code executed.

The measurement method of current consumption is described in Figure 4-4.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum current consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 72MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK} / 4$, $f_{PCLK2} = f_{HCLK} / 2$.
- $V_{DD}=3.63\text{V}$, ambient temperature equal to 105°C

The parameters given in Table 4-8 and Table 4-9 are based on the test at ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-8 Typical current consumption in operating mode where the data processing code is run from internal flash

Symbol	Parameter	Conditions	f _{HCLK}	Typ ⁽¹⁾	Unit
				VDD=3.63V, T _A = 105°C	
I _{DD} ⁽²⁾	Supply current in RUN mode Supply current in RUN mode	External clock, enable all peripherals	72MHz	9.58	mA
			64MHz	8.92	
			32MHz	6.25	
			16MHz	4.92	
			8MHz	4.30	
		External clock, disable all peripherals	72MHz	7.92	
			64MHz	7.43	
			32MHz	5.51	
			16MHz	4.55	
			8MHz	4.02	
I _{DD} ⁽²⁾	Supply current in RUN mode	Internal clock, enable all peripherals	72MHz	7.25	mA
			64MHz	6.54	
			32MHz	3.73	
			16MHz	2.34	
			8MHz	1.69	
		Internal clock, disable all peripherals	72MHz	5.49	
			64MHz	4.98	
			32MHz	2.95	
			16MHz	1.95	
			8MHz	1.39	

1. Evaluated by characterization, not tested in production.
2. PLL is enabled when f_{HCLK} > 8MHz.

Table 4-9 Typical current consumption in sleep mode, code running in internal flash running

Symbol	Parameter	Conditions	f _{HCLK}	Typ ⁽¹⁾	Unit
				VDD=3.63V, T _A = 105°C	
I _{DD} ⁽²⁾	Supply current in sleep mode	External clock, enable all peripherals	72MHz	7.59	mA
			64MHz	7.14	
			32MHz	5.35	
			16MHz	4.47	
			8MHz	4.08	
		External clock, disable all peripherals	72MHz	5.74	
			64MHz	5.50	
			32MHz	4.54	
			16MHz	4.06	
			8MHz	3.77	
I _{DD} ⁽²⁾	Supply current in sleep mode	Internal clock, enable all peripherals	72MHz	5.15	mA
			64MHz	4.68	
			32MHz	2.80	
			16MHz	1.87	
			8MHz	1.45	
		Internal clock, disable all peripherals	72MHz	3.21	
			64MHz	2.96	
			32MHz	1.94	
			16MHz	1.44	
			8MHz	1.14	

1. Based on characterization, not tested in production.
2. PLL is enabled when f_{HCLK}>8MHz.

4.3.5.2 Typical current consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 72MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 4-4.
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider). When the peripheral is turned on: f_{PCLK1} = f_{HCLK} /4, f_{PCLK2} = f_{HCLK} /2, f_{ADCCLK} = f_{HCLK} /2.

Table 4-10 Typical current consumption in operating mode, where data processing code is run from internal Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ ⁽¹⁾		Unit
				Enable all peripherals	Disable all peripherals	
$I_{DD}^{(2)}$	Supply current in operation mode	External clock	72MHz	8.08	6.38	mA
			64MHz	7.40	5.92	
			32MHz	4.75	4.02	
			16MHz	3.45	3.05	
			8MHz	2.81	2.52	
$I_{DD}^{(2)}$	Supply current in operation mode	Internal clock	72MHz	6.75	4.98	mA
			64MHz	6.04	4.47	
			32MHz	3.25	2.51	
			16MHz	1.92	1.52	
			8MHz	1.29	0.97	

- Typical values are measured at $T_A = 25^{\circ}C$ and $V_{DD} = 3.3V$.
- PLL is enabled when $f_{HCLK} > 8MHz$.

Table 4-11 Typical current consumption in sleep mode

Symbol	Parameter	Condition	f_{HCLK}	Typ ⁽¹⁾		Unit
				Enable all peripherals ⁽²⁾	Disable all peripherals	
$I_{DD}^{(3)}$	Supply current in sleep mode	External clock	72MHz	6.07	4.25	mA
			64MHz	5.64	4.01	
			32MHz	3.86	3.05	
			16MHz	2.98	2.57	
			8MHz	2.58	2.28	
$I_{DD}^{(3)}$	Supply current in sleep mode	Internal clock	72MHz	4.65	2.75	mA
			64MHz	4.19	2.53	
			32MHz	2.36	1.54	
			16MHz	1.45	1.01	
			8MHz	1.03	0.72	

- Typical values are measured at $T_A = 25^{\circ}C$ and $V_{DD} = 3.3V$.
- When ADC is on, 0.2mA(1MSPS) additional current consumption is added. In the application environment, this part of the current is increased only when the ADC is turned ON (set ADC_CTRL2.ON bit).
- PLL is enabled when $F_{HCLK} > 8MHz$.

4.3.5.3 Low power mode current consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level of $-V_{DD}$ or V_{SS} (no load).
- All peripherals are disabled unless otherwise noted.

Table 4-12 Typical current consumption in shutdown and standby mode

Symbol	Parameter	Condition	Typ ⁽¹⁾			Unit
			V _{DD} = 3.3 V T _A = -40 °C	V _{DD} = 3.3 V T _A = 25 °C	V _{DD} = 3.3 V T _A = 105 °C	
I _{DD_STOP2}	Supply current in Stop mode 2 (STOP2)	Low-speed internal RC oscillator is on, RTC is running, SRAM retention, all I/O states retention, and the independent watchdog is off	1.31	3.65	58.8	μA
I _{DD_STANDBY}	Supply current in STANDBY mode	Low-speed internal RC oscillator and independent watchdog are on, RTC is running , SRAM retention	0.94	1.73	20.3	
		Low-speed internal RC oscillator is on, RTC is running , SRAM retention, independent watchdog is off	0.92	1.67	20.2	
		Low-speed internal RC oscillator is on, RTC is running , SRAM not retention, independent watchdog is off	0.85	1.49	17.6	
		Low-speed internal RC oscillator is on, RTC is off , SRAM not retention, independent watchdog is off	0.77	1.39	17.4	

1. Guaranteed by characterization, not tested in production.

4.3.6 External clock source characteristics

4.3.6.1 High-speed external clock source (HSE)

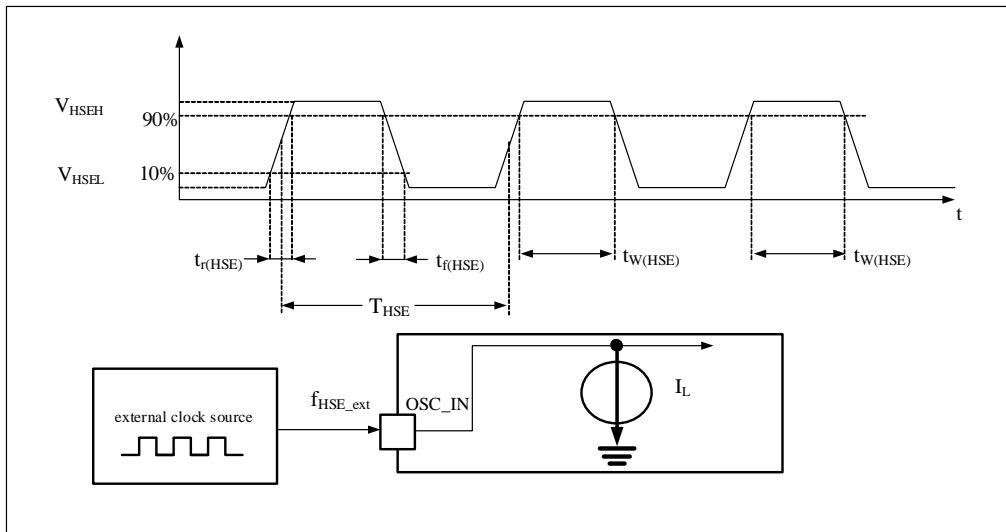
The characteristic parameters in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage refer to the conditions specified in Table 4-4.

Table 4-13 High-speed external user clock features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{HSE_ext}	User external clock frequency ⁽¹⁾	-	4	8	32	MHz
V _{HSEH}	OSC_IN Input pin high level voltage ⁽¹⁾		0.8V _{DD}	-	V _{DD}	V
V _{HSEL}	OSC_IN Input pin low level voltage ⁽¹⁾		V _{SS}	-	0.2V _{DD}	
t _{w(HSE)}	Time when OSC_IN is high or low ⁽¹⁾		16	-	-	ns
t _{r(HSE)} t _{f(HSE)}	OSC_IN rise or fall time ⁽¹⁾		-	-	20	
DuCy _(HSE)	Duty cycle ⁽¹⁾	-	45	-	55	%
I _L	OSC_IN Input leakage current ⁽¹⁾	V _{SS} ≤ V _{IN} ≤ V _{DD}	-1	-	+1	μA

1. Guaranteed by design, not tested in production.

Figure 4-5 AC timing diagram of an external high-speed clock source



High-speed external clock generated using a crystal/ceramic resonator

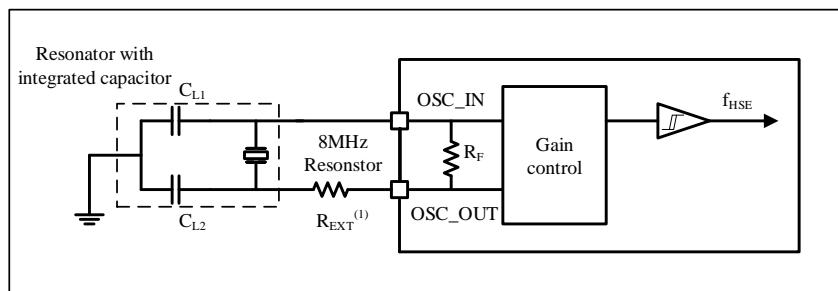
High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Table 4-14 HSE 4~32MHz oscillator characteristics ⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	C	160	-	K Ω
i_2	HSE driving current	$V_{DD} = 3.3\text{ V}$, $V_{IN} = V_{SS}$ 30 pF load	-	1.7	-	mA
g_m	Oscillator transconductance	Startup	-	10	-	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time (8M crystal)	V_{DD} is stabilized	-	7	-	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the start time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-6 typical application using 8MHz crystal



1. The R_{EXT} value depends on the properties of the crystal.

4.3.7 Internal clock source characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with Table 4-4.

4.3.7.1 High speed internal (HSI) RC oscillator

Table 4-15 HSI oscillator characteristics ⁽¹⁾⁽²⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	$V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}} = 25^{\circ}\text{C}$, after calibration	7.94 ⁽³⁾	8	8.04 ⁽³⁾	MHz
DuCy _(HSD)	Duty cycle	-	45	-	55	%
ACC _{HSI}	Accuracy of HSI oscillator ⁽⁴⁾	$V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}} = -40\sim 105^{\circ}\text{C}$	-1.5	-	2	%
		$V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}} = -10\sim 85^{\circ}\text{C}$	-1.2	-	1.6	%
		$V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}} = 0\sim 70^{\circ}\text{C}$	-1	-	1.2	%
$t_{\text{SU(HSD)}}$	HSI oscillator startup time	-	-	-	6	μs
$I_{\text{DD(HSD)}}$	HSI oscillator power consumption	-	-	120	-	μA

- $V_{\text{DD}} = 3.3\text{V}$, $T_{\text{A}} = -40\sim 105^{\circ}\text{C}$ unless otherwise specified.
- Guaranteed by design, not tested in production.
- Production calibration accuracy, excluding welding effects. Welding brings about 1% frequency deviation range.
- Frequency deviation includes the effect of welding, data is from sample testing, not tested in production.

4.3.7.2 Low speed internal (LSI) RC oscillator

Table 4-16 LSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{LSI}}^{(2)}$	Output frequency	25°C calibration, $V_{\text{DD}} = 3.3\text{V}$	38.8	40	41.2	KHz
		$V_{\text{DD}} = 2.4\text{V}$ to 3.6V , $T_{\text{A}} = -40 \sim 105^{\circ}\text{C}$	30	40	60	KHz
$t_{\text{SU(LSI)}}^{(2)}$	LSI oscillator startup time	-	-	40	80	μs
$I_{\text{DD(LSI)}}^{(2)}$	LSI oscillator power consumption	-	-	0.1	-	μA

- $V_{\text{DD}} = 3.3\text{V}$, $T_{\text{A}} = -40\sim 105^{\circ}\text{C}$, unless otherwise specified.
- Guaranteed by design, not tested in production.

4.3.8 Wakeup time from low power mode

The wake-up time listed in Table 4-17 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- Stop or standby mode: clock source is RC oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

All times were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-17 Wakeup time in low power mode

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}^{(1)}$	Wake up from SLEEP mode	7	HCLK
$t_{WUSTOP0}^{(1)}$	Wake up from STOP0 mode	15	μs
$t_{WUSTOP2}^{(1)}$	Wake up from STOP2 mode	33	μs
$t_{WUSTDBY}^{(1)}$	Wake up from STANDBY mode	75	μs

1. The wake up time is measured from the start of the wake up event until the first instruction is read by the user program.

4.3.9 PLL characteristics

The parameters listed in Table 4-18 are measured when the ambient temperature and power supply voltage refer to the conditions in Table 4-4.

Table 4-18 PLL features

Symbol	Parameter	Value			Unit
		Min	Typ	Max ⁽¹⁾	
f_{PLL_IN}	PLL input clock	4	8	32	MHz
	PLL Input clock duty cycle	40	50	60	%
f_{PLL_OUT}	PLL output clock ⁽²⁾	32	-	72	MHz
t_{LOCK}	PLL ready indicates signal output time ⁽³⁾	-	-	150	μs
Jitter	RMS cycle-to-cycle jitter @72MHz	-	8	-	ps
I_{pll}	Operating Current of PLL @72MHz VCO frequency. ⁽¹⁾	-	600	-	μA

1. Guaranteed by characterization results, not tested in production.
2. Care needs to be taken to use the correct frequency doubling factor to input the clock frequency according to PLL so that f_{PLL_OUT} is within the allowable range.
3. Guaranteed by design, not tested in production.

4.3.10 FLASH characteristics

Unless otherwise specified, all characteristic parameters are obtained at $T_A = -40 \sim 105^\circ C$.

Table 4-19 Flash characteristics

Symbol	Parameter	Condition	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
t_{prog}	32-bit programming time	$T_A = -40 \sim 105^\circ C$	-	60	-	μs
t_{ERASE}	Page (2K bytes) erase time	$T_A = -40 \sim 105^\circ C$	-	12.5	-	ms
t_{ME}	Mass erase time	$T_A = -40 \sim 105^\circ C$	-	-	20	ms
I_{DD}	The power supply current	Read mode, $f_{HCLK}=72MHz$, 2 waiting cycles, $V_{DD}=3.3V$	-	-	3.231	mA
		Write mode, $f_{HCLK}=72MHz$, $V_{DD}=3.3V$	-	-	6.5	mA
		Erase mode, $f_{HCLK}=72MHz$, $V_{DD}=3.3V$	-	-	4.5	mA
		Power-down mode, $V_{DD}=3.0$ to $3.6V$	-	-	4.63	μA
V_{prog}	Programming voltage	-	2.4	-	3.6	V

1. Guaranteed by design, not tested in production.

Table 4-20 Flash endurance and data retention

Symbol	Parameter	Condition	Min ⁽¹⁾	Unit
N _{END}	Endurance (note: erase times)	T _A = -40~105 °C(7 suffix versions)	10	Kcycle
t _{RET}	Data retention	T _A = 125°C	10	Years

1. Guaranteed by characterization results, not tested in production.

4.3.11 Absolute maximum (electrical sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-21 Absolute maximum ESD value

Symbol	Parameter	Condition	Type	Max ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, In accordance with MIL-STD-883K Method 3015.9	3A	4000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charging device model)	T _A = +25 °C, In accordance with ESDA/JEDEC JS-002-2018	C3	2000	

1. Guaranteed by characterization results, not tested in production.

Static Latch up

To evaluate the locking performance, two complementary static locking tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78E IC latch standard.

Table 4-22 Electrical sensitivity

Symbol	Parameter	Condition	Type
LU	Static locking classes	T _A = +105 °C, in accordance with JESD78E	II class A

4.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-23 I/O static characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL port	V_{SS}	-	0.8	V
V_{IH}	Input high level voltage		2	-	5.5	
V_{IL}	Input low level voltage	CMOS port	V_{SS}	-	$0.35V_{DD}$	
V_{IH}	Input high level voltage		$0.65V_{DD}$	-	$V_{DD}+0.5$	
V_{hys}	Schmitt trigger voltage lag ⁽¹⁾	$V_{DD} = 3.3\text{ V} / 2.5\text{ V}$	200	-	-	mV
I_{lkg}	Input leakage current ⁽²⁾	$V_{DD}=\text{Maximum}$ $V_{PAD} = 0$ or $V_{PAD} = V_{DD}$ ⁽⁴⁾	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistance ⁽³⁾	$V_{DD} = 3.3\text{ V}, V_{IN} = V_{SS}$	80	-	220	$\text{K}\Omega$
		$V_{DD} = 2.5\text{ V}, V_{IN} = V_{SS}$	90	-	300	$\text{K}\Omega$
R_{PD}	Weak pull-down equivalent resistance ⁽³⁾	$V_{DD} = 3.3\text{ V}, V_{IN} = V_{DD}$	80	-	220	$\text{K}\Omega$
		$V_{DD} = 2.5\text{ V}, V_{IN} = V_{DD}$	90	-	300	$\text{K}\Omega$
C_{IO}	Capacitance of I/O pins	-	-	5	-	pF

- The hysteresis voltage of Schmitt trigger switching level. Guaranteed by characterization results, not tested in production.
- The leakage current may be higher than the maximum if there is reverse current in adjacent pins.
- Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.
- V_{PAD} refers to the input voltage of the IO pin.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

- For V_{IH} :
 - If V_{DD} is between [2.4V~3.08V]; Use CMOS features but include TTL.
 - If V_{DD} is between [3.08V~3.6V]; Use TTL features but include CMOS.
- For V_{IL} :
 - If V_{DD} is between [2.4V~3.6V]; Use CMOS features but include TTL.

Output drive current

GPIO (universal input/output port) can absorb or output up to +/-12mA current.

Output voltage

Unless otherwise specified, guaranteed by design, not tested in production. The parameters listed in Table 4-24 were measured using ambient temperature and V_{DD} supply voltage in accordance with Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-24 IO Output drive capability characteristics

Drive class	$I_{OH}^{(1)}, V_{DD}=3.3\text{V}$	$I_{OL}^{(1)}, V_{DD}=3.3\text{V}$	$I_{OH}^{(1)}, V_{DD}=2.5\text{V}$	$I_{OL}^{(1)}, V_{DD}=2.5\text{V}$	Unit
2	-2	2	-1.5	1.5	mA
4	-4	4	-3	3	mA
8	-8	8	-7	7	mA
12	-12	12	-11	11	mA

- Guaranteed by design, not tested in production.

Table 4-25 Output voltage characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level	$V_{DD} = 3.3\text{ V}$, $I_{OL}^{(3)} = 2\text{mA}, 4\text{mA}, 8\text{mA}, \text{ and } 12\text{mA}$	V_{SS}	0.4	V
		$V_{DD} = 2.5\text{ V}$, $I_{OL}^{(3)} = 1.5\text{mA}, 3\text{mA}, 7\text{mA}, \text{ and } 11\text{mA}$	V_{SS}	0.4	
$V_{OH}^{(2)}$	Output high level	$V_{DD} = 3.3\text{ V}$, $I_{OH}^{(3)} = -2\text{mA}, -4\text{mA}, -8\text{mA}, \text{ and } -12\text{mA}$	2.4	V_{DD}	
		$V_{DD} = 2.5\text{ V}$, $I_{OH}^{(3)} = -1.5\text{mA}, -3\text{mA}, -7\text{mA}, \text{ and } -11\text{mA}$	1.8	V_{DD}	

1. The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS} .
2. The current I_{IO} output from the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD} .
3. Actual drive capability see Table 4-24.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in Figure 4-7 and Table 4-26 respectively.

Unless otherwise specified, the parameters listed in Table 4-26 were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-26 Input/output AC characteristics ⁽¹⁾

GPIOx_DS.DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
00 (2mA)	$f_{\max(IO)out}$	Maximum frequency ⁽²⁾	$C_L = 5\text{ pF}$, $V_{DD} = 3.3\text{ V}$	-	72	MHz
			$C_L = 5\text{ pF}$, $V_{DD} = 2.5\text{ V}$	-	50	
	$t_{(IO)out}$	Output delay (A to pad)	$C_L = 5\text{ pF}$, $V_{DD} = 3.3\text{ V}$	-	3.66	ns
			$C_L = 5\text{ pF}$, $V_{DD} = 2.5\text{ V}$	-	4.72	
10 (4mA)	$t_{(IO)in}$	Input delay (pad to Y)	$C_L = 50\text{ fF}$, $V_{DD} = 2.97\text{ V}$, $V_{DDD} = 0.81\text{ V}$ Input characteristics at 1.8V and 2.5V are derated	-	2	ns
	$f_{\max(IO)out}$	Maximum frequency ⁽²⁾	$C_L = 10\text{ pF}$, $V_{DD} = 3.3\text{ V}$	-	72	MHz
			$C_L = 10\text{ pF}$, $V_{DD} = 2.5\text{ V}$	-	60	
	$t_{(IO)out}$	The output delay (A to pad)	$C_L = 10\text{ pF}$, $V_{DD} = 3.3\text{ V}$	-	3.5	ns
			$C_L = 10\text{ pF}$, $V_{DD} = 2.5\text{ V}$	-	4.5	
01 (8mA)	$t_{(IO)in}$	Input delay (pad to Y)	$C_L = 50\text{ fF}$, $V_{DD} = 2.97\text{ V}$, $V_{DDD} = 0.81\text{ V}$ Input characteristics at 1.8V and 2.5V are derated	-	2	ns
	$f_{\max(IO)out}$	Maximum frequency ⁽²⁾	$C_L = 20\text{ pF}$, $V_{DD} = 3.3\text{ V}$	-	72	MHz
			$C_L = 20\text{ pF}$, $V_{DD} = 2.5\text{ V}$	-	70	
	$t_{(IO)out}$	The output delay (A to pad)	$C_L = 20\text{ pF}$, $V_{DD} = 3.3\text{ V}$	-	3.42	ns
			$C_L = 20\text{ pF}$, $V_{DD} = 2.5\text{ V}$	-	4.37	
11 (12mA)	$t_{(IO)in}$	Input delay (pad to Y)	$C_L = 50\text{ fF}$, $V_{DD} = 2.97\text{ V}$, $V_{DDD} = 0.81\text{ V}$ Input characteristics at 1.8V and 2.5V are derated	-	2	ns
	$f_{\max(IO)out}$	Maximum frequency ⁽²⁾	$C_L = 30\text{ pF}$, $V_{DD} = 3.3\text{ V}$	-	72	MHz
			$C_L = 30\text{ pF}$, $V_{DD} = 2.5\text{ V}$	-	70	
	$t_{(IO)out}$	The output delay (A to pad)	$C_L = 30\text{ pF}$, $V_{DD} = 3.3\text{ V}$	-	3.34	ns
			$C_L = 3\text{ pF}$, $V_{DD} = 2.5\text{ V}$	-	4.26	

GPIOx_DS.DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
	$t_{(IO)in}$	Input delay (pad to Y)	$C_L = 50 \text{ fF}$, $V_{DD} = 2.97 \text{ V}$, $V_{DDD} = 0.81 \text{ V}$ Input characteristics at 1.8V and 2.5V are derated	-	2	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O port drive capability can be configured via GPIOx_DS.DSy[1:0]. Refer the description of the GPIO port drive capability configuration register in N32G401F8S7-1 user manual.
2. The maximum frequency is defined in Figure 4-7.
3. Propagation delay is defined in Figure 4-8.

Figure 4-7 Definition of input/output AC characteristics

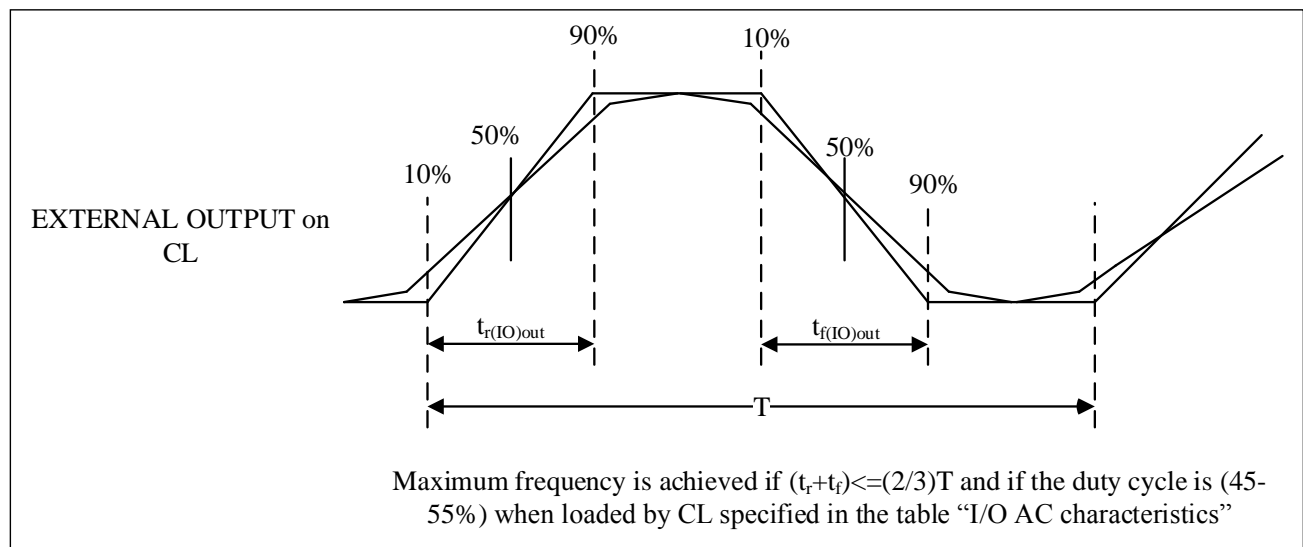
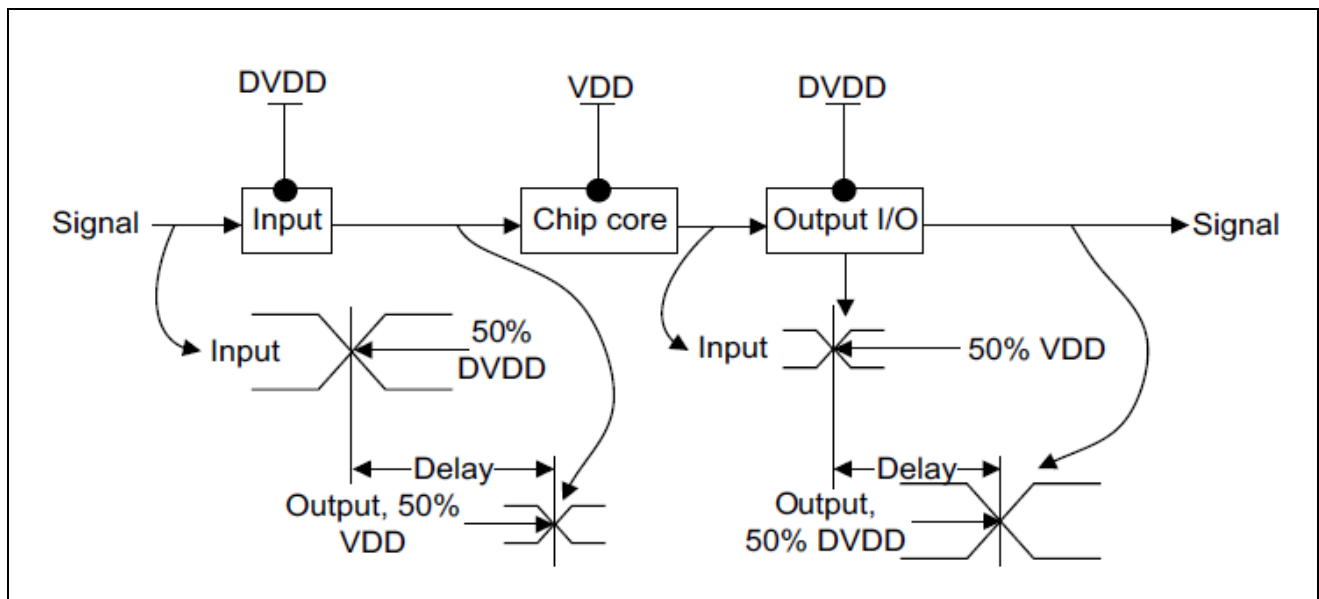


Figure 4-8 Propagation delay



4.3.13 NRST pin characteristics

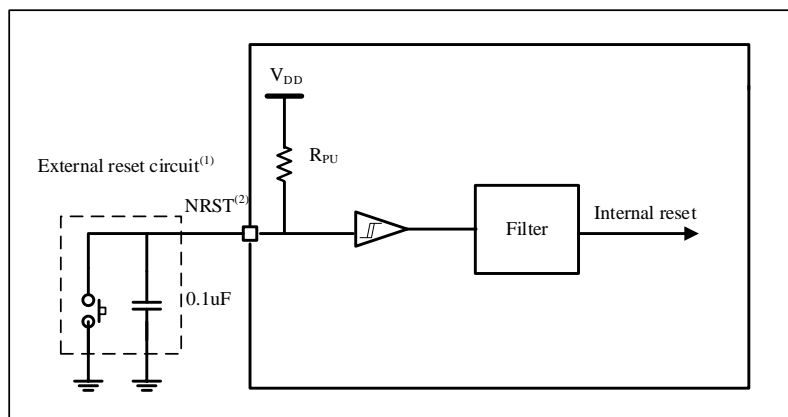
NRST pin is integrated with pull-up resistor, R_{PU} (see Table 4-23). Unless otherwise specified, the parameters listed in Table 4-27 were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-27 NRST pin characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST input low level voltage	$V_{DD} = 3.3\text{ V}$	V_{SS}	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST input high level voltage	$V_{DD} = 3.3\text{ V}$	2	-	VDD	
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis	-	-	100	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{DD} = 3.3\text{ V}$	30	50	70	K Ω
$V_{F(NRST)}^{(1)}$	NRST input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST input not filtered pulse	-	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal reset source	10	13	-	μs

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is designed as a true resistor in series for a not switchable PMOS implementation. The resistance of this PMOS switch is very small (about 10%).

Figure 4-9 Recommended NRST pin protection



1. Filter action.
2. The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in Table 4-27, otherwise the MCU cannot be reset.

4.3.14 Timer characteristics

The parameters listed in Table 4-28 and Table 4-29 are guaranteed by design.

See section 4.3.12 for details on the features of the I/O reuse function pins (output comparison, input capture, external clock, PWM output).

Table 4-28 TIM1/8 characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	t_{TIMCLK}
		$f_{TIMCLK}=72MHz$	13.9	-	ns
f_{EXT}	Timer CH1 to CH2 external clock frequency	-	0	$f_{TIMCLK}/2$	MHz
		$f_{TIMCLK}=72MHz$	0	36	MHz
Re_{TIM}	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	t_{TIMCLK}
		$f_{TIMCLK}=72MHz$	0.0319	910	μs
t_{MAX_COUNT}	Maximum count	-	-	65536 x 65536	t_{TIMCLK}
		$f_{TIMCLK}=72MHz$	-	59.625	s

Table 4-29 TIM2/3/4/5 characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer time resolution	-	1	-	t_{TIMCLK}
		$f_{TIMCLK}=64MHz$	15.62	-	ns
$f_{EXT}^{(1)}$	Timer CH1 to CH2 external clock frequency	-	0	$f_{TIMCLK}/2$	MHz
		$f_{TIMCLK}=64MHz$	0	32	MHz
Re_{TIM}	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	t_{TIMCLK}
		$f_{TIMCLK}=64MHz$	0.01562	1024	μs
t_{MAX_COUNT}	Maximum count with 32-bit counter	-	-	65536 x 65536	t_{TIMCLK}
		$f_{TIMCLK}=64MHz$	-	67.108	s

Note: If f_{TIMCLK} is running at the highest frequency, the system clock needs to be reduced to 64MHz.

Table 4-30 LPTIM characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(LPTIM)}$	Timer time resolution	-	1	-	$t_{LPTIMCLK}$
		$f_{LPTIMCLK}=32MHz$	31.25	-	ns
$f_{EXT}^{(1)}$	IN2 and OUT external clock frequency	-	0	32	MHz
		$f_{LPTIMCLK}=32MHz$	0	32	MHz
Re_{LPTIM}	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{LPTIMCLK}$
		$f_{LPTIMCLK}=32MHz$	0.03125	2048	μs
t_{MAX_COUNT}	Maximum count with 32-bit counter	-	-	65536 x 65536	$t_{LPTIMCLK}$
		$f_{LPTIMCLK}=32MHz$	-	134.217	s

Note: If $f_{LPTIMCLK}$ is running at the highest frequency, the system clock needs to be reduced to 64MHz.

Table 4-31 IWDG counting maximum and minimum reset time (LSI = 40 KHz)

Prescaler	IWDG_PREDIV. PD[2:0]	Min ⁽¹⁾ IWDG_RELV.REL[11:0]=0	Max ⁽¹⁾ IWDG_RELV.REL[11:0]=0xFFFF	Unit
/4	000	0.1	409.6	ms
/8	001	0.2	819.2	
/16	010	0.4	1638.4	
/32	011	0.8	3276.8	
/64	100	1.6	6553.6	

/128	101	3.2	13107.2	
/256	11x	6.4	26214.4	

1. Guaranteed by design, not tested in production.

Table 4-32 WWDG counting maximum and minimum reset time (APB1 PCLK1 = 32MHz)

Prescaler	WWDG_CFG.TI MERB[1:0]	Min ⁽¹⁾ WWDG_CFG.W[13:0]=0x3F	Max ⁽¹⁾ WWDG_CFG.W[13:0]=0x3FFF	Unit
/1	00	0.128	2089	ms
/2	01	0.256	4178	
/3	10	0.512	8356	
/4	11	1.024	16712	

1. Guaranteed by design, not tested in production.

4.3.15 I²C Interface characteristics

Unless otherwise specified, the parameters listed in Table 4-33 were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

The I²C interface of the N32G401F8S7-1 product conforms to the standard I²C communication protocol, but has the following limitations: SDA and SCL are not "true" open leak pins, and when configured for open leak output, the PMOS tube between the pin and V_{DD} is closed, but still exists.

I²C interface features are listed in Table 4-33. See Section 4.3.12 for details about the features of the input/output multiplexing function pins (SDA and SCL).

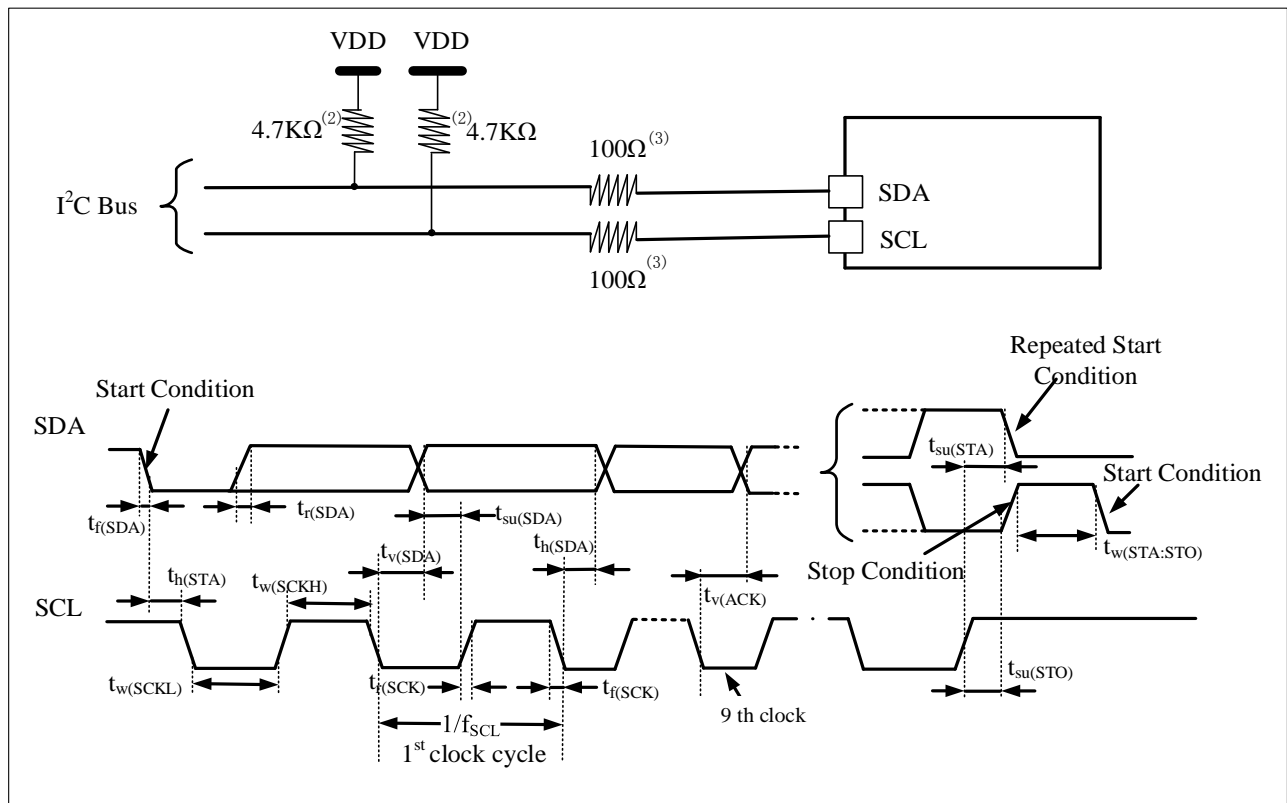
Table 4-33 I²C interface characteristics

Symbol	Parameter	Standard mode ^{(1) (2)}		Fast mode ^{(1) (2)}		Fast + mode ^{(1) (2)}		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	μs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.50	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{su(STA)}$	Repeat start condition setup time	4.7	-	0.6	-	0.26	-	μs
$t_{h(SDA)}$	SDA data hold time	-	3.4	-	0.9	-	0.4	μs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20+0.1Cb	300	-	120	ns
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	0.26	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.50	-	μs
C_b	Capacitive load for per bus	-	400	-	400	-	100	pf
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	0	35	0	35	0	35	μs
$t_v(SDA)$	Data validity time	-	3.45	-	0.9	-	0.45	
$t_v(ACK)$	Response time	-	3.45	-	0.9	-	0.45	

1. Guaranteed by design, not tested in production.

- To achieve the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 4MHz.

Figure 4-10 I²C bus AC waveform and measuring circuit ⁽¹⁾



- The measuring point is set at $0.3V_{DD}$ and $0.7V_{DD}$.
- The pull-up resistance depends on the I2C interface speed.
- The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.16 SPI/I²S interface characteristics

Unless otherwise specified, the SPI parameters listed in Table 4-34 and the I²S parameters listed in Table 4-35 are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

See section 4.3.12 for details on the characteristics of the I/O reuse pins (NSS, SCLK, MOSI, MISO for SPI, WS, CLK, SD for I²S).

Table 4-34 SPI characteristics ⁽¹⁾

Symbol	Parameter	Condition		Min	Max	Unit
f_{SCLK} $1/t_c(SCLK)$	SPI clock frequency	Master mode		-	18	MHz
		Slave mode		-	18	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		-	8	ns
DuCy(SCK)	SPI from the input clock duty cycle	Slave mode		45	55	%
$t_{su(NSS)}^{(1)}$	NSS setup time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}^{(1)}$ $t_{w(SCLKL)}^{(1)}$	SCLK high and low time	Master mode		$t_{PCLK} - 2$	$t_{PCLK} + 2$	ns
$t_{su(MI)}^{(1)}$	Data input setup time	Master mode	SPI1	4.5	-	ns
			SPI2	4.5	-	
$t_{su(SI)}^{(1)}$		Slave mode	SPI1	4.5	-	
			SPI2	4.5	-	
$t_{h(MI)}^{(1)}$	Data input hold time	Master mode	SPI1	2.5	-	ns
			SPI2	2.5	-	
$t_{h(SI)}^{(1)}$		Slave mode	SP1	2.5	-	
			SP2	2.5	-	
$t_{a(SO)}^{(1)(2)}$	Data output access time	Slave mode, $f_{PCLK} = 18MHz$		0	$3t_{PCLK}$	ns
$t_{dis(SO)}^{(1)(3)}$	Disable time of data output	Slave mode		2	10	ns
$t_{v(SO)}^{(1)}$	Valid time of data output	Slave mode (after enable edge)	SPI1	-	15	ns
			SPI2	-	15	
$t_{v(MO)}^{(1)}$		Master mode (after enabling edge)	SPI1	-	5.5	
			SPI2	-	5.0	
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	SPI1	4.0	-	ns
			SPI2	4.0	-	
$t_{h(MO)}^{(1)}$		Master mode (after enabling edge)	SPI1	-1.0	-	
			SPI2	-1.0	-	

1. Guaranteed by design, not tested in production.
2. The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.
3. The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

Figure 4-11 SPI timing diagram-slave mode and CLKPHA=0

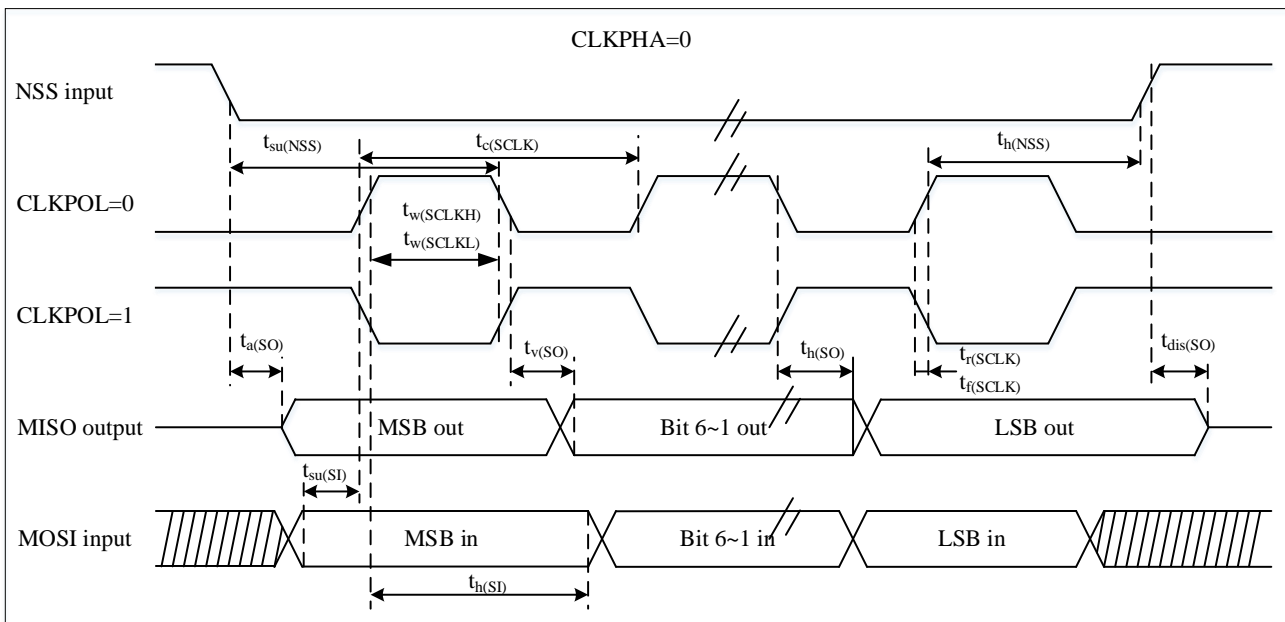
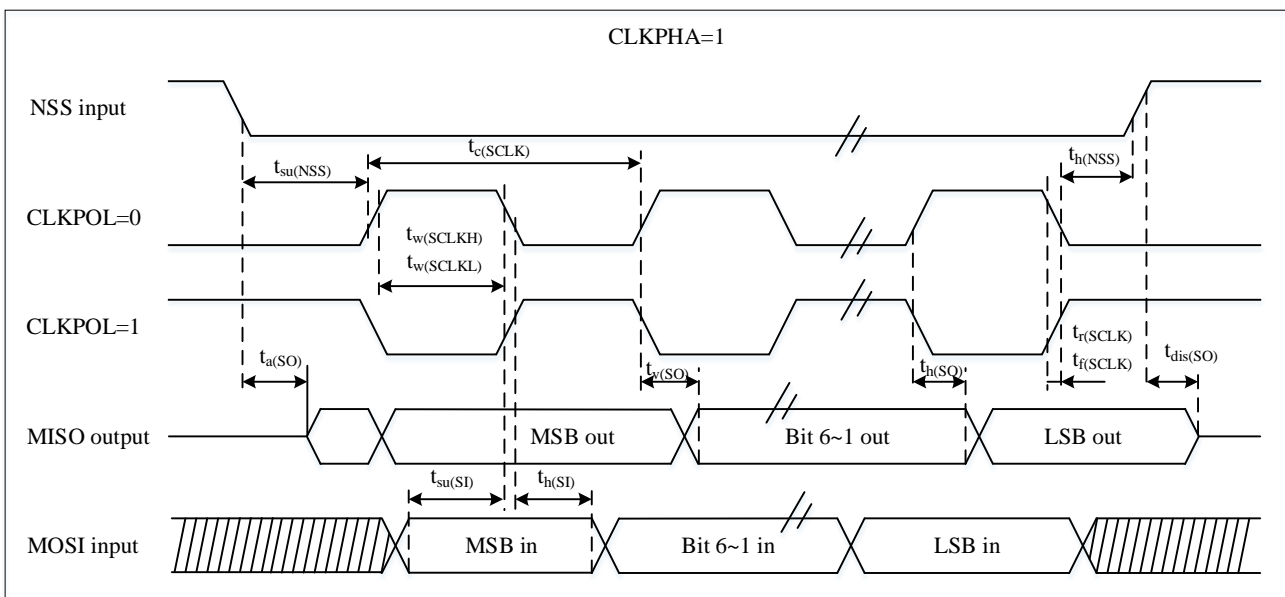
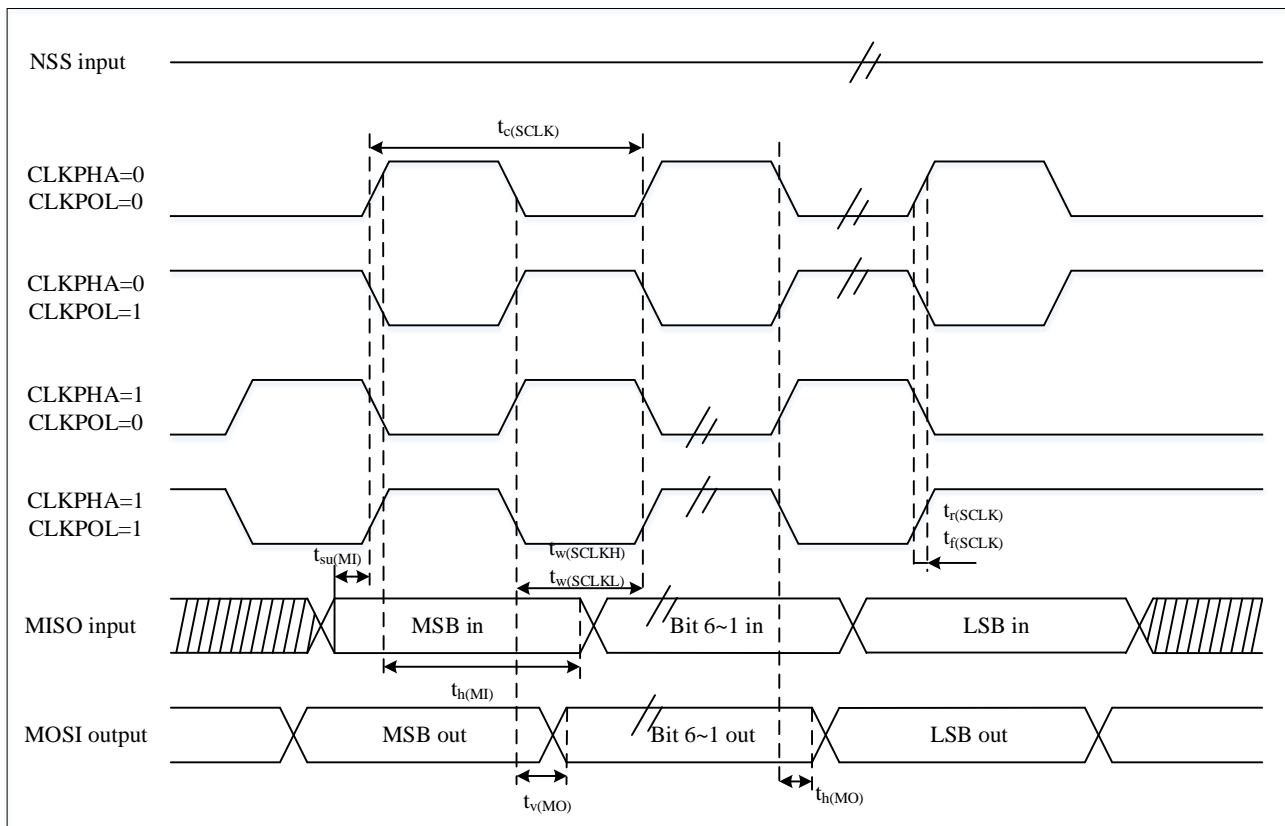


Figure 4-12 SPI timing diagram-slave mode and CLKPHA=1⁽¹⁾



1. The measuring point is set at $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 4-13 SPI timing diagram- master mode ⁽¹⁾



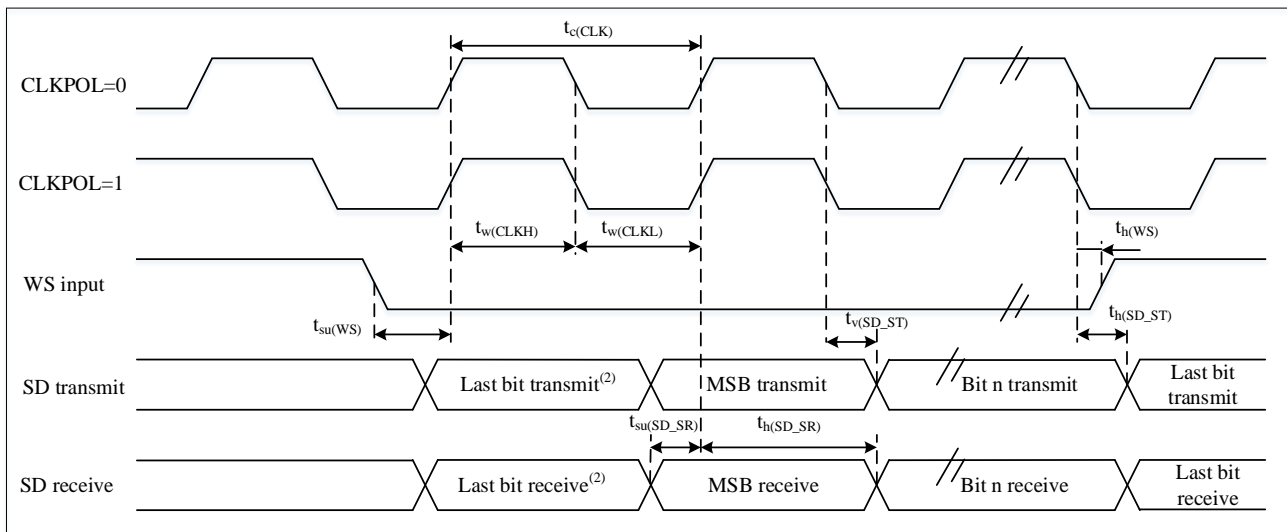
1. The measuring point is set at 0.3V and 0.7V.DDDD

Table 4-35 I²S characteristics ⁽¹⁾

Symbol	Parameter	Condition		Min	Max	Unit
f _{MCLK}	I ² S master clock	Master mode		-	256*Fs ⁽³⁾	MHz
f _{CLK} 1/t _{c(CLK)}	I ² S clock frequency	Master mode (32 bit)		-	64*Fs ⁽³⁾	MHz
		Slave mode (32 bit)		-	64*Fs ⁽³⁾	
DuCy(SCK)	I ² S clock frequency duty cycle	I2S Slave mode		30	70	%
t _{r(CLK)} t _{f(CLK)}	I ² S clock rise and fall time	Load capacitance: CL = 50pF		-	8	ns
t _{v(WS)} ⁽¹⁾	WS valid time	Master mode	I2S1	7.5	-	
			I2S2	6.0	-	
t _{h(WS)} ⁽¹⁾	WS hold time	Master mode	I2S1	0	-	
			I2S2	0	-	
t _{su(WS)} ⁽¹⁾	WS setup time	Slave mode	I2S1	4.5	-	
			I2S2	4.5	-	
t _{h(WS)} ⁽¹⁾	WS hold time	Slave mode	I2S1	2.5	-	
			I2S2	2.5	-	
t _{w(CLKH)} ⁽¹⁾	CLK high and low times	Master mode, f _{PCLK} = 16MHz, audio 48kHz		312.5	-	
t _{w(CLKL)} ⁽¹⁾				345	-	
t _{su(SD_MR)} ⁽¹⁾	Data input setup time	Master receiver	I2S1	5.0	-	
			I2S2	5.0	-	
t _{su(SD_SR)} ⁽¹⁾		Slave receiver	I2S1	4.5	-	
			I2S2	4.5	-	
t _{h(SD_MR)} ⁽¹⁾⁽²⁾	Data input hold time	Master receiver	I2S1	1.5	-	
			I2S2	1.5	-	
t _{h(SD_SR)} ⁽¹⁾⁽²⁾		Slave receiver	I2S1	1.5	-	
			I2S2	1.5	-	
t _{v(SD_ST)} ⁽¹⁾⁽²⁾	Data output valid time	Slave transmitter (after the enabled edge)	I2S1	-	16.0	
			I2S2	-	15.5	
t _{h(SD_ST)} ⁽¹⁾	Data output hold time	Slave generator (after enable edge)	I2S1	4.5	-	
			I2S2	4.5	-	
t _{v(SD_MT)} ⁽¹⁾⁽²⁾	Data output valid time	Master generator (after enabling edge)	I2S1	-	5.5	
			I2S2	-	5.5	
t _{h(SD_MT)} ⁽¹⁾	Data output hold time	Master generator (after enabling edge)	I2S1	1	-	
			I2S2	1	-	

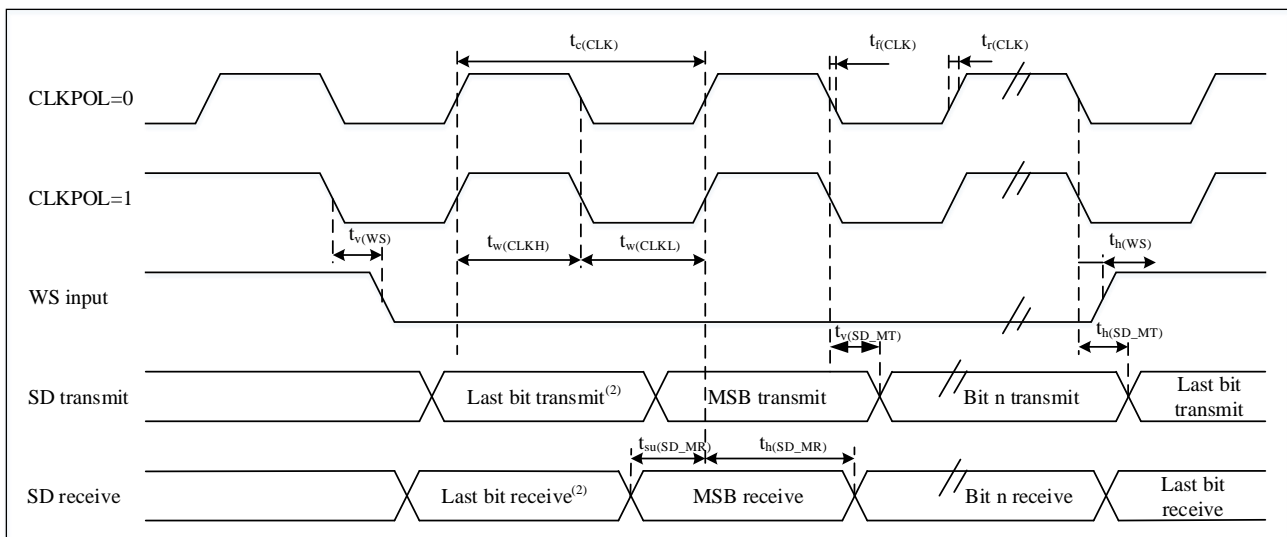
- Guaranteed by design, not tested in production.
- Depends on f_{PCLK}. For example, if f_{PCLK}=16MHz, then T_{PCLK}=1/f_{PCLK} =125ns.
- Audio signal sampling frequency.

Figure 4-14 I²S slave mode timing diagram (Philips Protocol) ⁽¹⁾



1. The measuring point is set at $0.3V_{DD}$ and $0.7V_{DD}$.
2. Transmit/receive of the last byte. There is no transmit/receive of this least significant bit before the first byte.

Figure 4-15 I²S master mode timing diagram (Philips protocol) ⁽¹⁾



1. The measuring point is set at $0.3V_{DD}$ and $0.7V_{DD}$.
2. Transmit/receive of the last byte. There is no transmit/receive of this last bit before the first byte.

4.3.17 Electrical parameters of 12 bit analog-to-digital converter (ADC)

Unless otherwise specified, the parameters in Table 4-36 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Note: It is recommended to perform a calibration at each power-on.

Table 4-36 ADC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{DDA}	The power supply voltage	Use an external reference voltage	2.4	-	3.6	V
V _{REF+}	Positive reference voltage	-	2.4	-	V _{DDA}	V
V _{REF-}	Negative reference voltage	-	0			V
f _{ADC}	ADC clock frequency	-	-	-	72	MHz
f _s ⁽²⁾	Sampling rate	2.4V ≤ V _{DD} ≤ 3.6V	-	-	4.2	Msp/s
f _{TRIG} ⁽²⁾	External trigger frequency ⁽³⁾	f _{ADC} =72MHz	-	-	4.2	MHz
		-	-	-	17	1/f _{ADC}
V _{AIN}	Switching voltage range	-	0 (V _{SSA} or V _{REF-} Connect to ground)	-	V _{REF+}	V
R _{AIN} ⁽²⁾	External input impedance	-	-	-	100 ⁽¹⁾	KΩ
R _{ADC} ⁽²⁾	Sampling switch resistance	Fast channel, 2.4V ≤ V _{DD} ≤ 3.6V	-	-	0.4	KΩ
R _{ADC} ⁽²⁾	Sampling switch resistance	Slow channel, 2.4V ≤ V _{DD} ≤ 3.6V	-	-	0.65	
C _{ADC} ⁽²⁾	Internal sampling and holding capacitor		-	5	-	pF
t _{cal} ⁽²⁾	The calibration time		82			1/f _{ADC}
t _{lat} ⁽²⁾	Injection trigger conversion latency	f _{ADC} = 72MHz	-	-	8.35	μs
		-	-	-	601.5	1/f _{ADC}
t _{latr} ⁽²⁾	Regular trigger conversion latency	f _{ADC} = 72MHz	-	-	8.35	μs
		-	-	-	601.5	1/f _{ADC}
SNDR	Signal noise distortion ration		-	65	-	dB
t _s ⁽²⁾	Sampling time	f _{ADC} = 72MHz(fast channel)	0.0208	-	8.35	us
		f _{ADC} = 72MHz(slow channel)	0.0208	-	8.35	
T _s ⁽²⁾	Sampling cycles	The fast channel	1.5	-	601.5	1/f _{ADC}
		The slow channel	1.5	-	601.5	
t _{STAB} ⁽²⁾	Power-up time	-	6	10	20	μs
t _{CONV} ⁽²⁾	Total conversion time (including sampling time)	-	14 ~ 614 (Sampling T _s + 6.5/8.5/10.5/12.5 for successive approximation)			1/f _{ADC}

1. Guaranteed by design, not tested in production., please refer to Table 4-37 for details.
2. Guaranteed by design, not tested in production.
3. Suitable for ADC continuous conversion mode.

Formula 1: maximum R_{AIN} formula

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12(representing 12-bit resolution).

Table 4-37 ADC sampling time⁽¹⁾

Input	Resolution	Rin(kΩ)	Minimum sampling time (ns)	Input	Resolution	Rin(kΩ)	Minimum sampling time (ns)
fast channel	12-bit	0	39.6	slow channel	12-bit	0	79.2
		0.05	43.5			0.05	83.1
		0.1	47.4			0.1	86.9
		0.2	55.1			0.2	94.7
		0.5	78.4			0.5	118.0
		1	117.2			1	156.8
		10	815.9			10	855.5
		20	1592.2			20	1631.8
		50	3921.2			50	3960.8
		100	7802.8			100	7842.4
fast channel	10-bit	0	33.9	slow channel	10-bit	0	67.9
		0.05	37.3			0.05	71.2
		0.1	40.6			0.1	74.5
		0.2	47.2			0.2	81.2
		0.5	67.2			0.5	101.1
		1	100.5			1	134.4
		10	699.4			10	733.3
		20	1364.8			20	1398.7
		50	3361.0			50	3395.0
		100	6688.1			100	6722.1
fast channel	8-bit	0	28.3	slow channel	8-bit	0	56.6
		0.05	31.1			0.05	59.3
		0.1	33.8			0.1	62.1
		0.2	39.4			0.2	67.7
		0.5	56.0			0.5	84.3
		1	83.7			1	112.0
		10	582.8			10	611.1
		20	1137.3			20	1165.6
		50	2800.9			50	2829.1
		100	5573.5			100	5601.7
fast channel	6-bit	0	22.6	slow channel	6-bit	0	45.2
		0.05	24.8			0.05	47.5
		0.1	27.1			0.1	49.7
		0.2	31.5			0.2	54.1
		0.5	44.8			0.5	67.4
		1	67.0			1	89.6
		10	466.2			10	488.9
		20	909.9			20	932.5
		50	2240.7			50	2263.3
		100	4458.8			100	4481.4

1. Guaranteed by design, not tested in production.

Table 4-38 ADC accuracy-limited test conditions ⁽¹⁾⁽²⁾

Symbol	Parameter	Condition	Max ⁽³⁾	Unit
ET	Comprehensive error ⁽⁴⁾	$f_{ADC} = 72\text{MHz}$, sample rate = 4.2MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Single-ended mode	± 4.5	LSB
		$f_{ADC} = 72\text{MHz}$, sample rate = 4.2MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Differential mode	± 4.5	
EO	Offset error	$f_{ADC} = 72\text{MHz}$, sample rate = 4.2MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Single-ended mode	± 1.5	
		$f_{ADC} = 72\text{MHz}$, sample rate = 4.2MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Differential mode	± 1.5	
EG	Gain error	$f_{ADC} = 72\text{MHz}$, sample rate = 4.2MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Single-ended mode	TBD	
		$f_{ADC} = 72\text{MHz}$, sample rate = 4.2MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Differential mode	TBD	
ED	Differential linearity error	$f_{ADC} = 72\text{MHz}$, sample rate = 1MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Single-ended mode	± 2.0	
		$f_{ADC} = 72\text{MHz}$, sample rate = 1MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Differential mode	± 1.5	
EL	Integral linearity error	$f_{ADC} = 72\text{MHz}$, sample rate = 1MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Single-ended mode	± 1.5	
		$f_{ADC} = 72\text{MHz}$, sample rate = 1MSPS, $V_{DDA} = 2.4\text{V} \sim 3.3\text{V}$, $T_A = 25^\circ\text{C}$, Differential mode	± 1.0	

1. The ADC accuracy of the ADC is measured after internal calibration.
2. ADC accuracy versus reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, as this can significantly reduce the accuracy of the conversion being performed on the other analog input pin. It is recommended to add a Schottky diode (between pin and ground) to standard analog pins that may generate reverse injection current. The forward injection current does not affect the ADC accuracy as long as it is within the range of $I_{INJ(PIN)}$ given in Table 4-2
3. Guaranteed by characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

Figure 4-16 ADC precision characteristics

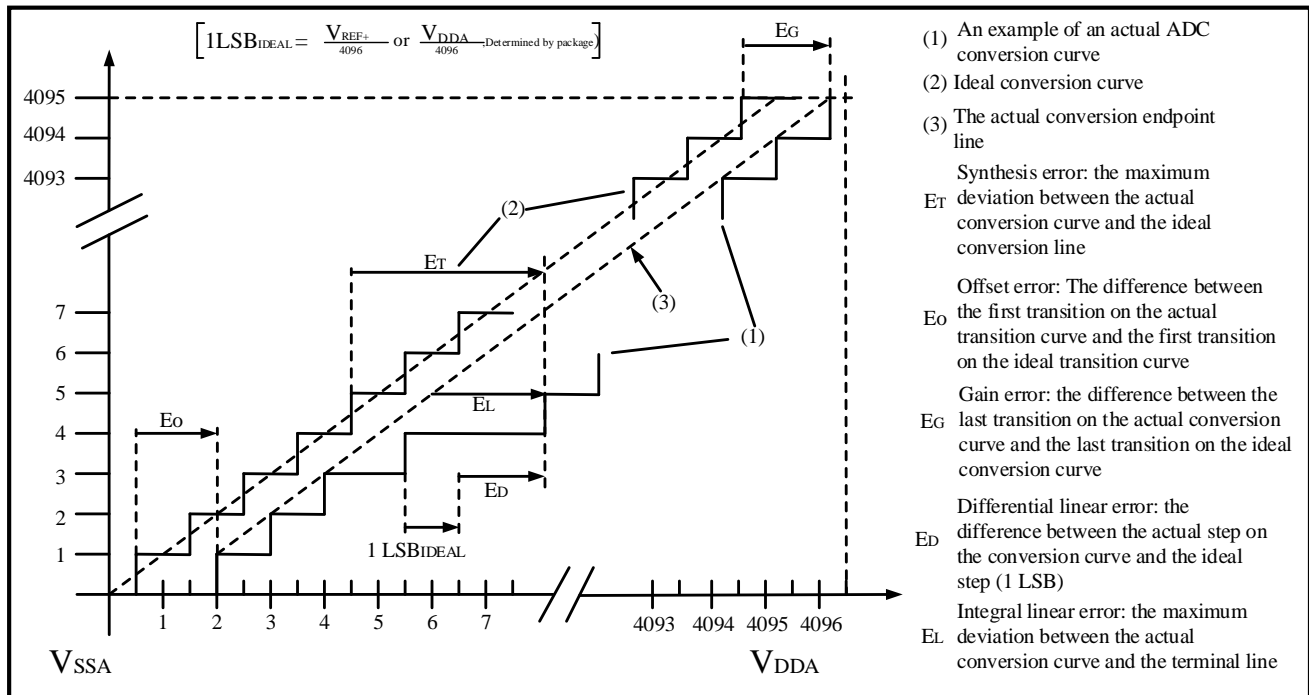
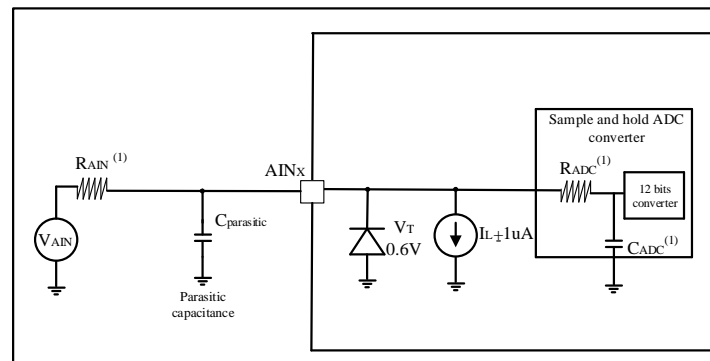


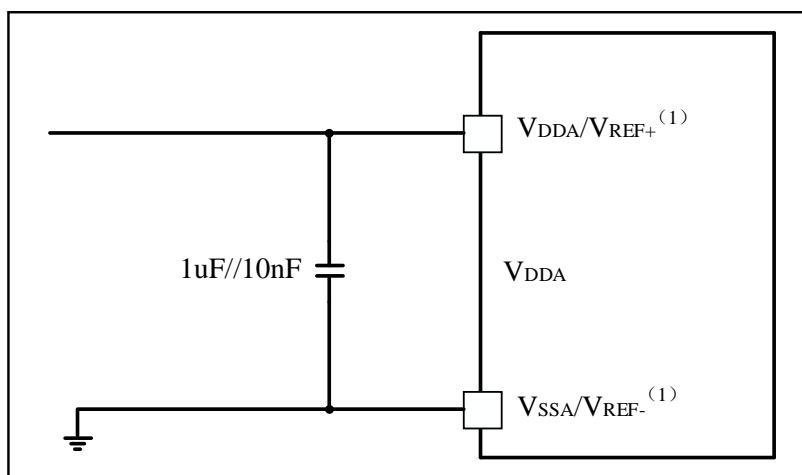
Figure 4-17 Typical connection diagram using ADC



1. For values of R_{AIN} , R_{ADC} , and C_{ADC} , see Table 4-36.
2. $C_{\text{parasitic}}$ indicates parasitic capacitance on PCB (related to welding and PCB layout quality) and pads (approximately 7pF). A larger $C_{\text{parasitic}}$ value would reduce the accuracy of the conversion and the solution was to reduce f_{ADC} .

PCB Design Suggestions

The decoupling of the power supply must be connected in accordance with Figure 4-18. The 10nF capacitors in the picture must be ceramic capacitors (good quality), and they should be as close as possible to the MCU chip.

Figure 4-18 Decoupling circuit of power supply and reference power supply (V_{REF+} is connected to V_{DDA})

1. V_{REF+} and V_{REF-} are internally connected to V_{DDA} and V_{SSA} .

4.3.18 Temperature sensor (TS) characteristics

Unless otherwise specified, the parameters in Table 4-39 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-39 Temperature sensor characteristics

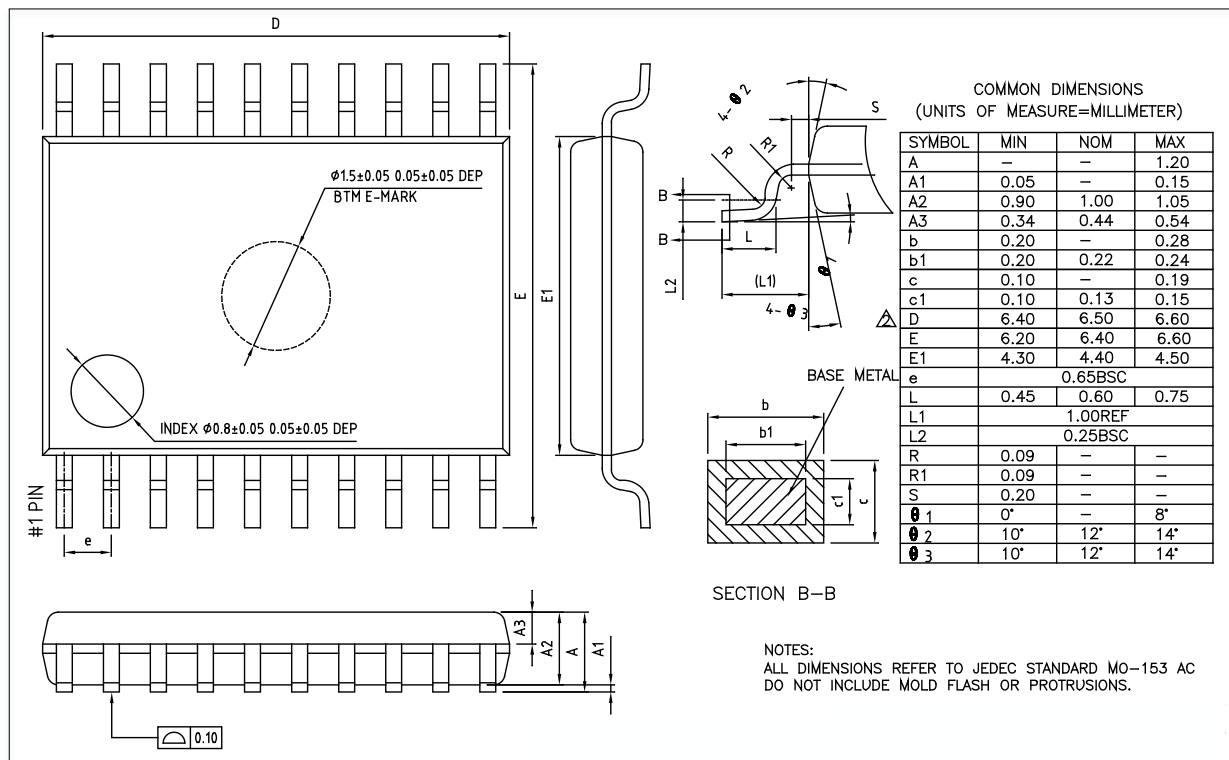
Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	Linearity of V_{SENSE} with respect to temperature	-	± 1	± 3	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	-3.7	-4	-4.3	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	-	1.32	-	V
$t_{START}^{(1)}$	Startup time	-	-	10	μs
$T_{S_temp}^{(2)(3)}$	When reading temperature, the ADC sampling time	8.2	-	17.1	μs

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design, not tested in production.
3. The minimum sampling time can be determined by the application through multiple loops.

5 Package Information

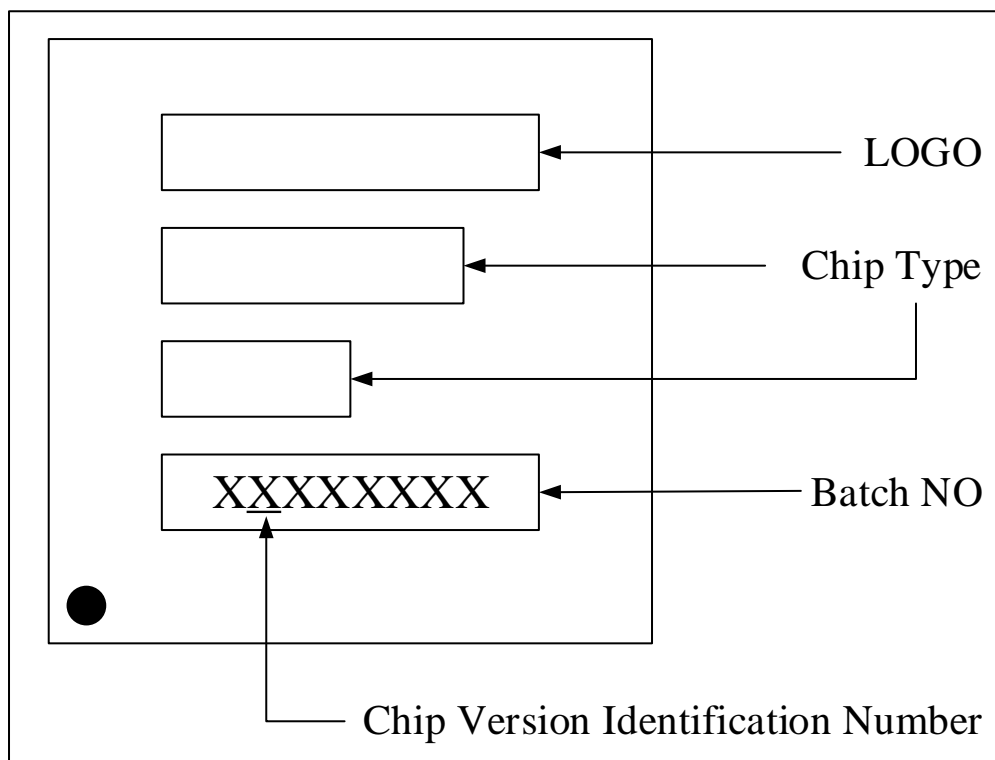
5.1 TSSOP20

Figure 5-1 TSSOP20 package outline



5.2 Marking Information

Figure 5-2 Marking information



6 Version history

Date	Version	Remark
2023/1/10	V1.0P	Initial release

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