

# NWF580 产品简介

(V2.1)

## 国民技术股份有限公司

二零二零年八月

#### 国民技术股份有限公司 Nations Technologies Inc.

1 地址:深圳市南山区高新北区宝深路109号国民技术大厦 电话: +86-755-86309900 传真: +86-755-86169100



# 重要声明:

随着产品的升级,本手册内容将会做相应的修改。国民技术股份有限公司保留对本手册内容进行修改的权利。

本手册的版权属于国民技术股份有限公司,未经许可不得以任何形式和手段复制或抄袭本手册内容。



# 目录

	版本记录	4
<b>—</b> .	芯片介绍	
<u> </u>	电气特性	6
三.	管脚布局和定义	9
	3.1 管脚布局	
	3.2 管脚定义	
四.	管脚封装	
, ,.	4.1 封装形式	
	4.2 封装规格	
	· 24 2/2/01H	



# 版本记录

版本	日期	修订人	说明
V1.0	2019.5.27	程维	创建文档
V2.0	2020.01.16	程维	车规版本
V2.1	2020.02.16	程维	修改细节



国民技术股份有限公司 Nations Technologies Inc.

地址:深圳市南山区高新北区宝深路109号国民技术大厦 4 电话: +86-755-86309900 传真: +86-755-86169100 邮箱: info@nationz.com.cn 邮编: 518057



# 一. 芯片介绍

NWF580 为国民技术研发的全集成射频收发芯片,满足中国电子收费专用短程通讯标准 GB/T20851.1-2007 和收费公路联网收费多义性路径识别技术要求(中华人民共和国交通运输部 2015 年 40 号公告),通过汽车电子 AEC-Q100测试,工作频率范围 5.73~6.2 GHz。接收灵敏度达-76 dBm(256 Kbps ASK 数据),芯片发射功率达 8 dBm,内置 SPI 接口与上位机通信及进行工作模式控制。

在无外部控制条件下 NWF580 可以被基于 GB/T20851.1-2007 标准定义的唤醒信号唤醒,射频唤醒灵敏度达 -85 dBm,等效电流为 2 uA。NWF580 在接收到有效数据时可以通过中断通知上位机。

NWF580 集成完整的 DSRC 协议处理功能,包括 FM0 编解码、数据 CRC 校验、标志位查找及 128 字节 FIFO 数据缓冲等功能。

#### 主要特点

名称	性能参数				
工作频率范围	5.73~6.2 GHz				
数据传输率	256 Kbps / 512 Kbps				
唤醒灵敏度	-85dBm				
RF 接收灵敏度	-80dBm@调制系数 85%:				
发射功率	-6.1 ∼ 8.4 dBm				
工作功耗	待机: 0.1 uA				
	唤醒: 2 uA				
	接收: 37 mA				
	发送: 47 mA@ 0 dBm				

#### 应用领域

可应用于ETC、电子车牌和无绳电话等领域。



# 二. 电气特性

表 2.1 规定了 NWF580 芯片工作的电器特性。超过规定的使用参数将会造成芯片永久损坏。长时间在规定参数最大值附近工作会影响使用寿命。

表 2.1 电气规格

Parameter	Min	Тур	Max	Units
模拟电源电压	2.2	3.3	4.0	V
数字接口电源电压	2.2	3.3	4.0	V
射频输入功率	-83	-50	-4	dBm
唤醒状态电流消耗	-	2	-	μΑ
接收模式电流消耗	-	37	<u>,</u>	mA
发射模式电流消耗	54	47	95	mA
输入逻辑电平范围	1.8	3.3	4.0	V
输出逻辑电平范围	-	3.3		V
电源建立时间		150		μs
工作温度范围	-45	25	105	°C

表 2.2 发射模块电气规格

Parameter	Min	Тур	Max	Units
射频发射信号载波频率	5.73	5.79/5.80	6.20	GHz
发射功率	-6.1	0	8.4	dBm
发射 ASK 数据传输速率	256	512	512	Kbps
发射杂散信号功率:				
@30 MHz~1000 MHz		-67.56		
@2.4 GHz~2.483 GHz	-	-63.506	-	dBm
@3.4 GHz~3.53 GHz		-62.728		
@Other 1 GHz~20 GHz		-59.084		
发射 AM 调制系数	0.7	0.85	1	-
发射链路增益调谐范围	-6.1	2.0	8.4	dBm
发射功率带宽	-	1.1	-	MHz
相邻信道泄露功率抑制比	-	-58	-	dBm
发射链路建立时间 (不含电源建立时间)	-	-	50	μs



#### 表 2.3 接收模块电气规格

Parameter	Min	Тур	Max	Units
射频输入管脚差分输入阻抗	-	50	-	ohm
射频接收灵敏度@ 256 Kbps: (BER < 10E-5,调制系数 85%)	-80	-76	-4	dBm
射频端口相位噪声 (5790/5800MHz):				
@ 1 KHz offset @ 10 KHz offset	-	-65	-	dBc/Hz
@ 10 KHz offset		-70		
@ 100 KHz offset		-75	1	
动态范围		76		dBm
接收模块建立时间	-	22		μs

## 表 2.4 唤醒模块电气规格

Parameter	Min	Тур	Max	Units
射频唤醒灵敏度	-83	-80	-14	dBm
唤醒信号持续时间 (可调节)	1.0	1.00	4.0	ms
唤醒信号带宽	9	-	16	kHz
接收使能信号持续时间 (可调节)	1	1	32	ms
射频唤醒信号载波输入频率 -3 dB 带宽(唤醒信号为 14 KHz 周期 OOK 调制)	5.82	5.83/5.84	5.85	GHz



表 2.5 频率综合模块电气规格

农2.3 %中苏古侯久记 (%)相							
Parameter	Min	Тур	Max	Units			
VCO 频率范围	5.73	-	6.2-	GHz			
输入参考时钟频率	-	32.768	-	MHz			
输出频率调谐精度	-	0.7	-	ppm			
频率综合建立时间	-	-	50	μs			
VCO 输出信号相位噪声: @5.79 GHz 10 KHz offset 100 KHz offset 1 MHz offset	-	-65 -69 -92	-	dBc/Hz			

# 表 2.6 外部晶体模块电气规格

Parameter	Min	Тур	Max	Units
参考晶体时钟频率	-	32.768	-	MHz
32.768 MHz 时钟晶体建立时间	-	100	-	μs



# 三. 管脚布局和定义

## 3.1 管脚布局

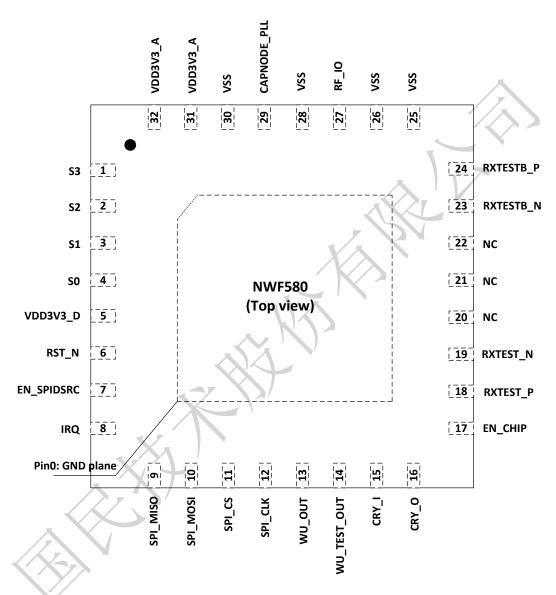


图 3.1 NWF580 管脚布局(Top-View,QFN32)

地址:深圳市南山区高新北区宝深路109号国民技术大厦 电话: +86-755-86309900 传真: +86-755-86169100



# 3.2 管脚定义

#### 说明: PIN 0 必须接 GND

connect to VSS  Solution  Digital output port for test  Solution  Out  Digital output port for test	说明: PIN 0 4 PIN Num.	Name	Input/Output	Discription		
Connect to VSS	1	S3	In	Digital input port for test, must		
3 S1 Out Digital output port for test 4 S0 In Digital input port for test, must connect to VSS 5 VDD3V3_D Power Digital Power supply, 3.3 V 6 RST_N In Chip Reset, low effective 7 EN_SPIDSRC In SPI & DSRC Enable, high effective 8 IRQ Out SPI digital signals 9 SPI_MISO Out 10 SPI_MOSI In SPI_CS In SPI_CLK In WU_OUT Out Wakeup Test Signals 11 SPI_CS In Passive crystal input 12 SPI_CLK In Passive crystal input 16 CRY_O In Chip Enable, high effective 18 RXTEST_P Out RX positive test signal without buffer 19 RXTEST_N Out RX negative test signal without buffer 20 NC 21 NC 22 NC 23 RXTESTB_N Out RX negative test signal with buffer 24 RXTESTB_P Out RX positive test signal with buffer 25 VSS GND Chip Ground 27 RF_IO In/out RF input/output signal 28 VSS GND Chip Ground 29 CAPNODE_PLL In/Out PLL test pin for debug 30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V	1			connect to VSS		
SO	2	S2	Out	Digital output port for test		
Connect to VSS	3	S1	Out	Digital output port for test		
5         VDD3V3_D         Power         Digital Power supply, 3.3 V           6         RST_N         In         Chip Reset, low effective           7         EN_SPIDSRC         In         SPI & DSRC Enable, high effective           8         IRQ         Out         SPI digital signals           9         SPI_MISO         Out         SPI digital signals           10         SPI_MOSI         In           11         SPI_CS         In           12         SPI_CLK         In           13         WU_OUT         Out         WU Interrupt/14 kHz WU signal           14         WU_TEST_OUT         Out         Wakeup Test Signals           15         CRY_I         In         Passive crystal input           16         CRY_O         In         Passive crystal input           16         CRY_O         In         Chip Enable, high effective           18         RXTEST_P         Out         RX positive test signal without buffer           19         RXTEST_P         Out         RX negative test signal without buffer           20         NC         In         RX negative test signal with buffer           21         NC         RX         RX negative test signal with buffer </th <th>4</th> <th>S0</th> <th>In</th> <th></th>	4	S0	In			
6 RST_N In Chip Reset, low effective 7 EN_SPIDSRC In SPI & DSRC Enable, high effective 8 IRQ Out SPI digital signals 9 SPI_MISO Out 10 SPI_MOSI In 11 SPI_CS In 12 SPI_CLK In 13 WU_OUT Out WU Interrupt/14 kHz WU signal 14 WU_TEST_OUT Out Wakeup Test Signals 15 CRY_I In Passive crystal input 16 CRY_O In 17 EN_CHIP In Chip Enable, high effective 18 RXTEST_P Out RX positive test signal without buffer 19 RXTEST_N Out RX negative test signal without buffer 20 NC 21 NC 22 NC 23 RXTESTB_N Out RX positive test signal with buffer 24 RXTESTB_P Out RX positive test signal with buffer 25 VSS GND Chip Ground 26 VSS GND Chip Ground 27 RF_IO In/out RF input/output signal 28 VSS GND Chip Ground 29 CAPNODE_PLL In/Out PLL test pin for debug 30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V						
7         EN_SPIDSRC         In         SPI & DSRC Enable, high effective           8         IRQ         Out         SPI digital signals           9         SPI_MISO         Out         SPI digital signals           10         SPI_MOSI         In           11         SPI_CS         In           12         SPI_CLK         In           13         WU_OUT         Out         WU Interrupt/14 kHz WU signal           14         WU_TEST_OUT         Out         Wakeup Test Signals           15         CRY_I         In         Passive crystal input           16         CRY_O         In         Passive crystal input           16         CRY_O         In         Chip Enable, high effective           18         RXTEST_P         Out         RX positive test signal without buffer           19         RXTEST_P         Out         RX negative test signal without buffer           20         NC         In         RX negative test signal with buffer           21         NC         RX         RX positive test signal with buffer           24         RXTESTB_P         Out         RX positive test signal with buffer           25         VSS         GND         Chip Ground		_		111		
8 IRQ Out SPI digital signals  9 SPI_MISO Out  10 SPI_MOSI In  11 SPI_CS In  12 SPI_CLK In  13 WU_OUT Out Wu Interrupt/14 kHz WU signal  14 WU_TEST_OUT Out Wakeup Test Signals  15 CRY_I In Passive crystal input  16 CRY_O In  17 EN_CHIP In Chip Enable, high effective  18 RXTEST_P Out RX positive test signal without buffer  19 RXTEST_N Out RX negative test signal without buffer  20 NC  21 NC  22 NC  23 RXTESTB_N Out RX positive test signal with buffer  24 RXTESTB_P Out RX positive test signal with buffer  25 VSS GND Chip Ground  26 VSS GND Chip Ground  27 RF_IO In/out RF input/output signal  28 VSS GND Chip Ground  29 CAPNODE_PLL In/Out PLL test pin for debug  30 VSS GND Chip Ground  31 VDD3V3_A Power Analog Power supply, 3.3 V	6	_				
9         SPI_MISO         Out           10         SPI_MOSI         In           11         SPI_CS         In           12         SPI_CLK         In           13         WU_OUT         Out         WU Interrupt/14 kHz WU signal           14         WU_TEST_OUT         Out         Wakeup Test Signals           15         CRY_I         In         Passive crystal input           16         CRY_O         In         Chip Enable, high effective           17         EN_CHIP         In         Chip Enable, high effective           18         RXTEST_P         Out         RX positive test signal without buffer           20         NC         RX negative test signal without buffer           21         NC         RX negative test signal with buffer           22         NC         RX positive test signal with buffer           24         RXTESTB_N         Out         RX positive test signal with buffer           25         VSS         GND         Chip Ground           26         VSS         GND         Chip Ground           27         RF_IO         In/out         RF input/output signal           28         VSS         GND         Chip Ground </th <th>7</th> <th>_</th> <th>In</th> <th></th>	7	_	In			
10	8	`		SPI digital signals		
11	9	_	Out			
12 SPI_CLK In  13 WU_OUT Out WU Interrupt/14 kHz WU signal  14 WU_TEST_OUT Out Wakeup Test Signals  15 CRY_I In Passive crystal input  16 CRY_O In  17 EN_CHIP In Chip Enable, high effective  18 RXTEST_P Out RX positive test signal without buffer  19 RXTEST_N Out RX negative test signal without buffer  20 NC  21 NC  22 NC  23 RXTESTB_N Out RX negative test signal with buffer  24 RXTESTB_P Out RX positive test signal with buffer  25 VSS GND Chip Ground  26 VSS GND Chip Ground  27 RF_IO In/out RF input/output signal  28 VSS GND Chip Ground  29 CAPNODE_PLL In/Out PLL test pin for debug  30 VSS GND Chip Ground  31 VDD3V3_A Power Analog Power supply, 3.3 V	10	SPI_MOSI	In			
13 WU_OUT Out WU Interrupt/14 kHz WU signal 14 WU_TEST_OUT Out Wakeup Test Signals 15 CRY_I In Passive crystal input 16 CRY_O In 17 EN_CHIP In Chip Enable, high effective 18 RXTEST_P Out RX positive test signal without buffer 19 RXTEST_N Out RX negative test signal without buffer 20 NC 21 NC 22 NC 23 RXTESTB_N Out RX positive test signal with buffer 24 RXTESTB_P Out RX positive test signal with buffer 25 VSS GND Chip Ground 26 VSS GND Chip Ground 27 RF_IO In/out RF input/output signal 28 VSS GND Chip Ground 29 CAPNODE_PLL In/Out PLL test pin for debug 30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V	11	SPI_CS	In			
14 WU_TEST_OUT Out Wakeup Test Signals 15 CRY_I In Passive crystal input 16 CRY_O In 17 EN_CHIP In Chip Enable, high effective 18 RXTEST_P Out RX positive test signal without buffer 19 RXTEST_N Out RX negative test signal without buffer 20 NC 21 NC 22 NC 23 RXTESTB_N Out RX negative test signal with buffer 24 RXTESTB_P Out RX positive test signal with buffer 25 VSS GND Chip Ground 26 VSS GND Chip Ground 27 RF_IO In/out RF input/output signal 28 VSS GND Chip Ground 29 CAPNODE_PLL In/Out PLL test pin for debug 30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V	12	SPI_CLK	In			
15 CRY_I In Passive crystal input  16 CRY_O In  17 EN_CHIP In Chip Enable, high effective  18 RXTEST_P Out RX positive test signal without buffer  19 RXTEST_N Out RX negative test signal without buffer  20 NC  21 NC  22 NC  23 RXTESTB_N Out RX negative test signal with buffer  24 RXTESTB_P Out RX positive test signal with buffer  25 VSS GND Chip Ground  26 VSS GND Chip Ground  27 RF_IO In/out RF input/output signal  28 VSS GND Chip Ground  29 CAPNODE_PLL In/Out PLL test pin for debug  30 VSS GND Chip Ground  31 VDD3V3_A Power Analog Power supply, 3.3 V	13	WU_OUT	Out	WU Interrupt/14 kHz WU signal		
16         CRY_O         In           17         EN_CHIP         In         Chip Enable, high effective           18         RXTEST_P         Out         RX positive test signal without buffer           19         RXTEST_N         Out         RX negative test signal without buffer           20         NC	14	WU_TEST_OUT	Out	Wakeup Test Signals		
17 EN_CHIP In Chip Enable, high effective  18 RXTEST_P Out RX positive test signal without buffer  19 RXTEST_N Out RX negative test signal without buffer  20 NC  21 NC  22 NC  23 RXTESTB_N Out RX negative test signal with buffer  24 RXTESTB_P Out RX positive test signal with buffer  25 VSS GND Chip Ground  26 VSS GND Chip Ground  27 RF_IO In/out RF input/output signal  28 VSS GND Chip Ground  29 CAPNODE_PLL In/Out PLL test pin for debug  30 VSS GND Chip Ground  31 VDD3V3_A Power Analog Power supply, 3.3 V	15	CRY_I	In	Passive crystal input		
18 RXTEST_P Out RX positive test signal without buffer  19 RXTEST_N Out RX negative test signal without buffer  20 NC  21 NC  22 NC  23 RXTESTB_N Out RX negative test signal with buffer  24 RXTESTB_P Out RX positive test signal with buffer  25 VSS GND Chip Ground  26 VSS GND Chip Ground  27 RF_IO In/out RF input/output signal  28 VSS GND Chip Ground  29 CAPNODE_PLL In/Out PLL test pin for debug  30 VSS GND Chip Ground  31 VDD3V3_A Power Analog Power supply, 3.3 V	16	CRY_O	In			
19 RXTEST_N Out RX negative test signal without buffer 20 NC 21 NC 22 NC 23 RXTESTB_N Out RX negative test signal with buffer 24 RXTESTB_P Out RX positive test signal with buffer 25 VSS GND Chip Ground 26 VSS GND Chip Ground 27 RF_IO In/out RF input/output signal 28 VSS GND Chip Ground 29 CAPNODE_PLL In/Out PLL test pin for debug 30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V	17	EN_CHIP	In	Chip Enable, high effective		
20 NC 21 NC 22 NC 23 RXTESTB_N Out RX negative test signal with buffer 24 RXTESTB_P Out RX positive test signal with buffer 25 VSS GND Chip Ground 26 VSS GND Chip Ground 27 RF_IO In/out RF input/output signal 28 VSS GND Chip Ground 29 CAPNODE_PLL In/Out PLL test pin for debug 30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V	18	RXTEST_P	Out	RX positive test signal without buffer		
21 NC 22 NC 23 RXTESTB_N Out RX negative test signal with buffer 24 RXTESTB_P Out RX positive test signal with buffer 25 VSS GND Chip Ground 26 VSS GND Chip Ground 27 RF_IO In/out RF input/output signal 28 VSS GND Chip Ground 29 CAPNODE_PLL In/Out PLL test pin for debug 30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V	19	RXTEST_N	Out	RX negative test signal without buffer		
23 RXTESTB_N Out RX negative test signal with buffer 24 RXTESTB_P Out RX positive test signal with buffer 25 VSS GND Chip Ground 26 VSS GND Chip Ground 27 RF_IO In/out RF input/output signal 28 VSS GND Chip Ground 29 CAPNODE_PLL In/Out PLL test pin for debug 30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V	20	NC				
23RXTESTB_NOutRX negative test signal with buffer24RXTESTB_POutRX positive test signal with buffer25VSSGNDChip Ground26VSSGNDChip Ground27RF_IOIn/outRF input/output signal28VSSGNDChip Ground29CAPNODE_PLLIn/OutPLL test pin for debug30VSSGNDChip Ground31VDD3V3_APowerAnalog Power supply, 3.3 V	21	NC				
24RXTESTB_POutRX positive test signal with buffer25VSSGNDChip Ground26VSSGNDChip Ground27RF_IOIn/outRF input/output signal28VSSGNDChip Ground29CAPNODE_PLLIn/OutPLL test pin for debug30VSSGNDChip Ground31VDD3V3_APowerAnalog Power supply, 3.3 V	22	NC				
25         VSS         GND         Chip Ground           26         VSS         GND         Chip Ground           27         RF_IO         In/out         RF input/output signal           28         VSS         GND         Chip Ground           29         CAPNODE_PLL         In/Out         PLL test pin for debug           30         VSS         GND         Chip Ground           31         VDD3V3_A         Power         Analog Power supply, 3.3 V	23	RXTESTB_N	Out	RX negative test signal with buffer		
26         VSS         GND         Chip Ground           27         RF_IO         In/out         RF input/output signal           28         VSS         GND         Chip Ground           29         CAPNODE_PLL         In/Out         PLL test pin for debug           30         VSS         GND         Chip Ground           31         VDD3V3_A         Power         Analog Power supply, 3.3 V	24	RXTESTB_P	Out	RX positive test signal with buffer		
27         RF_IO         In/out         RF input/output signal           28         VSS         GND         Chip Ground           29         CAPNODE_PLL         In/Out         PLL test pin for debug           30         VSS         GND         Chip Ground           31         VDD3V3_A         Power         Analog Power supply, 3.3 V	25	VSS	GND	Chip Ground		
28         VSS         GND         Chip Ground           29         CAPNODE_PLL         In/Out         PLL test pin for debug           30         VSS         GND         Chip Ground           31         VDD3V3_A         Power         Analog Power supply, 3.3 V	26	VSS	GND	Chip Ground		
29 CAPNODE_PLL In/Out PLL test pin for debug 30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V	27	RF_IO	In/out	RF input/output signal		
30 VSS GND Chip Ground 31 VDD3V3_A Power Analog Power supply, 3.3 V	28	VSS	GND	Chip Ground		
31 VDD3V3_A Power Analog Power supply, 3.3 V	29	CAPNODE_PLL	In/Out	PLL test pin for debug		
	30	VSS	GND	Chip Ground		
32 VDD3V3_A Power Analog Power supply, 3.3 V	31	VDD3V3_A	Power	Analog Power supply, 3.3 V		
	32	VDD3V3_A	Power	Analog Power supply, 3.3 V		

1

地址:深圳市南山区高新北区宝深路109号国民技术大厦 电话: +86-755-86309900 传真: +86-755-86169100

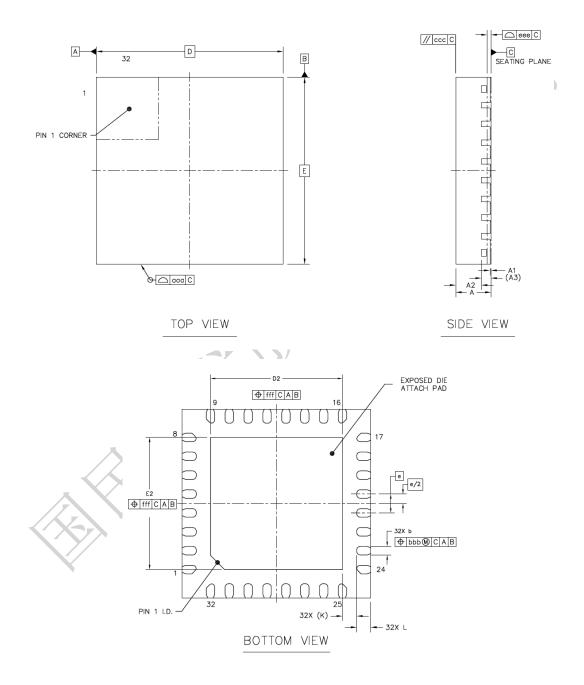


# 四. 管脚封装

#### 4.1 封装形式

NWF580 封装形式为 QFN32

#### 4.2 封装规格



1

地址: 深圳市南山区高新北区宝深路109号国民技术大厦 电话: +86-755-86309900 传真: +86-755-86169100



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		Α	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2		0.55	
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
BOD 1 SIZE	Y	E		4 BSC	
LEAD PITCH		е		0.4 BSC	
EP SIZE	X	D2	2.7	2.8	2.9
EF SIZE	Y	E2	2.7	2.8	2.9
LEAD LENGTH		Г	0.2	0.3	0.4
LEAD TIP TO EXPOSED	PAD EDGE	К	0.3 REF		
PACKAGE EDGE TOLERA	NCE	aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.07		
EXPOSED PAD OFFSET		fff	0.1		

地址:深圳市南山区高新北区宝深路109号国民技术大厦 1 电话: +86-755-86309900 传真: +86-755-86169100 邮箱: info@nationz.com.cn 邮编: 518057