N32G435x8/xB datasheet

N32G435 series based on 32-bit ARM Cortex-M4F kernel, run up to 108MHz, support floating-point unit and DSP instructions, up to 128KB embedded flash, 32KB SRAM, integrated high-performance analog interface, built-in 1x12bit 5Msps ADC, 2x independent rail-to-rail operational amplifiers, 2x high-speed comparators, 1x 1Msps 12bit DAC, Integrated multi-channel U(S)ART, I2C, SPI, USB, CAN and other digital communication interfaces, built-in hardware acceleration engine for cryptographic algorithm.

Key features

- **CPU core**
  - 32-bit ARM Cortex-M4 + FPU, single-cycle hardware multiplication and division instruction, support DSP instruction and MPU
  - Built-in 2KB instruction Cache, which support Flash acceleration unit to execute program 0 wait
  - Run up to 108MHz, 135DMIPS
- **Encrypted memory**
  - Up to 128KByte of embedded Flash memory, support encrypted storage, multi-user partition management and data protection, hardware ECC check, 100,000 cycling and 10 years data retention.
  - 32KByte of SRAM, including 24Kbyte SRAM1(In STOP2 mode can be configured to retention) and 8 Kbyte SRAM2(In STANDBY and STOP2 mode can be configured to retention), support hardware parity check
- **Low power management**
  - STANDBY mode: 2.5uA, all backup registers retention, IO retention, optional RTC Run, 8KByte SRAM2 can be configured to retention, fast wake up
  - STOP2 mode: 6uA, RTC Run, 8KByte SRAM2 and 24Kbyte SRAM1 can be configured to retention, CPU register retention, IO retention, fast wake up
  - RUN mode: 90uA/MHz@108MHz
  - LPRUN mode: PLL off, MSI as the system master clock, MR off, LPR on, USB/CAN/SAC power off, other peripherals are optional
- **High-performance analog interface**
  - 1x 12bit 5Msps ADC, multiple precision configurable, sampling rate up to 9Msps in 6-bit mode, up to 16 external single-ended input channels, support differential mode
  - 2x rail-to-rail operational amplifiers with built-in maximum 32x programmable gain amplifier
  - 2x high-speed analog comparators, built-in 64-level adjustable comparison reference, COMP1 support working in STOP2 mode
  - 1x 12bit DAC, sampling rate 1Msps
  - Internal 2.048V independent reference voltage reference source
  - Internal integrated low-voltage detection unit
- **Clock**
  - HSE: 4MHz~32MHz external high-speed crystal
  - LSE: 32.768KHz External low-speed crystal
  - HSI: Internal high-speed RC 16MHz
  - MSI: Internal multi-speed RC 100K~4MHz
  - LSI: Internal low-speed RC 40KHz
  - Built-in high speed PLL

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- MCO: Support 1-channel clock output, which can be configured as low-speed or high-speed clock output

- **Reset**
  - Support power-on/brown-out/external pin reset
  - Support watchdog reset
- **Support up to 52 GPIOs**
- **Communication interface**
  - 5x U(S)ART interfaces, including 3x USART interfaces (support ISO7816, IrDA, LIN) and 2x UART interfaces
  - 1x LPUART, support wake-up MCU in STOP2 mode
  - 2x SPI interfaces, up to 27 Mbps, support I2S
  - 2x I2C interfaces, up to 1 MHz, master-slave mode is configurable, slave mode support dual-address response
  - 1x USB2.0 FS Device interface
  - 1x CAN 2.0A/B bus interface
- **1x DMA controller, each controller support 8 channels, channel source address and destination address can be arbitrarily configurable**
- **1x RTC real-time clock, support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
- **Timing counter**
  - 2x 16-bit advanced timer counters, support input capture, complementary output, quadrature encoder input, maximum control accuracy 9.25ns; each timer has 4 independent channels, of which 3 channels support 6 complementary PWM outputs
  - 5x 16-bit general purpose timer counters, each timer has 4 independent channels, support input capture/output comparison/PWM output
  - 2x 16-bit basic timer counters
  - 1x 16-bit low-power timer counter, support double pulse counting function, can work in STOP2 mode
  - 1x 24-bit SysTick
  - 1x 7-bit Window Watchdog (WWDG)
  - 1x 12-bit Independent Watchdog (IWDG)
- **Programming mode**
  - Support SWD/JTAG online debugging interface
  - Support UART and USB Bootloader
- **Security features**
  - Built-in cryptographic algorithm hardware acceleration engine
  - Support AES, DES, TDES, SHA1/224/256, SM1, SM3, SM4, and SM7 algorithms
  - Flash storage encryption, Multi-user partition Management Unit (MMU)
  - TRNG true random number generator
  - CRC16/32 operation
  - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Support security start-up, program encryption download, security update
  - Support external clock failure detection, tamper detection

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- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃ ~ 105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Encapsulation**
  - QFN28(4mm×4mm)
  - LQFP32(7mm×7mm)
  - LQFP48(7mm×7mm)
  - LQFP64(10mm×10mm)
  - LQFP64(7mm×7mm)
- **Ordering information**

Series	Part Number
N32G435x8	N32G435G8Q7, N32G435K8L7, N32G435C8L7, N32G4352R8L7
N32G435xB	N32G435KBL7, N32G435CBL7, N32G435RBL7(1) N32G435GBQ7, N32G435RBL7-1(2)

Note:

1. *Package is LQFP64 (10mm×10mm)*
2. *Package is LQFP64 (7mm×7mm)*

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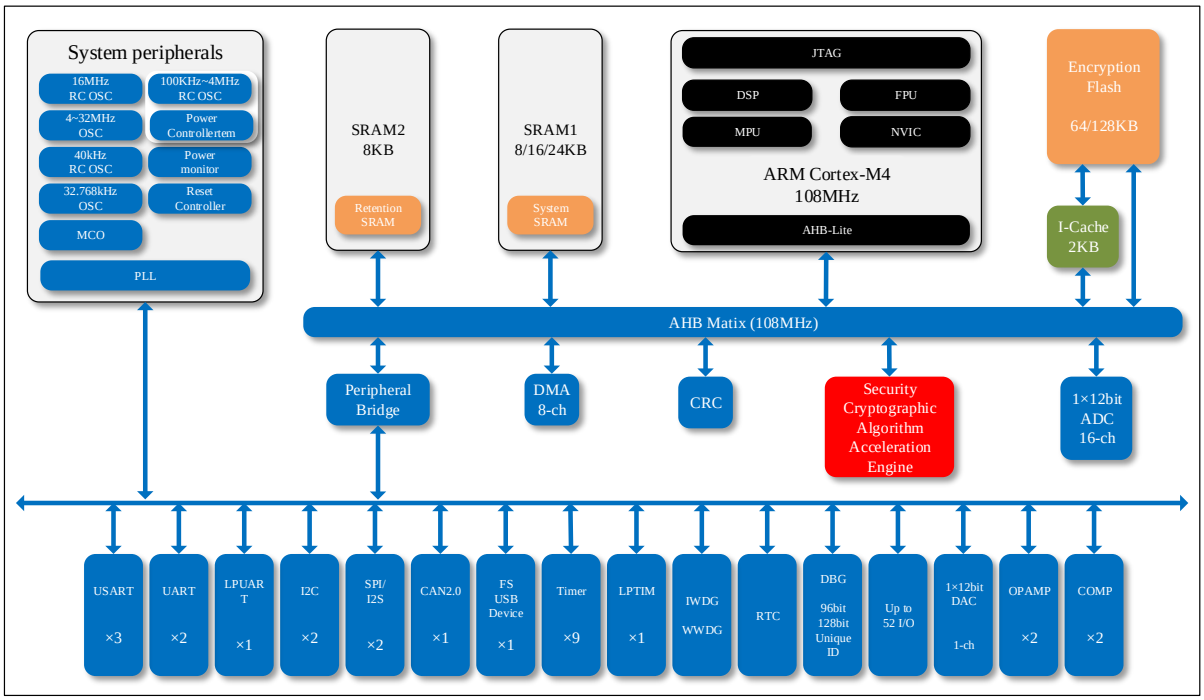
1 Product introduction

N32G435 family of microcontrollers features a high-performance 32-bit ARM Cortex™-M4F core, integrated floating point operation unit (FPU) and digital signal processing (DSP), and supports parallel computing instructions. Maximum operating main frequency 108MHz, integrated up to 128KB of in-chip encrypted storage Flash, supports multi-user partition permission management, maximum 32KB of embedded SRAM, including 8KB of Retention RAM. It has an internal high speed AHB bus, two low speed peripherals clock bus APB and bus matrix. It supports up to 52 alternate I/Os and provides a rich array of high performance analog interfaces, including 1x 12-bit 5Msps ADC, up to 16 external input channels and 3 internal channels, and 1x 1Msps 12-bit DAC. At the same time, it provides a variety of digital communication interfaces, including 5x U(S)ART, 1x LPUART, 2x I2C, 2x SPI/ I2S, 1x FS USB 2.0 device, 1x CAN 2.0B communication interface, built-in password algorithm hardware acceleration engine, supporting a variety of international and national encryption algorithm hardware acceleration.

N32G435 series products can work stably in the temperature range of -40°C to +105°C, supply voltage from 1.8V to 3.6V, provide a variety of power modes for users to choose, meet the requirements of low-power applications. This series of products are available in 28/32/36/48/64 pin package, according to the different package form, the device in the peripheral configuration is different.

Figure 1-1 N32G435 series block diagram



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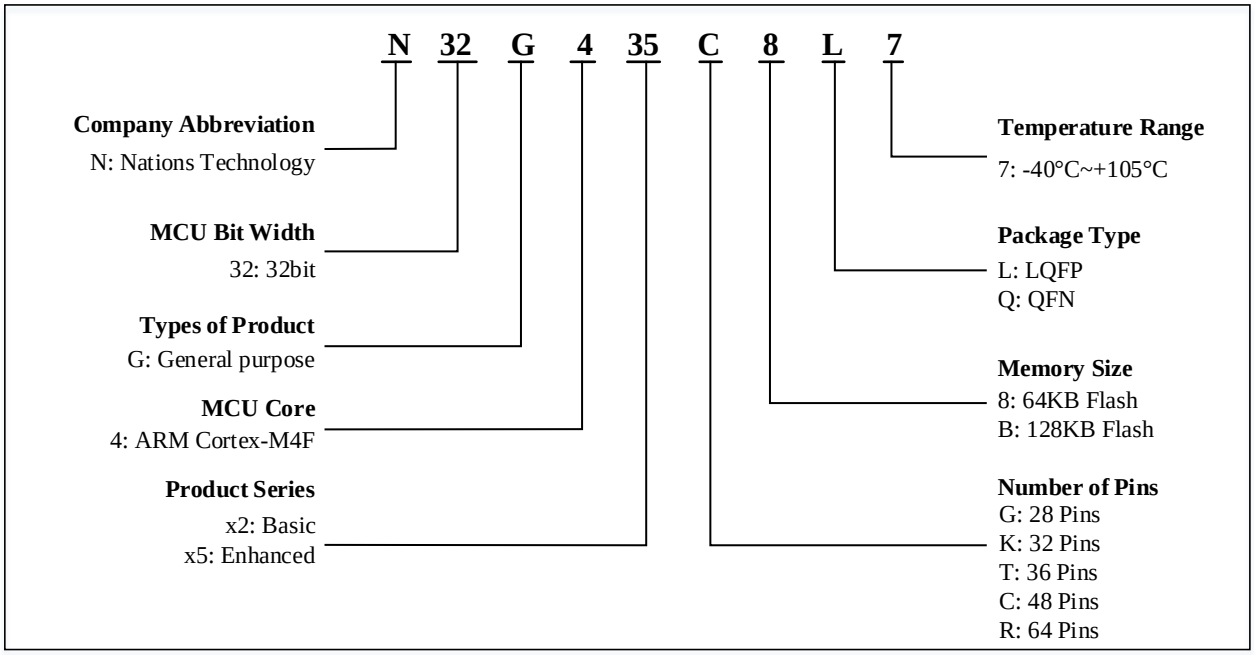
1.1 Part number information

Figure 1-2 N32G435 series part number information



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1.2 List of devices

Table 1-1 N32G435 series resource configuration

Part Number		N32G435G8/B		N32G435K8/B		N32G435C8/B		N32G435R8/B	
Flash (KB)		64	128	64	128	64	128	64	128
SRAM (KB)		16	32	16	32	24	32	24	32
CPU frequency		ARM Cortex-M4 @ 108MHz, 135DMIPS							
Working environment		1.8~3.6V/-40~105℃							
Timer	General	5							
	Advanced	2							
	Basic	2							
	LPTIM	1							
Communication interface	SPI(1)	1		2					
	I2S(1)	1		2					
	I2C	2							
	UART	2							
	USART	2		2		3			
	LPUART	1							
	USB	不支持		1					
	CAN	不支持		1					
GPIO		24		26		38		52	
DMA Number of Channels		1x 8 Channel							
12bit ADC Number of channels		1x 10 Channel						1x 16 Channel	
12bit DAC Number of channels		1x 1 Channel							
OPAMP/COMP		2/2							
Algorithm support		DES/TDES, AES, SHA1/SHA224/SHA256 SM1, SM3, SM4, SM7, CRC16/CRC32, TRNG							
Security protection		Read-write protection (RDP/WRP), storage encryption, partition protection, secure boot							
Package		QFN28		LQFP32		LQFP48		LQFP64	

1. SPI1 and SPI2 interfaces have the flexibility to switch between SPI mode and I2S audio mode.

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2 Function introduction

2.1 Processor core

The N32G435 family integrates the latest generation of embedded ARM Cortex™-M4F processors, enhanced computing power based on the Cortex™-M3 core, new floating point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 1.25DMIPS/MHz. Its efficient signal processing capabilities are combined with the advantages of low power consumption, low cost, and ease of use of the Cortex-M family of processors to meet the requirements of a mixture of control and signal processing capabilities and easy to use applications.

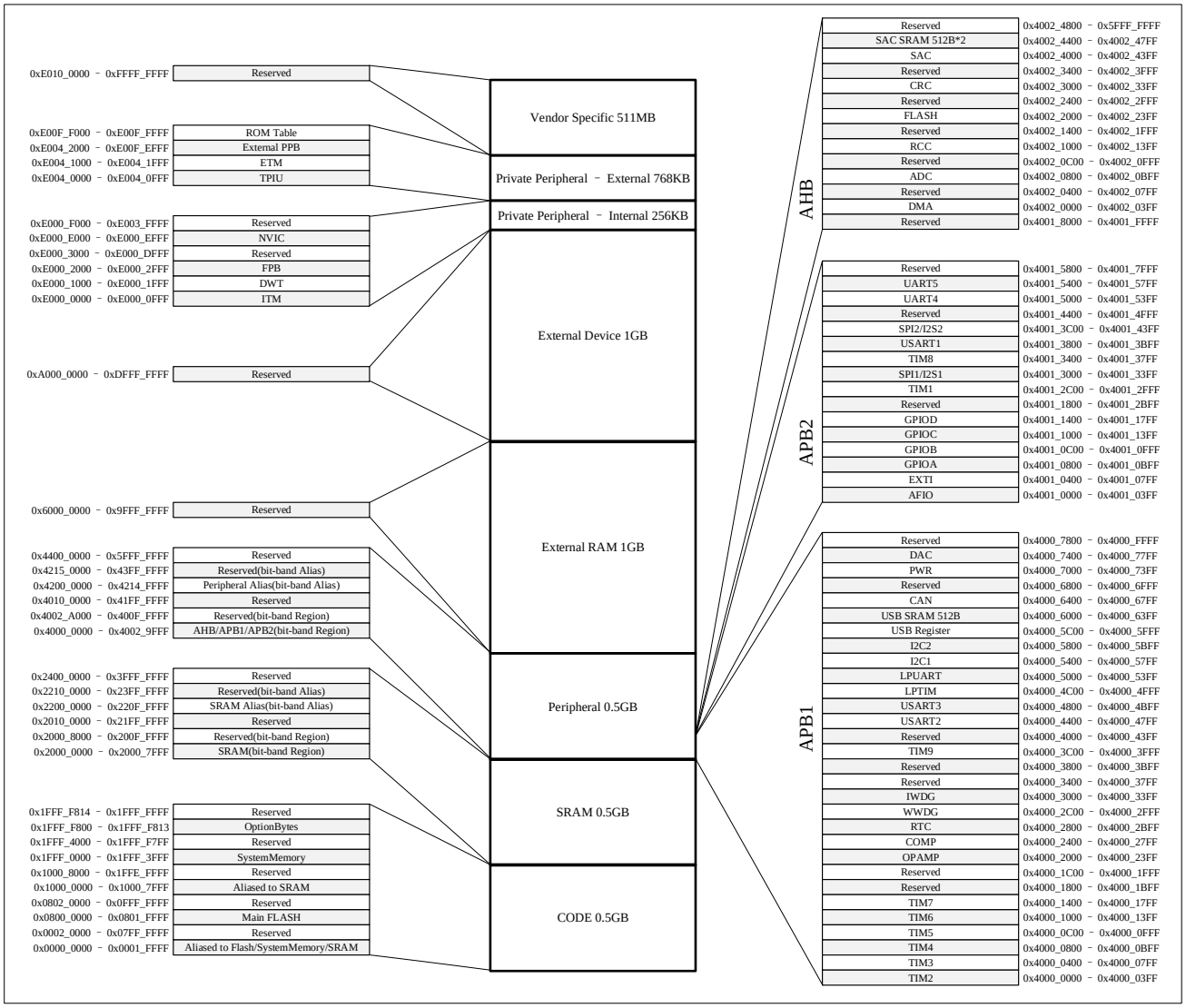
The ARM Cortex™-M4F 32-bit compact instruction set processor provides excellent code efficiency.

Note: Cortex-M4F is backward compatible with Cortex-M3 code.

2.2 Storage

N32G435 series devices include embedded encrypted Flash memory and embedded SRAM.

Figure 2-1 Memory map



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2.2.1 Embedded FLASH memory

Integrated from 64K to 128K bytes embedded encryption FLASH (FLASH), used to store programs and data, page size of 2Kbyte, supporting page erasing, word writing, word reading, half word reading, byte reading operations.

Support storage encryption protection, write automatic encryption, read automatic decryption (including program execution operation).

Support user partition management, can be divided into a maximum of three user partitions, different users cannot access each other's data (only executable code).

2.2.2 Embedded SRAM

The chip integrates a built-in SRAM of up to 32K bytes, including SRAM1 and SRAM2. The maximum size of SRAM1 is 24K bytes, and that of SRAM2 is 8K bytes. In STOP2 mode, SRAM1 and SRAM2 can retain data. In STANDBY mode, only SRAM2 can retain data.

2.2.3 Nested vector interrupt controller (NVIC)

Built-in nested vector interrupt controller, capable of handling up to 66 maskable interrupt channels (not including the 16 Cortex™-M4F interrupts) and 16 priorities.

- Tightly coupled NVIC enables low latency interrupt response processing
- Interrupt vector entry address directly into the kernel
- Tightly coupled NVIC interface
- Allows early handling of interrupts
- Handles late arriving higher-priority interrupts
- Support interrupt tail link function
- Automatically saves processor state
- Automatically resumes when the interrupt returns with no additional instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.3 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 25 edge detectors for generating interrupt/event requests.Each interrupt line can be independently configured with its triggering event (rising edge or falling edge or bilateral edge) and can be individually shielded. There is a suspended register that maintains the state of all interrupt requests. EXTI can detect clock cycles with pulse widths smaller than internal APB2. Up to 52 universal I/O ports are connected to 16 external interrupts.

2.4 Clock system

The device provides a variety of clocks for users to choose from, including internal high speed RC oscillator HSI (16MHz), internal multi-speed clock MSI (100K-4MHz configurable), internal low speed clock LSI (40KHz), external high speed clock HSE (4MHz~32MHz), external low speed clock LSE (32.768KHz), PLL.

During reset, the internal MSI clock is set as the default CPU clock, and then the user can choose the external HSE clock with failure monitoring function.When an external clock failure is detected, it will be isolated, the system will automatically switch to MSI, and if interrupts are enabled, the software can receive the corresponding interrupt.Also, complete interrupt management of the PLL clock can be adopted when needed (such as when an indirectly used external oscillator fails).

MSI clock can be used to wake up quickly and execute instructions in STOP2 state, or provide clock for the system in low power operation state, and some other scenarios with low clock accuracy and high power consumption requirements.

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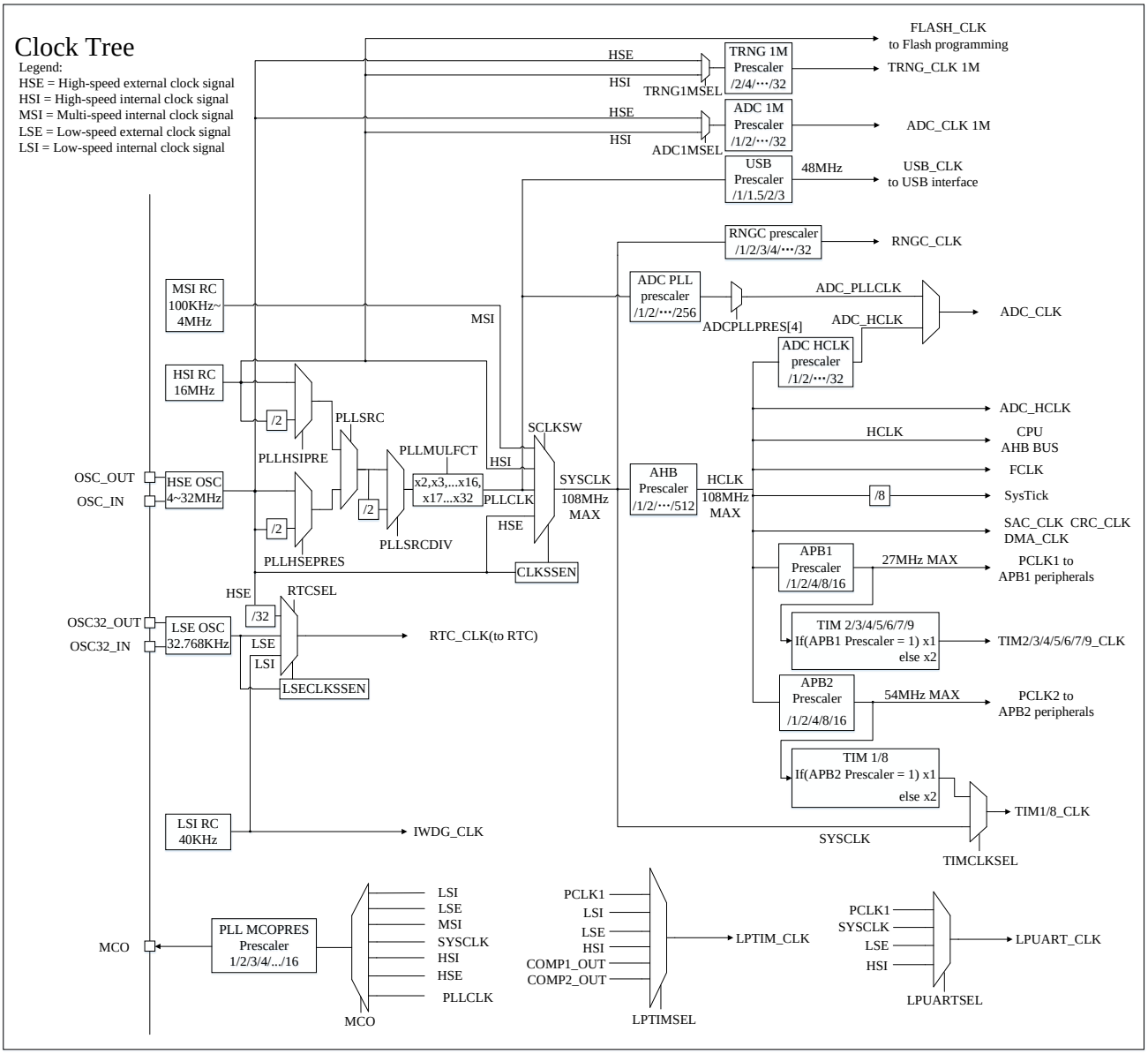
The built-in clock security system detects whether the external HSE or LSE fails in real time. If the external clock fails, the system automatically switches to the internal clock and generates an interrupt alarm.

Multiple prescalers are used to configure the AHB frequency, high speed APB (APB2) and low speed APB (APB1) regions. AHB has a maximum frequency of 108MHz, APB2 has a maximum frequency of 54MHz and APB1 has a maximum frequency of 27MHz.

When using USB function, both HSE and PLL must be used and the CPU frequency must be 48MHz, 72MHz or 96MHz.

Figure 2-2 Clock tree



2.5 **Boot mode**

At BOOT time, the BOOT mode after reset can be selected with the BOOT0 pin and option byte BOOT configuration (USER2):

- Boot from program FLASH memory
- Boot from system memory
- Boot from internal SRAM

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The Bootloader is stored in the system memory and can program the flash memory through USART1 or USB interface.

2.6 Power supply scheme

- V_{DD} = 1.8~3.6V: The V_{DD} pin supplies power to the I/O pin and the internal voltage regulator.
- V_{SSA}, V_{DDA} = 1.8~3.6V: provides power supply for ADC, DAC, OPAMP and COMP. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively. See **Figure 4-3 Power supply scheme**.

2.7 Reset

POR and BOR circuits are integrated inside the device. This part of the circuit is always in working state to ensure that the system works stably when the power supply exceeds 1.8V. When V_{DD} falls below a set threshold ($V_{POR/BOR}$), place the device in the reset state without using an external reset circuit.

2.8 Programmable voltage detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD} and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be started through the program. See **Table 4-6** for values of $V_{POR/PDR}$ and V_{PVD}.

2.9 Voltage regulator

The voltage regulator has 2 control modes:

- Master mode, MCU run in RUN, SLEEP modes
- Low power mode, MCU run in LP RUN, LP SLEEP, STOP2, and STANDBY modes

The voltage regulator is always in the master mode after the MCU reset.

2.10 Low power mode

The N32G435 series supports five low-power modes.

- LP-RUN mode

In LP-RUN (Low Power RUN) mode, CPU running at MSI clock, executes programs in FLASH or SRAM, and PLL turned off. USB/CAN/algorithm (SAC) module turned off, other peripherals are configurable.

- SLEEP mode

In SLEEP mode, only CPU stop, all peripherals are configurable and can wake up the CPU when an interrupt/event occurs.

- LP-SLEEP mode

In LP-SLEEP (Low Power SLEEP) mode, CPU stop, PLL turned off, USB/CAN/SAC module turned off, other peripherals are configurable, and all IOs remain in the same state as in RUN mode.

- STOP2 mode

STOP2 mode is based on the Cortex®-M4F deep sleep mode, and all the core digital logic areas are powered off. Main voltage regulator (MR) is off, HSE/HSI/MSI/PLL is off. CPU register retention, LSE/LSI optional work, RCC retention, all GPIO retention, SRAM1 and SRAM2 optional retention, SPI, USART/UART, I2C, WWDG retention, 80 byte backup register retention, RET domain and low power supply domain work normally.

The microcontroller can be woken up from STOP2 mode by any signal configured as EXTI, which can be 16 external EXTI signals (I/O related), WKUP pin wakeup, RTC periodic wake up, RTC alarm, RTC tamper, RTC timestamp,

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NRST reset, IWDG reset.

- STANDBY mode

In STANDBY mode, the current consumption is low. Internal voltage regulator is turned off, PLL, HSI RC oscillator and HSE crystal oscillator are also turned off, only LSE and LSI can optionally work. After entering STANDBY mode, main domain register contents will be lost, SRAM2 is optional, and the STANDBY circuit still works.

External reset signal on the NRST, IWDG reset, rising/falling edge on the WKUP pin, RTC periodic wake up, RTC alarm, RTC timestamp and RTC tamper can wake up the microcontroller from STANDBY mode.

Note: RTC, IWDG and corresponding clock can not be stopped when entering standby mode.

2.11 Direct memory access (DMA)

The device integrates a flexible general-purpose DMA controller that supports eight DMA channels to manage data transfers from memory to memory, peripherals to memory, and memory to peripherals. The DMA controller supports the management of ring buffers, avoiding interruptions when controller transfers reach the end of the buffer.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The transmission length, source address and destination address of each channel can be set separately by software.

DMA can be used with major peripherals: SPI, I2C, USART, TIMx (general, basic and advanced timers), DAC, I2S and ADC.

2.12 Real time clock (RTC)

RTC is a set of continuously running counters with a built-in calendar clock module that provides a perpetual calendar function, as well as alarm interrupt and periodic interrupt (minimum 2 clock cycles) functions. The RTC will not be reset by the system or power reset source, nor will it be reset when woken up from STANDBY mode. The RTC can be driven by either a 32.768kHz external crystal oscillator, an internal low-power 40kHz RC oscillator, or a high-speed external clock with 128 frequency divisions. For application scenarios requiring very high timing accuracy, it is recommended to use an external 32.768kHz clock as the clock source. Meanwhile, to compensate for the clock deviation of natural crystal, a 256Hz signal can be output to calibrate the clock of RTC. The RTC has a 22-bit predivider for a time-based clock, which will produce a 1-second long time reference at 32.768kHz by default. In addition, RTC can be used to trigger wake up in low-power mode.

2.13 Timer and watchdog

Up to 2 advanced control timers, 5 general-purpose timers and 2 basic timers, 1 low power timer, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 2-1 Comparison of timer functions

Timer	Counter resolution	Counter type	Prescaler factor	Generate DMA requests	Capture/compare channels	Complementary output
TIM1 TIM8	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	Y
TIM2 TIM3 TIM4 TIM5 TIM9	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	N
TIM6 TIM7	16	up	Any integer between 1 and 65536	Y	0	N

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2.13.1 Low power timer (LPTIM)

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes except for Standby mode. LPTIM can run without internal clock source, it can be used as a "Pulse Counter". Also, the LPTIM can wake up the system from low-power modes, to realize "Timeout functions" with extreme low power consumption.

Main features:

- 16-bit up counter
- 3-bit prescaler, 8 kinds of frequency division factors (1, 2, 4, 8, 16, 32, 64, 128)
- Multiple clock sources:
  - Internal clock source: LSE, LSI, HSI, PCLK1, COMP1_OUT or COMP2_OUT
  - External clock source: External clock source through LPTIM Input1 (operating without LP oscillator, for pulse counter applications)
- 16-bit auto-load register (LPTIM_ARR)
- 16-bit compare register (LPTIM_COMP)
- Continuous or one-shot mode counting mode
- Programmable software or hardware input trigger
- Programmable digital filter for glitch filtering
- Configurable output (square wave, PWM)
- Configurable IO polarity
- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting (quadrature and non-quadrature)

2.13.2 Basic timer (TIM6 and TIM7)

Basic timers TIM6 and TIM7 each contain a 16-bit auto-reload counter. These two timers are independent of each other and do not share any resources. The basic timer can provide a time reference for general purpose timers, and in particular can provide a clock for a digital-to-analog converter (DAC). The basic timer is directly connected to the DAC inside the chip and drives the DAC directly through the trigger output.

Main features:

- 16-bit auto-reload up-counting counters
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Synchronization circuit for triggering DAC
- The events that generate the interrupt/DMA are as follows:
  - Update event

2.13.3 General-purpose timer (TIMx)

The general-purpose timers (TIM2, TIM3, TIM4, TIM5 and TIM9) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- TIM2, TIM3, TIM4, TIM5 and TIM9 up to 4 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture

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- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Supports capture of internal comparator output signals. TIM9 supports capture of internal HSE, LSI, and LSE signals

2.13.4 Advanced control timer (TIM1 and TIM8)

The advanced control timers (TIM1 and TIM8) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc. Advanced timers have complementary output function with dead-time insertion and break function. Suitable for motor control.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 and TIM8 up to 4 capture/compare channels:
  - PWM output
  - Ouput compare
  - One-pulse mode output
  - Input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with adjustable dead-time
  - For TIM1 and TIM8, channel 1,2,3 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- TIM1_CC5 and TIM8_CC5 for COMP blanking
- TIM1_CC6 is used to switch the input channel of OPAMP1 and OPAMP2; TIM8_CC6 can switch the input channel of OPAMP2
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and

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position

- Hall sensor interface: used to do three-phase motor control

2.13.5 SysTick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard down-counter.

Main features:

- 24 bit down-counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.13.6 Watchdog (WDG)

Support for two watchdog independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and a 3-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP2 and STANDBY modes. Once activated, if the dog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. The option byte can be configured to start the watchdog software or hardware. Reset and low power wake up are available.

Window watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the down-counter value is flushed before the T6 bit becomes 0, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 7-bit down-counter value (in the control register) is flushed before the down-counter reaches the window register value, then an MCU reset will also occur. This indicates that the down-counter needs to be refreshed in a finite time window.

Main features:

- The clock of the window watchdog (WWDG) is obtained by dividing the APB1 clock frequency by 4096.
- Programmable free-running down-counter
- Reset condition:
  - When the down-counter is less than 0x40, a reset occurs (if the watchdog is started)
  - A reset occurs when the down-counter is reloaded outside the window (if the watchdog is started)
  - If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWINT) occurs when the down-counter equals 0x40, which can be used to reload the counter to avoid WWDG reset

2.14 I^2C bus interface

The device integrates up to two independent I2C bus interfaces, which provide multi-host function and control all I2C bus-specific timing, protocol, arbitration and timeout. Supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, SMBus (System Management Bus) and PMBus (Power Management Bus).

Main features:

- Multi-master function: this module can be used as master device or slave device

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- I2C master device function:
  - Generate a clock
  - Generate start and stop signals
- I2C slave device function:
  - Programmable address detection
  - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode
  - Stop bit detection
- Generate and detect 7-bit/10-bit addresses and broadcast calls
- Support different communication speeds
  - Standard speed (up to 100 kHz)
  - Fast (up to 400 kHz)
  - Fast+ (up to 1MHz)
- Status flags:
  - Transmitter/receiver mode flag
  - Byte transfer complete flag
  - I2C bus busy flag
- Error flags:
  - Arbitration loss in master mode
  - Acknowledge (ACK) fail after address/data transfer
  - Error start or stop condition detected
  - Overrun or underrun when clock extending is disable
- Two interrupt vectors:
  - 1 interrupt for address/data communication success
  - 1 interrupt for an error
- Optional extend clock function
- DMA of single-byte buffers
- Generation or verification of configurable PEC(Packet error detection)
- In transmit mode, the PEC value can be transmitted as the last byte
- PEC error check for the last received byte
- SMBus 2.0 compatible
  - Timeout delay for 25ms clock low
  - 10ms accumulates low clock extension time of master device
  - 25ms accumulates low clock extension time of slave device
  - PEC generation/verification of hardware with ACK control
  - Support address resolution protocol (ARP)
- Compatible with the PMBus

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2.15 Universal synchronous/asynchronous transceiver (USART)

N32G435 series products integrate up to 5 serial transceiver interfaces, including 3 universal synchronous/asynchronous transceivers (USART1, USART2 and USART3) and 2 universal asynchronous transceivers (UART4 and UART5). All five interfaces provide asynchronous communication, support for IrDA SIR ENDEC transmission codec, multi-processor communication mode, single-wire half-duplex communication mode, and LIN master/slave function.

The USART1, USART2, and USART3 interfaces have hardware CTS and RTS signal management, ISO7816-compatible smart card mode, and similar to SPI communication mode, all of which can use DMA operations.

Main features:

- Full duplex, asynchronous communication
- NRZ standard format
- Fractional baud rate generator system, baud rate programmable, used for sending and receiving
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates 13 bit interrupters and detects 10/11 bit interrupters
- Output clock for synchronous transmission
- IRDA SIR encoder decoder, supports 3/16 bit duration in normal mode
- Smart card simulation function:
  - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3
  - 0.5 and 1.5 stop bits for smart cards
- Single-wire half duplex communication
- Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer
- Independent transmitter and receiver enable bits
- Detect flag:
  - Receive buffer is full
  - Send buffer empty
  - Transmission complete
- Parity control:
  - Send parity bit
  - Check the received data
- Four error detection flags:
  - Overflow error
  - Noise error
  - Frame error
  - Parity error
- 10 USART interrupt sources with flags:
  - CTS change

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- LIN break detection
- Send data register empty
- Send complete
- Received data register is full
- Bus was detected to be idle
- Overflow error
- Frame error
- Noise error
- Parity error

- Multi-processor communication, if the address does not match, then enter the silent mode
- Wake up from silent mode (via idle bus detection or address flag detection)
- Mode configuration:

USART modes	USART1	USART2	USART3	UART4	UART5
Asynchronous mode	support	support	support	support	support
Hardware flow control	support	support	support	nonsupport	nonsupport
Multiple buffer communication (DMA)	support	support	support	support	support
Multiprocessor communication	support	support	support	support	support
Synchronous mode	support	support	support	nonsupport	nonsupport
Smart card	support	support	support	nonsupport	nonsupport
Half duplex (Single wire mode)	support	support	support	support	support
IrDA	support	support	support	support	support
LIN	support	support	support	support	support

2.16 Low power asynchronous transceiver (LPUART)

The device integrates a low-power asynchronous serial transceiver (LPUART), which can receive data in STOP2 state (maximum baud rate 9600) and wake up MCU after generating an interrupt event. In addition, by configuring the clock as a high-speed clock (such as APB or HSE clock), it can be used as a regular asynchronous serial port to support higher baud rate.

Main features:

- Provide standard asynchronous communication bits (start, parity, and stop bits)
  - Generates 1 start bit
  - Generates 1-bit parity bit (odd or even parity can be set) or no parity bit
  - Generates 1 stop bit
  - Bytes are transmitted from the lowest to the highest
- Support 32 bytes receive FIFO and 1 byte send FIFO
- Provides send mode control bits
- Programmable baud rate
- Full duplex communication
- Support data communication and error handling interruption
- Access to status bits can be done in two ways: query or interrupt

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- Parity error flag
- Baud rate parameter register
- Support hardware flow control
- Support DMA data transfer
- Support the following interrupt event sources to wake up the MCU in STOP2 state:
  - Start bit detection
  - Receive buffer non-empty detection
  - Received the specified 1 bytes of data
  - Received the specified 4 bytes of data

2.17 Serial peripheral interface (SPI)

The device integrates two SPI interfaces, which allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner. This interface can be configured in master mode and provides a communication clock (SCK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-line simplex synchronous transmission using a two-way data line, and reliable communication using CRC checks.

Main features:

- 3-wire full-duplex synchronous transmission
- Two-wire simplex synchronous transmission with or without a third bidirectional data line
- 8 or 16 bit transmission frame format selection
- Master or slave operations
- Support multi-master mode
- 8 master mode baud rate predivision frequency coefficient (Max $f_{PCLK}/2$)
- Slave mode frequency (Max $f_{PCLK}/2$)
- Fast communication between master mode and slave mode
- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes
- Programmable clock polarity and phase
- Programmable data order, MSB before or LSB before
- Dedicated send and receive flags that trigger interrupts
- SPI bus busy flag
- Hardware CRC for reliable communication:
  - In send mode, the CRC value can be sent as the last byte
  - In full-duplex mode, CRC is automatically performed on the last byte received
- Master mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffer with DMA capability: generates send and receive requests
- Maximum interface speed: 27Mbps

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2.18 Serial audio interface (I^2S)

I^2S is a 3-pin synchronous serial interface communication protocol. The device integrates two standard I^2S interfaces (multiplexed with SPI) and can operate in master or slave mode. The two interfaces can be configured for 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8kHz to 96kHz. It supports four audio standards, including Philips I^2S, MSB and LSB alignment, and PCM.

It can work in master and slave mode in half duplex communication. When it acts as a master device, it provides clock signals to external slave devices through an interface.

Main features:

- Simplex communication (send or receive only)
- Master or slave operations
- 8-bit linear programmable prescaler for accurate audio sampling frequencies (8KHz to 96KHz)
- The data format can be 16, 24, or 32 bits
- Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame)
- Programmable clock polarity (steady state)
- The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel
- Supported I^2S protocols:
  - I^2S Philips standard
  - MSB alignment standard (left aligned)
  - LSB alignment standard (right aligned)
  - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame)
- The data direction is always MSB first
- Both send and receive have DMA capability
- The master clock can be output to external audio devices at a fixed rate of 256xFs(Fs is the audio sampling frequency)

2.19 Controller area network (CAN)

The device integrates a CAN bus interface compatible with 2.0A and 2.0B (active) specifications, with bit rates up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

Main features:

- Support CAN protocol 2.0A and 2.0B active mode
- Baud rate up to 1Mbps
- Supports time-triggered communication
- Send:
  - Three sending mailboxes
  - The priority of sent packets can be configured by software
  - Records the timestamp of the time when the SOF was sent

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- Receive:
  - Level 3 depth of 2 receiving FIFO
  - Variable filter group
  - There are 14 filter groups
  - Identifier list
  - The FIFO overflow processing mode is configurable
  - Record the time stamp of the receipt of the SOF
- Time-triggered communication mode:
  - Disable automatic retransmission mode
  - 16-bit free run timer
  - Timestamp can be sent in the last 2 bytes of data
- Management:
  - Interrupt masking
  - The mailbox occupies a separate address space to improve software efficiency

2.20 Universal serial bus (USB)

The device is embedded with a full speed USB compatible device controller that follows the full speed USB device (12Mbit/s) standard. The endpoint can be configured by software and has suspend/resume function. The USB dedicated 48MHz clock is generated directly from the internal PLL.

Main features:

- Comply with the technical specifications of USB2.0 full-speed equipment
- 1 to 8 USB endpoints can be configured
- CRC(cyclic redundancy check) generation/check, reverse non-return to zero (NRZI) encoding/decoding and bit filling
- Double buffer mechanism for bulk/isochronous endpoints
- Support USB suspend/resume operation
- Frame lock clock pulse generation
- Integrated USB DP signal line pull-up 1.5K resistor (user can enable or disable through software control)

2.21 General purpose input/output interface (GPIO)

Up to 52 GPIO, which can be divided into four groups (GPIOA/GPIOB/GPIOC/GPIOD). Each group of GPIOA, GPIOB, GPIOC and GPIOD has 16 ports. Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up or pull-down), or alternate peripheral function port. Most GPIO pins are shared with digital or analog alternate peripherals, and some I/O pins are multiplexed with clock pins. All GPIO pins except ports with analog input capability have high current passing capability.

Main features:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
  - Input floating
  - Input pull up (weak pull up)

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- Input pull down (weak pull down)
- Analog function
- Open drain output
- Push-pull output
- Push-pull alternate function
- Open drain alternate function

- General I/O (GPIO)
  - During and just after reset, the alternate function is not enabled, except for BOOT0 (which is an input pull-down), and the I/O port is configured to analog input mode
  - After reset, the default state of pins associated with the debug system is enable SWJ, the JTAG pin is placed in input pull-up or pull-down mode:
    - JTDI in pull-up mode
    - JTCK in pull-down mode
    - JTMS in pull-up mode
    - NJTRST in pull-up mode
  - When configured as output, values written to the output data registers are output to the appropriate I/O pins. Can be output in push pull mode or open drain mode
- Separate bit setting or bit clearing functions
- External interrupt/wake up: All ports have external interrupt capability. In order to use external interrupts, ports must be configured in input mode
- Alternate function: (port bit configuration register must be programmed before using default alternate function)
- GPIO lock mechanism, which freezes I/O configurations.When a LOCK is performed on a port bit, the configuration of the port bit cannot be changed until the next reset

2.22 Analog/Digital converter (ADC)

The device supports a 12-bit 5Msps sequential comparison ADC with a sampling rate of single-ended and differential inputs, measuring 16 external and 3 internal sources.

Main features:

- Support 12/10/8/6-bits resolution configurable
  - The maximum sampling rate at 12bit resolution is 5.14MSPS
  - The maximum sampling rate at 10bit resolution is 6MSPS
  - The maximum sampling rate at 8bit resolution is 7.2MSPS
  - The maximum sampling rate at 6bit resolution is 9MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - AHB_CLK can be configured as the working clock source, up to 108MHz
  - PLL can be configured as a sampling clock source, up to 72MHZ, support 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128, 256 frequency division

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- The AHB_CLK can be configured as the sampling clock source, up to 72MHz, and supports frequency 1,2,4,6,8,10,12,16,32
- The timing clock is used for internal timing functions and the frequency must be configured to 1MHz

- Supports timer trigger ADC sampling
- Support 2.048V internal reference voltage $V_{REFBUFFER}$
- Interrupts when conversion ends, injection conversion ends, and analog watchdog events occur
- Single and continuous conversion modes
- Automatic scan mode from channel 0 to channel N
- Support for self-calibration
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately by channel
- Both regular conversions and injection conversions have external triggering options
- Continuous mode
- ADC power supply requirements: 1.8V to 3.6V
- ADC input range: VREF- ≤ VIN ≤ VREF+
- ADC can use DMA operations, and DMA requests are generated during regular channel conversion
- Analog watchdog function can monitor one, multiple, or all selected channels with great precision. When the monitored signal exceeds the preset threshold, an interruption will occur

2.23 Operational amplifier (OPAMP)

The device integrates up to 2 independent operational amplifiers with multiple operating modes such as external amplifier, internal follower and programmable amplifier (PGA) (or both internal amplifier and external filter).

Main features:

- Support rail to rail input
- Forward and reverse input checkboxes
- OPAMP working mode can be configured as:
  - Independent mode (external gain setting)
  - PGA mode, programmable gain 2X, 4X, 8X, 16X, 32X
  - Follower mode
- The internally connected ADC channel is used to measure the output signal of the operational amplifier

2.24 Analog comparator (COMP)

The device integrates up to 2 comparators, among which COMP1 supports low power mode and can work in STOP2 state. It can be used as a separate device (all ports of the comparator are plugged into the I/O) or in combination with a timer. In the case of motor control, it can be combined with the PWM output from the timer to form periodic current control.

Main features:

- Rail to rail comparators are supported

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- The reverse and forward sides of the comparator support the following inputs
  - Optional I/O
  - DAC channel output
  - Internal 64 level adjustable voltage input reference:
    - VREF1 is a low-power voltage reference source, which can only be used for COMP1
    - VREF2 is a non-low power voltage reference source, which can be used for COMP1 and COMP2
- Programmable hysteresis can be configured as no hysteresis, low hysteresis, medium hysteresis, and high hysteresis
- The comparator can output to EITHER I/O or timer input for triggering
  - Capture events
  - OCREF_CLR events (for periodic current control)
  - The brake events
- The comparator supports output filtering, including analog and digital filtering
- COMP1/COMP2 can form a window comparator
- Support comparator output with blanking, you can choose forbidden energy blanking or Timer1_OC5, Timer8_OC5 as blanking input
- Each comparator can have interrupt wake up capability, support from SLEEP mode wake up, COMP1 can support under STOP2 wake up

2.25 Digital/Analog converter (DAC)

The device integrates a digital to analog converter (DAC), which is a 12-bit digital input and voltage output digital/analog converter with an output channel of built-in Buffer. DAC can be referenced via V_{DDA} or $V_{REFBUFFER}$.

Main features:

- An output channel for a built-in Buffer
- Configurable 8/12-bits output
- Configurable left and right data alignment in 12-bit mode
- Synchronous update function
- Generate noise wave
- Generate triangle wave
- DMA support
- External trigger for conversion

2.26 Temperature sensor (TS)

The temperature sensor generates a voltage that varies linearly with temperature in the range of $1.8V<V_{DDA}<3.6V$. The temperature sensor is internally connected to the ADC_IN17 input channel for converting the output of the temperature sensor to digital values.

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2.27 Cyclic redundancy check calculation unit (CRC)

Integrated CRC32 and CRC16 functions, the cyclic redundancy check (CRC) caculating unit is based on a fixed generation polynomial to obtain any CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting flash memory errors, CRC cells can be used to calculate signatures of software in real time and compare them with signatures generated when linking and generating the software.

Main features:

- CRC16: supports polynomials $X^{16} + X^{15} + X^2 + 1$
- CRC32: supports polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- CRC16 calculation time: 1 AHB clock cycles (HCLK)
- CRC32 calculation time: 1 AHB clock cycles (HCLK)
- The initial value for cyclic redundancy computing is configurable
- Support DMA mode

2.28 Algorithmic hardware acceleration engine (SAC)

Embedded algorithm hardware acceleration engine, support a variety of international algorithms and national cryptosymmetric cryptography algorithm and hash cryptography algorithm acceleration, compared with pure software algorithm can greatly improve the encryption and decryption speed.

The hardware supports the following algorithms:

- Supports DES symmetric algorithms
  - DES and 3DES encryption and decryption operations are supported
  - TDES supports 2KEY and 3KEY mode
  - Supports CBC and ECB mode
- Supports the SYMMETRIC AES algorithm
  - Supports 128bits, 192bits, or 256bits key length
  - Supports CBC, ECB, and CTR mode
- SHA hash algorithm is supported
  - Supports SHA1, SHA244, SHA256
- Supports the MD5 digest algorithm
- Supports symmetric SM1, SM4, SM7 algorithm and SM3 hash algorithm

2.29 Unique device serial number (UID)

N32G435 series products have two built-in unique device serial numbers of different lengths, which are 96-bit unique device ID (UID) and 128-bit unique customer ID (UCID). These two device serial numbers are stored in the system configuration block of flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32G435 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing flash memory, this unique identifier is

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combined with software encryption and decryption algorithm to further improve the security of code in flash memory. It can also be used to activate Secure Bootloader with security functions.

UCID is 128-bit, which complies with the definition of national technology chip serial number. It contains the information related to chip production and version.

2.30 Serial single-wire JTAG debug port (SWJ-DP)

Embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-wire debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

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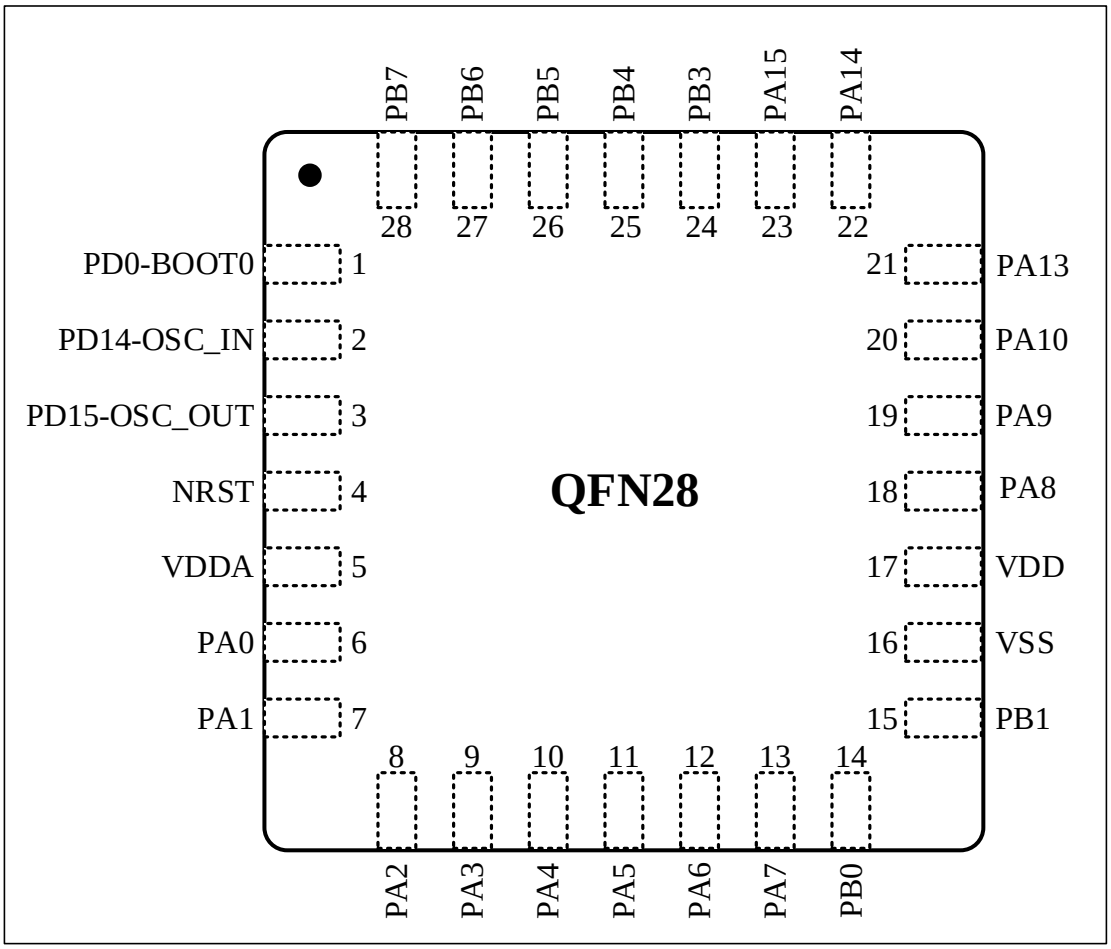
3 Pin and description

3.1 Pinouts

3.1.1 QFN28

Figure 3-1 N32G435 series QFN28 pinout



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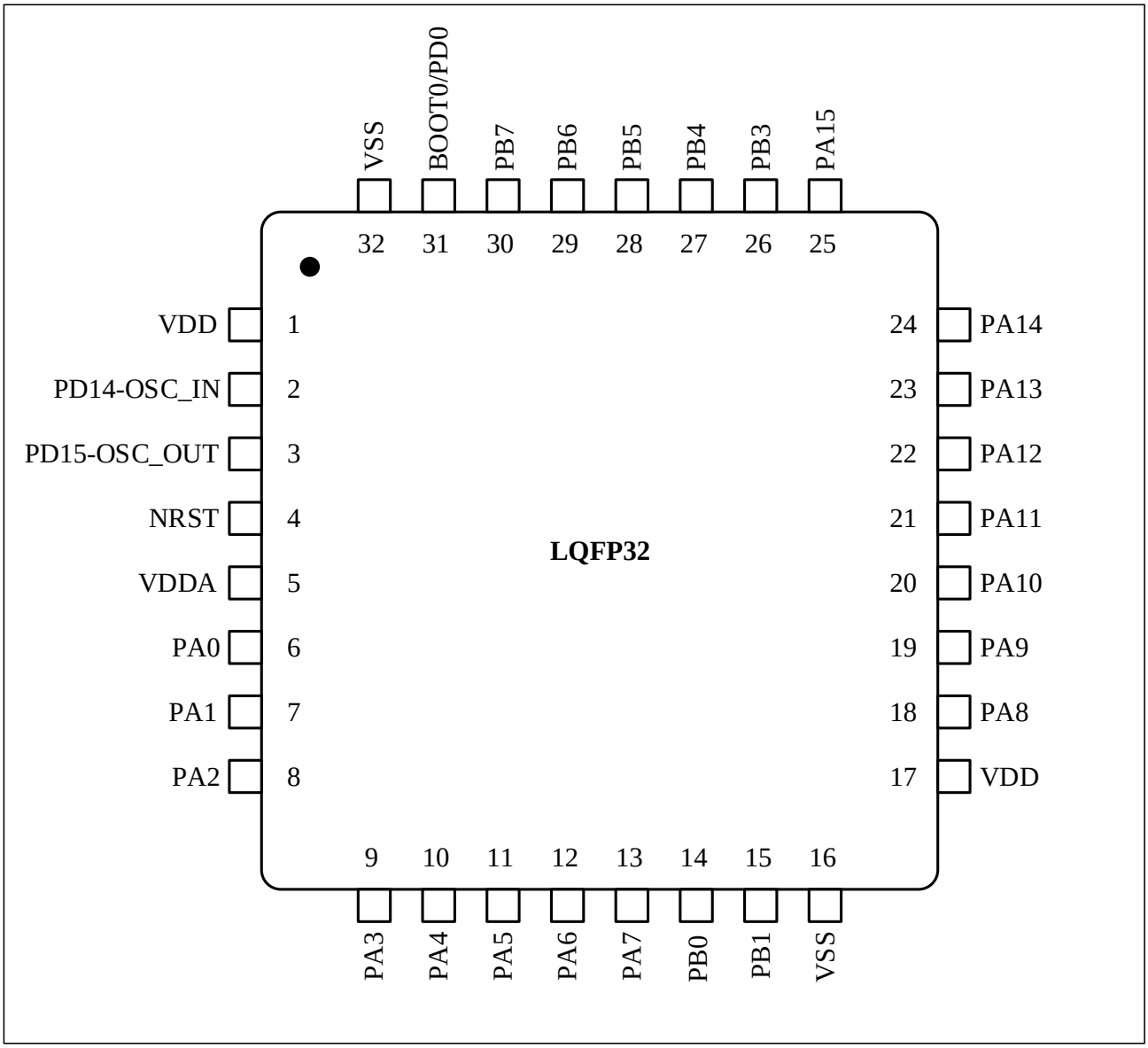
3.1.2 LQFP32

Figure 3-2 N32G435 series LQFP32 pinout



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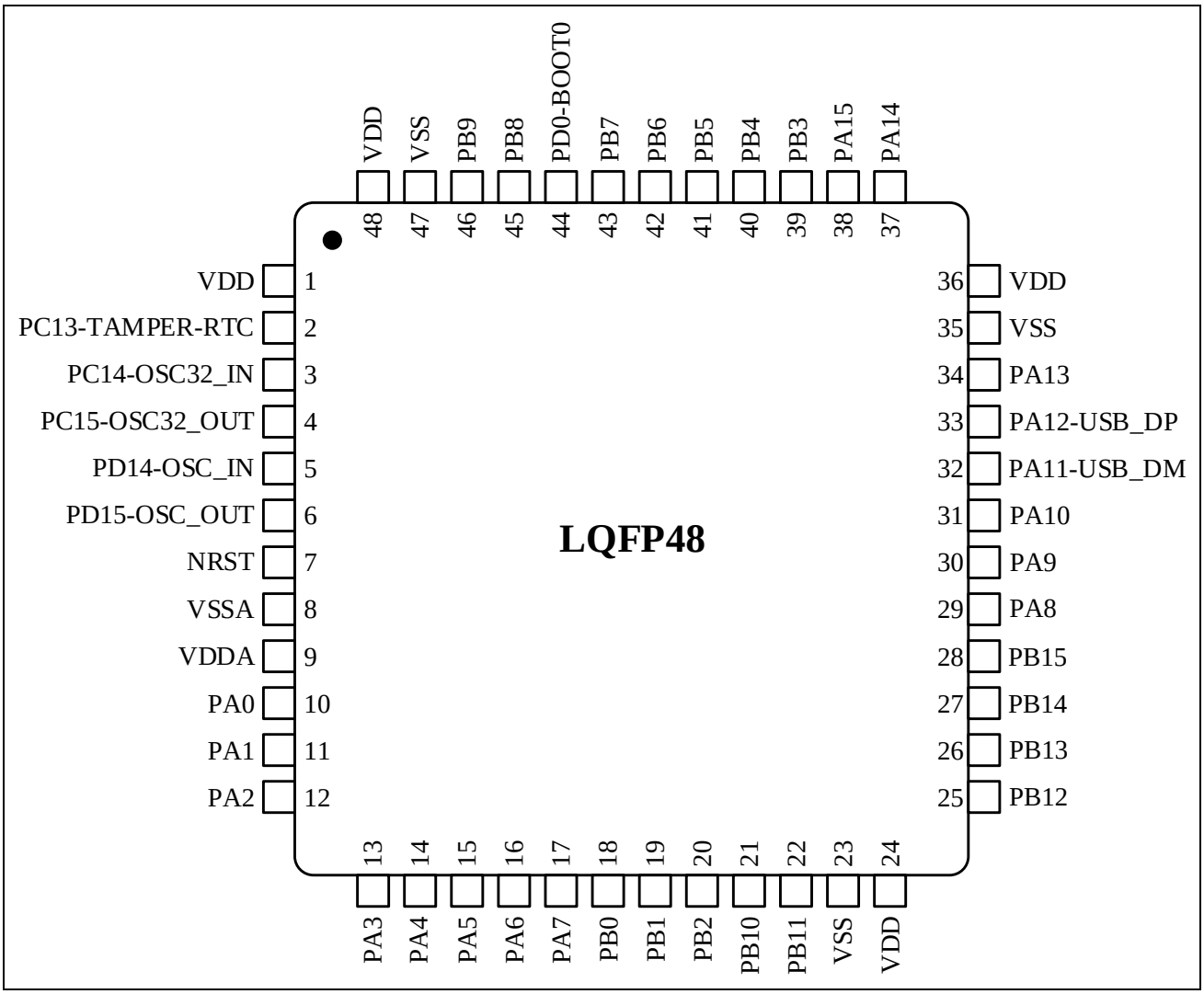
3.1.3 LQFP48

Figure 3-3 N32G435 series LQFP48 pinout



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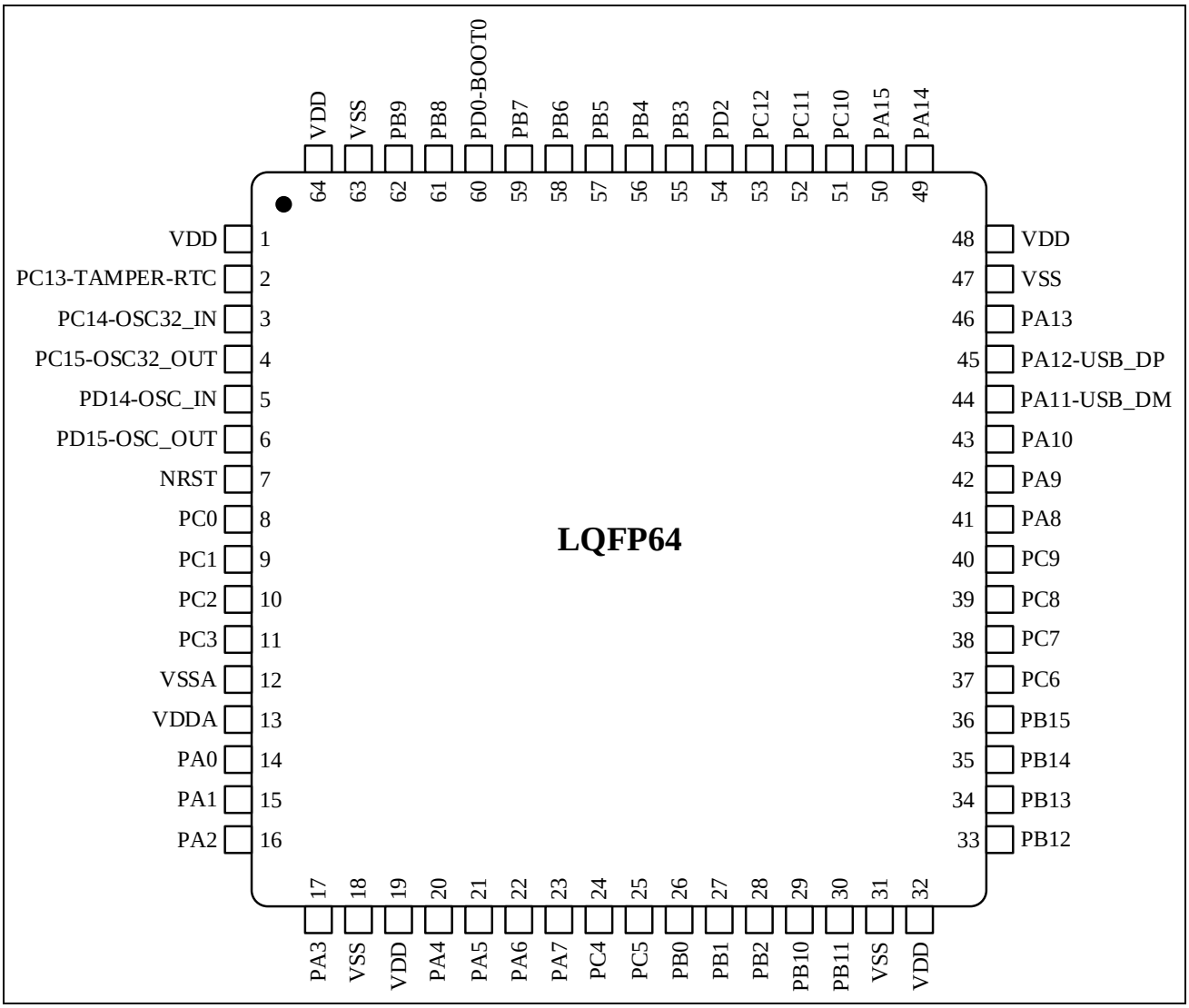
3.1.4 LQFP64

Figure 3-4 N32G435 series LQFP64 pinout



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3.2 Pin definition

Table 3-1 Pin definition

QFN28	LQFP32	LQFP48	LQFP64	Pin Name (after reset)	Type(1)	I/O structure(2)	Fail-safe(4) support	Alternate function(3)	Optional function
-	1	1	1	VDD	S	-	-	-	-
-	-	2	2	PC13-TAMPER- RTC(9)	I/O	TTa	Yes	TIM1_CH1N EVENTOUT	TAMP1-RTC RTC_OUT WKUP2
-	-	3	3	PC14- OSC32_IN	I/O	TTa	Yes	-	OSC32_IN
-	-	4	4	PC15- OSC32_OUT	I/O	TTa	Yes	-	OSC32_OUT
2	2	5	5	PD14-OSC_IN	I/O	TTa	No	USART2_TX I2C2_SDA TIM1_CH3N	OSC_IN
3	3	6	6	PD15-OSC_OUT	I/O	TTa	No	USART2_RX I2C2_SCL	OSC_OUT
4	4	7	7	NRST	I	-	-	-	-
-	-	-	8	PC0(9)	I/O	TTa	Yes	I2C1_SCL LPTIM_IN1 EVENTOUT	ADC_IN11(6)
-	-	-	9	PC1(9)	I/O	TTa	Yes	LPTIM_OUT I2C1_SDA EVENTOUT	ADC_IN12(6)
-	-	-	10	PC2(9)	I/O	TTa	Yes	EVENTOUT LPTIM_IN2	ADC_IN13(6)
-	-	-	11	PC3(9)	I/O	TTa	Yes	LPTIM_ETR EVENTOUT	ADC_IN14(6)
-	-	8	12	VSSA/VREF-	S	-	-	-	-
5	5	9	13	VDDA/VREF+	S	-	-	-	-
6	6	10	14	PA0	I/O	TTa	Yes	USART2_CTS LPUART_RX TIM2_CH1 TIMER2_ETR TIM5_CH1 TIM8_ETR SPI1_MISO I2S1_MCK EVENTOUT COMP1_OUT	ADC_IN1(5) COMP1_INM COMP1_INP WKUP1 TAMP2-RTC
7	7	11	15	PA1	I/O	TTa	Yes	USART2_RTS LPUART_TX TIM5_CH2 TIM2_CH2 EVENTOUT	ADC_IN2(5) COMP1_INP OPAMP1_VINP
8	8	12	16	PA2	I/O	TTa	Yes	USART2_TX TIM5_CH3 TIM2_CH3 I2C2_SDA COMP2_OUT EVENTOUT	ADC_IN3(5) OPAMP1_VOUT COMP1_INP(8) COMP2_INM
9	9	13	17	PA3	I/O	TTa	Yes	USART2_RX LPUART_RX TIM5_CH4 I2C2_SCL EVENTOUT	ADC_IN4(5) COMP1_INP(7) COMP2_INP OPAMP1_VINM
-	-	-	18	VSS	S	-	-	-	-
-	-	-	19	VDD	S	-	-	-	-
10	10	14	20	PA4	I/O	TTa	No	USART2_CK	DAC_OUT

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QFN28	LQFP32	LQFP48	LQFP64	Pin Name (after reset)	Type(1)	I/O structure(2)	Fail-safe(4) support	Alternate function(3)	Optional function
								LPUART_TX I2C1_SCL SPI1_NSS I2S1_WS USART1_TX EVENTOUT	ADC_IN5(5) COMP1_INM COMP2_INM OPAMP1_VINP OPAMP2_VINP
11	11	15	21	PA5	I/O	TTa	Yes	SPI1_SCK I2C1_SDA I2S1_CK USART1_RX EVENTOUT	ADC_IN6(6) COMP1_INM COMP2_INM OPAMP1_VINP OPAMP2_VINM
12	12	16	22	PA6	I/O	TTa	Yes	LPUART_CTS SPI1_MISO I2S1_MCK TIM8_BKIN TIM3_CH1 TIM1_BKIN COMP2_OUT EVENTOUT	ADC_IN7(6) OPAMP2_VOUT COMP2_INM COMP2_INP
13	13	17	23	PA7	I/O	TTa	Yes	SPI1_MOSI I2S1_SD TIM1_CH1N TIM8_CH1N TIM3_CH2 COMP2_OUT EVENTOUT	ADC_IN8(6) COMP2_INP OPAMP1_VINP OPAMP2_VINP
-	-	-	24	PC4(9)	I/O	TTa	Yes	LPUART_TX I2C1_SCL EVENTOUT	ADC_IN15(6)
-	-	-	25	PC5	I/O	TTa	Yes	LPUART_RX I2C1_SDA EVENTOUT	ADC_IN16(6) OPAMP1_VINM OPAMP2_VINM
14	14	18	26	PB0	I/O	TTa	Yes	TIM1_CH2N TIM3_CH3 TIM8_CH2N UART4_TX EVENTOUT	ADC_IN9(6) OPAMP2_VINM
15	14	19	27	PB1(9)	I/O	TTa	Yes	LPUART_RTS TIM1_CH3N TIM3_CH4 TIM8_CH3N UART4_RX EVENTOUT	ADC_IN10(6)
-	-	20	28	PB2	I/O	TTa	No	LPTIM_OUT TIM9_ETR EVENTOUT	-
-	-	21	29	PB10	I/O	TTa	Yes	USART3_TX LPUART_TX I2C2_SCL TIM2_CH3 EVENTOUT	COMP1_INP
-	-	22	30	PB11(9)	I/O	TTa	Yes	USART3_RX LPUART_RX I2C2_SDA TIM2_CH4 EVENTOUT	-
16	16	23	31	VSS	S	-	-	-	-
17	-	24	32	VDD	S	-	-	-	-

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-	-	25	33	PB12(9)	I/O	TTa	Yes	SPI2_NSS I2S2_WS I2C2_SMBA USART3_CK TIM1_BKIN LPUART_RTS TIM9_CH1 EVENTOUT	-
-	-	26	34	PB13(9)	I/O	TTa	Yes	SPI2_SCK I2S2_CK USART3_CTS I2C2_SCL LPUART_CTS TIM1_CH1N TIM9_CH2 EVENTOUT	-
-	-	27	35	PB14	I/O	TTa	Yes	SPI2_MISO I2S2_MCK TIM1_CH2N USART3_RTS I2C2_SDA LPUART_RTS TIM9_CH3 EVENTOUT UART4_TX	OPAMP2_VINP
-	-	28	36	PB15(9)	I/O	TTa	Yes	UART4_RX SPI2_MOSI I2S2_SD TIM1_CH3N TIM9_CH4 EVENTOUT	-
-	-	-	37	PC6(9)	I/O	TTa	Yes	SPI2_NSS I2S2_WS TIM8_CH1 TIM3_CH1 EVENTOUT	-
-	-	-	38	PC7(9)	I/O	TTa	Yes	SPI2_SCK I2S2_CK TIM3_CH2 TIM8_CH2 EVENTOUT	-
-	-	-	39	PC8(9)	I/O	TTa	Yes	SPI2_MISO I2S2_MCK TIM8_CH3 TIM3_CH3	-
-	-	-	40	PC9(9)	I/O	TTa	Yes	SPI2_MOSI I2S2_SD TIM3_CH4 TIM8_CH4 EVENTOUT	-
18	18	29	41	PA8(9)	I/O	TTa	Yes	USART1_CK I2C2_SMBA TIM1_CH1 I2C2_SDA SPI1_NSS I2S1_WS MCO EVENTOUT	WKUP0 TAMP3-RTC
19	19	30	42	PA9(9)	I/O	TTa	Yes	USART1_TX I2C2_SCL TIM1_CH2	-

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QFN28	LQFP32	LQFP48	LQFP64	Pin Name (after reset)	Type(1)	I/O structure(2)	Fail-safe(4) support	Alternate function(3)	Optional function
								EVENTOUT	
20	20	31	43	PA10(9)	I/O	TTa	Yes	USART1_RX I2C2_SDA SPI1_SCK SPI2_SCK I2S1_CK I2S2_CK TIM1_CH3 EVENTOUT	-
-	21	32	44	PA11	I/O	TTa	No	USART1_CTS SPI2_MISO I2S2_MCK CAN_RX TIM1_CH4 COMP1_OUT EVENTOUT	USB_DM COMP2_INP
-	22	33	45	PA12	I/O	TTa	No	USART1_RTS SPI2_MOSI I2S2_SD CAN_TX TIM1_ETR COMP2_OUT EVENTOUT	USB_DP COMP1_INP
21	23	34	46	PA13(9)	I/O	TTa	Yes	SWDIO-JTMS SPI2_NSS I2S2_WS EVENTOUT	-
-	-	35	47	VSS	S	-	-	-	-
-	-	36	48	VDD	S	-	-	-	-
22	24	37	49	PA14(9)	I/O	TTa	Yes	SWCLK-JTCK USART2_CK I2C1_SDA COMP2_OUT	-
23	25	38	50	PA15	I/O	TTa	Yes	JTDI USART2_CTS I2C1_SCL SPI2_NSS I2S2_WS TIM2_CH1 TIM2_ETR EVENTOUT	COMP2_INP
-		-	51	PC10(9)	I/O	TTa	Yes	USART3_TX UART4_TX LPUART_TX EVENTOUT	-
-		-	52	PC11(9)	I/O	TTa	Yes	USART3_RX UART4_RX LPUART_RX EVENTOUT	-
-		-	53	PC12(9)	I/O	TTa	Yes	USART3_CK UART5_TX EVENTOUT	-
-		-	54	PD2(9)	I/O	TTa	Yes	TIM3_ETR UART5_RX LPUART_RTS EVENTOUT	-
24	26	39	55	PB3	I/O	TTa	Yes	USART2_RTS SPI1_SCK I2S1_CK	COMP1_INP COMP2_INM

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QFN28	LQFP32	LQFP48	LQFP64	Pin Name (after reset)	Type(1)	I/O structure(2)	Fail-safe(4) support	Alternate function(3)	Optional function
								TIM2_CH2 JTDO-TRACESWO EVENTOUT	
25	27	40	56	PB4	I/O	TTa	Yes	USART2_TX SPI1_MISO I2S1_MCK TIM3_CH1 UART5_TX EVENTOUT NJTRST	COMP1_INP
26	28	41	57	PB5	I/O	TTa	Yes	USART2_RX I2C1_SMBA SPI1_MOSI I2S1_SD TIM3_CH2 UART5_RX LPTIM_IN1 EVENTOUT	COMP1_INM
27	29	42	58	PB6(9)	I/O	TTa	Yes	USART1_TX LPUART_TX I2C1_SCL SPI1_NSS I2S1_WS TIM1_CH2N TIM4_CH1 SPI2_SCK I2S2_CK LPTIM_ETR COMP1_OUT EVENTOUT	
28	30	43	59	PB7	I/O	TTa	Yes	USART1_RX LPUART_RX I2C1_SDA TIM4_CH2 EVENTOUT LPTIM_IN2 PVD_IN	COMP2_INP
1	31	44	60	BOOT0/PD0(9)	I/O	TTa	Yes	TRACECK	-
-		45	61	PB8(9)	I/O	TTa	Yes	I2C1_SCL CAN_RX TIM4_CH3 USART1_TX UART5_TX COMP1_OUT EVENTOUT	
-		46	62	PB9(9)	I/O	TTa	Yes	I2C1_SDA CAN_TX TIM4_CH4 UART5_RX COMP2_OUT EVENTOUT	
-	32	47	63	VSS	S	-	-	-	-
-	-	48	64	VDD	S	-	-	-	-

1. I = input, O = output, S = power supply.

2. TTa: 3.3V Standard IO.

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3. *This alternate function can be configured by the software to other pins (if the corresponding package model has such pins). For detailed information, please refer to the alternate function I/O chapter and debug setting chapter of the N32G435xx user reference manual.*
4. *Fail-safe indicates that when the chip has no power input, a high input level is added to the IO. The high input level does not flood into the chip, resulting in a certain voltage on the power supply and current consumption.*
5. *The corresponding ADC channel is a fast channel and supports a maximum sampling rate of 5.14MSPS (12Bit).*
6. *The corresponding ADC channel is a slow channel and supports a maximum sampling rate of 4.23MSPS (12Bit).*
7. *Only applicable if the second character in the 8-bit code in the last line of the chip silk screen is not "B".*
8. *Only applicable if the second character in the 8-bit code in the last line of the chip silk screen is "B".*
9. *No more than 5V can be tolerated on the pin.*

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4 Electrical characteristics

4.1 Parameter conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and maximum values

Unless otherwise specified, all minimums and maximums will be guaranteed under the worst ambient temperature, supply voltage and clock frequency conditions by performing tests on 100% of the product on the production line at ambient temperatures T_A = 25℃.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production; Base on comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean ±3∑).

4.1.2 Typical numerical value

Unless otherwise specified, typical data are based on T_A = 25℃ and V_{DD} = 3.3V. These data are for design guidance only and not tested.

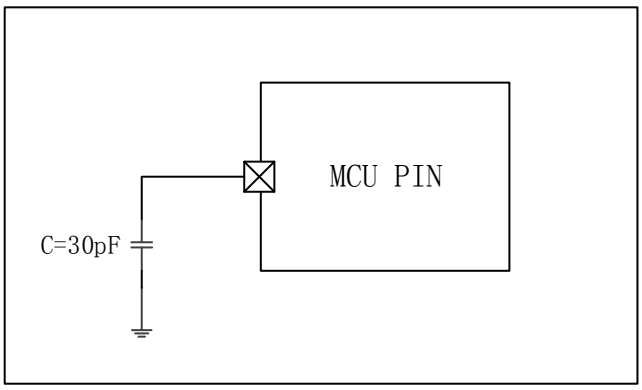
4.1.3 Typical curve

Unless otherwise specified, typical curves are for design guidance only and not tested.

4.1.4 Loading capacitor

The load conditions for measuring pin parameters are shown in the figure below:

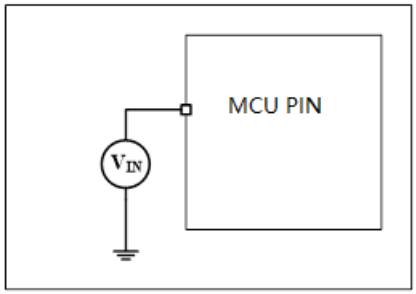
Figure 4-1 Load conditions of pins



4.1.5 Pin input voltage

The measurement of the input voltage on the pin is shown in the figure below:

Figure 4-2 Pin input voltage



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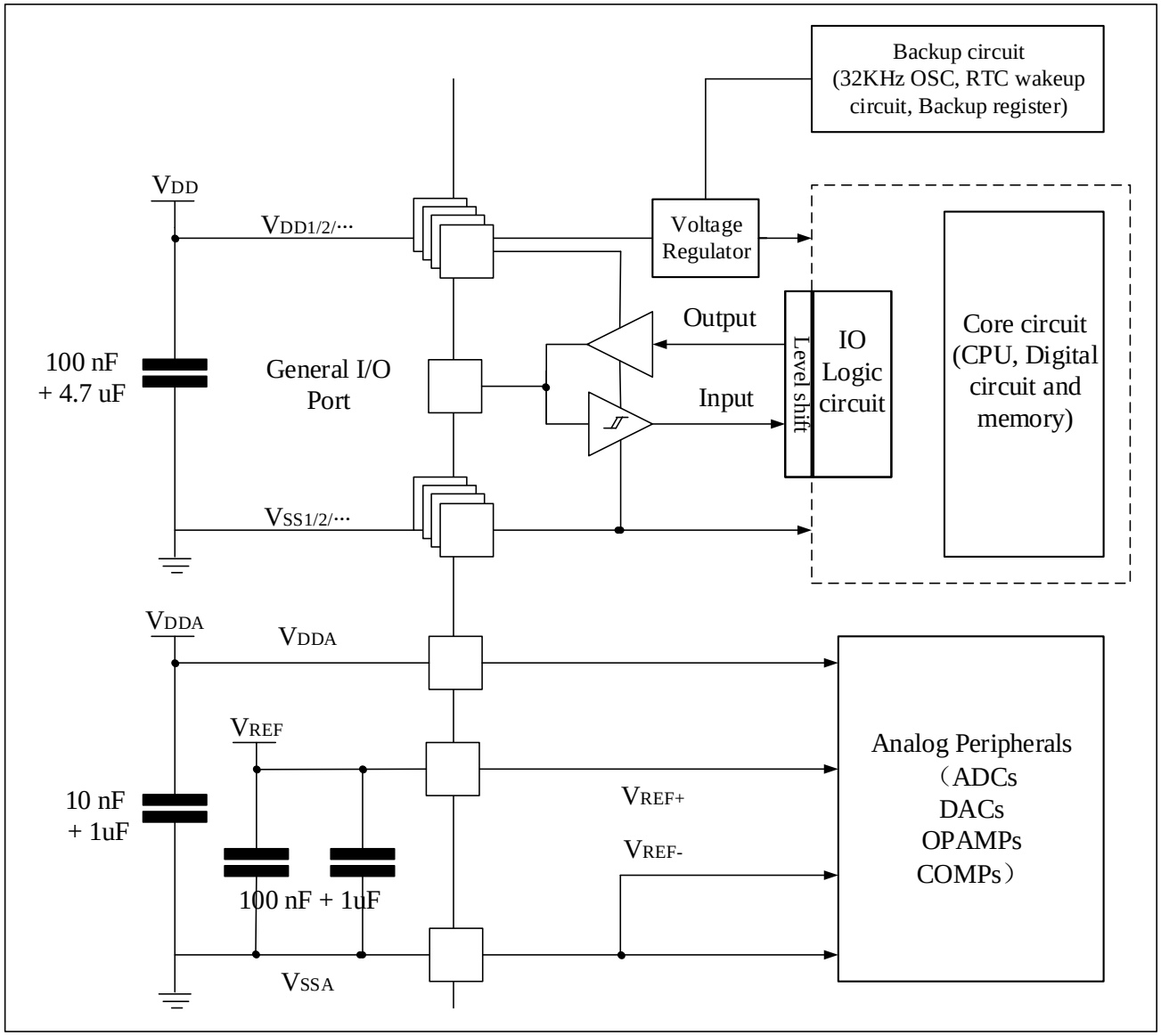
4.1.6 Power supply scheme

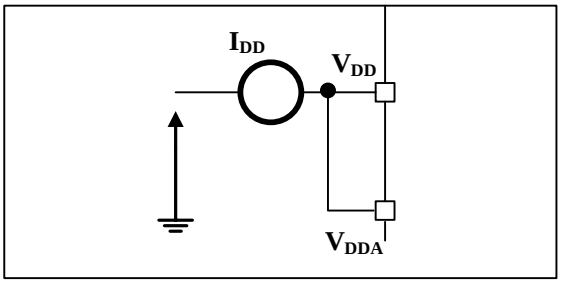
Figure 4-3 Power supply scheme



Note: Please refer to the hardware design guide for the capacitor connection method. V_{REF} is only available for ADC and DAC.

4.1.7 Current consumption measurement

Figure 4-4 Current consumption measurement scheme



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4.2 Absolute maximum rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (**Table 4-1**, **Table 4-2**, **Table 4-3**). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage characteristics

Symbol	Describe	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{DD}) (1)	-0.3	4.0	V
V_{IN}	Input voltage on other pins(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\|\Delta V_{DDx}\|$	Voltage difference between different supply pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD Electrostatic discharge voltage (human body model)	See section 4.3.11		-

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.
2. V_{IN} shall not exceed its maximum value. Refer to **Table 4-2** for current characteristics.

Table 4-2 Current characteristics

Symbol	Describe	Max (1)	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) (1) (4)	200	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) (1) (4)	200	
I_{IO}	Output current sunk by I/O and control pins	12	
	Output current source by I/O and control pins	- 12	
$I_{INJ(PIN)}$(2)(3)	Injection current on NRST pin	-5/0	
	Injection current on other pins	+/-5	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.
2. When V_{IN}>V_{DD}, there is a forward injection current; when V_{IN}<V_{SS}, there is a reverse injection current. $I_{INJ(PIN)}$ should not exceed its maximum value. Refer to **Table 4-1** for voltage characteristics.
3. Reverse injection current can interfere with the analog performance of the device.See section 4.3.19.
4. When the maximum current occurs, the maximum allowable voltage drop of V_{DD} is 0.1V_{DD}.

Table 4-3 Temperature characteristics

Symbol	Describe	Value	Unit
T_{STG}	Storage temperature range	- 40 ~ + 125	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-4 General operating conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	108	MHz

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f_{PCLK1}	Internal APB1 clock frequency	-	0	27	
f_{PCLK2}	Internal APB2 clock frequency	-	0	54	
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}	Analog operating of working voltage	Must be the same potential as V_{DD}(1)	1.8	3.6	V
T_A	Ambient temperature (temperature number 7)	-	- 40	105	℃
T_J	Junction temperature range	7 suffix version	- 40	125	℃

1. It is recommended that the same power supply be used to power the V_{DD} and V_{DDA}. During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA}.

4.3.2 Operating conditions at power-on and power-off

The parameters given in the following table are based on the ambient temperatures listed in **Table 4-4**.

Table 4-5 Operating conditions at power-on and power-off

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Supply voltage goes from 0 to V_{DD}	20	∞	μs/V
	V_{DD} fall time rate	Supply voltage drops from V_{DD} to 0	80	∞	

4.3.3 Embedded reset and power control module characteristics

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in **Table 4-4**.

Table 4-6 Features of embedded reset and power control modules

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PVD0_rising	2.1	2.15	2.2	V
		PVD0_falling	2	2.05	2.1	V
		PVD1_rising	2.25	2.3	2.35	V
		PVD1_falling	2.15	2.2	2.25	V
		PVD2_rising	2.4	2.45	2.5	V
		PVD2_falling	2.3	2.35	2.4	V
		PVD3_rising	2.55	2.6	2.65	V
		PVD3_falling	2.45	2.5	2.55	V
		PVD4_rising	2.7	2.75	2.8	V
		PVD4_falling	2.6	2.65	2.7	V
		PVD5_rising	2.85	2.9	2.95	V
		PVD5_falling	2.75	2.8	2.85	V
		PVD6_rising	2.95	3	3.05	V
		PVD6_falling	2.85	2.9	2.95	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
V_{BOR}	VDD Power on/off Reset threshold	POR0	1.6	1.64	1.68	V
		PDR0	1.58	1.62	1.66	V
		POR1	2.05	2.1	2.15	V
		PDR1	1.95	2	2.05	V
		POR2	2.25	2.3	2.35	V
		PDR2	2.15	2.2	2.25	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		POR3	2.55	2.6	2.65	V
		PDR3	2.45	2.5	2.55	V
		POR4	2.85	2.9	2.95	V
		PDR4	2.75	2.8	2.85	V
$T_{RSTTEMPO}$(1)	Reset duration	-	-	0.15	-	ms

1. Guaranteed by design, not tested in production.

4.3.4 Internal reference voltage

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in **Table 4-4**.

Table 4-7 Internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 ℃ < T_A < + 105 ℃	1.164	1.20	1.236	V
$T_{S\_vrefint}$(1)	The sampling time of the ADC when reading the internal reference voltage	-	-	5.1	10(2)	μs

1. The shortest sampling time is obtained through multiple loops in the application.
2. Guaranteed by design, not tested in production.

4.3.5 Power supply current characteristics

Current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, turnover rate of I/O pins, program location in memory, and code executed.

The measurement method of current consumption is described in **Figure 4-4**.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum current consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting period from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64 to 96MHz, 3 waiting periods from 96 to 108MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$.

The parameters given in **Table 4-8** and **Table 4-9** are based on tests at the ambient temperature and V_{DD} supply voltage listed in **Table 4-4**.

Table 4-8 Maximum current consumption in operating mode where the data processing code is run from internal flash

Symbol	Parameter	Condition	f_{HCLK}	Typ (1)	Unit
				VDD=3.3V, T_A = 105℃	
I_{DD}(2)	Supply current in	External clock,	108MHz	13	mA

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	operation mode	enable all peripherals	72MHz	9.5	
			36MHz	6.4	
		External clock, disable all peripherals	108MHz	9.6	
			72MHz	7.4	
			36MHz	5.2	
I_{DD}(3)	Supply current in operation mode	Internal clock, enable all peripherals	64MHz	6.0	mA
			32MHz	3.8	
		Internal clock, disable all peripherals	64MHz	4.0	
			32MHz	2.5	

1. Based on comprehensive evaluation, not tested in production.
2. In Rang0 mode (MR = 1.1V), enable PLL when f_{HCLK} > 8MHz.
3. In Rang1 mode (MR = 1.0V), enable PLL when f_{HCLK} > 8MHz.

Table 4-9 Maximum current consumption in sleep mode, code running in internal flash running

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1)	Unit
				V_{DD} = 3.3V, T_A = 105℃	
I_{DD}(2)	Supply current in sleep mode	External clock, enable all peripherals	108MHz	8.9	mA
			72MHz	7.0	
			36MHz	5.2	
		External clock, disable all peripherals	108MHz	5.7	
			72MHz	5.0	
			36MHz	4.0	
I_{DD}(3)	Supply current in sleep mode	Internal clock, enable all peripherals	64MHz	4.2	mA
			32MHz	2.5	
		Internal clock, disable all peripherals	64MHz	2.2	
			32MHz	1.6	

1. Based on comprehensive evaluation, not tested in production.
2. In Rang0 mode (MR = 1.1V), enable PLL when f_{HCLK} > 8MHz.
3. In Rang1 mode (MR = 1.0V), enable PLL when f_{HCLK} > 8MHz.

4.3.5.2 Typical current consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disable unless otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 96 MHz, and 3 waiting periods from 96 to 108MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in **Table 4-4**.
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}$ /4, $f_{PCLK2} = f_{HCLK}$ /2, $f_{ADCCLK} = f_{PCLK2}$ /4.

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Table 4-10 Typical current consumption in operating mode, where data processing code is run from internal Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals	Disable all peripherals	
I_{DD}(2)	Supply current in operation mode	External clock	108MHz	11.5	8.4	mA
			72MHz	8.4	6.3	
			36MHz	5.3	4.3	
I_{DD}(3)	Supply current in operation mode	Internal clock	64MHz	5.9	3.7	mA
			32MHz	3.3	2.3	

1. Typical values are measured at T_A = 25℃ and V_{DD} = 3.3V.
2. In Rang0 mode (MR = 1.1V), enable PLL when f_{HCLK} > 8MHz.
3. In Rang1 mode (MR = 1.0V), enable PLL when f_{HCLK} > 8MHz.

Table 4-11 Typical current consumption in sleep mode, data processing code is run from internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Typ (1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}(3)	Supply current in sleep mode	External clock	108MHz	7.8	4.7	mA
			72MHz	6.0	3.9	
			36MHz	4.1	3	
I_{DD}(4)	Supply current in sleep mode	Internal clock	64MHz	3.8	2.0	mA
			32MHz	2.3	1.4	

1. Typical values are measured at T_A = 25℃ and V_{DD} = 3.3V.
2. ADC additional 0.2mA current consumption is added. In the application environment, this part of the current is increased only when the ADC is turned on (set ADC_CTRL2.ON bit).
3. In Rang0 mode (MR = 1.1V), enable PLL when f_{HCLK} > 8MHz.
4. In Rang1 mode (MR = 1.0V), enable PLL when f_{HCLK} > 8MHz.

4.3.5.3 Low power mode current consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level of -V_{DD} or V_{SS} (no load).
- All peripherals are off disabled otherwise noted.

Table 4-12 Typical and maximum current consumption in shutdown and standby mode

Symbol	Parameter	Condition	Typ(1)		Unit
			V_{DD} = 3.3 V T_A = 25 ℃	V_{DD} = 3.3 V T_A = 105 ℃	
I_{DD_STOP2}	Supply current in Stop mode 2 (STOP2)	The external low-speed clock is on, the RTC is running, SRAM2 is on, all I/O states are on, and the independent watchdog is off	6(1)	27(1)	μA
$I_{DD\_STANDBY}$	Supply current in STANDBY mode	Low speed internal RC oscillator and independent watchdog are on	2.6(1)	7.6(1)	
		The low speed internal RC oscillator is on and the independent watchdog is off	2.5(1)	7.5(1)	
		The low speed internal RC oscillator and independent watchdog are closed, and the low speed oscillator and RTC are closed	2.4(1)	7.3(1)	

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1. Based on comprehensive evaluation, not tested in production.

4.3.6 External clock source characteristics

4.3.6.1 High-speed external clock source (HSE)

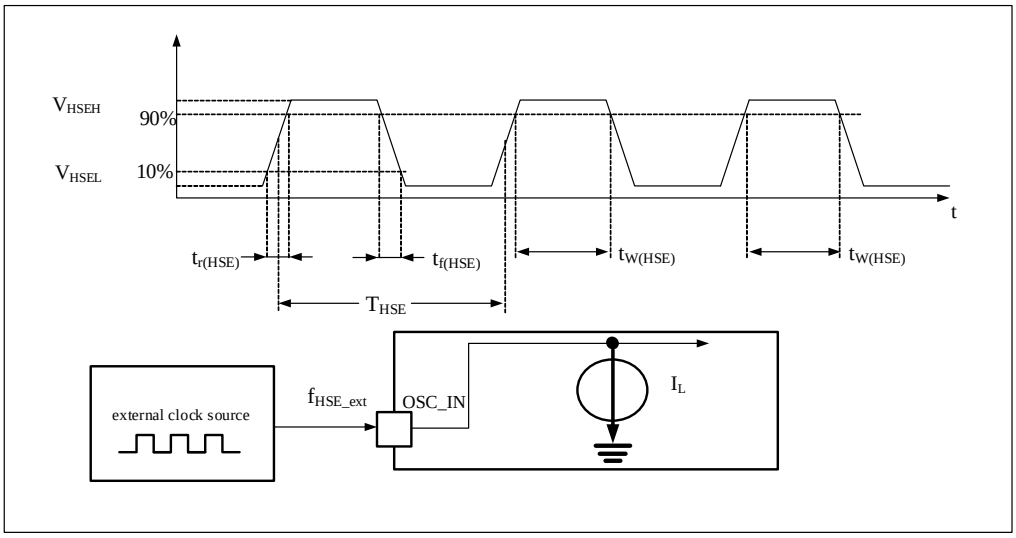
The characteristic parameters given in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage meet the conditions specified in **Table 4-4**.

Table 4-13 High-speed external user clock features(Bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency(1)	-	1	8	32	MHz
V_{HSEH}	OSC_IN Input pin high level voltage		0.8 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN Input pin low level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(HSE)}$	Time when OSC_IN is high or low(1)		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

Figure 4-5 AC timing diagram of an external high-speed clock source



4.3.6.2 Low-speed external clock source (LSE)

The characteristic parameters given in the following table are measured using a low speed external clock source, and the ambient temperature and supply voltage meet the conditions specified in **Table 4-4**.

Table 4-14 Features of a low-speed external user clock(Bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency(1)	-	0	32.768	1000	KHz
V_{LSEH}	OSC32_IN Input pin high level voltage		0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN Input pin low level voltage		V_{SS}	-	200	mV

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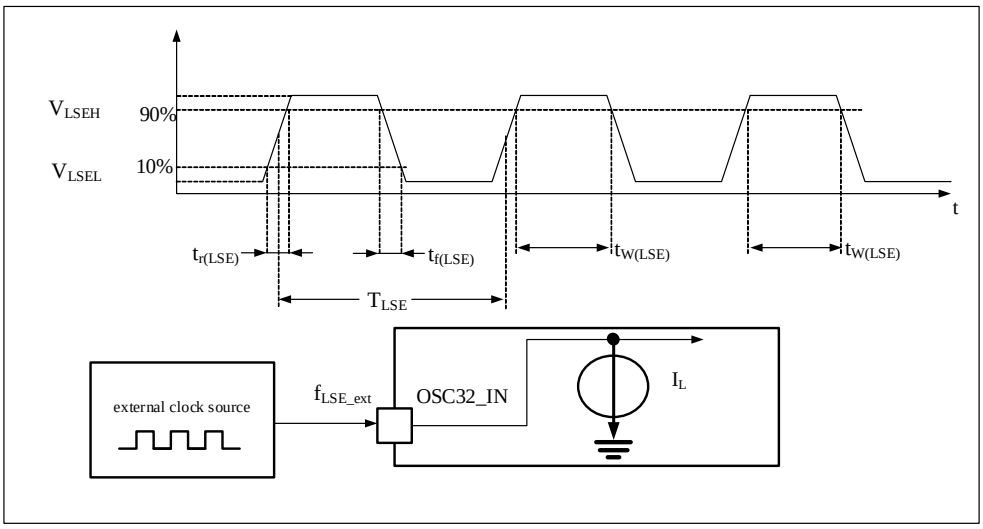
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(LSE)}$	OSC32_IN High or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN Rise or fall time(1)		-	-	50	
$DuCy_{(LSE)}$	Duty ratio	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

Figure 4-6 AC timing diagram of an external low speed clock source



High-speed external clock generated using a crystal/ceramic resonator

High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator.The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Table 4-15 HSE 4~32MHz oscillator characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	160	-	K Ω
i_2	HSE drive current	V_{DD} = 3.3V, V_{IN} = V_{SS} 30 pf load	-	1.5	-	mA
g_m	Transconductance of the oscillator	Start	-	10	-	mA/V
$t_{SU(HSE)}$(3)	Startup time (8M crystal)	V_{DD} is stabilized	-	3	-	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results, not tested in production.
3. $t_{SU(HSE)}$ is the start time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

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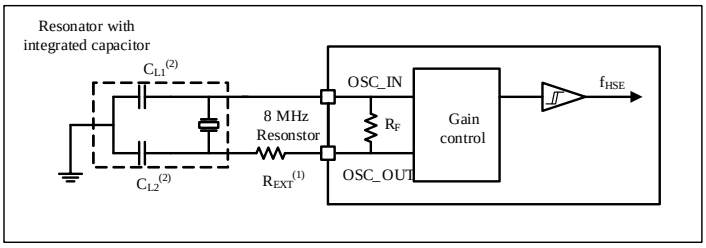
Figure 4-7 typical application using 8MHz crystal



1. The R_{EXT} value depends on the properties of the crystal. Typical values are 5 to 6 times R_S.
2. For C_{L1} and C_{L2}, it is recommended to use high quality ceramic dielectric vessels, and to select crystals or resonators that meet the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2}. When selecting C_{L1} and C_{L2}, the capacitance of PCB and MCU pins should be taken into account.

Low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator.The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in **Table 4-16**. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Note: For C_{L1} and C_{L2}, it is recommended to use high quality ceramic dielectric containers, and to select crystals or resonators that meet the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2}.

Load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

For example: If a resonator with load capacitance C_L = 6pF is selected and C_{stray} = 2pF, then $C_{L1} = C_{L2}$ = 8pF.

Table 4-16 LSE oscillator characteristics (f_{LSE} = 32.768kHz) (1) (2) (4) (5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistance	-	-	5	-	MΩ
g_m	Transconductance of the oscillator	-	-	15	-	μA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. See the cautions section at the top of this form.
3. $t_{SU(LSE)}$ is the starting time, which is the period from the LSE enabled by the software to the stable 32.768khz oscillation. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.
4. Please refer to the LSE crystal selection guide.
5. In order to ensure the stability of crystal operation, do not turn the adjacent pins when crystal is working.

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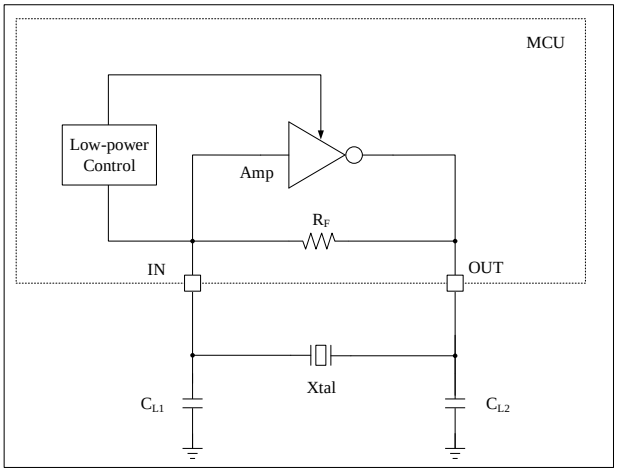
Figure 4-8 Typical application of 32.768kH crystal



4.3.7 Internal clock source characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

4.3.7.1 Multi-speed internal (MSI) RC oscillator

Table 4-17 MSI oscillator characteristics (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{MSI}	Range 0	MSI Frequency after Factory calibration, done at V_{DD} = 3.3V and T_A = 27 °C	-	100	-	KHz
	Range 1		-	200	-	KHz
	Range 2		-	400	-	KHz
	Range 3		-	800	-	KHz
	Range 4		-	1	-	MHz
	Range 5		-	2	-	MHz
	Range 6		3.96	4	4.1	MHz
Δ_{TEMP} (MSI) (2)	MSI oscillator frequency drift over temperature	T_A = 0 to 85 °C	-	±1%@4M ±1.2%@100k	-	%
		T_A = -40 to 105 °C	-	±2%@4M ±3%@100k	-	%
Δ_{VDD}(MSI) (2)	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	Range 0, V = 1.8V_{DD} to 3.6V	-	0.5 / - 1.5	-	%
		Range 6, V = 1.8V_{DD} to 3.6V	-	0.5 / - 5	-	%
t_{SU}(MSI) (3)	MSI oscillator start-up time	Range 0 /100k	-	20	-	µs
		Range 1 /200k	-	12	-	µs
		Range 2 /400k	-	8	-	µs
		Range 3 /800k	-	6	-	µs
		Range 4 /1M	-	10	-	µs
		Range 5 /2M	-	7	-	µs
		Range 6 /4M	-	6	-	µs
I_{DD}(MSI) (3)	MSI oscillator power consumption	Range 0 /100k	-	1.0	-	µA
		Range 1 /200k	-	1.2	-	µA
		Range 2 /400k	-	1.8	-	µA
		Range 3 /800k	-	3.2	-	µA
		Range 4 /1M	-	6	-	µA
		Range 5 /2M	-	9	-	µA

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Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Range 6 /4M	-	16	-	μA

1. V_{DD} = 3.3V, T_A = -40~105℃ unless otherwise specified.
2. This deviation range is the deviation of the oscillator after calibration;
3. Guaranteed by design, not tested in production.

4.3.7.2 High speed internal (HSI) RC oscillator

Table 4-18 HSI oscillator characteristics (1) (2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	V_{DD}=3.3V, T_A = 25℃, after calibration	15.84(3)	16(3)	16.16(3)	MHz
ACC_{HSI}	Temperature drift of HSI oscillator	V_{DD}=3.3V, T_A = -40~105℃, temperature drift	-2.5	-	2.5	%
		V_{DD}=3.3V, T_A = -10~85℃, temperature drift	-1.5(4)	-	1.0(4)	%
		V_{DD}=3.3V, T_A = 0~70℃, temperature drift	-1.2(4)	-	0.7(4)	%
$t_{SU(HSI)}$	HSI oscillator start time	-	-	-	5.0	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80(5)	100(5)	μA
			-	135(4)	160(4)	

1. V_{DD} = 3.3V, T_A = -40~105℃ unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. After Reflow, the frequency will drift, and the maximum drift value is about +1.6%.
4. Applicable to version F and later versions.
5. Applicable to the previous version of version F.

4.3.7.3 Low speed internal (LSI) RC oscillator

Table 4-19 LSI oscillator characteristics (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	Output frequency	25℃ calibration, V_{DD} = 3.3V	38	40	42	KHz
		V_{DD} = 1.8 V to 3.6 V, T_A = - 40 ~ 105 ℃	30	40	60	KHz
$t_{SU(LSI)}$ (2)	LSI oscillator startup time	-	-	40	80	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	0.12	-	μA

1. V_{DD} = 3.3V, T_A = -40~105℃ unless otherwise specified.
2. Guaranteed by characterization results, not tested in production.

4.3.8 Time to wake up from low power mode

The wake-up time listed in **Table 4-20** is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

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- STOP2 or STANDBY mode: clock source is RC oscillator
- SLEEP mode: The clock source is the clock used to enter sleep mode

All times were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

Table 4-20 Wake time in low power mode

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wake up from SLEEP mode	10	HCLK(2)
$t_{WUSLEEP}$(1)	Wake up from Low-Power SLEEP mode	10	HCLK(2)
$t_{WULPRUN}$(1)	Wake up from Low-Power RUN mode	5.5	μs (2)
$t_{WUSTOP2}$(1)	Wake up from STOP2 mode	12	μs (2)
$t_{WUSTDBY}$(1)	Wake up from STANDBY mode	50	

1. The wake up time is measured from the start of the wake up event until the first instruction is read by the user program.
2. The wake up time is obtained when MSI = 4MHz. If MSI is in other gears, the wake up time will be increased.

4.3.9 PLL characteristics

The parameters listed in **Table 4-21** are measured when the ambient temperature and power supply voltage meet the conditions in **Table 4-4**

Table 4-21 PLL features

Symbol	Parameter	Value			Unit
		Min	Typ	Max (1)	
f_{PLL_IN}	PLL PFD input clock(2)	4	8	32	MHz
	PLL Input clock duty cycle	40	50	60	%
f_{PLL_OUT}	PLL output clock(2)	32	-	108	MHz
t_{LOCK}	PLL Ready indicates signal output time(3)	-	-	150	μs
Jitter	RMS cycle-to-cycle jitter @108MHz(1)	-	6	-	ps
Ipll	Operating Current of PLL @108MHz VCO frequency. (1)	-	448	-	μA

1. Based on comprehensive evaluation, not tested in production.
2. The correct configuration coefficients need to be used so that the f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.
3. Guaranteed by design, not tested in production.

4.3.10 FLASH memory characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105℃.

Table 4-22 Flash memory characteristics

Symbol	Parameter	Condition	Min (1)	Typ (1)	Max (1)	Unit
tprog	32-bit programming time	T_A = - 40 ~ 105 ℃	-	100	-	μs
t_{ERASE}	Page (2K bytes) erasure time	T_A = - 40 ~ 105 ℃	-	2	20	ms
t_{ME}	Mass erase time	T_A = - 40 ~ 105 ℃	-	-	100	ms
I_{DD}	The power supply current	Read mode, f_{HCLK} = 108MHz, 3 waiting cycles, V_{DD} = 3.3V	-	-	3.42	mA
		Write mode, f_{HCLK} = 108MHz, V_{DD} = 3.3V	-	-	6.5	mA

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Symbol	Parameter	Condition	Min (1)	Typ (1)	Max (1)	Unit
		Erase mode, f_{HCLK} = 108MHz, V_{DD} = 3.3V	-	-	4.5	mA
		Power-down/stop mode, V_{DD} = 3.3~3.6V	-	-	0.035	μA
Vprog	Programming voltage	-	1.8	-	3.6	V

1. Guaranteed by design, not tested in production.

Table 4-23 Flash endurance and data retention life

Symbol	Parameter	Condition	Min (1)	Unit
N_{END}	Endurance (note: erasure times)	T_A = -40~105°C(7 suffix versions)	100	Kcycle
t_{RET}	Data retention period	10 kcycle(2) at T_A = 85°C	30	Years
		10 kcycle(2) at T_A = 105°C	20	
		10 kcycle(2) at T_A = 125°C	10	

1. Based on comprehensive evaluation, not tested in production.
2. Cycling performed over the whole temperature range.

4.3.11 Absolute maximum (electrical sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples, the size of which is related to the number of power pins on the chip (3 x (n+1) power pins).This test conforms to MIL-STD-883K Method 3015.9/ESDA/JEDEC JS-002-2018 standard.

Table 4-24 Absolute maximum ESD value

Symbol	Parameter	Condition	Type	Max (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, In accordance with MIL-STD-883K Method 3015.9	2	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 °C, In accordance with ESDA/JEDEC JS-002-2018	II	1000	

1. Based on comprehensive evaluation, not tested in production.

Static switch lock

To evaluate the locking performance, two complementary static locking tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to JEDEC78E IC latch standard.

Table 4-25 Electrical sensitivity

Symbol	Parameter	Condition	Type
LU	Static locking classes	T_A(1)= +85 °C, in accordance with JEDEC78E	II class A
		T_A(2)= +25 °C, in accordance with JEDEC78E	

1. Applicable to version F and later versions.

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2. Applicable to versions earlier than F.

4.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in **Table 4-4**. All I/O ports are CMOS and TTL compatible.

Table 4-26 I/O static characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL port	V_{SS}	-	0.8	V
V_{IH}	Input high level voltage		2	-	V_{DD}	
V_{IL}	Input low level voltage	CMOS port	V_{SS}	-	$0.35V_{DD}$	
V_{IH}	Input high level voltage		$0.65V_{DD}$	-	V_{DD}	
V_{hys}	Schmidt trigger voltage lag(1) (5)	-	0.1	-	-	V
V_{hys}	Schmidt trigger voltage lag(1) (6)	V_{DD} = 3.3V/2.5V	0.2	-	-	V
		V_{DD} = 1.8V	$0.1V_{DD}$	-	-	
I_{lkg}	Input leakage current(2)	V_{DD} = Maximum V_{PAD} = 0 or V_{PAD} = V_{DD}	-1	-	+1	μA
$I_{lkg,fail\text{-}safe}$	Input leakage current(3)	V_{DD} = 0, V_{PAD} = 3.63V or V_{DD} < V_{PAD}	-1	-	+1	μA
R_{PU}	Weak pull-up equivalent resistance(4)	V_{DD} = 3.3V, V_{IN} = V_{SS}	90	-	170(190(7))	KΩ
		V_{DD} = 2.5V, V_{IN} = V_{SS}	95	-	310	
		V_{DD} = 1.8V, V_{IN} = V_{SS}	135	-	500	
R_{PD}	Weak pull-down equivalent resistance(4)	V_{DD} = 3.3V, V_{IN} = V_{DD}	75(90(7))	-	235(200(7))	KΩ
		V_{DD} = 2.5V, V_{IN} = V_{DD}	85	-	315	
		V_{DD} = 1.8V, V_{IN} = V_{DD}	120	-	495	
C_{IO}	Capacitance of I/O pins	-	-	5	-	pF

1. The hysteresis voltage of Schmitt trigger switching level. Based on comprehensive evaluation, not tested in production.
2. The leakage current may be higher than the maximum if there is reverse current in adjacent pins.
3. GPIO that does not support Fail-safe include PD14, PD15, PA11, PA12, PA4, and PB2
4. Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.
5. Applicable to version F and later versions.
6. Applicable to versions earlier than F.
7. Applicable to version F and later versions.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

- For V_{IH}:

  If V_{DD} is between [1.8V ~ 3.08V]; Uses CMOS feature but includes TTL.

  If V_{DD} is between [3.08V ~ 3.60V]; Uses TTL feature but includes CMOS.

- For V_{IL}:

  If V_{DD} is between [1.8V ~ 2.28V]; Uses TTL feature but includes CMOS.

  If V_{DD} is between [2.28V ~ 3.60V]; Uses CMOS feature but includes TTL.

Output drive current

GPIO (universal input/output port) can absorb or output up to +/-12mA current. In the user application, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings given in Section 4.2.

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Output voltage

Unless otherwise specified, the parameters listed in **Table 4-28** were measured using ambient temperature and V_{DD} supply voltage in accordance with **Table 4-4**. All I/O ports are CMOS and TTL compatible

Table 4-27 IO Output drive capability characteristics

Drive class	I_{OH}(1) V_{DD}=3.3V	I_{OL}(1) V_{DD}=3.3V	I_{OH}(1) V_{DD}=2.5V	I_{OL}(1) V_{DD}=2.5V	I_{OH}(1) V_{DD}=1.8V	I_{OL}(1) V_{DD}=1.8V	Unit
2	-2	2	-1.5	1.5	-1.2	1.2	mA
4	-4	4	-3	3	-2.5	2.5	mA
8	-8	8	-7	7	-5	5	mA
12	-12	12	-11	11	-7.5	7.5	mA

1. Guaranteed by design, not tested in production.

Table 4-28 Output voltage characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}(1)	Output low level	V_{DD} = 3.3 V, I_{OL}(3) = 2mA, 4mA, 8mA, and 12mA	V_{SS}	0.4	V
		V_{DD} = 2.5 V, I_{OL}(3) = 1.5mA, 3mA, 7mA, and 11mA	V_{SS}	0.4	
		V_{DD} = 1.8 V, I_{OL}(3) = 1.2mA, 2.5mA, 5mA, and 7.5mA	V_{SS}	0.2 * V_{DD}	
V_{OH}(2)	Output high level	V_{DD} = 3.3 V, I_{OH}(3) = -2mA, -4mA, -8mA, and -12mA	2.4	V_{DD}	
		V_{DD} = 2.5 V, I_{OH}(3) = -1.5mA, -3mA, -7mA, and -11mA	2	V_{DD}	
		V_{DD} = 1.8 V, I_{OH}(3) = -1.2mA, -2.5mA, -5mA, and -7.5mA	0.8 * V_{DD}	V_{DD}	

1. The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in **Table 4-2**, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS}.
2. The current I_{IO} output from the chip must always follow the absolute maximum rating given in **Table 4-2**, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.
3. Actual drive capability see **Table 4-27**.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in **Figure 4-9** and **Table 4-29** respectively.

Unless otherwise specified, the parameters listed in **Table 4-29** were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

Table 4-29 Input/output AC characteristics (1)

GPIOx_DS.DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
00 (2mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 5pF, V_{DD} = 3.3V	-	75	MHz
			C_L = 5pF, V_{DD} = 2.5V	-	50	
			C_L = 5pF, V_{DD} = 1.8V	-	30	
	$t_{(IO)out}$	Output delay (A to pad)	C_L = 5pF, V_{DD} = 3.3V	-	3.66	ns
			C_L = 5pF, V_{DD} = 2.5V	-	4.72	
			C_L = 5pF, V_{DD} = 1.8V	-	7.12	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50fF, V_{DD} = 2.97V, V_{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	1.2	ns
10 (4mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 10pF, V_{DD} = 3.3V	-	90	MHz
			C_L = 10pF, V_{DD} = 2.5V		60	
			C_L = 10pF, V_{DD} = 1.8V		40	
	$t_{(IO)out}$	The output delay	C_L = 10pF, V_{DD} = 3.3V	-	3.5	ns
			C_L = 10pF, V_{DD} = 2.5V		4.5	

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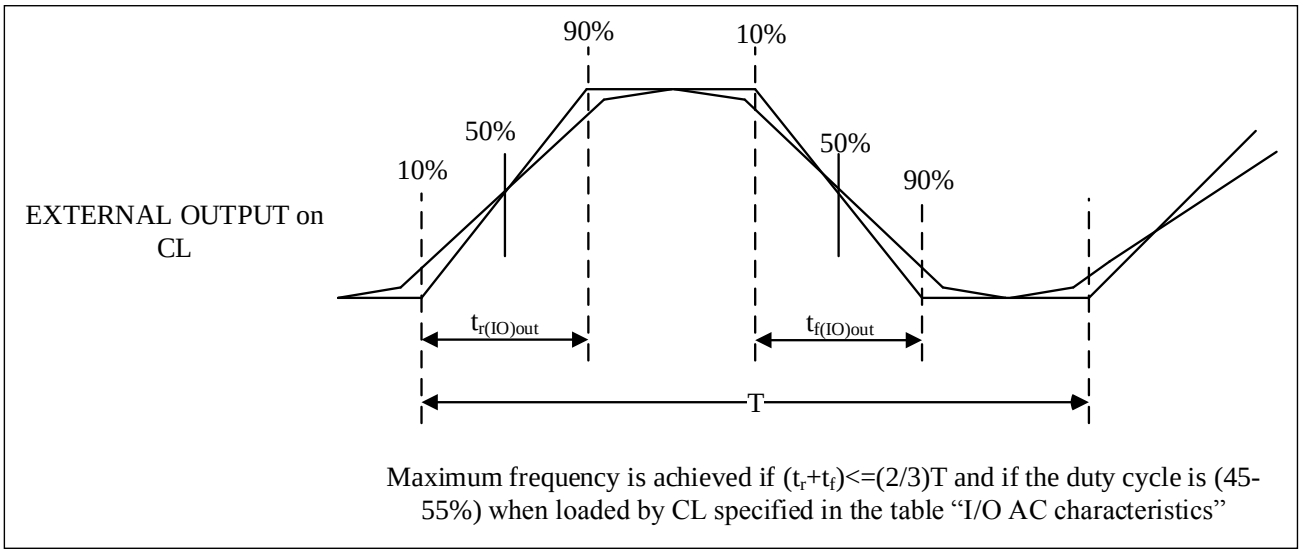
GPIOx_DS.DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
		(A to pad)	C_L = 10pF, V_{DD} = 1.8V		6.74	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50fF, V_{DD} = 2.97V, V_{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	1.2	
01 (8mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 20pF, V_{DD} = 3.3V	-	75	MHz
			C_L = 20pF, V_{DD} = 2.5V		50	
			C_L = 20pF, V_{DD} = 1.8V		30	
	$t_{(IO)out}$	The output delay (A to pad)	C_L = 20pF, V_{DD} = 3.3V	-	3.42	ns
			C_L = 20pF, V_{DD} = 2.5V		4.73	
			C_L = 20pF, V_{DD} = 1.8V		6.53	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50fF, V_{DD} = 2.97V, V_{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	1.2	
11 (12mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30pF, V_{DD} = 3.3V	-	75	MHz
			C_L = 30pF, V_{DD} = 2.5V	-	50	
			C_L = 30pF, V_{DD} = 1.8V	-	30	
	$t_{(IO)out}$	The output delay (A to pad)	C_L = 30pF, V_{DD} = 3.3V	-	3.34	ns
			C_L = 3pF, V_{DD} = 2.5V	-	4.26	
			C_L = 3pF, V_{DD} = 1.8V	-	6.34	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50fF, V_{DD} = 2.97V, V_{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	1.2	

1. The speed of the I/O port can be configured via GPIOx_DS.DSy[1:0]. Refer to the N32G435 user manual for instructions on configuring registers for GPIO ports.
2. The maximum frequency is defined in **Figure 4-9**.

Figure 4-9 Definition of input/output AC characteristics



4.3.13 NRST pin characteristics

The NRST pin input driver uses the CMOS process, which is connected to an unbreakable pull-up resistor, R_{PU} (see **Table 4-26**). Unless otherwise specified, the parameters listed in **Table 4-30** were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

Table 4-30 NRST pin characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	V_{DD} = 3.3 V	Vss	-	0.8	V
		V_{DD} = 1.8 V	Vss	-	0.3*VDD	

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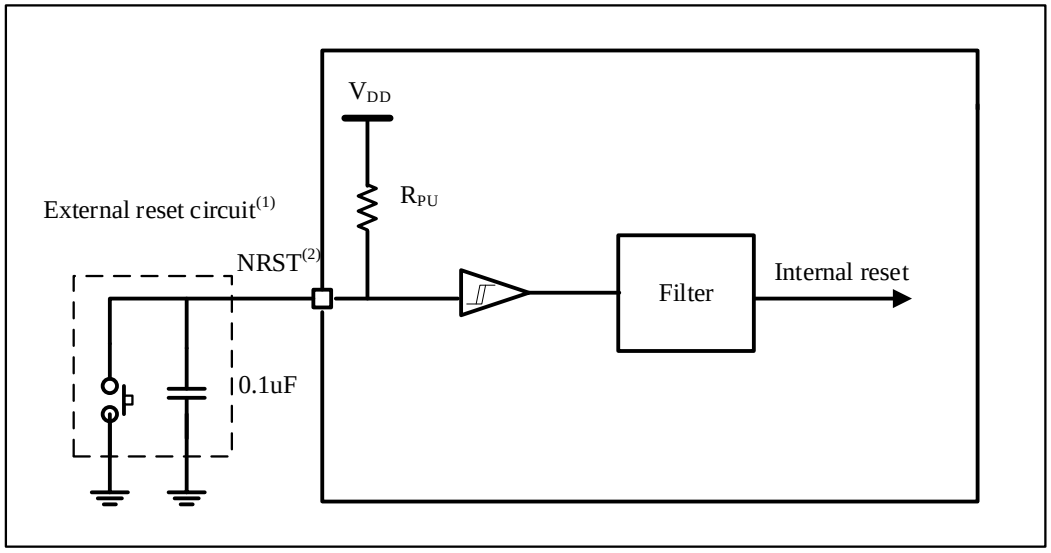
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IH(NRST)}$(1)	NRST input high level voltage	V_{DD} = 3.3 V	2	-	VDD	
		V_{DD} = 1.8 V	0.7*VDD	-	VDD	
$V_{hys(NRST)}$	NRST Schmidt trigger voltage hysteresis	V_{DD} = 3.3 V	200	-	-	mV
		V_{DD} = 1.8 V	0.1*VDD	-	-	V
R_{PU}	Weak pull-up equivalent resistance(2)	V_{DD} = 3.3 V	30	50	70	KΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is designed as a real resistor in series for a switchable PMOS implementation. The resistance of this PMON/NMOS switch is very small (about 10%).

Figure 4-10 Recommended NRST pin protection



1. Resetting the network is to prevent parasitic resets.
2. The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in **Table 4-30**, otherwise the MCU cannot be reset.

4.3.14 Timer and watchdog characteristics

The parameters listed in **Table 4-31**, **Table 4-32** and **Table 4-33** are guaranteed by design.

See section 1 for details on the features of the I/O reuse function pins (output comparison, input capture, external clock, PWM output).

Table 4-31 TIM1/8 characteristics

Symbol	Parameter	Condition	Min	Typ	Unit
$t_{res(TIM)}$	Timer time resolution	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 108MHz	9.259	-	ns
f_{EXT}	Timer CH1 to CH2 external clock frequency	-	0	f_{TIMCLK}/2	MHz
		f_{TIMCLK} = 108MHz	0	54	MHz
Res_{TIM}	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	t_{TIMCLK}
		f_{TIMCLK} = 108MHz	0.009259	606.814815	μs

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Symbol	Parameter	Condition	Min	Typ	Unit
t_{MAX_COUNT}	Maximum count	-	-	65536x65536	t_{TIMCLK}
		f_{TIMCLK} = 108MHz	-	39.768	s

Table 4-32 TIM2/3/4/5/6/7/9 characteristics

Symbol	Parameter	Condition	Min	Typ	Unit
$t_{res(TIM)}$	Timer time resolution	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 54MHz	18.519	-	ns
f_{EXT}	Timer CH1 to CH2 External clock frequency	-	0	$f_{TIMCLK}/2$	MHz
		f_{TIMCLK} = 54MHz	0	27	MHz
Res_{TIM}	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	t_{TIMCLK}
		f_{TIMCLK} = 54MHz	0.0185185	1213.62963	µs
t_{MAX_COUNT}	Maximum count	-	-	65536x65536	t_{TIMCLK}
		f_{TIMCLK} = 54MHz	-	79.536	s

Table 4-33 LPTIMER characteristics

Symbol	Parameter	Condition	Min	Typ	Unit
$t_{res(LPTIM)}$	Timer time resolution	-	1	-	$t_{LPTIMCLK}$
		$f_{LPTIMCLK}$ = 27MHz	37.037	-	ns
f_{EXT}	IN2 to OUT external clock frequency	-	0	27	MHz
		$f_{LPTIMCLK}$ = 27MHz	0	27	MHz
Res_{LPTIM}	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{LPTIMCLK}$
		$f_{LPTIMCLK}$ = 27MHz	0.037037	2427.25926	µs
t_{MAX_COUNT}	Maximum count	-	-	65536x65536	$t_{LPTIMCLK}$
		$f_{LPTIMCLK}$ = 27MHz	-	159.073	s

Table 4-34 IWDG counting maximum and minimum reset time (LSI = 40kHz)

Prescaler	IWDG_PREDIV.PD[2:0]	Min(1)IWDG_RELV.REL[11:0] = 0	Max(1)IWDG_RELV.REL[11:0] = 0xFFF	Unit
/4	000	0.1	409.6	ms
/8	001	0.2	819.2	
/16	010	0.4	1638.4	
/32	011	0.8	3276.8	
/64	100	1.6	6553.6	
/128	101	3.2	13107.2	
/256	11x	6.4	26214.4	

1. Guaranteed by design, not tested in production.

Table 4-35 WWDG counting maximum and minimum reset time (APB1 PCLK1 = 27MHz)

Prescaler	WWDG_CFG.TIMERB[2:0]	Min(1)WWDG_CFG.W[13:0] = 0x3F	Max(1)WWDG_CFG.W[13:0] = 0x3FFF	Unit

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/1	00	0.152	9.71	ms
/2	01	0.303	19.42	
/3	10	0.607	38.84	
/4	11	1.214	77.67	

1. Guaranteed by design, not tested in production.

4.3.15 I²C Interface characteristics

Unless otherwise specified, the parameters listed in **Table 4-36** were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with **Table 4-4**.

The I²C interface of the N32G435 product conforms to the standard I²C communication protocol, but has the following limitations: SDA and SCL are not "true" open leak pins, and when configured for open leak output, the PMOS tube between the pin and V_{DD} is closed, but still exists.

I²C interface features are listed in **Table 4-36**. See Section 1 for details about the features of the input/output alternate function pins (SDA and SCL).

Table 4-36 I²C interface characteristics

Symbol	Parameter	Standard model (1) (2)		Fast mode (1) (2)		Fast + mode (1) (2)		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	µs
$t_{su(STA)}$	Repeat start condition setup time	4.7	-	0.6	-	0.26	-	µs
$t_{h(SDA)}$	SDA data hold time	-	3.4	-	0.9	-	0.4	µs
$t_{su(SDA)}$	SDA setup time	250.0	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20+0.1Cb	300	-	120	ns
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	0.26	-	µs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.5	-	µs
Cb	Capacitive load per bus	-	400	-	400	-	100	pf
$t_{v(SDA)}$	Data validity time	-	3.45	-	0.9	-	0.45	µs
$t_{v\ (ACK)}$	Response time	-	3.45	-	0.9	-	0.45	µs

1. Guaranteed by design, not tested in production.
2. To achieve the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 4MHz.

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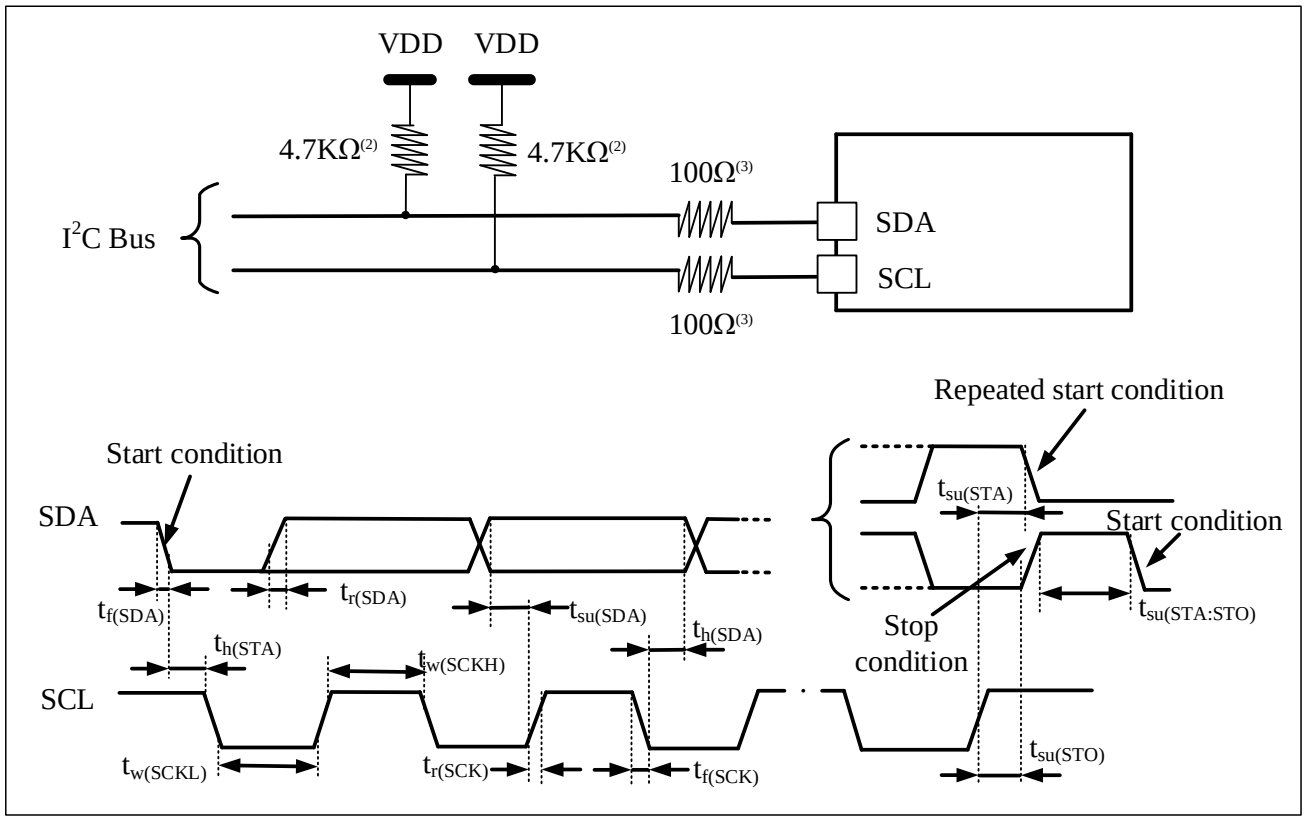
Figure 4-11 I²C bus AC waveform and measuring circuit (1)



1. The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.
2. The pull-up resistance depends on the I2C interface speed.
3. The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.16 SPI/I²S interface characteristics

Unless otherwise specified, the SPI parameters listed in **Table 4-37** and the I²S parameters listed in **Table 4-38** are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with **Table 4-4**.

See section 1 for details on the characteristics of the I/O reuse pins (NSS, SCLK, MOSI, MISO for SPI, WS, CLK, SD for I²S).

Table 4-37 SPI characteristics (1)

Symbol	Parameter	Condition		Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode		-	27	MHz
		Slave mode		-	27	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		-	8	ns
DuCy(SCK)	SPI from the input clock duty cycle	SPI from the pattern		45	55	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode		t_{PCLK}	t_{PCLK} + 2	ns
$t_{su(MI)}$(1)	Data entry setup time	Master mode	SPI1	6.2	-	ns
			SPI2	5	-	

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Symbol	Parameter	Condition		Min	Max	Unit
$t_{su(SI)}$(1)		Slave mode	SPI1	6.3	-	
			SPI2	3	-	
$t_{h(MI)}$(1)	Data entry hold time	Master mode		5	-	ns
$t_{h(SI)}$(1)		Slave mode		5.2	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 20MHz		0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Disable time of data output	Slave mode		2	10	ns
$t_{v(SO)}$(1)	Valid time of data output	Slave mode (after enable edge)	SPI1	-	20	ns
			SPI2	-	17	
$t_{v(MO)}$(1)		Master mode (after enabling edge)	SPI1	-	5	
			SPI2	-	4	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)		6.2	-	ns
$t_{h(MO)}$(1)		Master mode (after enabling edge)		- 1	-	

1. Guaranteed by design, not tested in production.
2. The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.
3. The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

Figure 4-12 SPI timing diagram-slave mode and CPHA=0

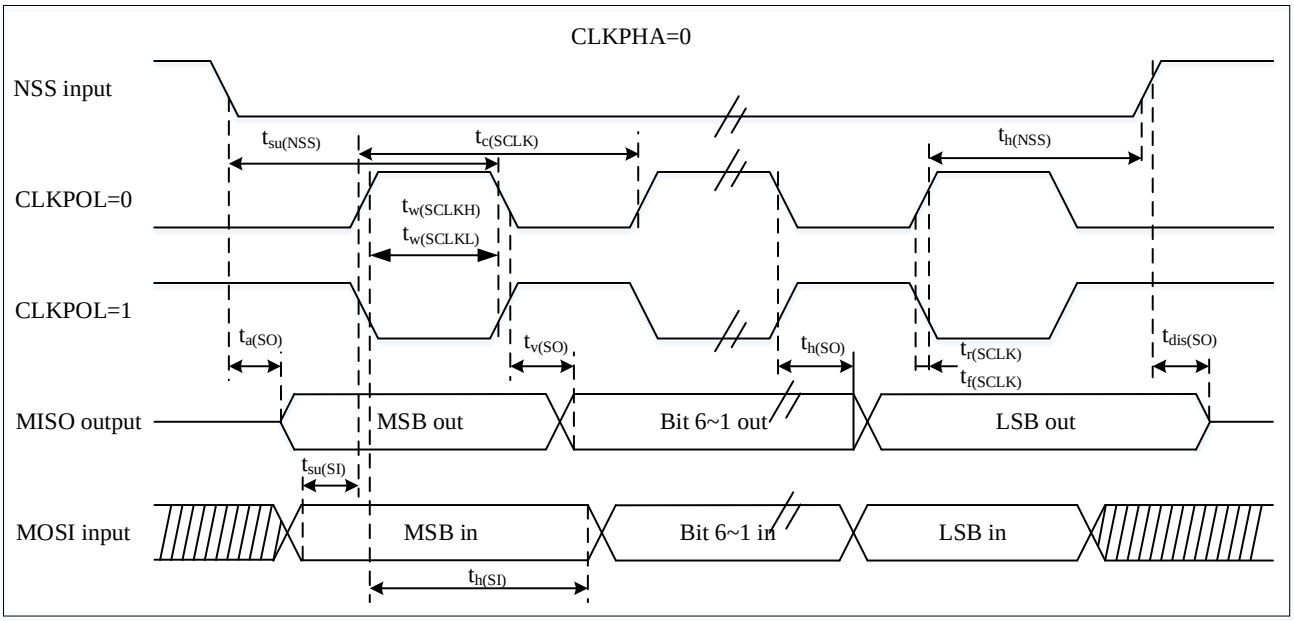

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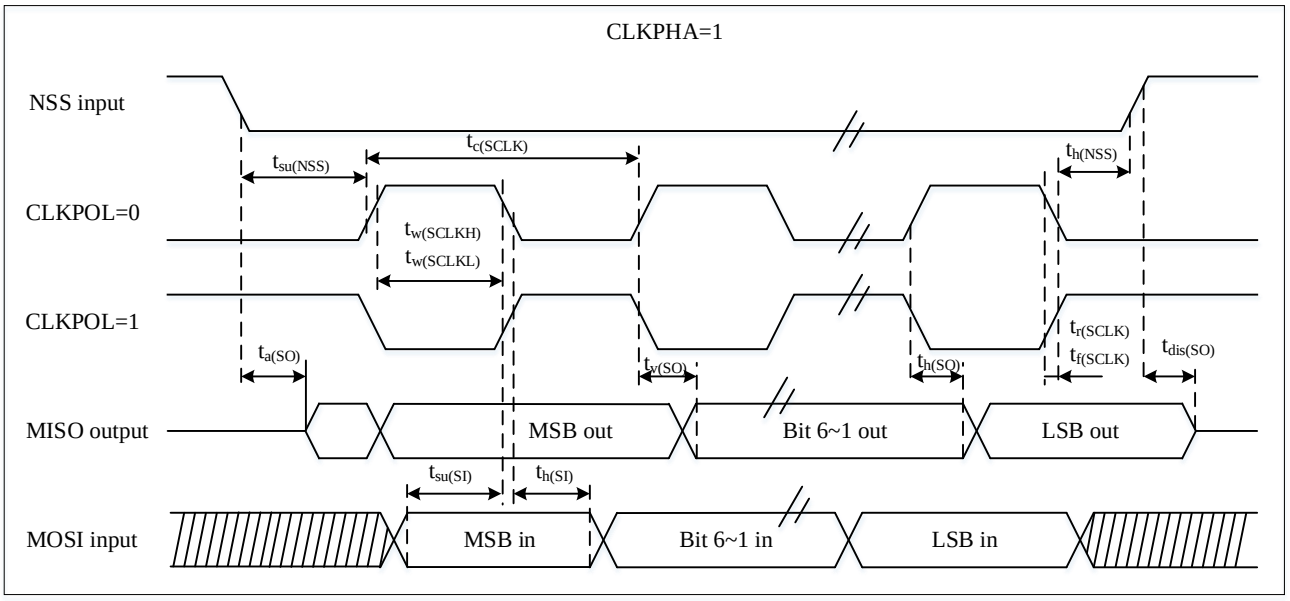
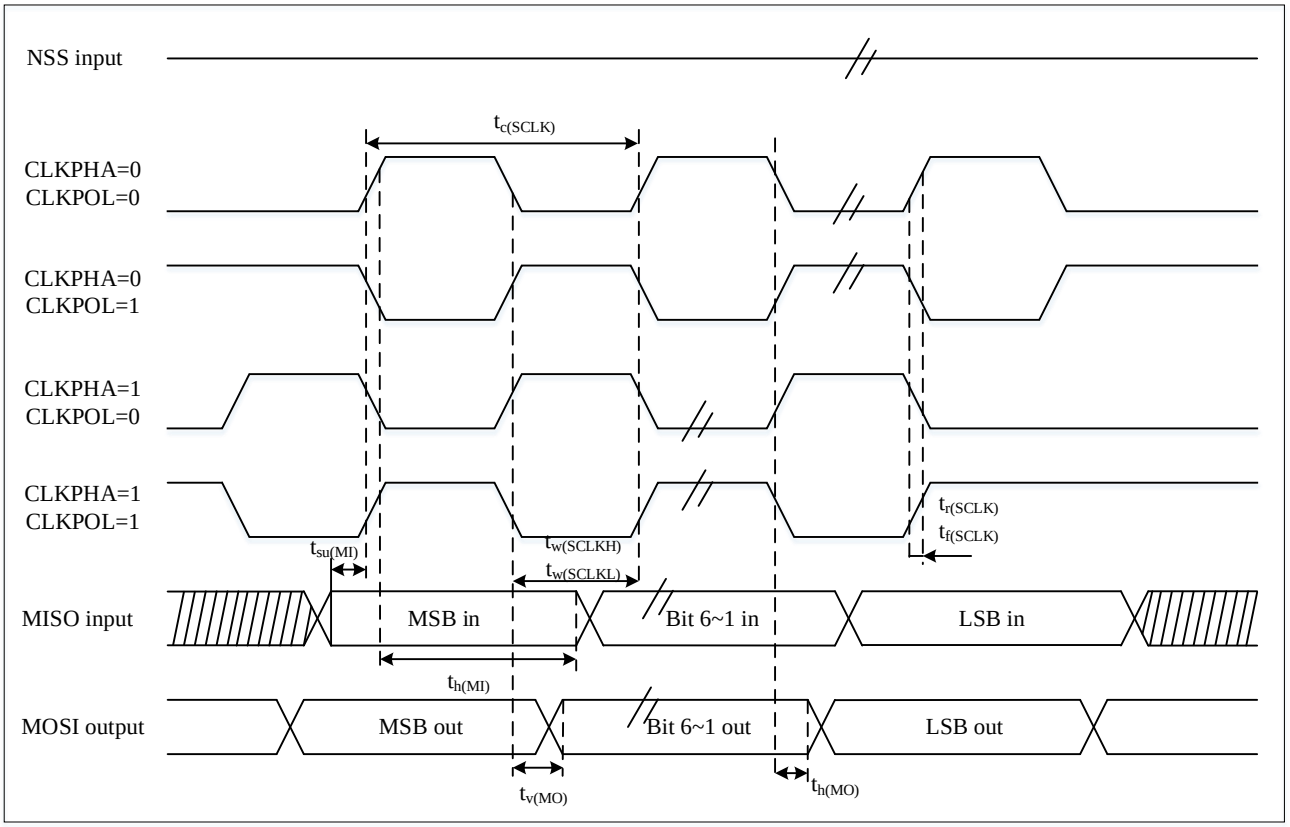
Figure 4-13 SPI timing diagram-slave mode and CPHA=1 (1)



1. The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 4-14 SPI timing diagram-master mode (1)



1. The measuring point is set at the CMOS level: 0.3V and $0.7V_{DD}$.

Table 4-38 I^2S characteristics (1)

Symbol	Parameter	Condition	Min	Max	Unit
DuCy(SCK)	I^2S clock duty cycle	I2S Slave mode	30	70	%

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Symbol	Parameter	Condition		Min	Max	Unit
f_{CLK} $1/t_{c(CLK)}$	I^2S clock frequency	Master mode (32 bit)		-	64*Fs(3)	MHz
		Slave mode (32 bit)		-	64*Fs(3)	
$t_{r(CLK)}$	I^2S clock rise and fall time	Load capacitance: CL = 50pF		-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	I2S1	5.3	-	
			I2S2	5	-	
$t_{h(WS)}$(1)	WS hold time	Master mode		0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I2S1	5.5	-	
			I2S2	5	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	I2S1	7	-	
			I2S2	3.6	-	
$t_{w(CLKH)}$(1)	CLK high and low times	Master mode, f_{PCLK} = 16MHz, audio 48kHz		312.5	-	
$t_{w(CLKL)}$(1)				345	-	
$t_{su(SD\_MR)}$(1)	Data entry setup time	The main receiver	I2S1	6.5	-	
			I2S2	5	-	
$t_{su(SD\_SR)}$(1)		Slave mode	I2S1	2.5	-	
			I2S2	2.5	-	
$t_{h(SD\_MR)}$(1)(2)	Data entry hold time	Master receiver	I2S1	4.4	-	
			I2S2	5.2	-	
$t_{h(SD\_SR)}$(1)(2)		Slave mode	I2S1	4.5	-	
			I2S2	5.2	-	
$t_{v(SD\_ST)}$(1)(2)	Valid time of data output	Slave transmitter (after the enabled edge)	I2S1	-	22	
			I2S2	-	22	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave generator (after enable edge)	I2S1	4	-	
			I2S2	4	-	
$t_{v(SD\_MT)}$(1)(2)	Valid time of data output	Master generator (after enabling edge)	I2S1	-	5.6	
			I2S2	-	4.5	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master generator (after enabling edge)		0.5	-	

1. Guaranteed by design, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK}=16MHz, then T_{PCLK}=1/f_{PCLK} =125ns.
3. Audio signal sampling frequency.

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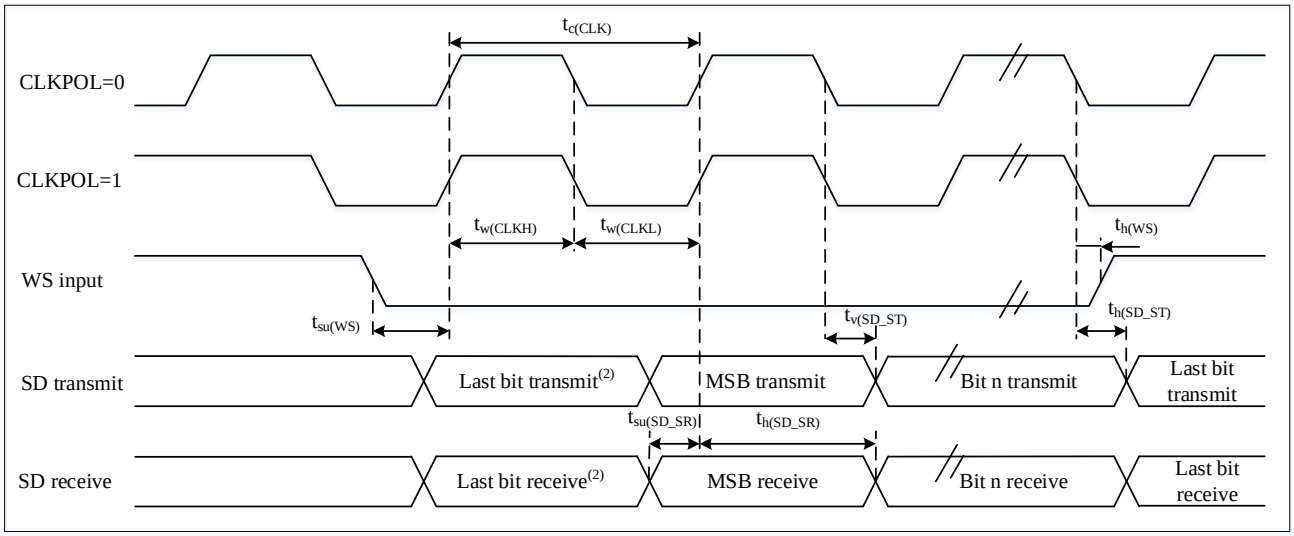
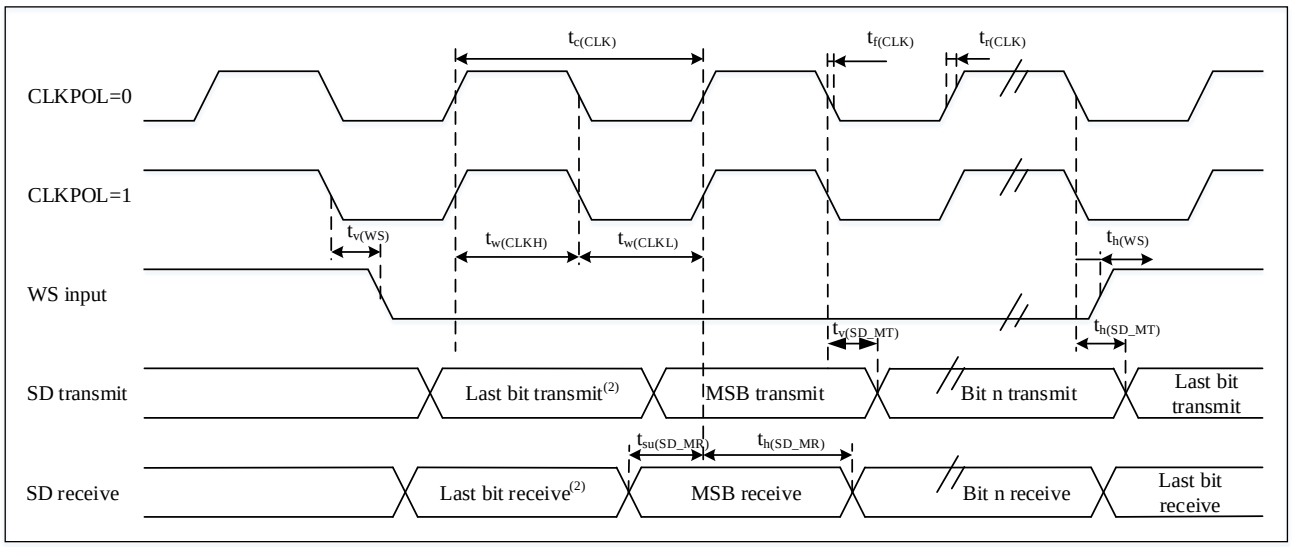
Figure 4-15 I²S slave mode timing diagram (Philips Protocol) (1)



1. The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Send/receive of the last byte.There is no least significant send/receive before the first byte.

Figure 4-16 I²S master mode timing diagram (Philips protocol) (1)



1. The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Send/receive of the last byte.There is no least significant send/receive before the first byte.

4.3.17 USB characteristics

USB (full speed) interface is certified by the USB-IF.

Table 4-39 USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	μs

1. Guaranteed by design, not tested in production.

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Table 4-40 USB DC characteristics

Symbol	Parameter	Condition	Min (1)	Max (1)	Unit
Input level					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I (USBDP and USBDM)	0.2	-	V
V_{CM}(4)	Differential common model range	Contains VDI ranges	0.8	2.5	
V_{SE}(4)	Single-end receiver threshold		1.3	2.0	
Output level					
V_{OL}	Static output low level	1.5KΩ RL is connected to 3.6V(5)	-	0.3	V
V_{OH}	Static output high level	15KΩ RL is connected to V_{SS}(5)	2.8	3.6	

1. All voltage measurements are based on the ground cable at the device end.
2. USB operating voltage is 3.0~3.6V in order to be compatible with USB2.0 full speed electrical specification.
3. The correct USB function of the N32G435 series products can be guaranteed at 2.7V, instead of dropping the electrical characteristics in the 2.7-3.0V voltage range.
4. Based on comprehensive evaluation, not tested in production.
5. R_L is the load attached to the USB drive.

Figure 4-17 USB timing: definition of rise and fall time of data signal

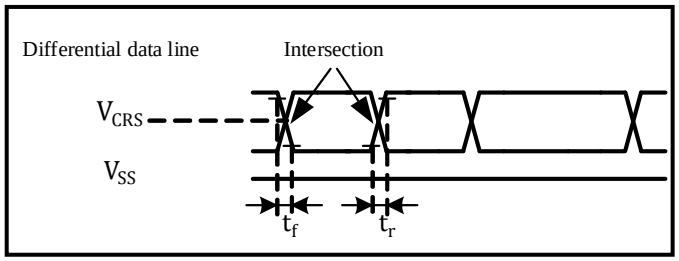

Table 4-41 Full speed of USB electrical characteristics

Symbol	Parameter	Condition	Min (1)	Max (1)	Unit
t_r	Rise time(2)	$C_L \leq 50pF$	4	20	ns
t_f	Fall time(2)	$C_L \leq 50pF$	4	20	ns
t_{rfm}	Rise and fall times match	t_r / t_f	90	111.1	%

1. Guaranteed by design, not tested in production.
2. Measured data signal from 10% to 90%.For more details, see Chapter 7 (version 2.0) of the USB specification.

4.3.18 Controller area network (CAN) interface characteristics

See Section 1 for details on the features of the input/output alternate function pins (CAN_TX and CAN_RX).

4.3.19 Electrical parameters of 12 bit analog-to-digital converter (ADC)

Unless otherwise specified, the parameters in **Table 4-42** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Note: It is recommended to perform a calibration at each power-on.

Table 4-42 ADC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	The power supply voltage	Use an external reference voltage	1.8	-	3.6	V

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Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	-	-	72	MHz
f_s(1)	Sampling rate	Resolution 12-bit	0.01	-	5.14	MHz
		Resolution 10-bit	0.012	-	6	MHz
		Resolution 8-bit	0.014	-	7.2	MHz
		Resolution 6-bit	0.0175	-	9	MHz
V_{AIN}	Switching voltage range(2)	-	0 (V_{SSA} or V_{REF-} Connect to ground)	-	V_{REF+}	V
R_{ADC}(1)	Sampling switch resistance	Fast channel	-		0.2	KΩ
R_{ADC}(1)	Sampling switch resistance	Slow channel	-		0.5	KΩ
C_{ADC}(1)	Internal sampling and holding capacitors	-	-	5		pF
SNDR	Singal noise distortion ration	-	-	65		dBFS
T_{cal}	The calibration time	-	82			$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 72 MHz(fast channel)	0.0208		8.35	µs
		f_{ADC} = 72 MHz(slow channel)	0.0625		8.35	
Ts(1)	Sampling cycles	Fast track	1.5	-	601.5	$1/f_{ADC}$
		The slow channel	4.5	-	601.5	
t_{STAB}(1)	Power on time	-	6	10	20	µs
t_{CONV}(1)(3)	Total conversion time (including sampling time)	-	8~614 (Sampling T_S + 6.5/8.5/10.5/12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. V_{REF+} connected to V_{DDA} internally, and V_{REF-} connected to V_{SSA} internally.
3. Single conversion mode has 3 more $1/f_{ADC}$ than continuous conversion mode

Formula 1: maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12(representing 12-bit resolution).

Table 4-43 ADC sampling time(1) (2)

Input	Resolution	Rin (kΩ)	Typ of minimum sampling time (ns)	Input	Resolution	Rin (kΩ)	Typ of minimum sampling time (ns)
fast channel	12-bit	0	11	slow channel	12-bit	0	19
		0.05	12			0.05	21
		0.1	14			0.1	23
		0.2	20			0.2	30

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Input	Resolution	Rin (kΩ)	Typ of minimum sampling time (ns)	Input	Resolution	Rin (kΩ)	Typ of minimum sampling time (ns)
		0.5	38			0.5	48
		1	64			1	77
		5	276			5	310
		10	543			10	607
		20	1082			20	1207
		50	2788			50	3144
		100	6162			100	8244
		0	10			0	17
		0.05	11			0.05	18
		0.1	13			0.1	20
		0.2	17			0.2	25
		0.5	32			0.5	40
fast channel	10-bit	1	54	slow channel	10-bit	1	64
		5	229			5	257
		10	448			10	499
		20	888			20	983
		50	2223			50	2457
		100	4500			100	5001
		0	9			0	14
		0.05	10			0.05	16
		0.1	11			0.1	17
		0.2	14			0.2	21
		0.5	26			0.5	33
fast channel	8-bit	1	43	slow channel	8-bit	1	52
		5	183			5	206
		10	358			10	399
		20	707			20	783
		50	1759			50	1941
		100	3523			100	3887
		0	8			0	12
		0.05	8			0.05	13
		0.1	9			0.1	14
		0.2	12			0.2	17
		0.5	20			0.5	25
fast channel	6-bit	1	33	slow channel	6-bit	1	40
		5	138			5	156
		10	269			10	300
		20	531			20	588
		50	1316			50	1451
		100	2627			100	2894

1. Guaranteed by design, not tested in production.
2. Typical values are obtained when TA=25 and VDD=3.3V.

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Table 4-44 ADC accuracy-limited test conditions (1) (2)

Symbol	Parameter	Condition	Typ	Max (3)	Unit
ET	Comprehensive error(4)	f_{HCLK} = 72MHz, f_{ADC} = 72MHz, sample Rate = 1.75m SPS, V_{DDA} = 3.3V, T_A = 25 ℃ Measurements are made after the ADC is calibrated $V_{REF+} = V_{DDA}$	±1.3	-	LSB
EO	Offset error(5)		±1	-	
ED	Differential linear error		±0.7	-	
EL	Integral linear error		±0.8	-	

1. The DC accuracy of the ADC is measured after internal calibration.
2. ADC accuracy versus reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, as this can significantly reduce the accuracy of the conversion being performed on the other analog input pin.It is recommended to add a Schottky diode (between pin and ground) to standard analog pins that may generate reverse injection current.
3. The forward injection current does not affect the ADC accuracy as long as it is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in **Table 4-2**
4. Based on comprehensive evaluation, not tested in production.
5. Guaranteed by design, not tested in production.

Figure 4-18 ADC precision characteristics

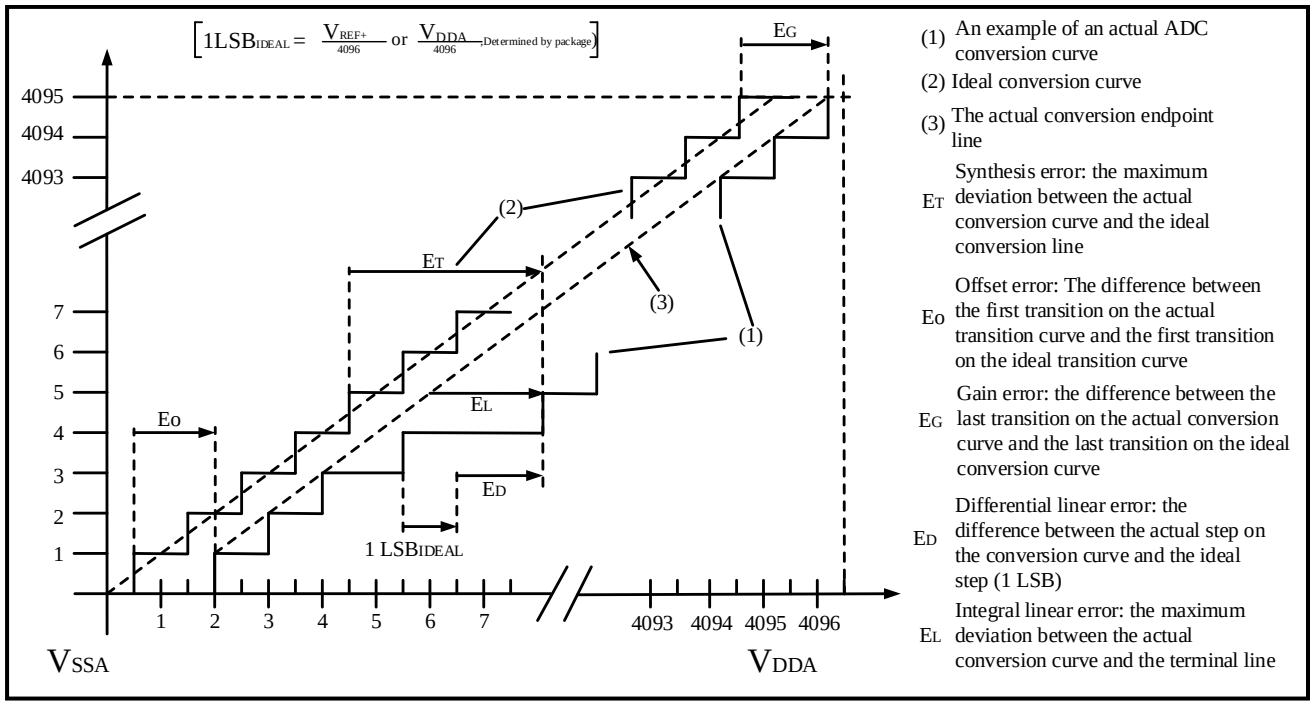

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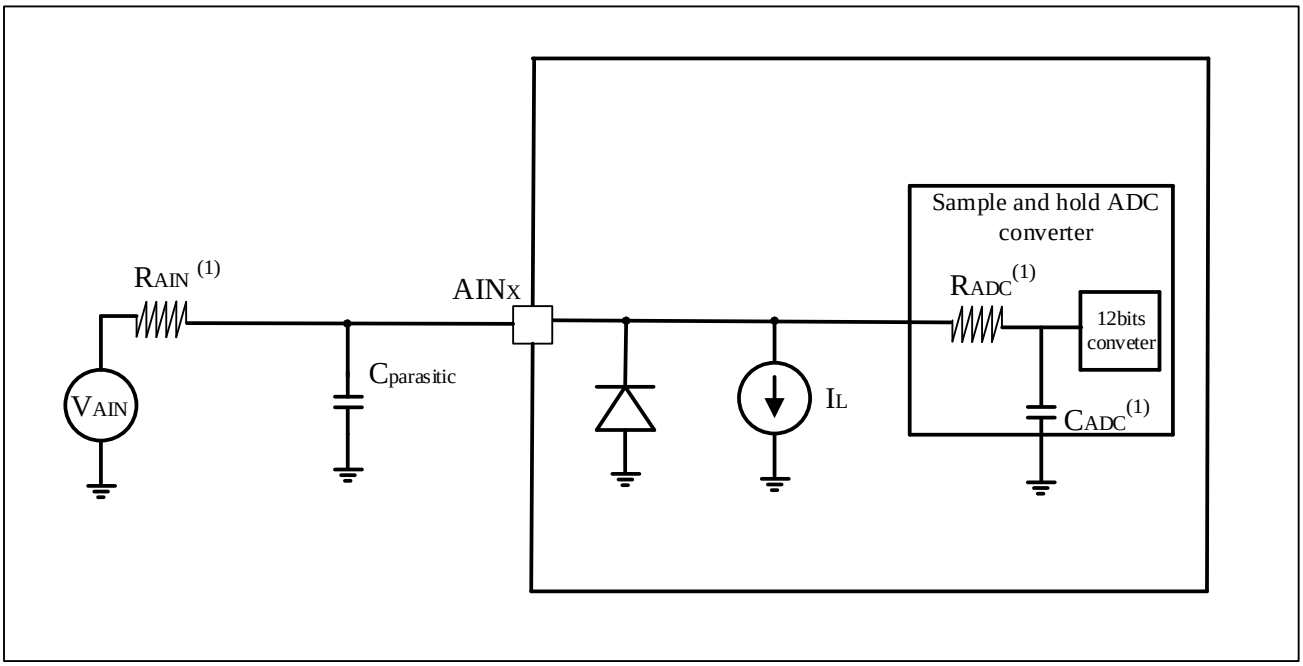
Figure 4-19 Typical connection diagram using ADC



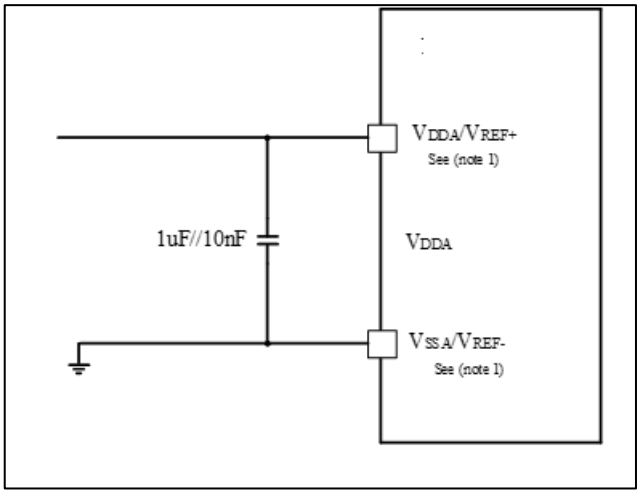
1. For values of R_{AIN}, R_{ADC}, and C_{ADC}, see **Table 4-42**.
2. Cparasitic indicates parasitic capacitance on PCB (related to welding and PCB layout quality) and pads (approximately 7pF).A larger Cparasitic value would reduce the accuracy of the conversion and the solution was to reduce f_{ADC} from medine.

Note: Input voltage less than -0.2V is prohibited on ADC channel

PCB Design Suggestions

The decoupling of the power supply must be connected in accordance with **Figure 4-20**. The 10nF capacitors in the picture must be ceramic capacitors (good quality), and they should be as close as possible to the MCU chip.

Figure 4-20 Decoupling circuit of power supply and reference power supply (V_{REF+} is connected to V_{DDA})



1. V_{REF+} and V_{REF-} are internally connected to VDDA and VSSA.

4.3.20 Internal reference source ($V_{REFBUFF}$) electrical parameters

Unless otherwise specified, the parameters in **Table 4-45** are measured using ambient temperature, f_{HCLK} frequency and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

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Table 4-45 $V_{REFBUFF}$ characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	2.4	-	3.6	V
V_{REFBUF_OUT}	Voltage reference output	Normal mode	-	2.048	-	V
I_{DDA}	V_{REFBUF} consumption from V_{DDA}	I_{load} = 0 μA	-	600	-	μA
t_{START}(1)	Start-up time	-	1	-	-	μs

1. Guaranteed by design, not tested in production.

4.3.21 12 bit DAC electrical parameters

Unless otherwise specified, the parameters of **Table 4-46** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions of **Table 4-4**.

Table 4-46 DAC characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit	Annotation
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	
V_{REF+}	The reference voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground wire	0	-	0	V	
R_L	Load resistance when the buffer is open	5	-	-	KΩ	Minimum load resistance between DAC_OUT and V_{SSA}
C_L	The load capacitance	-	-	50	pF	The maximum capacitance on the DAC_OUT pin
I_{DD}	DAC DC consumption in operating mode (V_{DDA} +V_{REF+})	-	425	600	μA	No load. The median value is 0x800
I_{DDQ}	DAC DC consumption in off mode (V_{DDA}+V_{REF+})	-	5	350	nA	No load
DAC_OUT Min	Low DAC_OUT voltage when buffer is closed	VSS+1LSB	-	-	V	The maximum DAC output span is given. When V_{REF+} = 3.6V corresponds to a 12-bit input value 0x0E0~0xF1C, When V_{REF+} = 2.4V corresponds to a 12-bit input value 0x155~0xEAB.
	Low DAC_OUT voltage when buffer is open	0.2	-	-		
DAC_OUT Max	Low DAC_OUT voltage when buffer is closed	-	-	V_{REF+} - 5LSB		
	Low DAC_OUT voltage when buffer is open	-	-	V_{REF+} - 0.2		
DNL	Differential non linearity (Difference between two consecutive code)	-	±2	-	LSB	The DAC configuration is 12 bits
INL	Integral non linearity (difference between measured value at Code I and the value at Code i on a line drawn between Code 0 and last Code 4095)	-	±7	-	LSB	The DAC configuration is 12 bits
The offset	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	±15	-	mV	The DAC configuration is 12 bits
		-	±18	-	LSB	When V_{REF+} is 3.6V, the DAC is configured as 12 bits
Gain error	Gain error	-	±0.5	-	%	The DAC is configured as 2 bits
amplifier gain	Amplifier gain in open loop	80	85	-	dB	5KΩ load (maximum load), The median value of input is 0x800
$t_{SETTLING}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input	-	5	7	μs	C_{LOAD}≤50pF R_{LOAD}≥5KΩ

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Symbol	Parameter	Min	Typ	Max	Unit	Annotation
	codes when DAC_OUT reaches final value ±1LSB)					
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	C_{LOAD}≤50pF R_{LOAD}≥5KΩ
t_{WAKEUP}	Wake up time from closed state (Set the CHxEN in the DAC control register)	-	6.5	10	μs	C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5KΩ The input code is between the minimum and maximum possible values
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	-67	-40	dB	No R_{LOAD}, C_{LOAD} ≤ 50pF

1. Guaranteed by design, not tested in production.

4.3.22 Operational amplifier (OPAMP) electrical parameters

Unless otherwise specified, the parameters in **Table 4-47** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Table 4-47 OPAMP characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common mode voltage input range	-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage (after calibration)	-	-	±1	±3.5	mV
Δ VI_{OFFSET}	Input offset voltage temperature drift	-	-	10	-	UV / ° C
I_{LOAD}	Drive current	-	-	-	0.5	mA
I_{DDA}	Operational amplifier current consumption	No load, quiescent mode	-	-	1.5	mA
TS_OPAMP_VOUT	ADC sampling time as opamp output	-	400	-	-	ns
CMMR	Common mode rejection ratio	-	-	84	-	dB
PSRR	Power rejection ratio	-	-	100	-	dB
GBW	Gain bandwidth	-	-	4	-	MHz
SR	Conversion rate	-	-	2.5	-	V/μs
RLOAD	Minimum impedance load	-	4	-	-	KΩ
CLOAD	Maximum capacitive load	-	-	-	50	pF
$t_{STARTUP}$	Start-up setup time	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ, Follower configuration	-	3	-	μs
PGA Gain error	Programmable gain error	Input signal amplitude> 100mV	-	±2.5	-	%
PGA BW	PGA bandwidth for different noninverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	2	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload =4 KΩ	-	1	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
		PGA Gain = 16, Cload = 50pF,	-	0.25	-	

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Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Rload = 4 KΩ				
		PGA Gain = 32, Cload = 50pF, Rload = 4KΩ	-	0.125	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	111	-	nV/√Hz
		@ 10KHz, Output loaded with 4 KΩ	-	44	-	

1. Guaranteed by design, not tested in production.

4.3.23 Comparator 2(COMP2) electrical parameters

Unless otherwise specified, the parameters in **Table 4-48** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Table 4-48 COMP2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	
t_{START}(1)	Comparator startup setup time	-	-	10	-	μs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	-	-	70	-	ns
V_{OFFSET}	Comparator input offset error	Full common mode range	-	±10	-	mV
V_{hys}	Comparator hysteresis	No hysteresis	-	0	-	mV
		Low hysteresis	-	10	-	
		Medium hysteresis	-	20	-	
		High hysteresis	-	30	-	
I_{DDA}	Comparator current consumption	Static	-	45	-	μA
		With 50 KHz ±100 mV Overdrive Square Signal	-	47	-	

1. Guaranteed by design, not tested in production.

4.3.24 Comparator 1(COMP1) electrical parameters

Unless otherwise specified, the parameters in **Table 4-49** and **Table 4-50** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Table 4-49 COMP1 normal mode characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	
t_{START}(1)	Comparator startup setup time	-	-	10	-	μs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	-	-	70	-	ns
V_{OFFSET}	Comparator input offset error	Full common mode range	-	±5	±20	mV
V_{hys}	Comparison hysteresis	No hysteresis	-	0	-	mV
		Low hysteresis	-	10	-	
		Medium hysteresis	-	20	-	
		High hysteresis	-	30	-	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}	Comparator current consumption	Static	-	45	-	µA
		With 50 kHz ±100 mV overdrive square signal	-	47	-	

1. Guaranteed by design, not tested in production.

Table 4-50 COMP1 low power mode characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	
t_{START}(1)	Comparator startup setup time	-	-	15	-	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	V_{DDA}>=2.7V	-	300	-	ns
V_{OFFSET}	Comparator input offset error	VDDA=3V,25°C	-	±10	-	mV
V_{hys}	Comparison hysteresis	No hysteresis	-	0	-	mV
		Low hysteresis	-	10	-	
		Medium hysteresis	-	20	-	
		High hysteresis	-	30	-	
I_{DDA}	Comparator current consumption	Static	-	10	-	µA
		With 50 kHz ±100 mV overdrive square signal	-	11.5	-	

1. Guaranteed by design, not tested in production.

4.3.25 Temperature sensor (TS) characteristics

Unless otherwise specified, the parameters in **Table 4-51** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Table 4-51 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±4	ºC
Avg_Slope(1)	Average slope	-	-4.0	-	mV/ºC
V_{25}(1)	Voltage at 25ºC	-	1.32	-	V
t_{START}(1)	Startup time	-	10	20	µs
T_{S_temp}(2)(3)	ADC sampling time when reading the tempearture	8.3	-	-	µs

1. Based on comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

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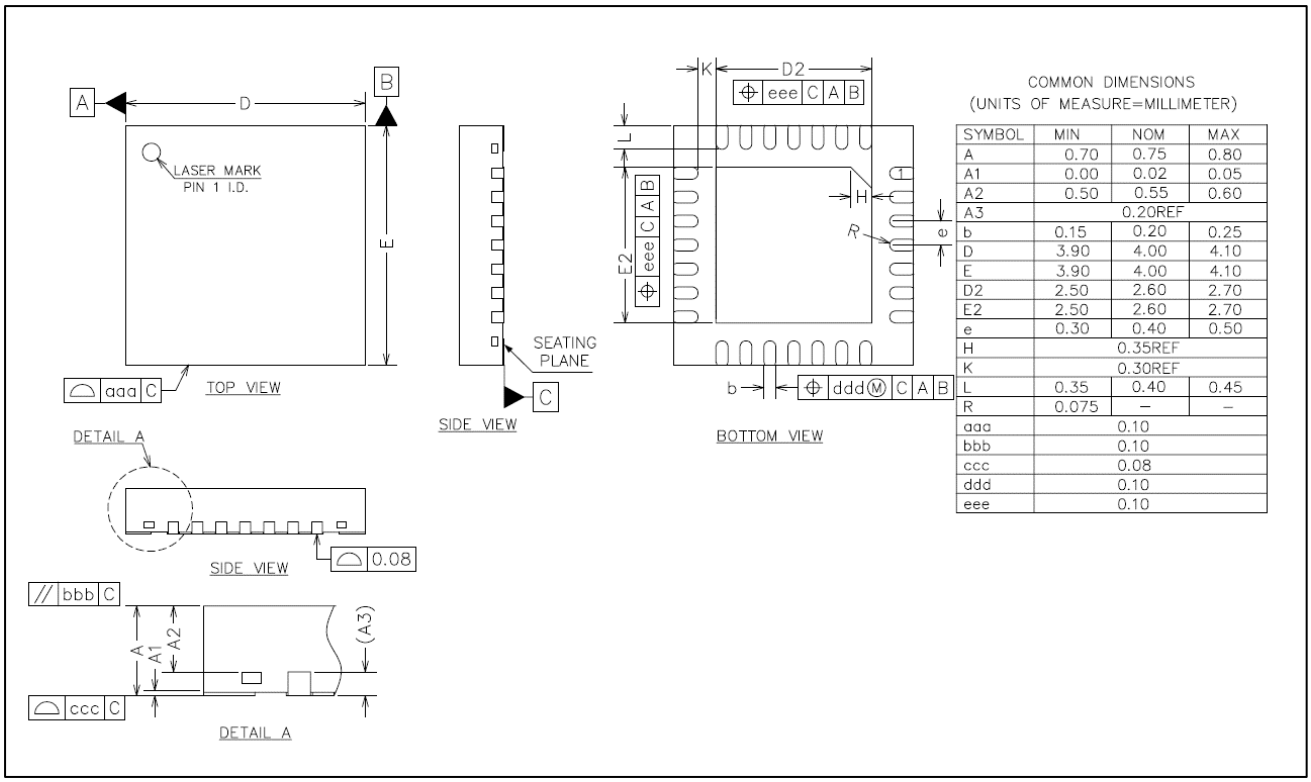
5 Package information

5.1 QFN28 (4mm×4mm)

Figure 5-1 QFN28(4mmx4mm) package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.30	0.40	0.50
H		0.35REF	
K		0.30REF	
L	0.35	0.40	0.45
R	0.075	–	–
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

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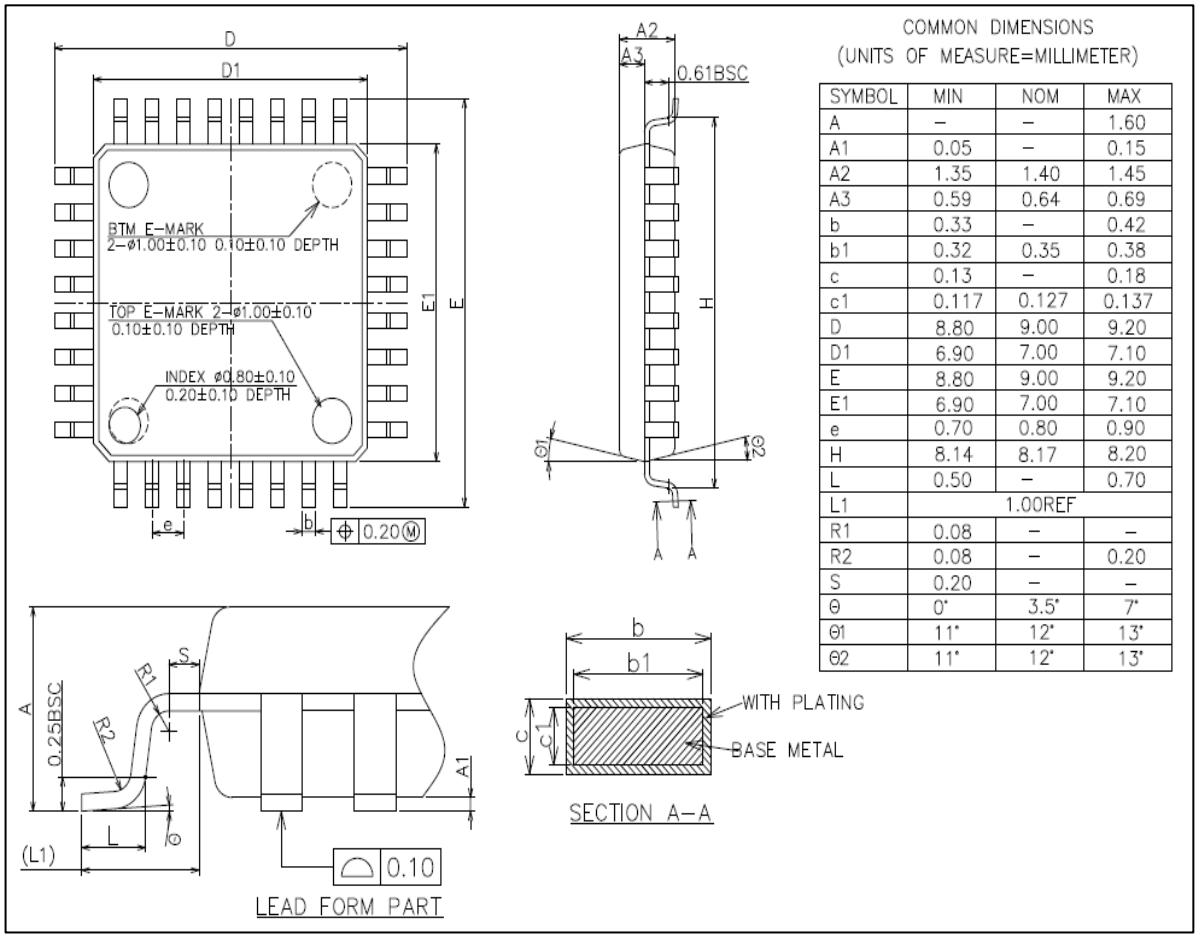
5.2 LQFP32 (7mm×7mm)

Figure 5-2 LQFP32(7mmx7mm) package outline



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	–	0.42
b1	0.32	0.35	0.38
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

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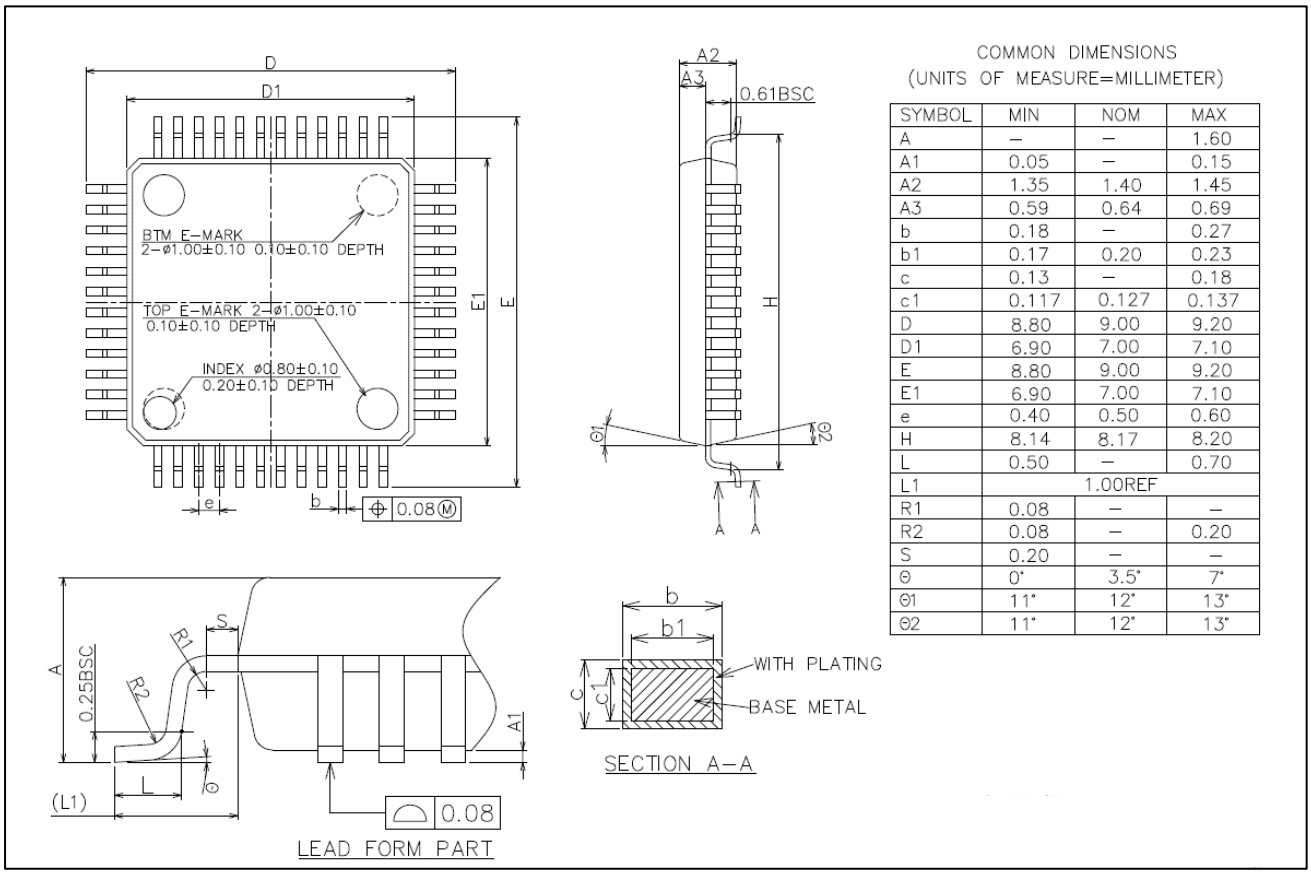
5.3 LQFP48 (7mm×7mm)

Figure 5-3 LQFP48(7mmx7mm) package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

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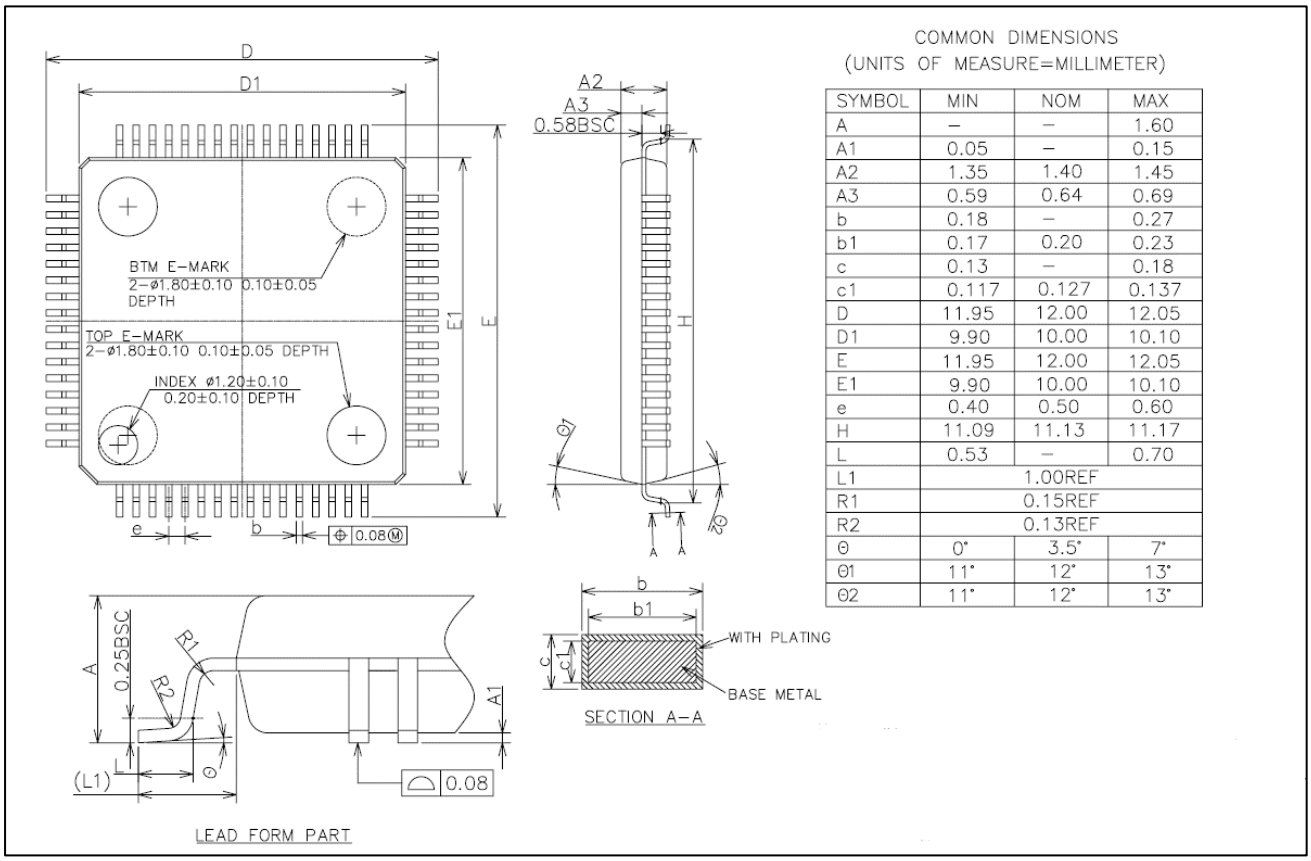
5.4 LQFP64 (10mm×10mm)

Figure 5-4 LQFP64 (10mm×10mm) package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

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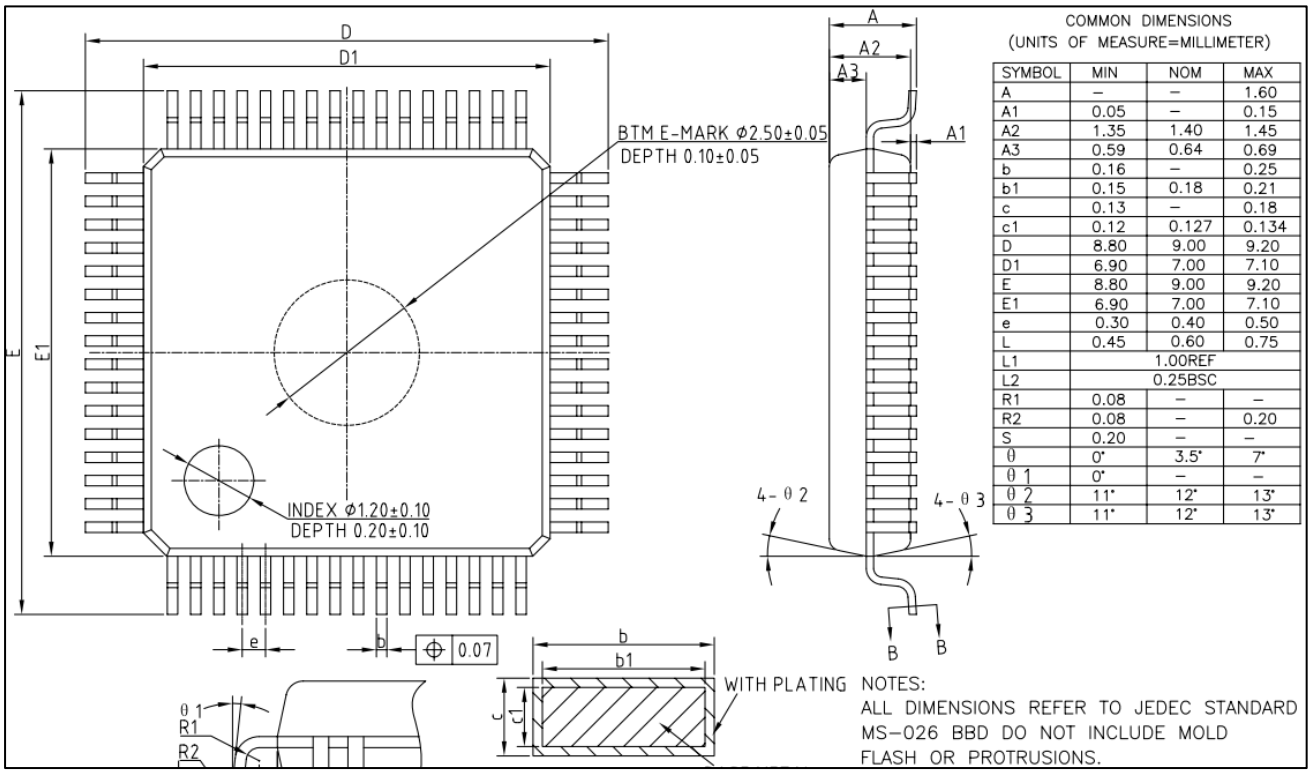
5.5 LQFP64 (7mm×7mm)

Figure 5-5 LQFP64(7mm×7mm) package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	–	0.25
b1	0.15	0.18	0.21
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.30	0.40	0.50
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

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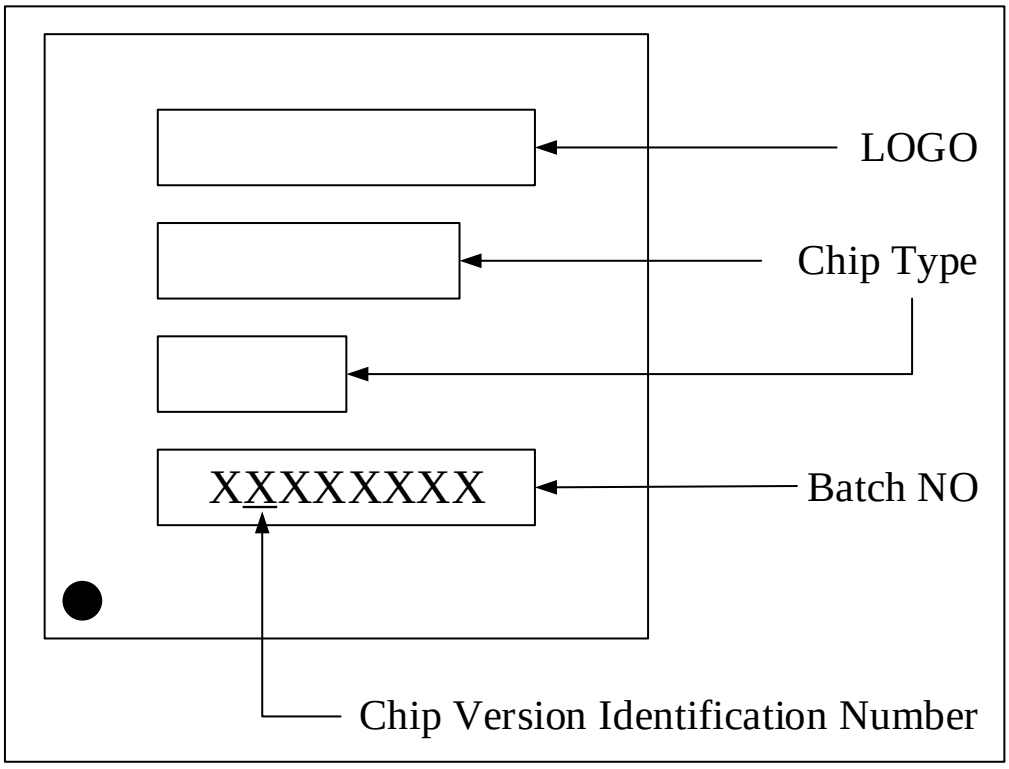
5.6 Marking information

Figure 5-6 Marking information



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6 Version history

Date	Version	Remark
2020/7/29	V0.6	Initial version
2020/11/13	V0.8	1. Improved electrical characteristics 2. Modify the maximum speed of the SPI interface to 27Mbps. 3. Unified SPI interface speed unit is Mbps.
2021/01/25	V0.9	1. Added N32G435G8Q7 model, pin definition, package size information
2021/04/15	V1.0	1. 4.3 Chapter Data Check
2021/06/12	V1.1	1. Add model N32G435GBQ7. 2. Modify the timing diagram of I2S master mode. 3. Add PA2/PA3 COMP_INP version note. 4. Add LQFP64 (7mmx7mm) model and package size. 5. Add the introduction of LPRUN mode. 6. Modify 4.3.18 Figure 4-19 Remove the upper tube of ADC pin. 7. Modify 4.3.11 I/O port characteristics. 8. Modify 4.3.7.1 MSI Maximum. 9. Modify Figure 4-10 10. Modify Table 3 1 IO/level to IO/structure
2022/07/11	V1.2	1. Modify Table 4-18 and add Note 3 2. Modify Table 2-1 Timer function comparison 3. Added 4.3.19 ADC chapter notes 4. Deleted 3.2 Pin Alternate Definition Note 4 PC13, PC14 and PC15 pins can only sink limited current (3mA) 5. Modify Table 4-42 ADC characteristic t_{STAB} value 6. Modify Table 4-16 to remove ESR CL restrictions 7. Add NJTRST function 8. Table 4-42 t_{CONV} increase Note 3 9. Modified Figure 4-8 Typical application using 32.768kH crystal 10. Add Table 4-32, Table 4-33, Table 4-34, and Table 4-35 11. Modify Table 4-2 NRST pin injection current 12. Modify the number of shielded interrupt channels of interrupt controller 13. Revise the number of edge detectors of EXTI in Section 2.3 14. Revise the CPU frequency requirements for USB usage in Section 2.4 15. Add the description of LP-sleep mode in Section 2.10 16. Add the wake up condition of STOP2 mode in 2.10

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		17. Revise PMBus compatibility in I2C main Features in 2.14 18. Revise CRC calculation time to 1 AHB clock cycle 19. Modify the actual frequency deviation of the HSI oscillator in Note 3 of Table 4-18 20. Modify the conditions of the power supply current in Table 4-22: Read mode, fHCLK = 108MHz, three waiting periods 21. Revise GPIOx_DS.DSy[1:0] of 4/8mA in Table 4-29 22. Modify Table 4-37 SPI slave mode input clock duty cycle 23. Modify the maximum and minimum values of V_{REFINT} in Table 4-7 and delete the $V_{REFBUFFER}$ 24. Modify the minimum value of f_{HSE_ext} in Table 4-13 and add (Bypass mode) to the table name 25. Modify the maximum value of V_{LSEL} in Table 4-14 and add (Bypass mode) to the table name 26. Figure 4-5 and Figure 4-6 are modified 27. Modify the description of Table 4-15 and comments 28. Figure 4-7 Adding comment 2 29. Modify the maximum and minimum gm values in Table 4-16. Add comment 4 and comment 5 30. Modify the maximum, typical, and minimum values in Table 4-18. Add comment 4 and comment 5 31. Modify the typical and maximum values for $t_{SU(LSI)}$ and typical values for $I_{DD(LSI)}$ in Table 4-19 32. Modify the conditions listed in Table 4-24 33. Table 4-25 Added +85 °C, Added comments 1 and comment 2 34. Modify the minimum, typical, and maximum values in Table 4-26 and modify the comments for the table 35. Added Table 4-27 and table comments 36. Modified The conditions in Table 4-28, and added comment 3 37. Delete V_{CRS} listed in Table 4-41 38. Table 4-43 and added table comments 39. Added comment 5 in Table 4-44 40. Figure 4-19 is modified 41. Modify the minimum and maximum values of V_{REFBUF_OUT} in Table 4-45 42. Table 4-46 added DAC_OUT Min and DAC_OUT Max, modified the typical values for DNL, INL, and offsets, and modified the typical values and maximum values for $t_{SETTLING}$

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		43. Modify the typical value and maximum value of I_{LOAD} and typical value of SR in Table 4-47 44. Modify the minimum, typical, and maximum values of Avg_Slope in Table 4-51 45. Modify the condition and minimum value of t_{RET} in Table 4-23 46. Modify the Figure 4-16
2022/08/30	V1.3	1. Modify the description of Note 2 in Table 4-42 2. Modify the description of the output drive current and output voltage section in chapter 4.3.12 3. Add "-" to blank (no data) part of all tables in Section 4 4. Modify the description of Note 3 in Table 4-18 5. Add note 9 in chapter 3.2 6. Add note 7 in chatper 4.3.12 7. Delete OPAMP2_VINP function from PB0 in chapter 3.2 8. Modify the table of Flash endurance and data retention life in chapter 4.3.10 9. Modify Table 6-1 I2C interface characteristics 10. Modify PC8 pin serial number in table 3-1

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