

Laboratory Report #6

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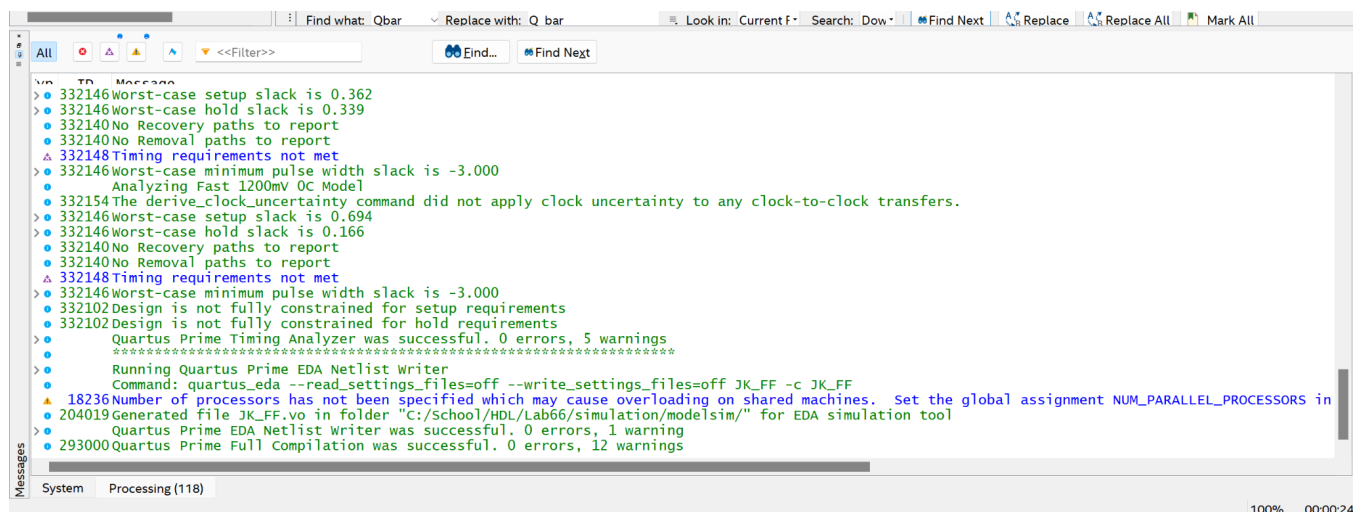
Laboratory Exercise Title: Behavioral Modeling of Sequential Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 6A:



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> 332146Worst-case setup slack is 0.362
> 332146Worst-case hold slack is 0.339
> 332140No Recovery paths to report
> 332140No Removal paths to report
> 332148Timing requirements not met
> 332146Worst-case minimum pulse width slack is -3.000
> Analyzing Fast 1200mV 0c Model
> 332154The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
> 332146Worst-case setup slack is 0.694
> 332146Worst-case hold slack is 0.166
> 332140No Recovery paths to report
> 332140No Removal paths to report
> 332148Timing requirements not met
> 332146Worst-case minimum pulse width slack is -3.000
> 332102Design is not fully constrained for setup requirements
> 332102Design is not fully constrained for hold requirements
> Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
> Running Quartus Prime EDA Netlist Writer
> Command: quartus_eda --read_settings_files=off --write_settings_files=off JK_FF -c JK_FF
> 18236Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in
> 204019generated file JK_FF.vo in folder "C:/School/HDL/Lab66/simulation/modelsim/" for EDA simulation tool
> Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
> 293000Quartus Prime Full Compilation was successful. 0 errors, 12 warnings
  
```

Figure 1. Proof of successful design synthesis

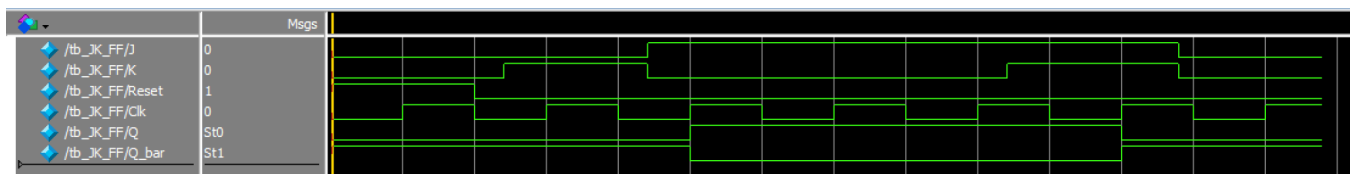


Figure 2. Proof of successful simulation results

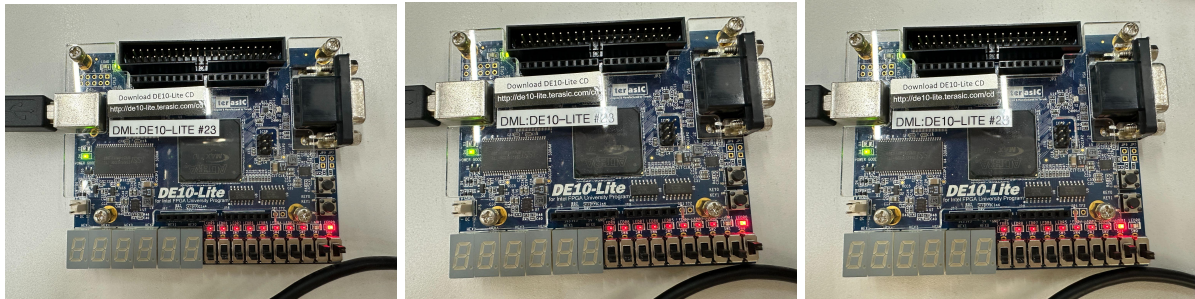


Figure 3. Proof of successful FPGA implementation

Exercise 6B:

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All Find... Find Next
Messages
332148Timing requirements not met
332146worst-case setup slack is -1.103
332146worst-case hold slack is 1.555
332140No Recovery paths to report
332140No Removal paths to report
332146worst-case minimum pulse width slack is -3.000
Analyzing Fast 1200mV OC Model
332123Deriving Clock Uncertainty. Please refer to report_sdc in the Timing Analyzer to see clock uncertainties.
332146worst-case setup slack is 0.023
332146worst-case hold slack is 0.700
332140No Recovery paths to report
332140No Removal paths to report
332148Timing requirements not met
332146worst-case minimum pulse width slack is -3.000
332102Design is not fully constrained for setup requirements
332102Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
*****
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off Counter_4bit -c Counter_4bit
18236Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in
204019Generated file counter_4bit.vo in folder "C:/School/HDL/Lab6b/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000Quartus Prime Full compilation was successful. 0 errors, 17 warnings
System Processing (124) 100% 00:00:2
  
```

Figure 1. Proof of successful design synthesis

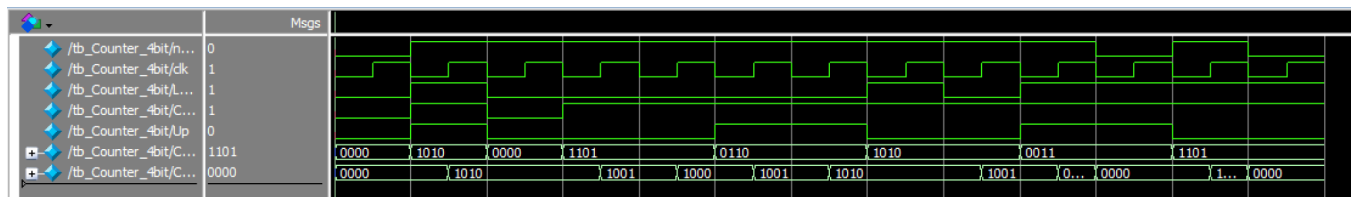


Figure 2. Proof of successful simulation results