



## Laboratory Report # 1

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Laboratory Exercise Title: Design Flow of Digital Systems

### Target Course Outcomes:

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

**CO2:** Verify the functionality of HDL-based components through design verification tools.

### Exercise 1C:

### Project Settings Summary

New Project Wizard

### Summary

When you click Finish, the project will be created with the following settings:

Project directory:	Z:\Lab#1
Project name:	HalfAdder
Top-level design entity:	HalfAdder
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	MAX 10 (DA/DF/DC/SA/SC)
Device:	10M50DAF484C7G
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	<None> (<None>)
Timing analysis:	()
Operating conditions:	
Core voltage:	1.2V
Junction temperature range:	0-85 °C

< Back   Next >   **Finish**   Cancel   Help



## Verilog HDL Design Entry

```
/*=====
```

```
SCHEDULE: FRI 11:00 AM - 2:00 PM  
COURSE:   CPE 3101L, Group 2  
AUTHOR:   Paul Emmanuel G. Corsino
```

```
=====*/
```

```
module HalfAdder (x, y, c, s);
```

```
    input    x , y;  
    output   c , s;
```

```
    xor      x1 (s, x, y);  
    and      a1 (c, x, y);
```

```
endmodule
```

## Compilation Report for the Flow Summary

The screenshot displays the Quartus Prime Lite Edition interface. The 'Table of Contents' pane on the left shows the 'Flow Summary' selected. The main window displays the 'Flow Summary' report for the 'HalfAdder.v' project.

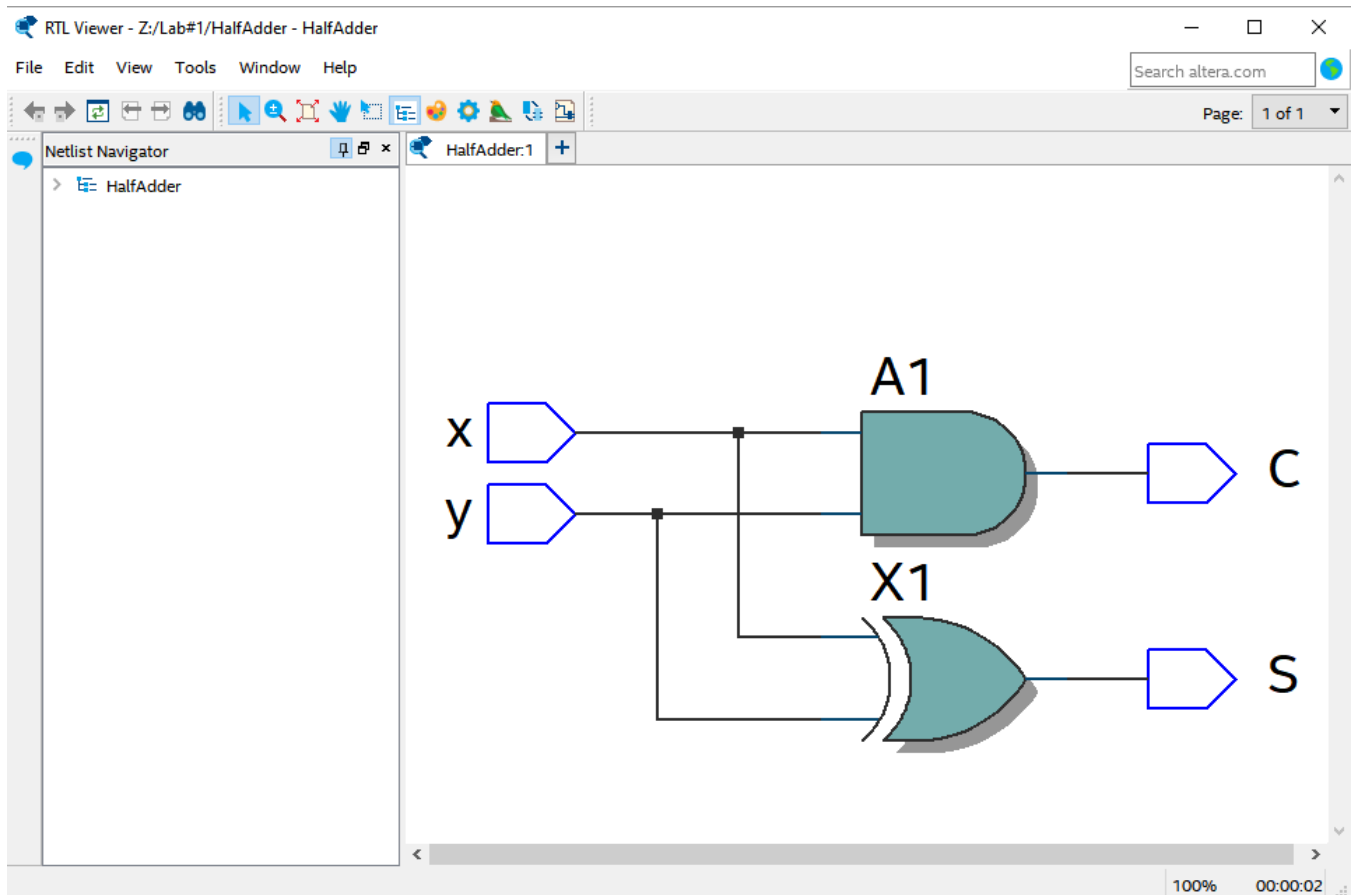
Flow Status	Successful - Fri Sep 01 12:57:28 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	HalfAdder
Top-level Entity Name	HalfAdder
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	N/A until Partition Merge
Total registers	N/A until Partition Merge
Total pins	N/A until Partition Merge

The 'Messages' pane at the bottom shows the following log:

```
*****  
> Running Quartus Prime Analysis & Elaboration  
Command: quartus_map --read_settings_files=on --write_settings_files=off HalfAdder -c HalfAdder --analysis_and_elaboration  
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS  
20030 Parallel compilation is enabled and will use 6 of the 6 processors detected  
> 12021 Found 1 design units, including 1 entities, in source file halfadder.v  
12127 Elaborating entity "HalfAdder" for the top level hierarchy  
> Quartus Prime Analysis & Elaboration was successful. 0 errors, 1 warning
```



## Schematic Diagram of Synthesized Circuit



## Message Window

