Laboratory Report # 4

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Laboratory Exercise Title: **Dataflow Modeling of Combinational Circuits**

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 4A: 4-Bit Comparator

Exercise 4A: 4-Bit Comparator

- Proof of successful design synthesis *(screenshot showing 0 errors)*
- Proof of successful simulation results with required number of test cases *(screenshots of simulation results with annotations or discussion of results)*

Figure 1.0 – *Flow Summary*

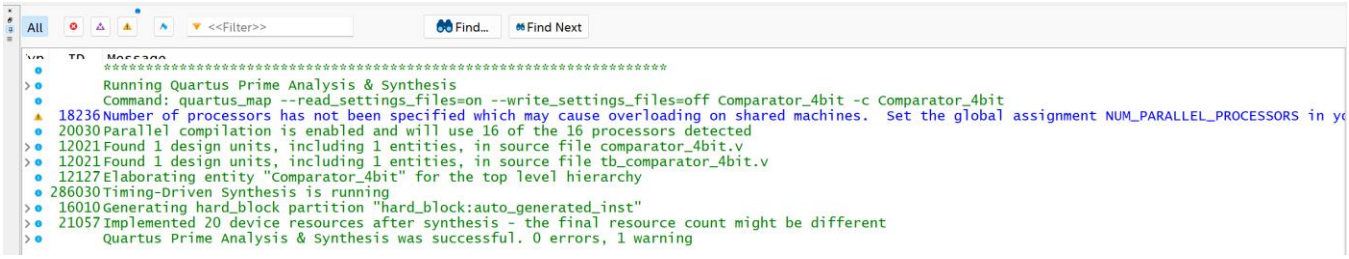

Figure 1.1 - *Proof of successful design synthesis*

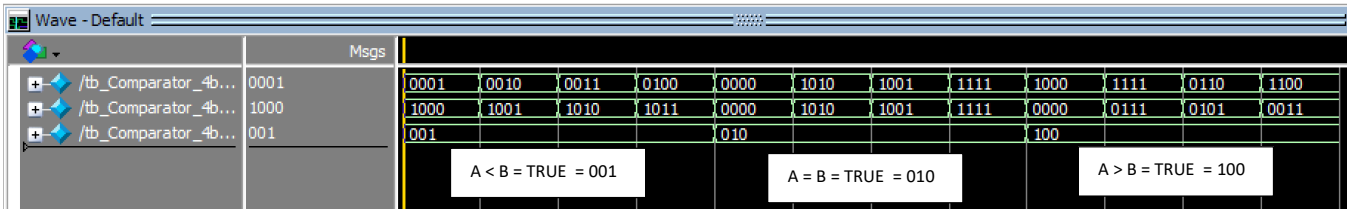

Figure 1.2– *4-Bit Comparator RTL Simulation Output (Waveform)*

```
# =-= Test Bench of 4-Bit Comparator =-=
# A < B
# Time =  0 ns A =  1 | [0001] B =  8 [1000] R = 001
# Time = 10 ns A =  2 | [0010] B =  9 [1001] R = 001
# Time = 20 ns A =  3 | [0011] B = 10 [1010] R = 001
# Time = 30 ns A =  4 | [0100] B = 11 [1011] R = 001
# A == B
# Time = 40 ns A =  0 | [0000] B =  0 [0000] R = 010
# Time = 50 ns A = 10 | [1010] B = 10 [1010] R = 010
# Time = 60 ns A =  9 | [1001] B =  9 [1001] R = 010
# Time = 70 ns A = 15 | [1111] B = 15 [1111] R = 010
# A > B
# Time = 80 ns A =  8 | [1000] B =  0 [0000] R = 100
# Time = 90 ns A = 15 | [1111] B =  7 [0111] R = 100
# Time = 100 ns A =  6 | [0110] B =  5 [0101] R = 100
# Time = 110 ns A = 12 | [1100] B =  3 [0011] R = 100
# ** Note: $stop    : C:/School/HDL/Comparator_4bit/tb_Comparator_4bit.v(42)
#    Time: 120 ns  Iteration: 0  Instance: /tb_Comparator_4bit
# Break in Module tb_Comparator_4bit at C:/School/HDL/Comparator_4bit/tb_Comparator_4bit.v line 42
```

Figure 1.3 – *4-Bit Comparator Testbench Monitor Output*

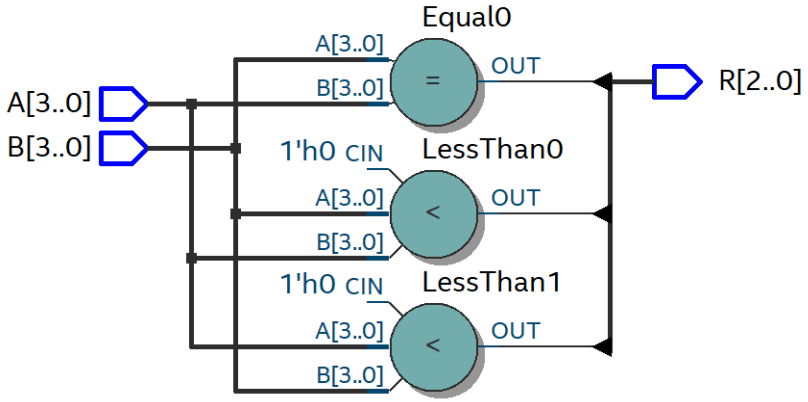

Figure 1.4 – *4-Bit Comparator RTL Viewer*

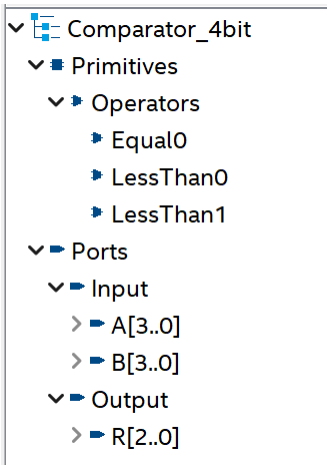

Figure 1.5 – *I/O Ports*

Exercise 4B: n-Bit 4-to-1 Line Multiplexer (Part 1: 4-Bit 4x1 Line Multiplexer)

Exercise 4B: n-Bit 4-to-1 Line Multiplexer (Part 1 and Part 2)

- Proof of successful design synthesis *(screenshot showing 0 errors)*
- Proof of successful simulation results with required number of test cases *(screenshots of simulation results with annotations or discussion of results)*

Figure 2.0 – *Flow Summary*

```
      ************************************************************
      Running Quartus Prime Analysis & Synthesis
      Command: quartus_map --read_settings_files=on --write_settings_files=off Mux_4x1_nbit -c Mux_4x1_nbit
18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in yo
20030 Parallel compilation is enabled and will use 16 of the 16 processors detected
12021 Found 1 design units, including 1 entities, in source file mux_4x1_nbit.v
12021 Found 1 design units, including 1 entities, in source file tb_mux_4x1_4bit.v
12021 Found 1 design units, including 1 entities, in source file tb_mux_4x1_8bit.v
12127 Elaborating entity "Mux_4x1_nbit" for the top level hierarchy
286030 Timing-Driven Synthesis is running
16010 Generating hard_block partition "hard_block:auto_generated_inst"
21057 Implemented 30 device resources after synthesis - the final resource count might be different
      Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning
```

Figure 2.1 – *Proof of successful design synthesis*

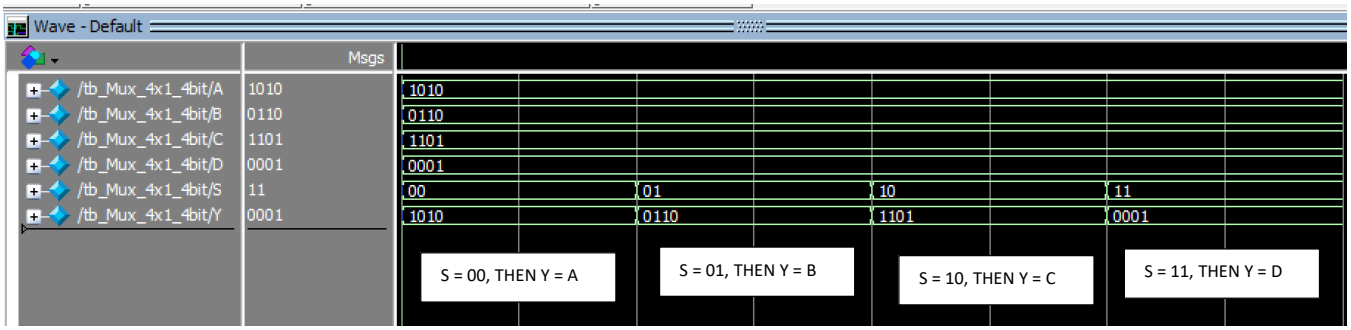

Figure 2.2 - *4-Bit 4x1 Line Multiplexer RTL Simulation Output (Waveform)*

```
# =-= Test Bench of 4-Bit 4x1 Multiplexer =-=
# =-= A =-=
# Time =  0 ns |A = 10 [1010]| |B =  6 [0110]| |C = 13 [1101]| |D =  1 [0001]| |S = 0 [00]| |Y = 10 [1010]|
# =-= B =-=
# Time = 10 ns |A = 10 [1010]| |B =  6 [0110]| |C = 13 [1101]| |D =  1 [0001]| |S = 1 [01]| |Y =  6 [0110]|
# =-= C =-=
# Time = 20 ns |A = 10 [1010]| |B =  6 [0110]| |C = 13 [1101]| |D =  1 [0001]| |S = 2 [10]| |Y = 13 [1101]|
# =-= D =-=
# Time = 30 ns |A = 10 [1010]| |B =  6 [0110]| |C = 13 [1101]| |D =  1 [0001]| |S = 3 [11]| |Y =  1 [0001]|
# ** Note: $stop    : C:/School/HDL/Mux_4x1_nbit/tb_Mux_4x1_4bit.v(41)
#    Time: 40 ps  Iteration: 0  Instance: /tb_Mux_4x1_4bit
# Break in Module tb_Mux_4x1_4bit at C:/School/HDL/Mux_4x1_nbit/tb_Mux_4x1_4bit.v line 41
```

Figure 2.3 – *4-Bit 4x1 Line Multiplexer Testbench Monitor Output*

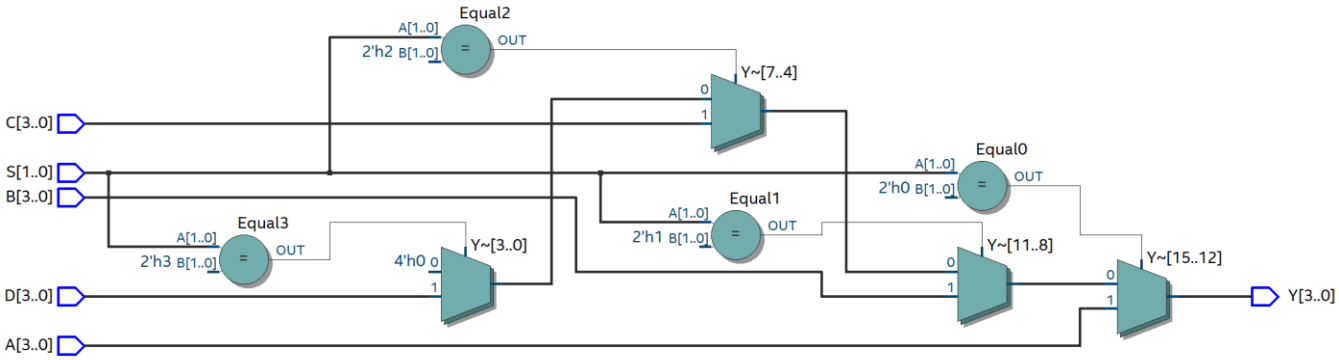

Figure 2.4 – *4-Bit 4x1 Line Multiplexer RTL Viewer*

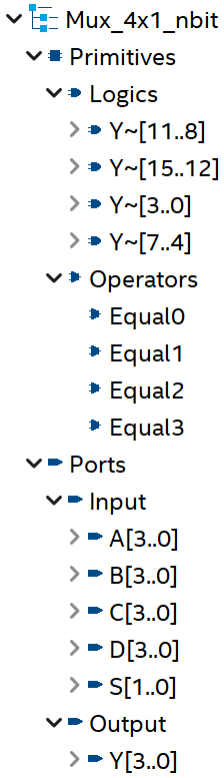

Figure 2.5 – *I/O Ports*

n-Bit 4-to-1 Line Multiplexer (Part 2: 8-Bit 4x1 Line Multiplexer)

Exercise 4B: n-Bit 4-to-1 Line Multiplexer (Part 1 and Part 2)

- Proof of successful design synthesis *(screenshot showing 0 errors)*
- Proof of successful simulation results with required number of test cases *(screenshots of simulation results with annotations or discussion of results)*

Figure 3.0 – *Flow Summary*

```
      ************************************************************
      Running Quartus Prime Analysis & Synthesis
      Command: quartus_map --read_settings_files=on --write_settings_files=off Mux_4x1_nbit -c Mux_4x1_nbit
18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in yo
20030 Parallel compilation is enabled and will use 16 of the 16 processors detected
12021 Found 1 design units, including 1 entities, in source file mux_4x1_nbit.v
12021 Found 1 design units, including 1 entities, in source file tb_mux_4x1_4bit.v
12021 Found 1 design units, including 1 entities, in source file tb_mux_4x1_8bit.v
12127 Elaborating entity "Mux_4x1_nbit" for the top level hierarchy
286030 Timing-Driven Synthesis is running
16010 Generating hard_block partition "hard_block:auto_generated_inst"
21057 Implemented 30 device resources after synthesis - the final resource count might be different
      Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning
```

Figure 3.1 – *Proof of successful design synthesis*

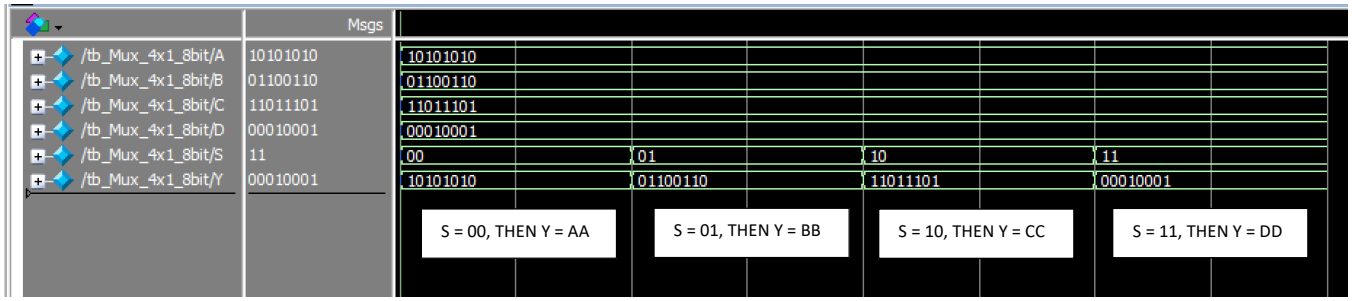

Figure 3.2 – *8-Bit 4x1 Line Multiplexer RTL Simulation Output (Waveform)*

```
# =-= Test Bench of 8-Bit 4x1 Multiplexer =-=
# =-= A =-=
# Time =  0 ns |A = 170 [10101010]| |B = 102 [01100110]| |C = 221 [11011101]| |D =  17 [00010001]| |S = 0 [00]| |Y = 170 [10101010]|
# =-= B =-=
# Time = 10 ns |A = 170 [10101010]| |B = 102 [01100110]| |C = 221 [11011101]| |D =  17 [00010001]| |S = 1 [01]| |Y = 102 [01100110]|
# =-= C =-=
# Time = 20 ns |A = 170 [10101010]| |B = 102 [01100110]| |C = 221 [11011101]| |D =  17 [00010001]| |S = 2 [10]| |Y = 221 [11011101]|
# =-= D =-=
# Time = 30 ns |A = 170 [10101010]| |B = 102 [01100110]| |C = 221 [11011101]| |D =  17 [00010001]| |S = 3 [11]| |Y =  17 [00010001]|
# ** Note: $stop    : C:/School/HDL/Mux_4x1_nbit/tb_Mux_4x1_8bit.v(41)
#    Time: 40 ps  Iteration: 0  Instance: /tb_Mux_4x1_8bit
# Break in Module tb_Mux_4x1_8bit at C:/School/HDL/Mux_4x1_nbit/tb_Mux_4x1_8bit.v line 41
```

Figure 3.3 – *8-Bit 4x1 Line Multiplexer Testbench Monitor Output*

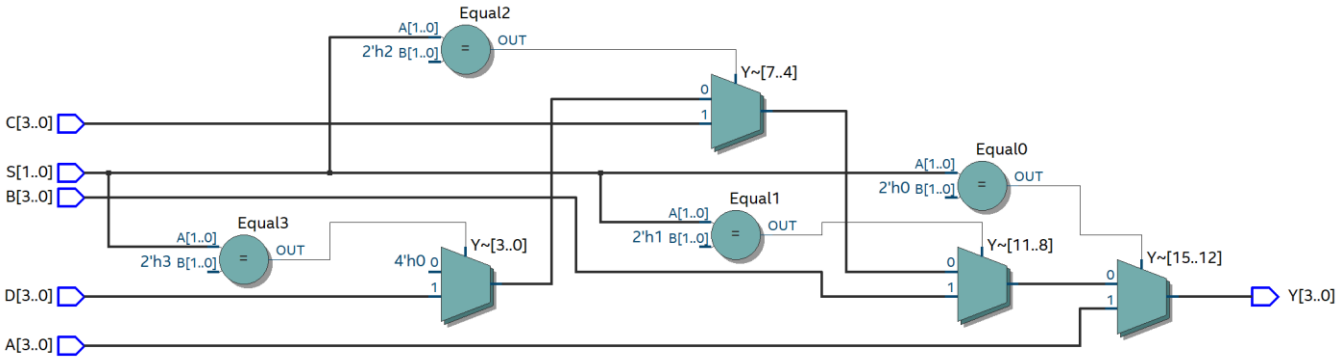

Figure 3.4 – *8-Bit 4x1 Line Multiplexer RTL Viewer*

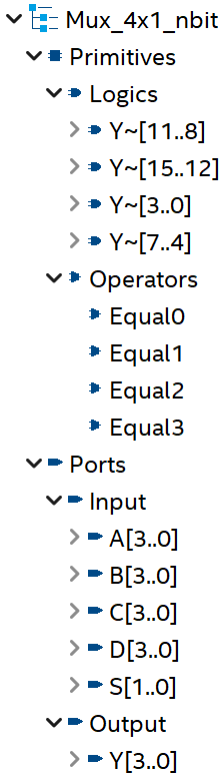

Figure 3.5 – *I/O Ports*