Laboratory Report #6

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Laboratory Exercise Title: Behavioral Modeling of Sequential Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 6A:

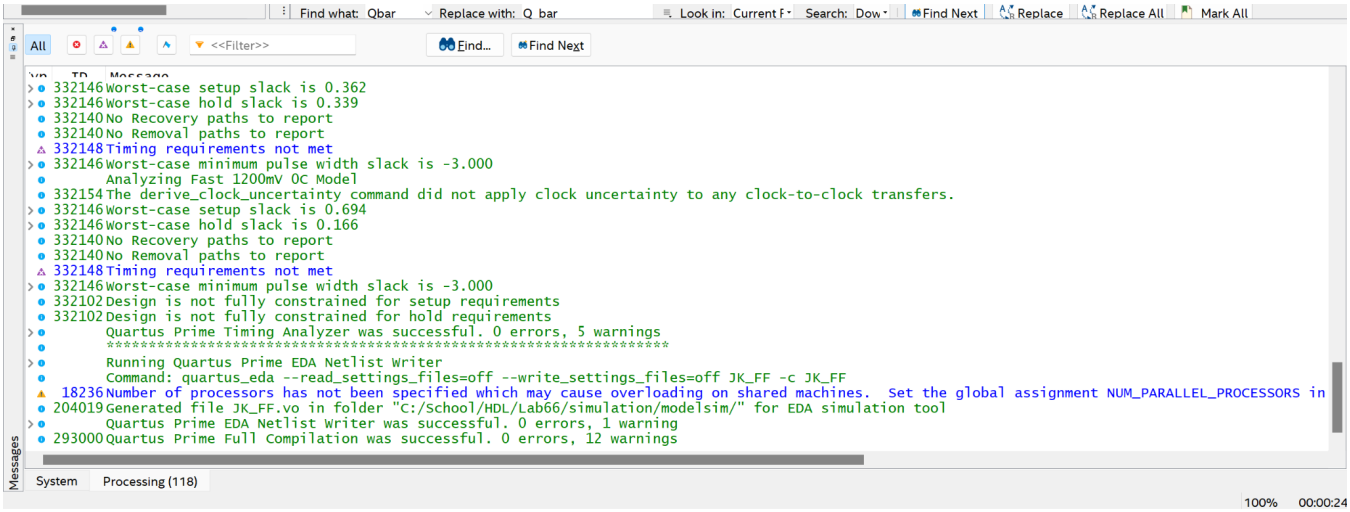

Figure 1. *Proof of successful design synthesis*

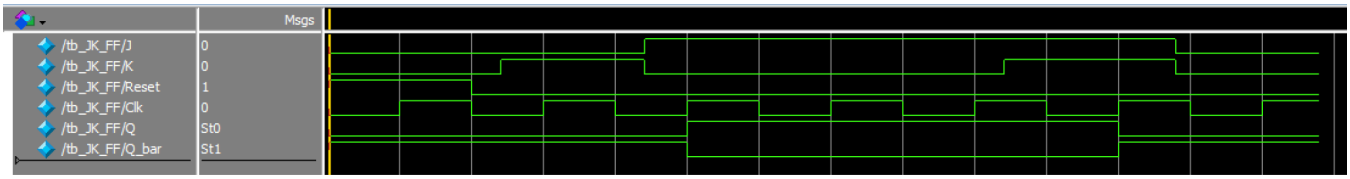

Figure 2. *Proof of successful simulation results*

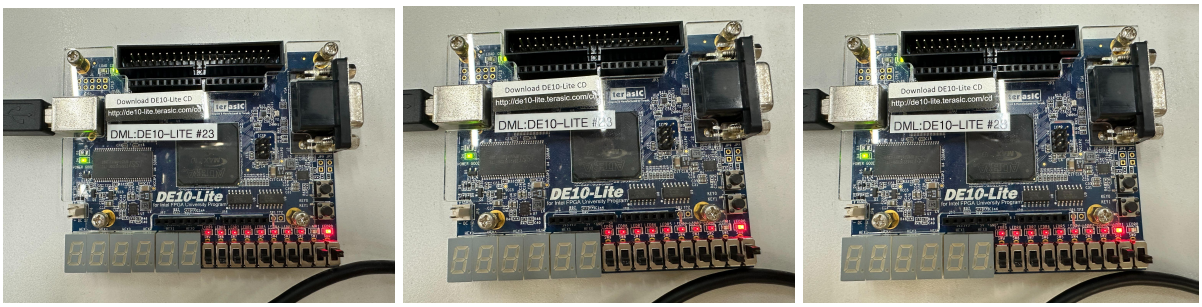

Figure 3. *Proof of successful FPGA implementation*

Exercise 6B:

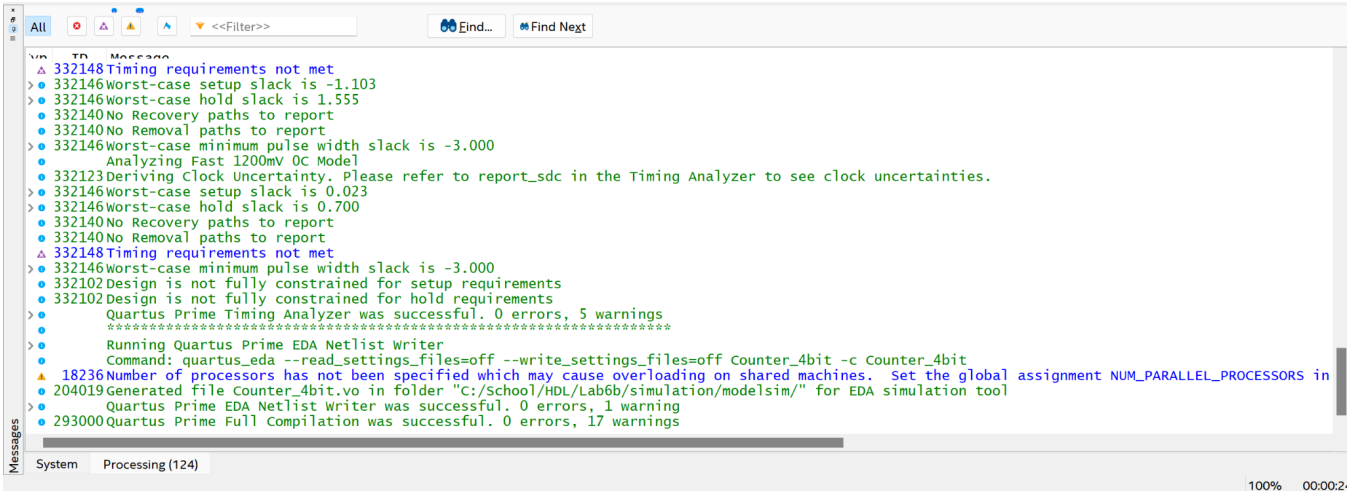

Figure 1. *Proof of successful design synthesis*

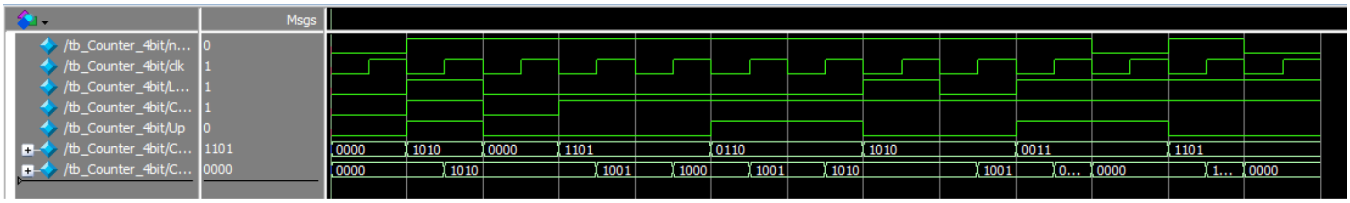

Figure 2. *Proof of successful simulation results*