# Laboratory Report # 1

**Name:** Paul Emmanuel G. Corsino **Date Completed:** 01/09/2023

**Laboratory Exercise Title:** Design Flow of Digital Systems

***Target Course Outcomes:***

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

**CO2:** Verify the functionality of HDL-based components through design verification tools.

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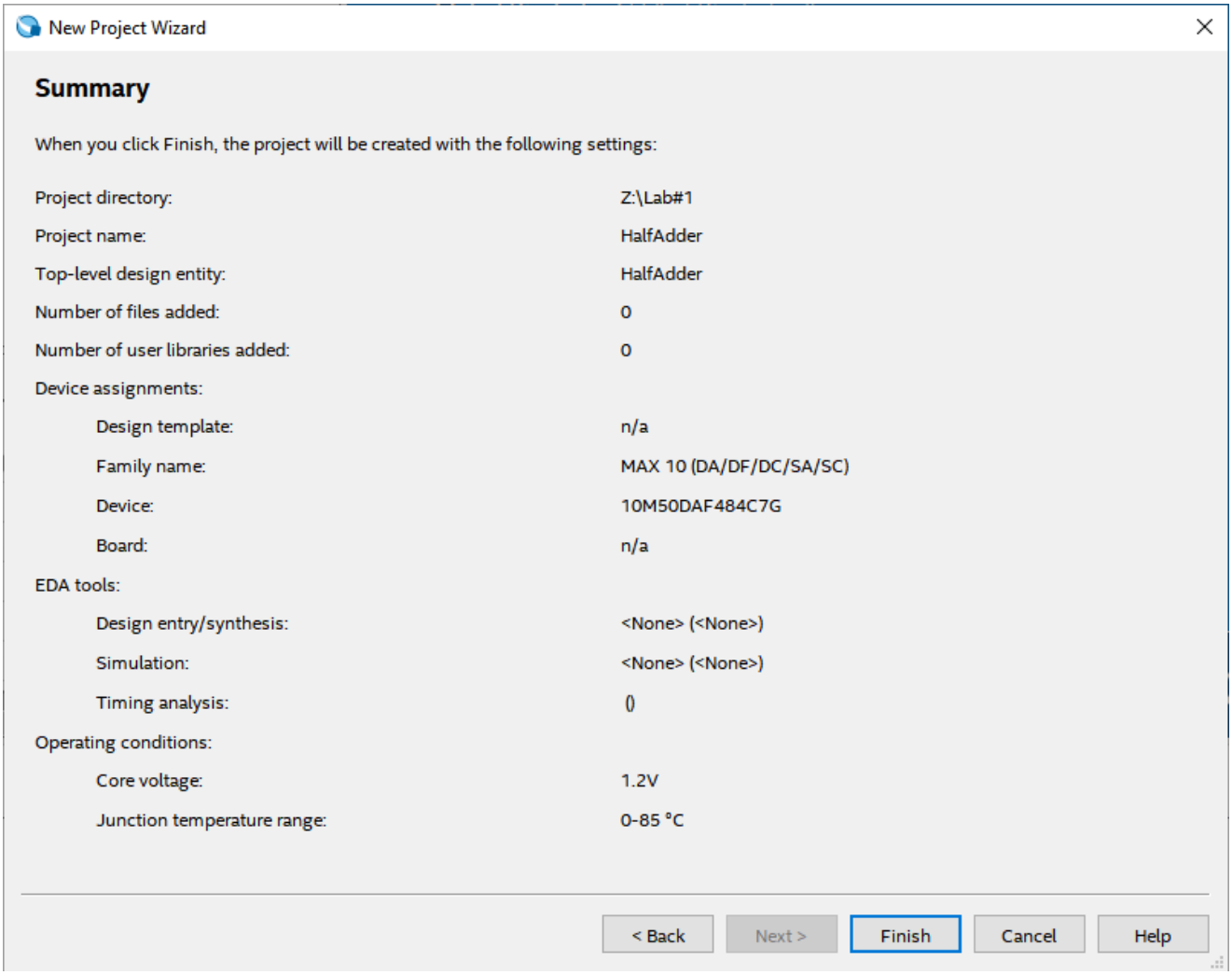
**Exercise 1C:**

## Project Settings Summary



## Verilog HDL Design Entry

```
/*=========================================

    SCHEDULE: FRI 11:00 AM - 2:00 PM
    COURSE:   CPE 3101L, Group 2
    AUTHOR:   Paul Emmanuel G. Corsino

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module HalfAdder (x, y, C, S);

    input    x , y;
    output   C , S;

    xor      X1 (S, x, y);
    and      A1 (C, x, y);

endmodule
```
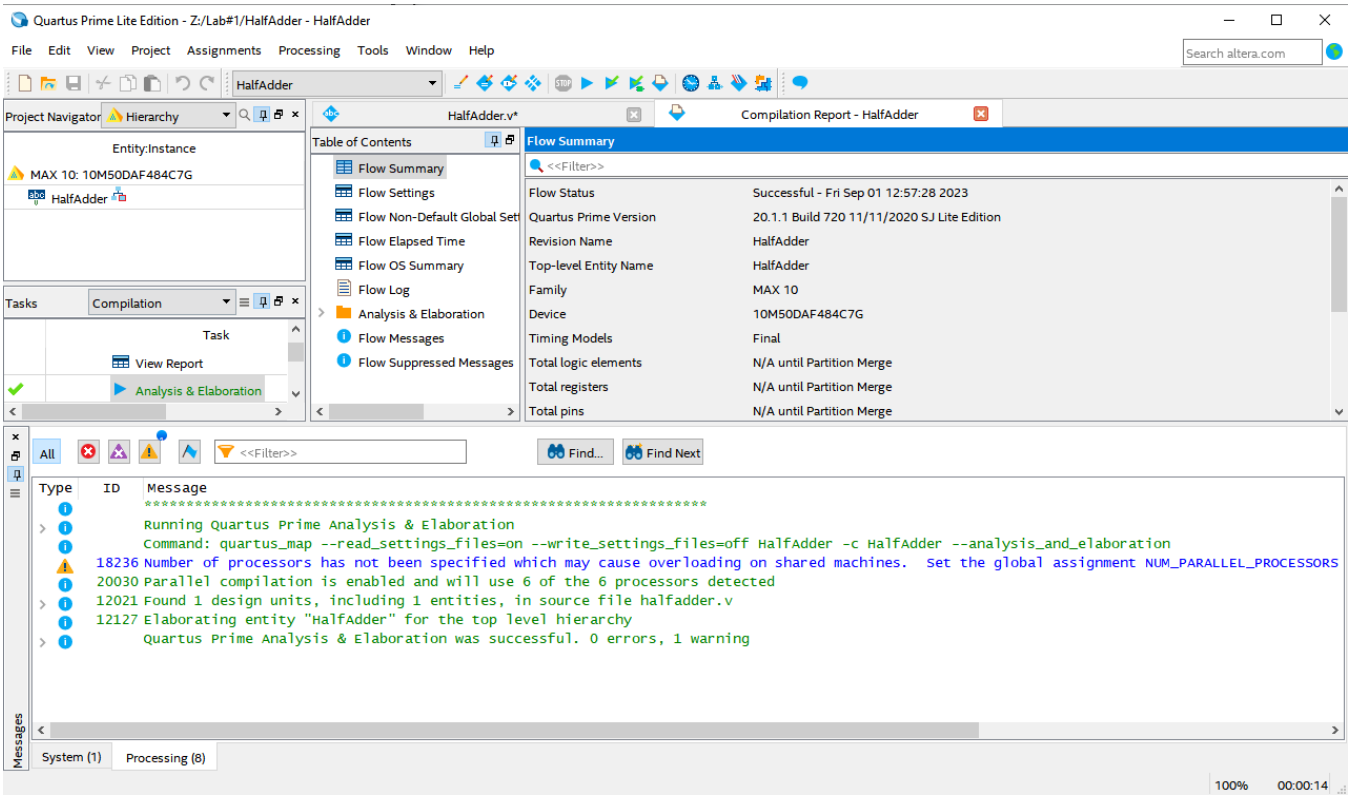
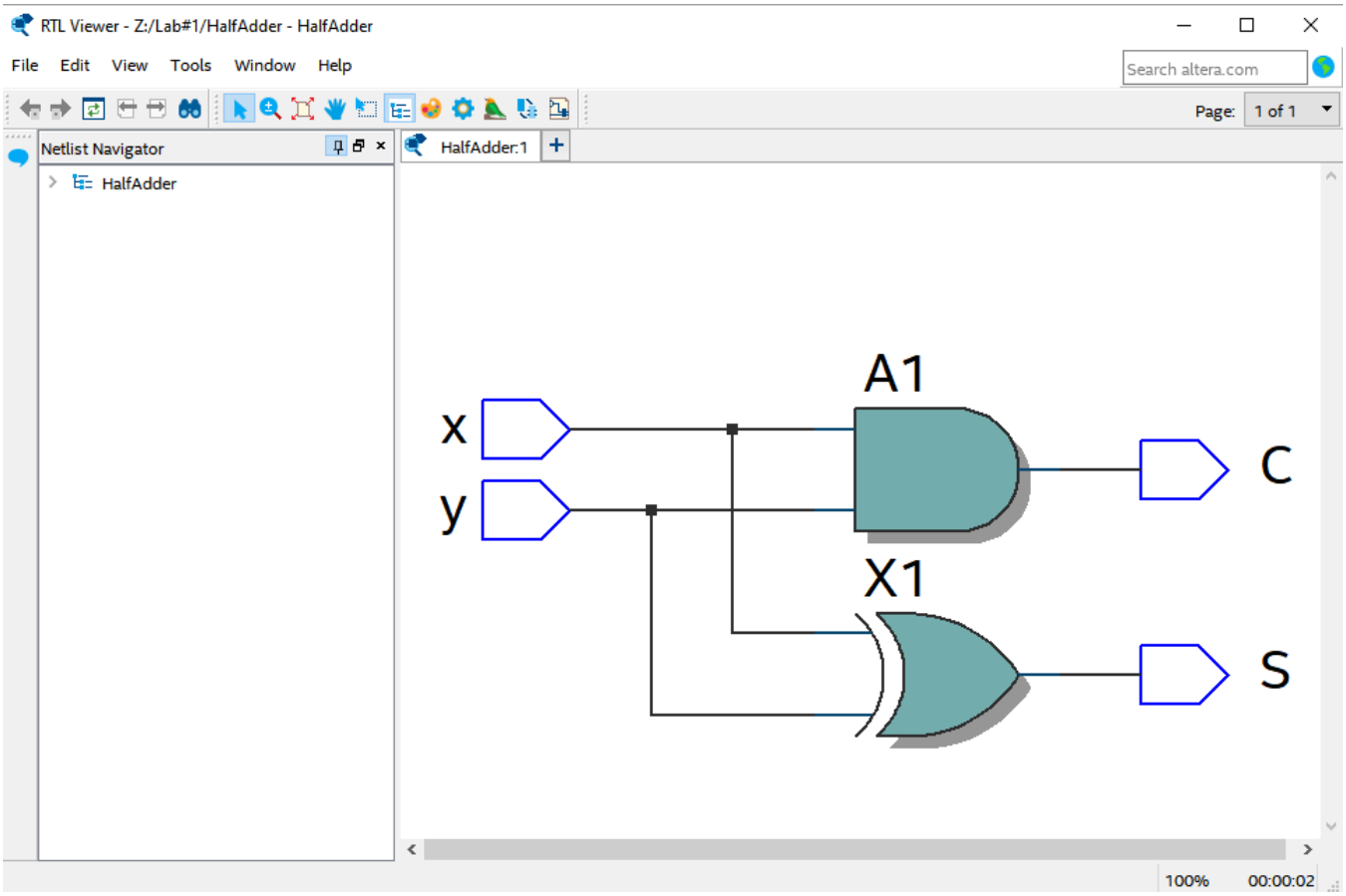

## Compilation Report for the Flow Summary



## Schematic Diagram of Synthesized Circuit




## Message Window