Laboratory Report #5

Name: Paul Emmanuel G. Corsino **Date Completed:** 17/11/2023

Laboratory Exercise Title: Behavioral Modeling of Combinational Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 5A:

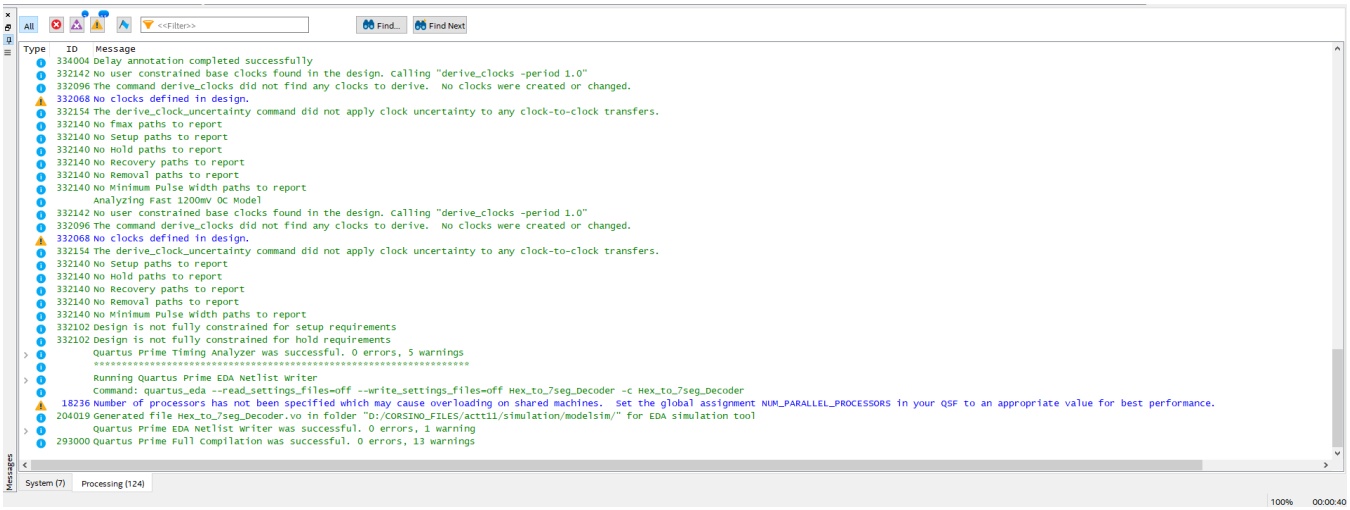

Figure 1. *Proof of successful design synthesis*

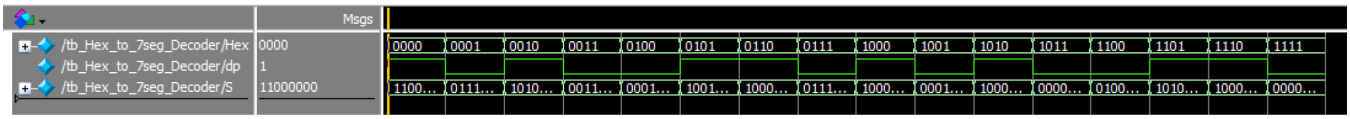

Figure 2. *Proof of successful simulation results*

Explanation:

Given the input, 0000, it results in an output in the 7-segment showing 0, with 0 having “1111110” via Figure 4, as an output in the 7-segment to visualize the variable “0”, It can be seen in Figure 2 that the S is valued “11000000” as the decimal point is turned on, while the following 8 bits is the alternate of the value of 0 via Figure 4. As 1 is 0 in S(in my wave), while the 1 bit in S is 0 to the value of bit in the truth table. Also, it is reversed from right to left, to left to right. Everything applies to the next set of waves. As my last wave’s S value contains “00001110”, and via the truth table, to display F, the 7 segment’s value has to be “10001111”.

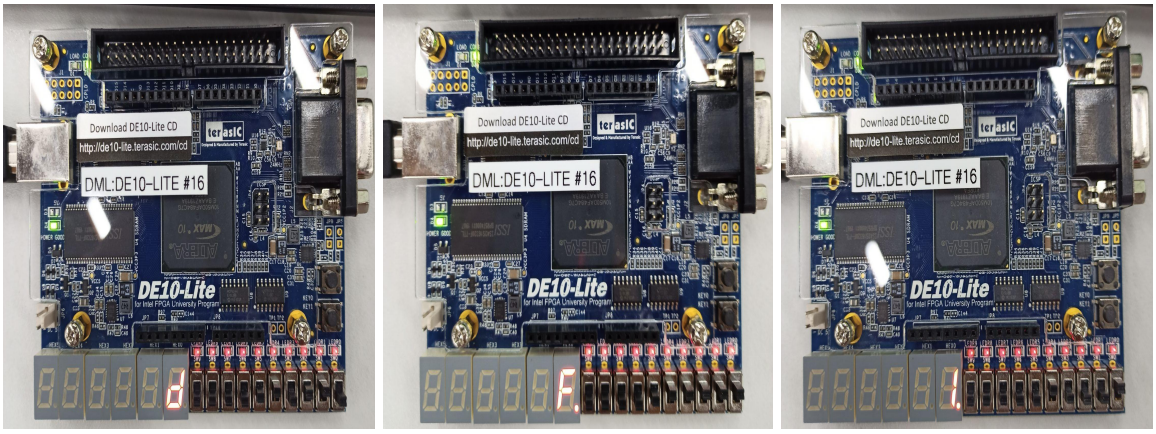

Figure 3. *Proof of successful FPGA implementation*

Inputs				Segments							
A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	For display 0
0	0	0	1	0	1	1	0	0	0	0	For display 1
0	0	1	0	1	1	0	1	1	0	1	For display 2
0	0	1	1	1	1	1	1	0	0	1	For display 3
0	1	0	0	0	1	1	0	0	1	1	For display 4
0	1	0	1	1	0	1	1	0	1	1	For display 5
0	1	1	0	1	0	1	1	1	1	1	For display 6
0	1	1	1	1	1	1	0	0	0	0	For display 7
1	0	0	0	1	1	1	1	1	1	1	For display 8
1	0	0	1	1	1	1	1	0	1	1	For display 9
1	0	1	0	1	1	1	0	1	1	1	For display A
1	0	1	1	0	0	1	1	1	1	1	For display b
1	1	0	0	1	0	0	1	1	1	0	For display C
1	1	0	1	0	1	1	1	1	0	1	For display d
1	1	1	0	1	0	0	1	1	1	1	For display E
1	1	1	1	1	0	0	0	1	1	1	For display F

Figure 4. *Hex to 7-segment decoder truth table*

Exercise 5B:

```
Info: 332140 No Hold paths to report
Info: 332140 No Recovery paths to report
Info: 332140 No Removal paths to report
Info: 332140 No Minimum Pulse Width paths to report
Info:        Analyzing Fast 1200mV 0C Model
Info: 332142 No user constrained base clocks found in the design. Calling "derive_clocks -period 1.0"
Info: 332096 The command derive_clocks did not find any clocks to derive.  No clocks were created or changed.
Warning: 332068 No clocks defined in design.
Info: 332154 The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
Info: 332140 No Setup paths to report
Info: 332140 No Hold paths to report
Info: 332140 No Recovery paths to report
Info: 332140 No Removal paths to report
Info: 332140 No Minimum Pulse Width paths to report
Info: 332102 Design is not fully constrained for setup requirements
Info: 332102 Design is not fully constrained for hold requirements
Info:        Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
Info:        ******************************************************************
Info:        Running Quartus Prime EDA Netlist Writer
Info:        Command: quartus_eda --read_settings_files=off --write_settings_files=off ALU_nbit -c ALU_nbit
Warning: 18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in
Info: 204019 Generated file ALU_nbit.vo in folder "C:/School/HDL/LAB5-act2/simulation/modelsim/" for EDA simulation tool
Info:        Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
Info: 293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
```

Figure 1. *Proof of successful design synthesis*

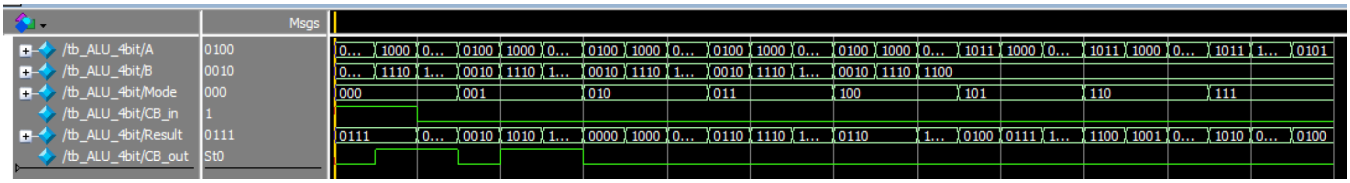

Figure 2. *Proof of successful simulation results*

Explanation:

```
# Initiating simulation at 0 ns.
# Time =  0 ns Mode = 000 A = 0100 B = 0010 CB_in = 1 Result = 0111 CB_out = 0
# Time = 10 ns Mode = 000 A = 1000 B = 1110 CB_in = 1 Result = 0111 CB_out = 1
# Time = 20 ns Mode = 000 A = 0101 B = 1100 CB_in = 0 Result = 0001 CB_out = 1
# Time = 30 ns Mode = 001 A = 0100 B = 0010 CB_in = 0 Result = 0010 CB_out = 0
# Time = 40 ns Mode = 001 A = 1000 B = 1110 CB_in = 0 Result = 1010 CB_out = 1
# Time = 50 ns Mode = 001 A = 0101 B = 1100 CB_in = 0 Result = 1001 CB_out = 1
# Time = 60 ns Mode = 010 A = 0100 B = 0010 CB_in = 0 Result = 0000 CB_out = 0
# Time = 70 ns Mode = 010 A = 1000 B = 1110 CB_in = 0 Result = 1000 CB_out = 0
# Time = 80 ns Mode = 010 A = 0101 B = 1100 CB_in = 0 Result = 0100 CB_out = 0
# Time = 90 ns Mode = 011 A = 0100 B = 0010 CB_in = 0 Result = 0110 CB_out = 0
# Time = 100 ns Mode = 011 A = 1000 B = 1110 CB_in = 0 Result = 1110 CB_out = 0
# Time = 110 ns Mode = 011 A = 0101 B = 1100 CB_in = 0 Result = 1101 CB_out = 0
# Time = 120 ns Mode = 100 A = 0100 B = 0010 CB_in = 0 Result = 0110 CB_out = 0
# Time = 130 ns Mode = 100 A = 1000 B = 1110 CB_in = 0 Result = 0110 CB_out = 0
# Time = 140 ns Mode = 100 A = 0101 B = 1100 CB_in = 0 Result = 1001 CB_out = 0
# Time = 150 ns Mode = 101 A = 1011 B = 1100 CB_in = 0 Result = 0100 CB_out = 0
# Time = 160 ns Mode = 101 A = 1000 B = 1100 CB_in = 0 Result = 0111 CB_out = 0
# Time = 170 ns Mode = 101 A = 0101 B = 1100 CB_in = 0 Result = 1010 CB_out = 0
# Time = 180 ns Mode = 110 A = 1011 B = 1100 CB_in = 0 Result = 1100 CB_out = 0
# Time = 190 ns Mode = 110 A = 1000 B = 1100 CB_in = 0 Result = 1001 CB_out = 0
# Time = 200 ns Mode = 110 A = 0101 B = 1100 CB_in = 0 Result = 0110 CB_out = 0
# Time = 210 ns Mode = 111 A = 1011 B = 1100 CB_in = 0 Result = 1010 CB_out = 0
# Time = 220 ns Mode = 111 A = 1000 B = 1100 CB_in = 0 Result = 0111 CB_out = 0
# Time = 230 ns Mode = 111 A = 0101 B = 1100 CB_in = 0 Result = 0100 CB_out = 0
# Simulation finished at 240 ns.
# ** Note: $stop    : C:/School/HDL/LAB5-act2/tb_ALU_4bit.v(75)
#    Time: 240 ns  Iteration: 0  Instance: /tb_ALU_4bit
```

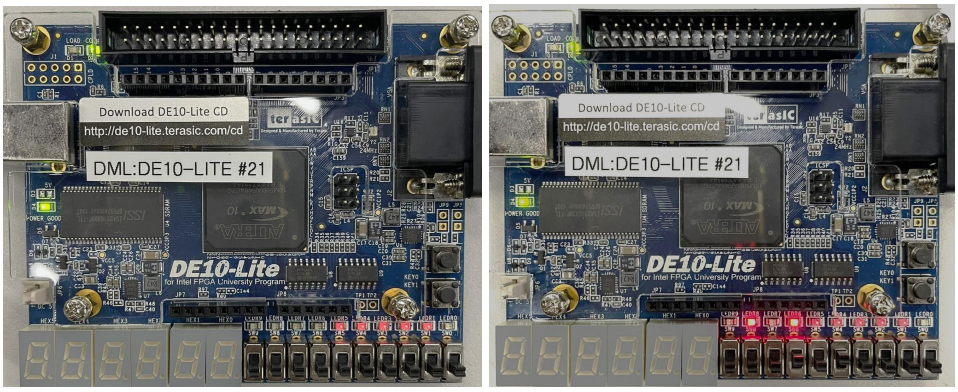

Figure 3. *Proof of successful FPGA implementation*