Laboratory Report #3

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Laboratory Exercise Title: **Structural Modeling of Combinational Circuits**

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 3A: 2x4 Decoder

- Boolean function, logic diagram, and the respective solutions
- Label the logic diagram that corresponds to its Verilog design entry *(names of I/O ports, internal signals, etc.)*
- Proof of successful design synthesis *(screenshot showing 0 errors)*
- Proof of successful simulation results *(screenshots of simulation results with annotations or discussion of results)*

Figure 1. Flow Summary

2x4 Decoder Boolean Function:

D[0] = (E)(!A[1])(!A[0])

D[1] = (E)(!A[1])(A[0])

D[2] = (E)(A[1](!A[0])

D[3] = (E)(A[1])(A[0])

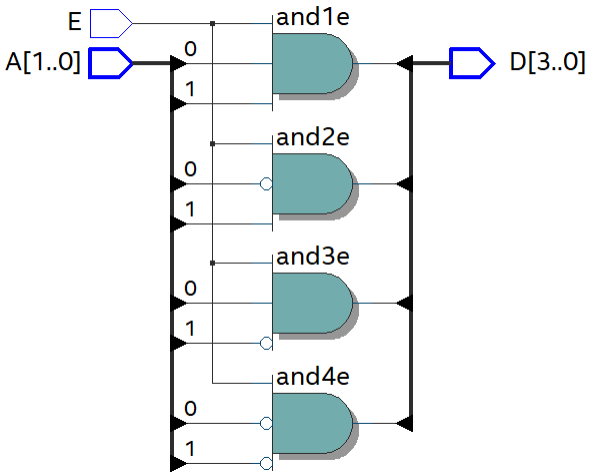

Figure 2. Logic Diagram (RTL Viewer)

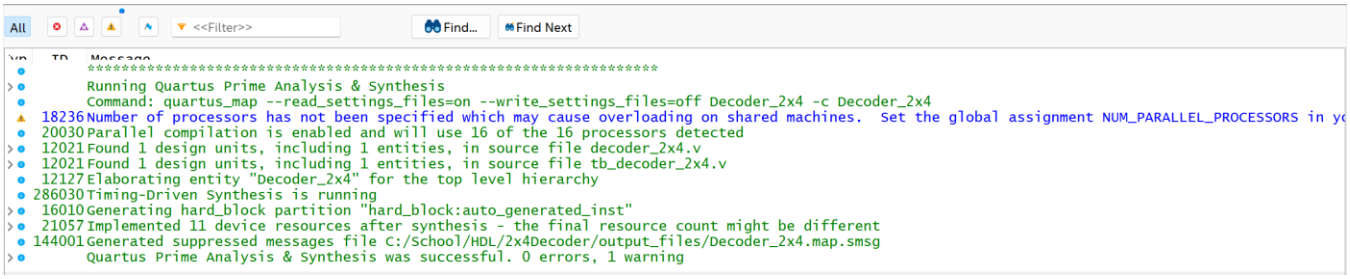

Figure 3. Proof of successful design synthesis

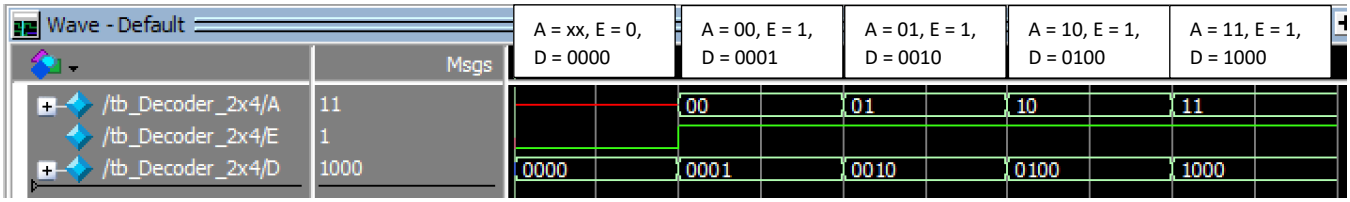

Figure 4. Simulation results w/ annotations

Inputs		Output
E	**A**	**D**
0	xx	0000
1	00	0001
1	01	0010
1	10	0100
1	11	1000

Figure 5. Truth table

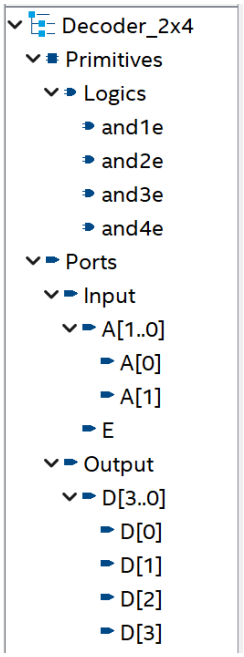

Figure 6. I/O Ports

Exercise 3B: 3x8 Decoder

- Boolean function, logic diagram, and the respective solutions
- Label the logic diagram that corresponds to its Verilog design entry *(names of I/O ports, internal signals, etc.)*
- Proof of successful design synthesis *(screenshot showing 0 errors)*
- Proof of successful simulation results *(screenshots of simulation results with annotations or discussion of results)*

Figure 7. Flow Summary

3x8 Decoder Boolean Function:

D[0] = (!A)(!B)(!C) D[4] = (A)(!B)(!C)

D[1] = (!A)(!B)(C) D[5] = (A)(!B)(C)

D[2] = (!A)(B)(!C) D[6] = (A)(B)(!C)

D[3] = (!A)(B)(C) D[7] = (A)(B)(C)

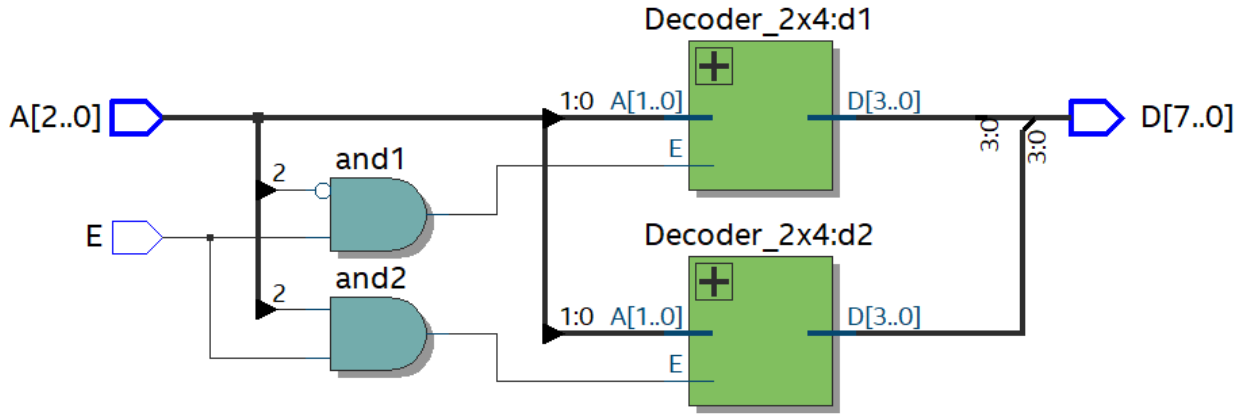

Figure 8. Logic Diagram (RTL Viewer)

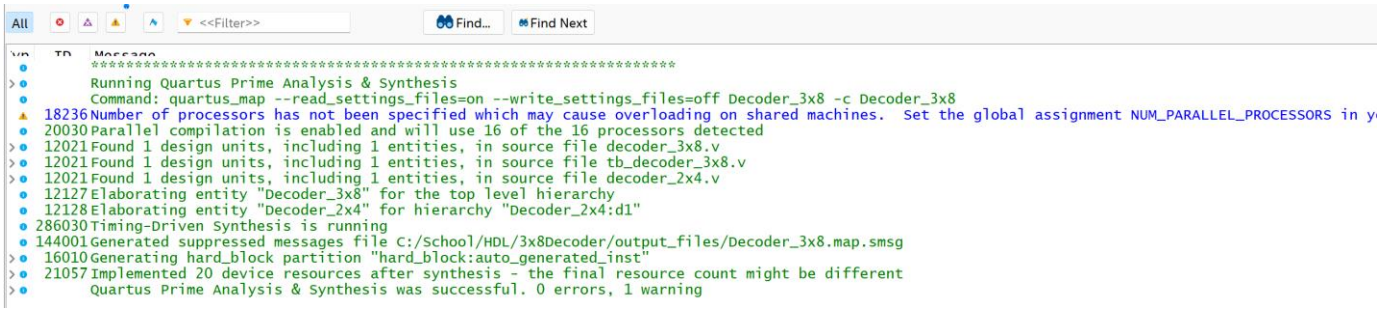

Figure 9. Proof of successful design synthesis

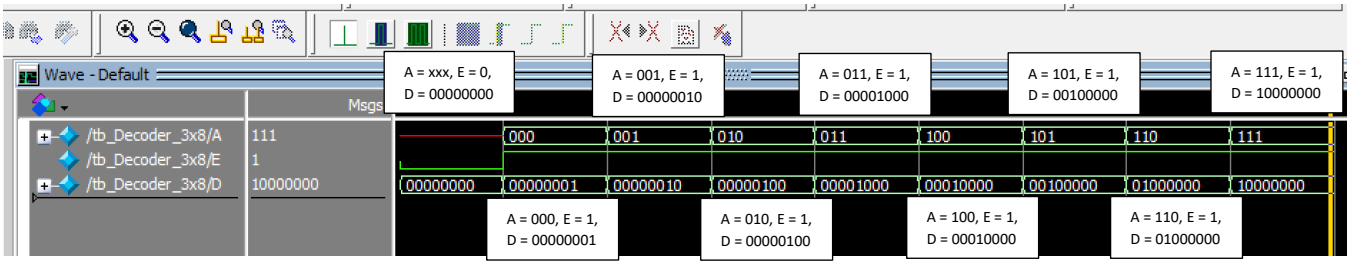

Figure 10. Simulation results w/ annotations

Enable	INPUTS			Outputs							
E	A_2	A_1	A_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Figure 11. Truth Table

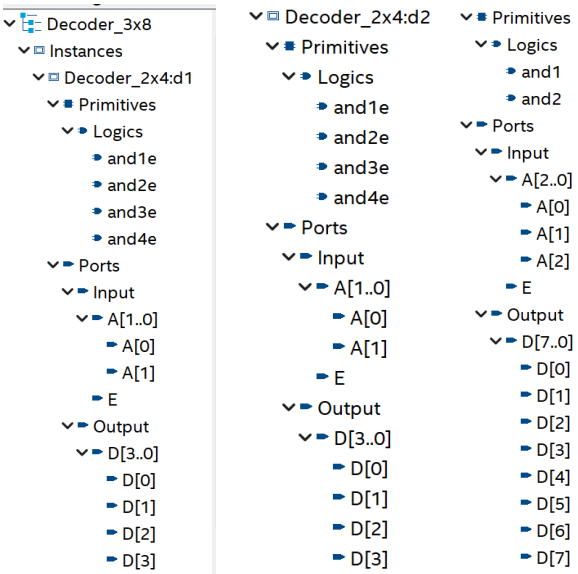

Figure 12. I/O Ports