



Laboratory Report #3

Name: Paul Emmanuel G. Corsino

Date Completed: 9/25/2023

Laboratory Exercise Title: Structural Modeling of Combinational Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 3A: 2x4 Decoder

- Boolean function, logic diagram, and the respective solutions
- Label the logic diagram that corresponds to its Verilog design entry (*names of I/O ports, internal signals, etc.*)
- Proof of successful design synthesis (*screenshot showing 0 errors*)
- Proof of successful simulation results (*screenshots of simulation results with annotations or discussion of results*)

Figure 1. Flow Summary

2x4 Decoder Boolean Function:

$$D[0] = (E)(\neg A[1])(\neg A[0])$$

$$D[1] = (E)(\neg A[1])(A[0])$$

$$D[2] = (E)(A[1])(\neg A[0])$$

$$D[3] = (E)(A[1])(A[0])$$

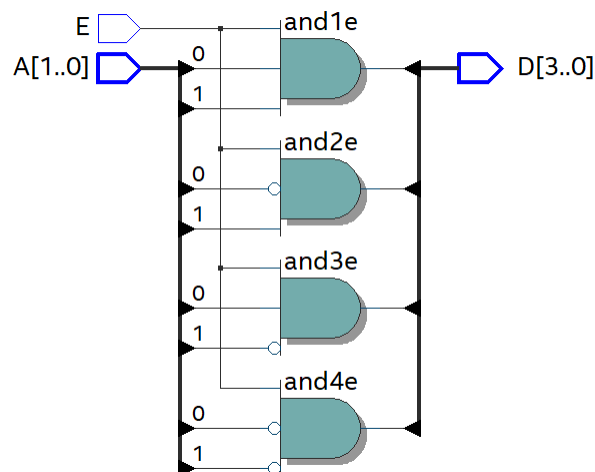


Figure 2. Logic Diagram (RTL Viewer)

```

All Find... Find Next
*****
> Running Quartus Prime Analysis & Synthesis
> Command: quartus_map --read_settings_files=on --write_settings_files=off Decoder_2x4 -c Decoder_2x4
> 18236Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in y
> 20030Parallel compilation is enabled and will use 16 of the 16 processors detected
> 12021Found 1 design units, including 1 entities, in source file decoder_2x4.v
> 12021Found 1 design units, including 1 entities, in source file tb_decoder_2x4.v
> 12127Elaborating entity "Decoder_2x4" for the top level hierarchy
> 286030Timing-Driven Synthesis is running
> 16010Generating hard_block partition "hard_block:auto_generated_inst"
> 21057Implemented 11 device resources after synthesis - the final resource count might be different
> 144001Generated suppressed messages file c:/School/HDL/2x4Decoder/output_files/Decoder_2x4.map.smsg
> Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning
  
```

Figure 3. Proof of successful design synthesis

Wave - Default		A = xx, E = 0, D = 0000	A = 00, E = 1, D = 0001	A = 01, E = 1, D = 0010	A = 10, E = 1, D = 0100	A = 11, E = 1, D = 1000
/tb_Decoder_2x4/A	11	00	01	10	11	
/tb_Decoder_2x4/E	1					
/tb_Decoder_2x4/D	1000	0000	0001	0010	0100	1000

Figure 4. Simulation results w/ annotations

Inputs		Output
E	A	D
0	xx	0000
1	00	0001
1	01	0010
1	10	0100
1	11	1000

Figure 5. Truth table

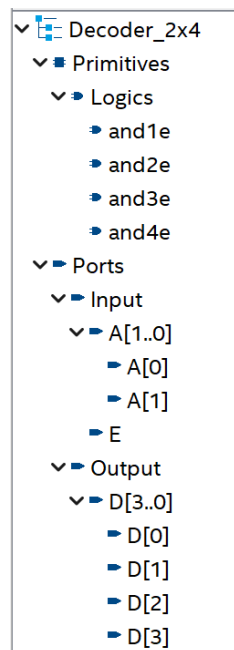


Figure 6. I/O Ports

Exercise 3B: 3x8 Decoder

- Boolean function, logic diagram, and the respective solutions
- Label the logic diagram that corresponds to its Verilog design entry (*names of I/O ports, internal signals, etc.*)
- Proof of successful design synthesis (*screenshot showing 0 errors*)
- Proof of successful simulation results (*screenshots of simulation results with annotations or discussion of results*)

Figure 7. Flow Summary

3x8 Decoder Boolean Function:

$D[0] = (!A)(!B)(!C)$	$D[4] = (A)(!B)(!C)$
$D[1] = (!A)(!B)(C)$	$D[5] = (A)(!B)(C)$
$D[2] = (!A)(B)(!C)$	$D[6] = (A)(B)(!C)$
$D[3] = (!A)(B)(C)$	$D[7] = (A)(B)(C)$

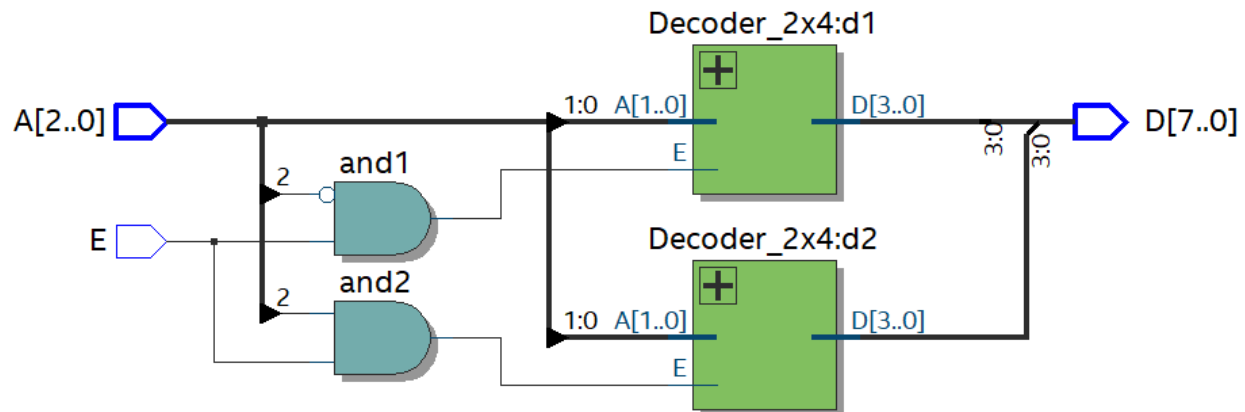


Figure 8. Logic Diagram (RTL Viewer)

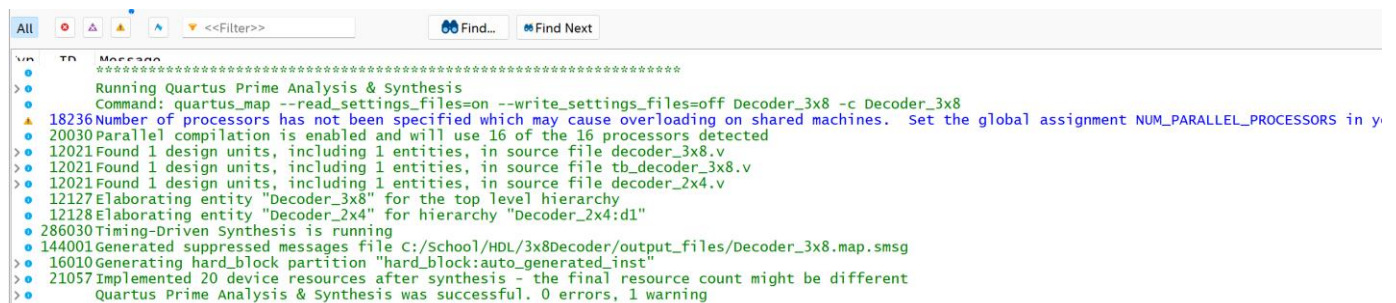


Figure 9. Proof of successful design synthesis

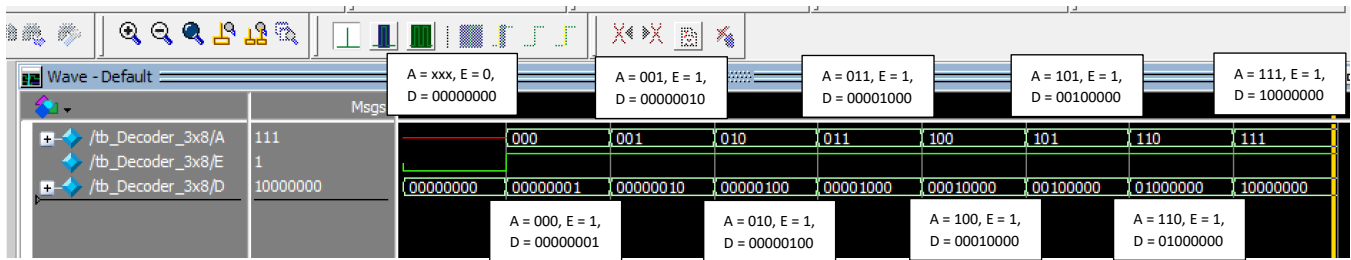


Figure 10. Simulation results w/ annotations

Enable	INPUTS			Outputs							
E	A ₂	A ₁	A ₀	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Figure 11. Truth Table

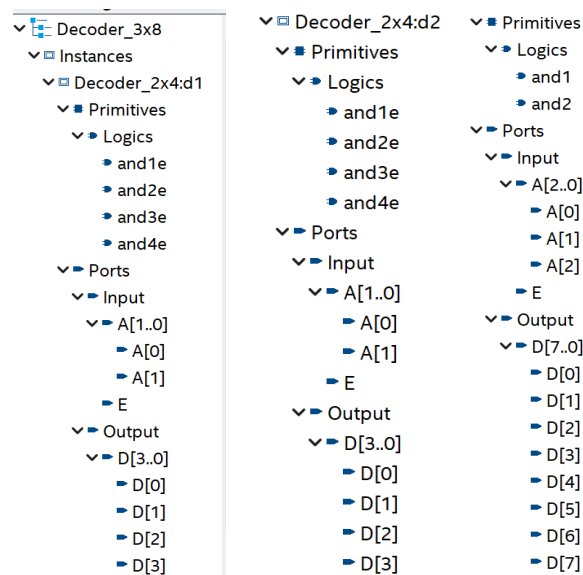


Figure 12. I/O Ports