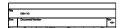
Dragon Board 4 V3



SHEET BLOCK	SCHEMATIC	SHEET BLOCK	SCHEMATIC	SHEET BLOCK	SCHEMATIC	SHEET BLOCK	SCHEMATIC
1 \ 2 \ 3 \ 4 \ 5 \ 6 \ 6 \ 7 \ 8 \ 9 \ 10 \ 11 \ 12 \ 13 \ 14 \ 15 \ 16 \ 17 \ 18 \ 19 \ 20 \ 21 \ 22 \ 23 \ 24 \ 25 \ 26 \ 27 \ 28 \ 29 \ 30 \ 31 \ 32 \ 33 \ 34 \ 35 \ \	TITLE TABLE OF CONTENTS APQ8016 - CONTROL APQ8016 - EBI0-LPDDR3 APQ8016 - GPI0 0-73 APQ8016 - GPI0 0-73 APQ8016 - GPI0 74-121 / DNC APQ8016 - BOOT CONFIG SW APQ8016 - MIPI CSI/DSI APQ8016 - FINTERFACE APQ8016 - PWR1 APQ8016 - PWR2 APQ8016 - PWR3 APQ8016 - GND APQ8016 - GND APQ8016 - DECOUPLING EXTERNAL BUCK REGULATORS PM8916 - CONTROL/CLOCKS PM8916 - CONTROL/CLOCKS PM8916 - CONTROL/CLOCKS PM8916 - LDOS PM8916 - AUDIO MEMORY - LPDDR3 + EMMC - CONT MEMORY - LPDDR3 + EMMC - POWE MEMORY - USD CONNECTOR USB - SWITCH HUB USB - CONNECTORS DISPLAY - DSI TO HDMI BRIDGE SWITCHES/LEDS HS / LS EXPANSION CONNECTORS JTAG / UART / ANALOG EXPANSION WCN3680B - RF / CONTROL WCN3680B - FEM WGR7640 - GPS USB to Ethernet	ER.					

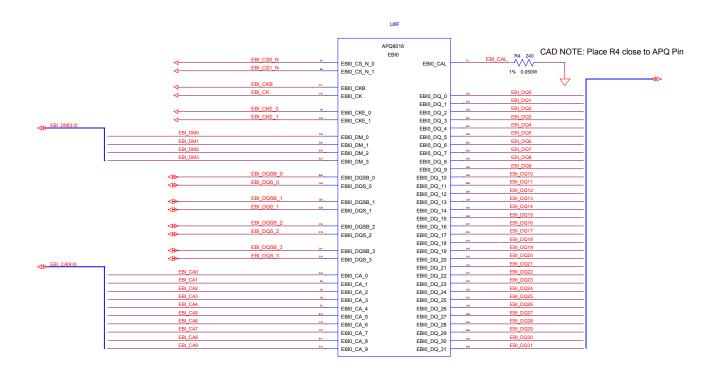


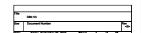
#### APQ8016 - CONTROL Note: CLK\_OUT trace (WCN36xx output 24 MHz clock) should have a 1MOhm pulldown resistor at host (MSMAPQ) side to prevent corner case MSM leakage current in dual-band wifi designs. For single-band designs not using CLK\_OUT line, connect WCSS\_XO MSMAPQ pin directly to ground. wcss\_xo⊲<del>⊳</del> R313 APQ8016 CONTROL CAD NOTE: Place R2, R3 close to APQ pin Route BBCLK1 as daisy chain.AD35 pin first and then AL34 second wcss\_xo CXO CXO\_EN SDC1\_CLK SDC1\_CMD SLEEP\_CLK SDC1\_CMD D APQ RESIN N APQ RESOUT N SDC1\_DATA\_0 RESIN N SDC1\_DATA\_0 SDC1\_DATA\_1 RESOUT\_N SDC1 DATA 2 SDC1\_DATA\_2 SDC1\_DATA\_3 MODE\_0 SDC1\_DATA\_3 MODE\_1 SDC1\_DATA\_4 SDC1\_DATA\_4 SDC1 DATA 5 SDC1\_DATA\_5 SDC1\_DATA\_6 APQ\_PS\_HOLD PS\_HOLD SDC1\_DATA\_6 SDC1\_DATA\_7 SDC1\_DATA\_7 ▶ JTAG SRST N SRST\_N SDC2\_CLK > JTAG\_TCK JTAG\_TDI TCK SDC2\_CLK JTAG\_TDO JTAG\_TMS JTAG\_TRST\_N TDI SDC2\_CMD SDC2 DATA 0 ♣ TDO SDC2\_DATA\_0 SDC2 DATA 1 TMS SDC2\_DATA\_1 SDC2\_DATA\_2 TRST\_N SDC2\_DATA\_2 SDC2 DATA 3 SDC2\_DATA\_3 VREF\_EBI0\_CA 0.1UF USB HS D M ◀▷ VREF\_EBI0\_D0\_D2 USB2\_HS\_DM USB\_HS\_D\_P ◀▷ USB2\_HS\_DP VREF\_EBI0\_D1\_D3 USB2\_HS\_ID USB2\_HS\_TXRTUNE BBCLK1 ◀ USB2\_HS\_SYSCLOCK SPMI CLK NC PLL\_TEST\_SE PMIC\_SPMI\_CLK SPMI DATA PMIC\_SPMI\_DATA R80 C173 ≥ 200 1% 33PF Install C2, C173 if SPMI\_DATA/CLK signrals requires slew control 33PF ATEST0 ATEST1 DNI DNI

CAD NOTE: Place R80 close to APQ pin

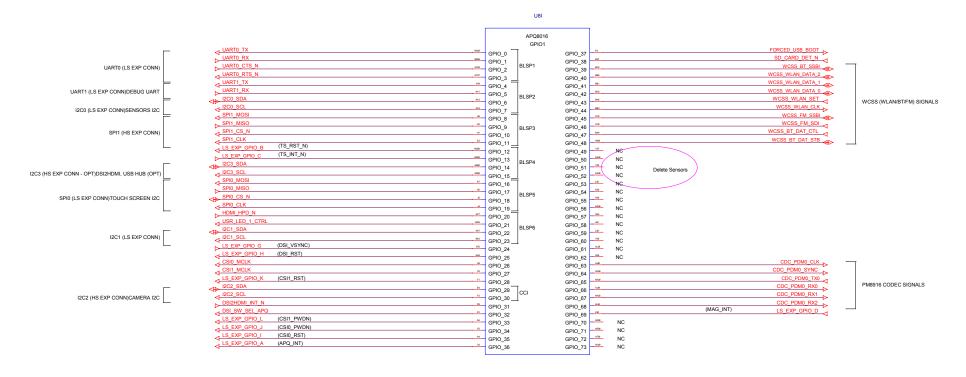


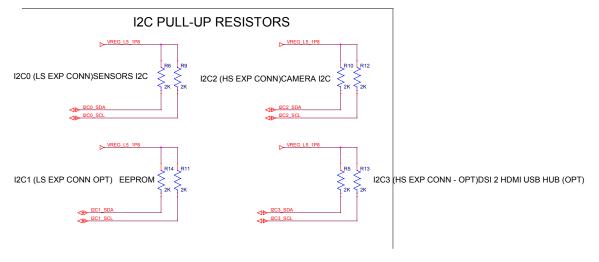
## APQ8016 - EBI0-LPDDR3



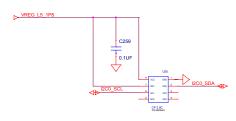


## APQ8016 - GPIO 0-73



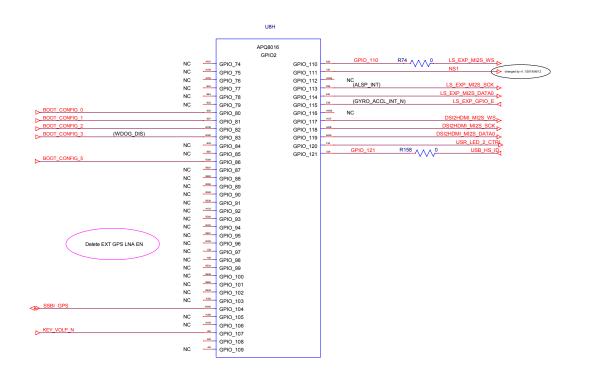


## Apple Authentication Copprocessor 2.0C

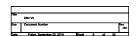




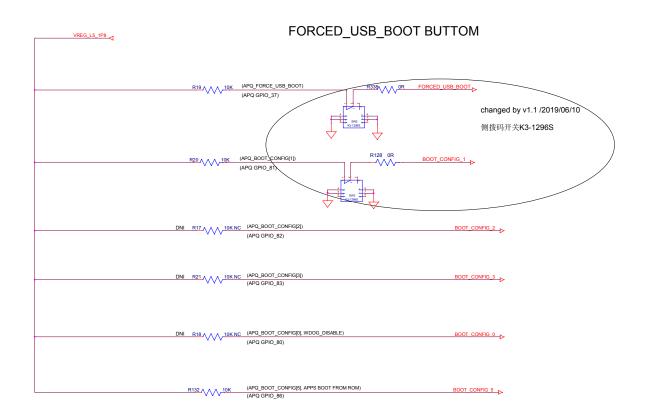
## APQ8016 - GPIO 74-121 / DNC







## APQ8016 - BOOT CONFIG SW

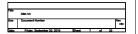


Note 1: Short between resistors pads to force boot from USB when dip-switch is not installed Note 2: Short between resistors pads to boot from uSD when dip-switch is not installed

#### **BOOT CONFIGURATIONS**

BOOT_CONFIG[3:1]	BOOT OPTIONS
0b000	SDC1> SDC2> USB2.0
0b001	SDC2> SDC1> USB2.0
0b010	SDC1> USB2.0
0b011	USB2.0

Default Boot Config (0b000) is eMMC on the SDC1



U8B

```
APQ8016
                                                                                                                                                                                                                                            MIPL DSIO_CLK_N

MIPL DSIO_CLK_P

MIPL DSIO_CLK_P

MIPL DSIO_CLK_P

MIPL DSIO_LANEO_N

MIPL DSIO_DATAO_M

MIPL DSIO_LANEO_N

MIPL DSIO_DATAO_M

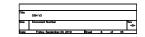
MIPL DSIO_DATAI_M

MIPL DSIO_LANEI_N

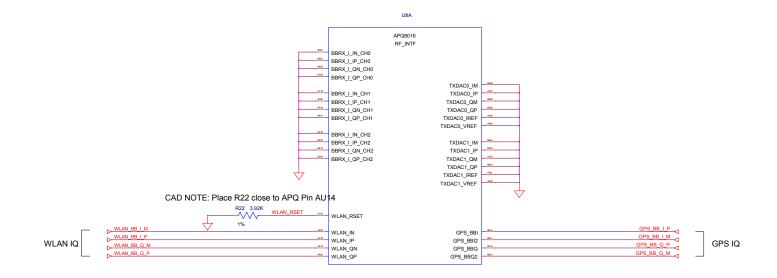
MIPL DSIO_LANEI_N

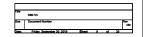
MIPL DSIO_DATAY_M

MI
                                                                                                                                                                                                         MIPI
    MIPI_CSI0_LANE1_N
       MIPI_CSI0_CLK_P
                                                                                                         MIPI_CSI0_LANE1_P
       MIPI_CSI0_DATA1_M ...
                                                                                                                MIPI_CSI0_LANE2_N
       MIPI_CSI0_DATA1_P h
                                                                                                                MIPI_CSI0_LANE2_P
                                                                                                                                                                                                                                               MIPL DSIO_LANE2_P
MIPL DSIO_LANE2_P
MIPL DSIO_LANE3_N
MIPL DSIO_LANE3_N
MIPL DSIO_LANE3_N
MIPL DSIO_LANE3_P
    MIPI_CSI0_DATA2_M ws
                                                                                                                MIPI_CSI0_LANE3_N
                                                                                                                MIPI_CSI0_LANE3_P
      MIPI_CSI0_DATA3_M MIPI_CSI0_DATA3_P VS
                                                                                                                MIPI_CSI0_LANE4_N
                                                                                                                MIPI_CSI0_LANE4_P
                                                                                                                                                                                                                                                  MIPI_DSI0_LANE3_P
MIPI_CSI1_DATA0_M MIPI_CSI1_LANE0_N MIPI_CSI1_LANE0_P MIPI_CSI1_LANE0_P
                                                                                                             MIPI_CSI1_LANE0_P
 MIPI_CSI1_CLK_M ASS MIPI_CSI1_LANE1_N
   MIPI_CSI1_CLK_P 46
                                                                                                                MIPI_CSI1_LANE1_P
    MIPI_CSI1_DATA1_M AG MIPI_CSI1_LANE2_N
   MIPI_CSI1_DATA1_P
                                                                                                                MIPI_CSI1_LANE2_P
```

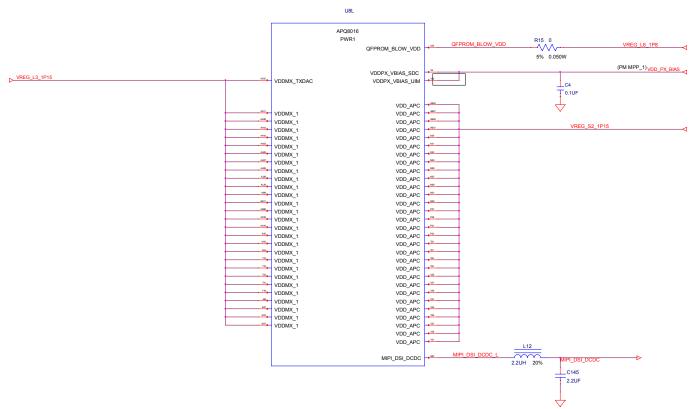


## APQ8016 - RF INTERFACE





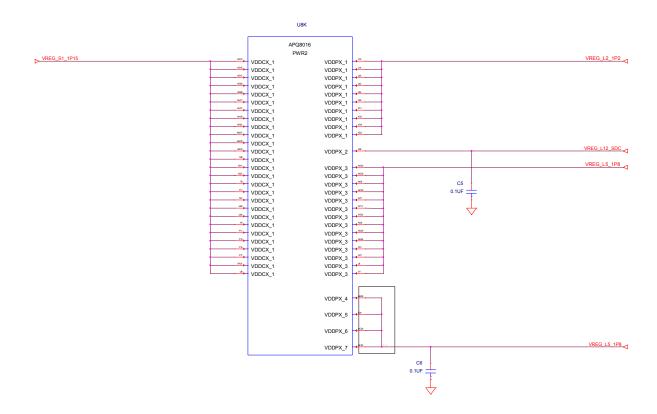
## APQ8016 - PWR1



CAD NOTE: Loop to be shorted with MSM AG6 Pin

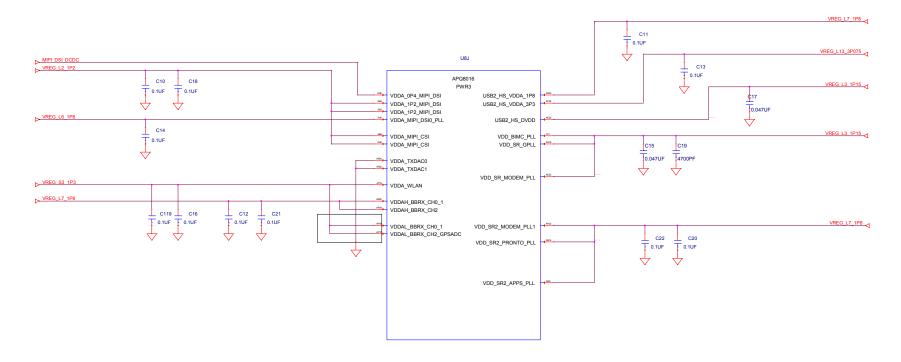


## APQ8016 - PWR2



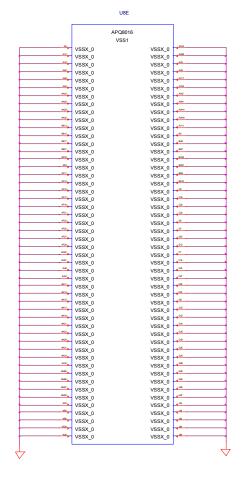


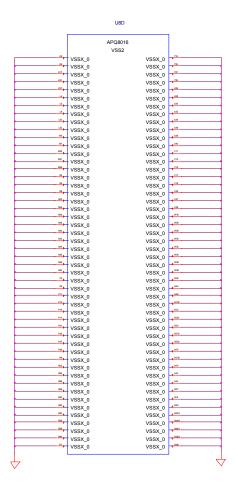
## APQ8016 - PWR3

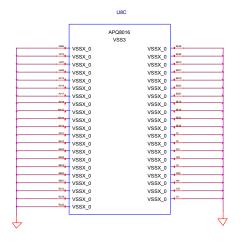


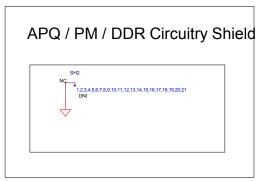


## APQ8016 - GND



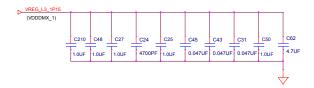


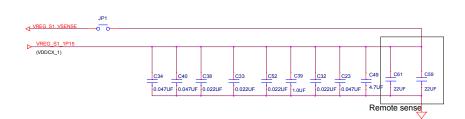


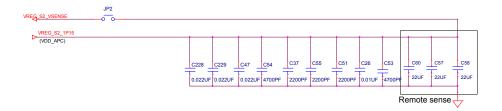


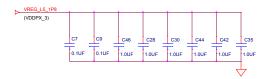


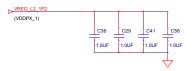
## **APQ8016 BYPASS CAPACITORS**





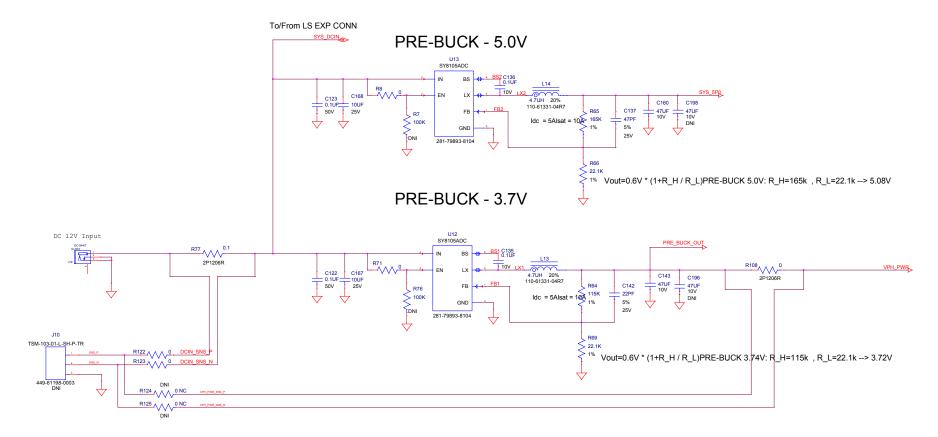








## **EXTERNAL BUCK REGULATORS**



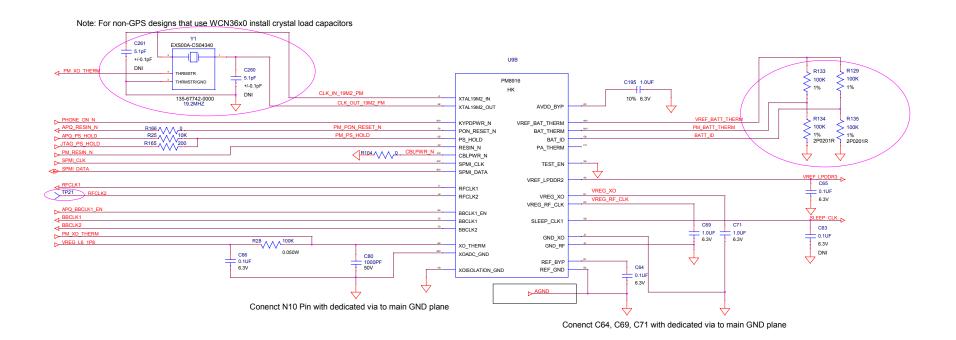
### ARM ENERGY PROBE (PWR MEAS)

SUPPORTED	ASSY OPTION
YES	INSTALL J10
NO	DNI J10

Delete VPH\_PWR SOURCE

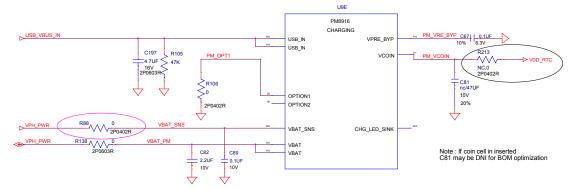


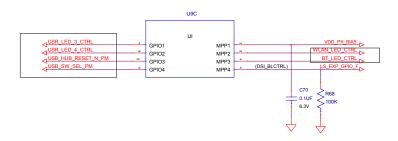
## PM8916 - CONTROL/CLOCKS

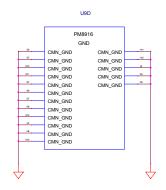


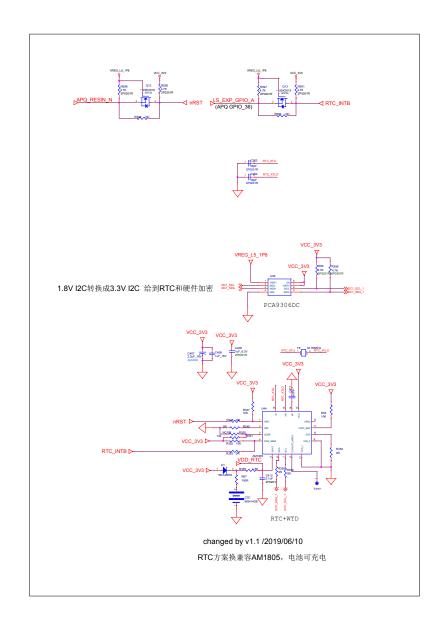


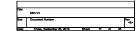
## PM8916 - CHARGER/GPIOS/MPPS



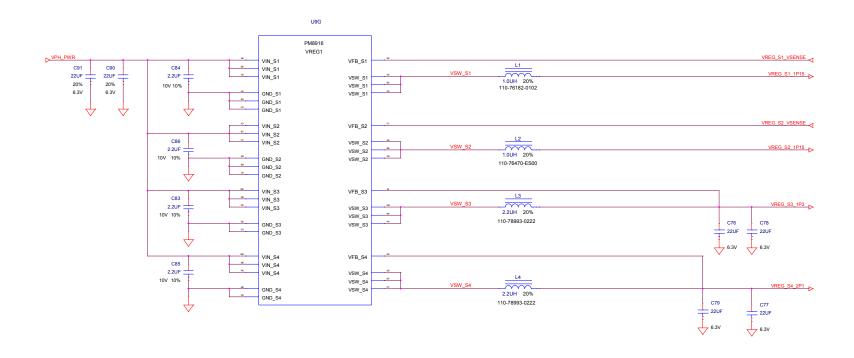


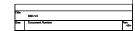




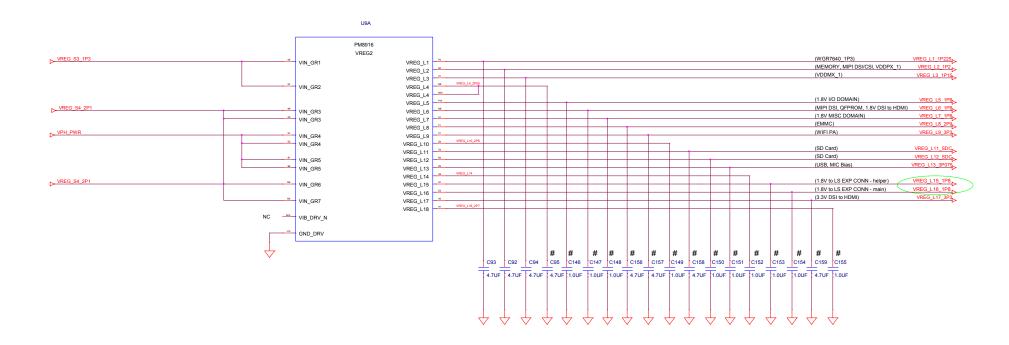


## PM8916 - SMPS





## PM8916 - LDOs



### NOTES:

Effective output capacitanceLDOs L1, L2, L3, L4, L8, L9, L11, L17 --> Cout\_eff = 4.7uFLDOs L5, L6, L7, L10, L12, L13, L14, L15, L16, L18 --> Cout\_eff = 1.0uF

PSEUDO CAPLESS LDOs (indicated by # near the capacitor)L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18 PSEUDO CAPLESS LDOs capacitors location is defined in 80-NK808-21



#### PM8916 - AUDIO VREG\_L5\_1P8 < C68 U9F VREG\_S4\_2P1 \_1 PM8916 CDC 1.0UF CDC\_VDDIO CDC\_VDD\_PA CAD Note: Place C98 and C99 close to pin A11 and B11.Place C87 close to pin G14. CDC\_VDD\_CP CDC\_VDD\_CP C99 22UF 10V DNI SPKR\_OUT\_P C98 22UF 10V DNI C88 CDC\_SPKDRV\_P C74 2P1206R SPKR\_OUT\_M 7 2.2UF CDC\_SPKDRV\_M CDC\_VDD\_SPKDRV 4.7UF 2.2UF 10V CDC\_SPKDRV\_M TP18 CDC\_MIC1\_P CDC\_IN1\_P CDC\_BOOST\_VREG\_5V CDC MIC2 P CDC\_IN2\_P CDC\_BOOST\_VREG\_5V CDC\_IN3\_P VPH\_PWR ⊲ CDC\_VBAT C100 10UF DNI CDC\_MIC\_BIAS1 CDC\_BOOST\_SW1 CDC MIC BIAS2 DNI CDC\_MIC\_BIAS2 CDC\_BOOST\_SW2 2.2UH 20% 110-72707-0222 CDC\_EAR\_P R35\_\_\_\_\_\_0 CDC\_HPH\_REF CDC\_HPH\_REF CDC\_HPH\_L CDC\_HPH\_L CDC\_PDM0\_CLK (APQ GPIO\_63) CDC\_PDM\_CLK CDC\_HPH\_R CDC\_HPH\_R CDC\_PDM0\_SYNC (APQ GPIO\_64) CDC\_PDM\_SYNC CDC\_HS\_DET C96 C97 \_\_\_\_\_C170 CDC\_PDM0\_TX0 (APQ GPIO\_65) 470PF PF 470PF 470PF DNI DNI CDC\_PDM\_TX CDC\_PDM0\_RX0 CDC\_PDM0\_RX1 CDC\_PDM0\_RX2 (APQ GPIO\_66) CDC\_PDM\_RX0 CDC\_GND\_CP (APQ GPIO\_67) CDC\_PDM\_RX1 (APQ GPIO\_68) CDC\_HS\_DET \_1 CDC\_PDM\_RX2 CDC\_GND\_CFILT CDC\_NCP\_FLYP C73 CDC\_NCP\_FLYP CDC\_GND\_SPKDRV CDC\_NCP\_FLYN 1.0UF 10V CDC\_NCP\_FLYN CDC GND BOOST Connect C13, E14, A14, B13 pins to the main ground directly. CDC\_NCP\_VNEG CDC\_GND\_BOOST CDC\_NCP\_VNEG CDC\_PA\_VNEG CDC\_REF\_GND FB1 C72 $\overline{m}$

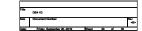
Delete ANALOG MIC Connector

1.0UF

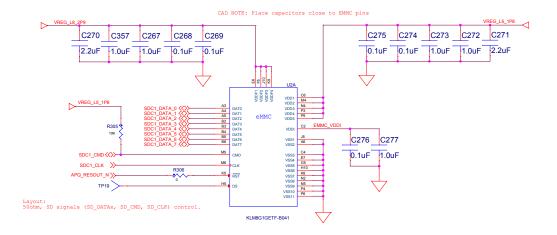
1200HM@100MHZ 112-18049-1201

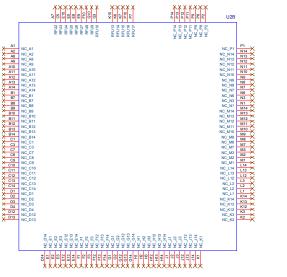
1.0UF

1.0UF 10V 2P0402R



# MEMORY - EMMC

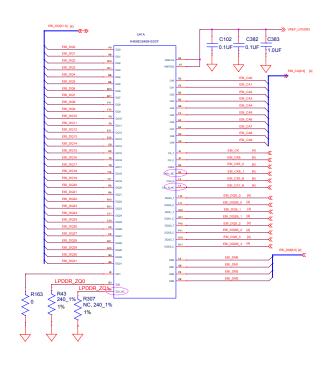


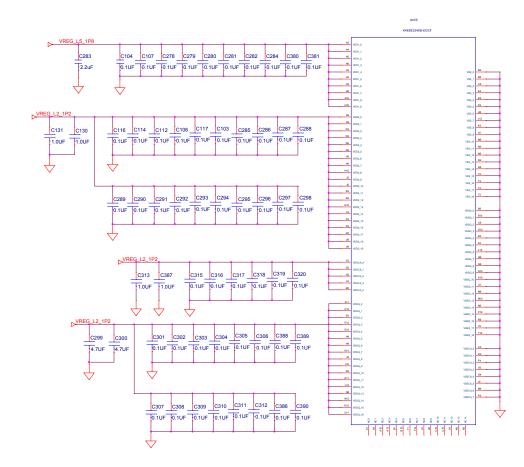


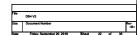
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Size	Document Number				R	ev <b></b>
Date:	Friday Sentember 20 2019	Sheet	21	nf.	35	

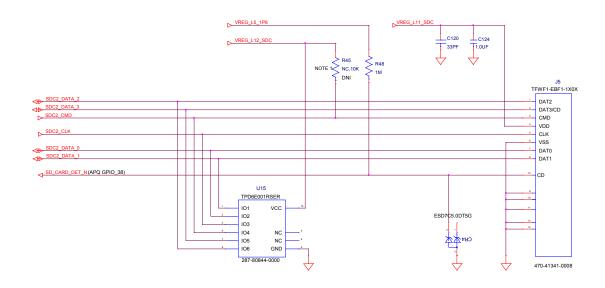
# **MEMORY - LPDDR3**







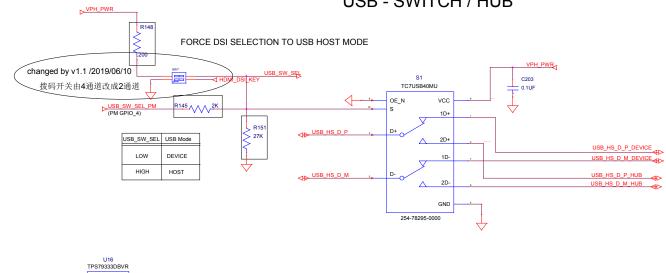
## **MEMORY - uSD CONNECTOR**

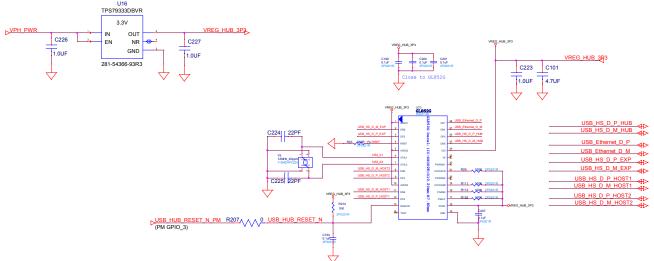


CARD DETECT	CASE	CD O
CARD NOT INSTALLED	CD-COMMON SW=OF	F
CARD INSTALLED	CD-COMMON SW=ON	COMMON O



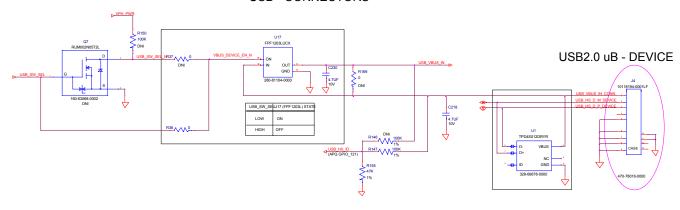
## USB - SWITCH / HUB



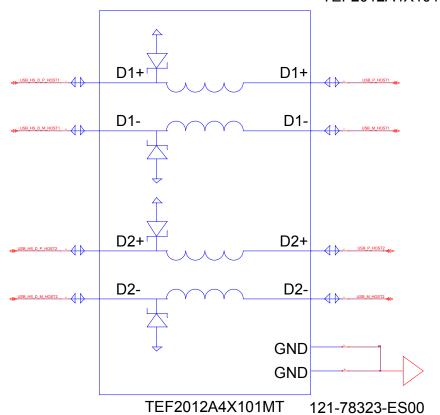


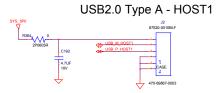




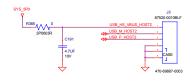


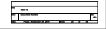
FL3 TEF2012A4X101MT



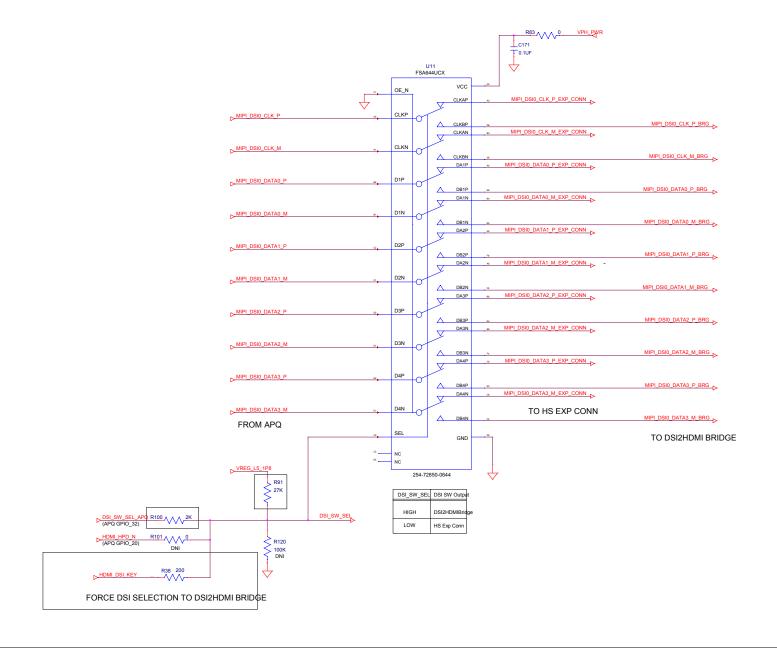


USB2.0 Type A - HOST2



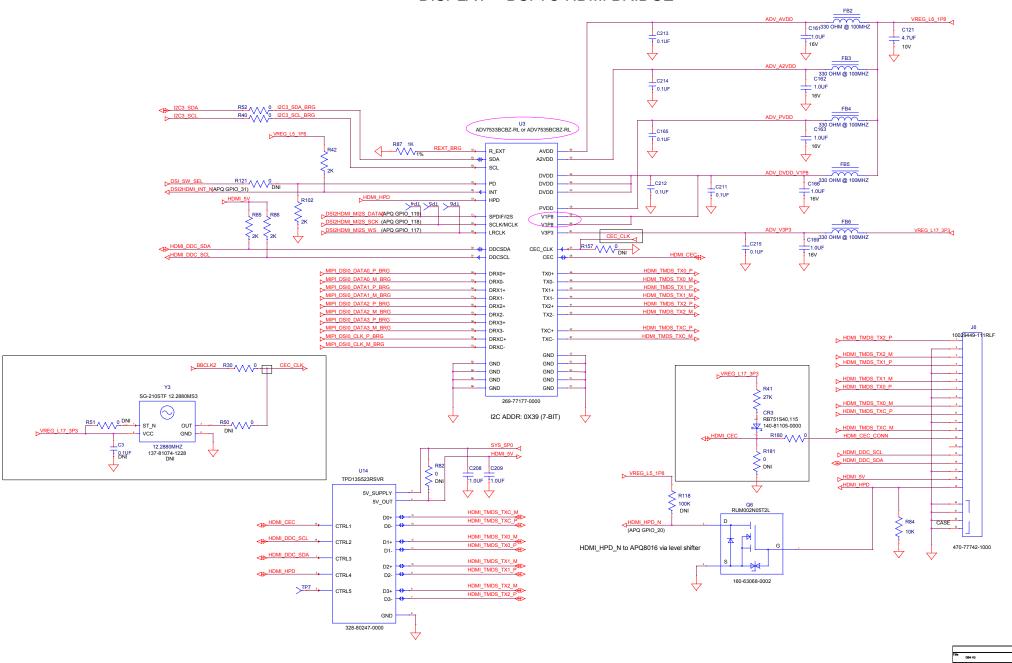


## **DISPLAY - DSI SWITCH**

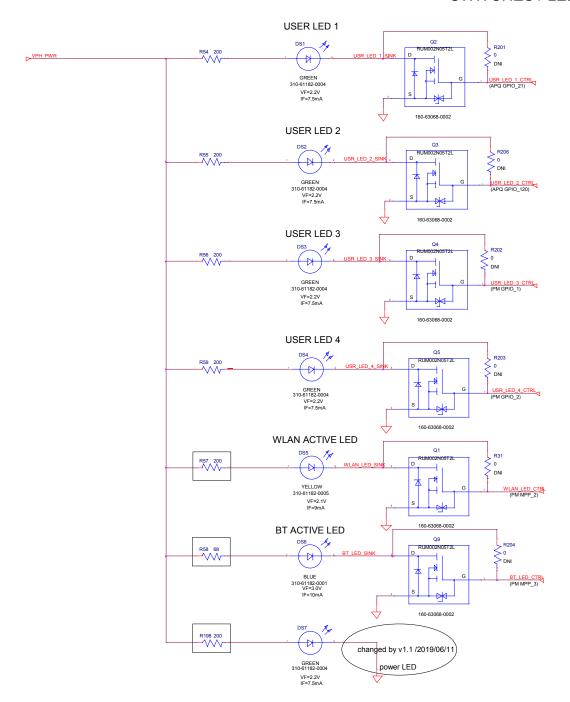


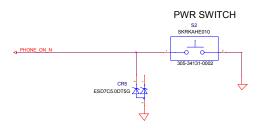


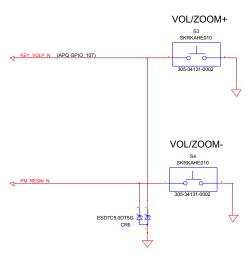
## **DISPLAY - DSI TO HDMI BRIDGE**



## SWITCHES / LEDS



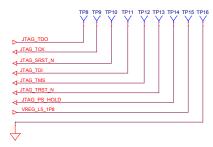




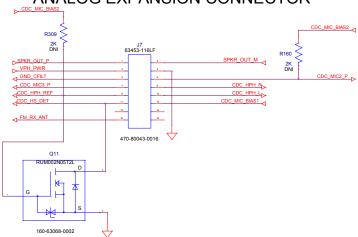


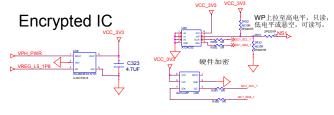
## JTAG / UART / ANALOG EXPANSION CONNECTORS

## JTAG INTERFACE (TOP)

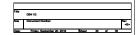


## ANALOG EXPANSION CONNECTOR



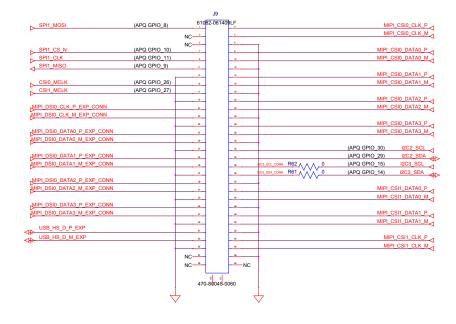


changed by v1.1 /2019/06/11

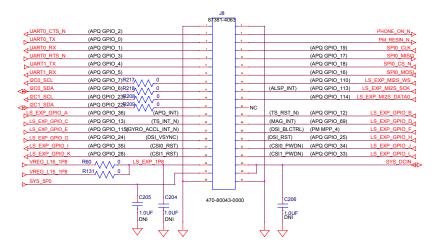


## LS / HS EXPANSION CONNECTORS

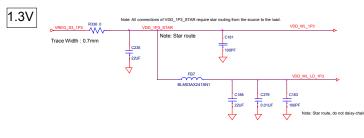
## HS EXPANSION CONNECTOR

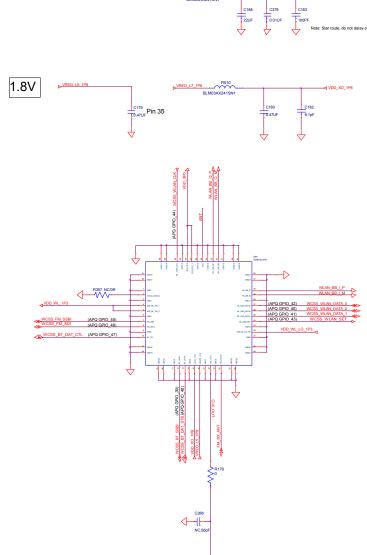


## LS EXPANSION CONNECTOR



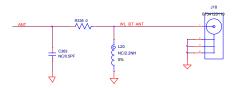


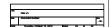












## WGR7640 - GPS

