

Article

A Compact Output Power Combiner for Broadband Doherty Power Amplifiers

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Abstract: A novel compact output power combiner for broadband Doherty Power Amplifiers is proposed in this paper. The proposed output power combiner avoids the use of quarter-wave impedance transformers as they are sizable and work over narrow bandwidths. Instead, the proposed combiner utilizes a distributed Brune Section to implement a compact broadband impedance inverter. The final area of the proposed output combiner is $\lambda^2/48$. When compared to the conventional broadband Doherty structure, which has an approximate area of $\lambda^2/16$, this structure offers an approximate size reduction of 67%. The proposed combiner is verified by using it in the design of a broadband Doherty power amplifier with an operating bandwidth of 1.7 GHz to 3.4 GHz. The saturated output power varies from 39.2 to 40.4 dBm with a peak power drain efficiency ranging from 58% to 66%. The drain efficiency at 6 dB Output Power Back-Off (OPBO) varies from 37.4% to 45% over an octave.

Keywords: Doherty Power Amplifier; Distributed Brune Section; Broadband Matching; Drain Efficiency

1. Introduction

The Doherty Power Amplifier (DPA) is an efficiency enhancement scheme which addresses efficiency at Output Power Back-Off (OPBO) and saturation simultaneously. Doherty Power Amplifiers utilize active loadpull to increase efficiency at OPBO. The standard DPA consists of two amplifiers and an Impedance Inverting Network (IIN). This implementation is narrowband by nature due to the fact that the IIN is usually implemented with a quarter-wave transmission line. Recent reports of broadband DPAs have been published [1–4]. Some of the broadband methods include the use of a lumped element equivalent of the quarter-wave IIN to absorb the output device capacitance of the amplifiers [5]. A Transformer-Less Load Modulated scheme was also proposed [6]. This method uses a combination of Tee and Pi three-element networks to construct the output power combining network. Since the Tee and Pi networks are inherently narrowband, the increase in bandwidth is modest. The conventional broadband Doherty architecture, which uses two quarter-wave transformers, is presented in Figure 1. Broadband behavior is achieved by reducing the Impedance Transformation Ratio (ITR) for the quarter-wave line connecting the Main and Auxiliary amplifiers [7,8].

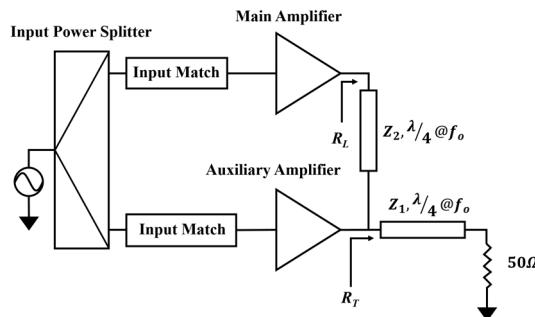


Figure 1. Simplified schematic of the conventional broadband Doherty Power Amplifier.

In this paper, a novel compact broadband output power combiner for Doherty Power Amplifiers is presented (Figure 2). The conventional power combining structure is compacted by replacing the two quarter-wave impedance transformers with a smaller broadband IIN structure. Section 2 describes the methods and materials used to design the DPA. In Section 3, the design of the broadband output power combiner is described. First, the design of the Main Amplifier portion of the output combiner is addressed. This includes the introduction of the equivalent circuit for the broadband K-Inverter, its distributed realization, and the final circuit for this portion of the output combiner. Next, the Output Matching Network (OMN) for the Auxiliary amplifier is discussed, and finally, the total output combiner is presented. In Section 4, the proposed output power combiner is verified by incorporating it into the design of a broadband Doherty Power Amplifier which operates from 1.7 GHz to 3.4 GHz.

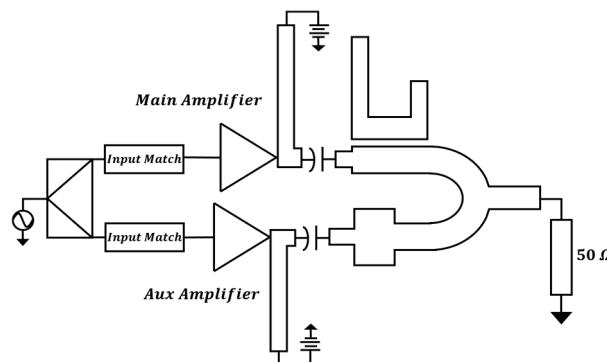


Figure 2. Proposed Doherty Output Combiner.

2. Materials and Methods

The proposed output power combiner was validated by implementing it in the design of a broadband Doherty Power Amplifier with a target frequency range of 1.7 to 3.4 GHz. The design uses Qorvo Semiconductor TGF2023-02 bare die GaN transistors for both the Main and Auxiliary amplifiers. The transistor for the Main amplifier is biased as a class A-B amplifier. The gate voltage is -2.8 V and the drain voltage was set to 28 V. The transistor for the Auxiliary amplifier was biased in class B mode with a gate voltage set to -3.6 V and the drain voltage set to 28 V. The nominal output power for this device when tuned for efficiency is 9.33 Watts with an average power gain of 17.1 dB. The output power combiner, input Wilkinson Power splitter, and input matching circuitry were implemented on Rogers 6002 high-frequency laminate.

The nonlinear simulation models for the Qorvo devices were provided by Modelithics. Simulated loadpull contours were used to determine the load values for power and efficiency at OPBO and output power saturation levels.

3. Circuit Design

A functional diagram of the proposed output power combiner is presented in Figure 3. The circuit was designed based on the impedance requirements for each of the amplifiers at OPBO and at output power saturation. The upper portion of the output combiner is the Main Amplifier output structure which transforms the current modulated load impedance, Z_{Load_Main} , into the optimum loads, Z_{opt_OPBO} and Z_{opt_Sat} . This section consists of a K-Inverting network which provides impedance inversion and an OMN which is required to absorb the parasitic drain capacitance. Since the K-Inverter provides the same functionality as the IIN, the two terms are used interchangeably in this paper. The optimum impedances Z_{opt_OPBO} and Z_{opt_Sat} are the load values required to optimize Power Added Efficiency (PAE) at OPBO and at output power saturation. The lower portion of the output combiner is the Auxiliary Amplifier output structure which transforms the active load, Z_{Load_Aux} , into the optimum impedance, Z_{opt_Sat} , at peak power levels and provides open circuit conditions at OPBO.

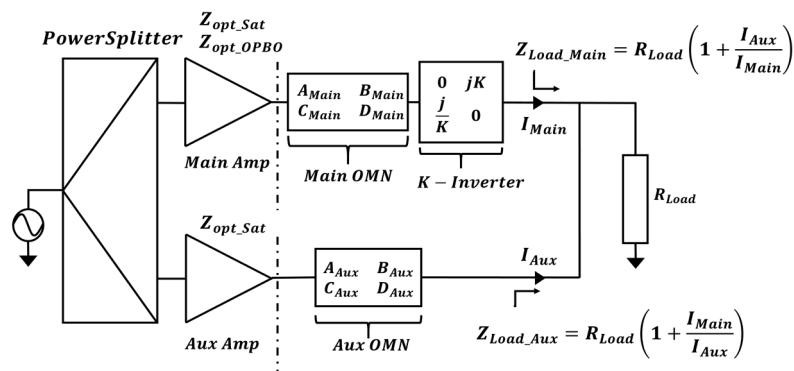


Figure 3. Simplified schematic of the proposed Doherty output combiner.

The design process for this DPA includes an initial design based on separation of the two amplifiers into subcircuits using equivalent modulated loads for each branch. This process was outlined in reference [9]. The initial assumption is that the modulating currents, I_{Main} and I_{Aux} , are in phase at the junction node and produce real impedances. This initial assumption is sufficient to produce the structure of the OMNs and the K-Inverter along with their initial characteristic impedances and electrical lengths. A final optimization is required to minimize the loading effects which occur when the subcircuits are joined. These loading effects manifest themselves as a phase mismatch between I_{Main} and I_{Aux} along with variation in their ratio. These effects introduce an imaginary component to the modulated active loads Z_{Load_Main} and Z_{Load_Aux} which varies with frequency.

3.1. K-Inverter Design

The K-Inverter used in most Doherty Power Amplifier designs is typically a quarter-wave transformer. For this design, the quarter-wave transformer was replaced by a broadband K-Inverting structure (see Figure 4). The equivalent circuit for the new K-Inverter is shown in Figure 4b. The 2-Port equivalent circuit consists of two transmission lines and a reactive Tee network.

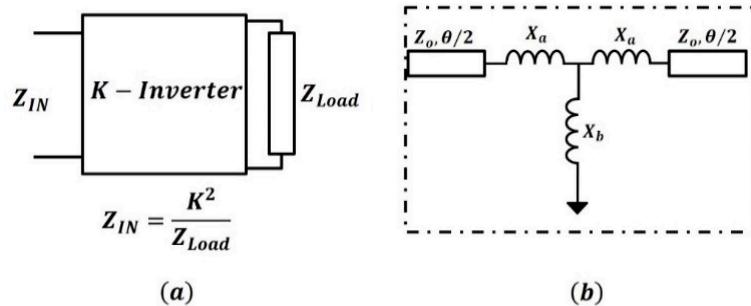


Figure 4. (a) Impedance relationship for the K-Inverter. (b) Equivalent circuit for the broadband K-Inverter.

The behavior of the 2-Port network is best described using the concept of image impedance and image phase. For a symmetrical 2-Port network, the image impedance is the load value required to produce an identical impedance value at the input port. The image phase is the delay a signal experiences when propagating through a 2-Port terminated with the image impedance. The image impedance and phase of the 2-Port are equivalent to the characteristic impedance and electrical length of a uniform transmission line. The structure in Figure 4b behaves as an IIN provided that the image impedance is real over the band of interest and the image phase is an odd multiple of $\pm\pi/2$. The conditions which guarantee this behavior are outlined in reference [9,10]. When these conditions are met, the input impedance is expressed as a function of the load and image impedance, K.

$$Z_{IN} = \frac{K^2}{Z_{Load}} \quad (1)$$

The design equations for the image impedance and the electrical transmission line lengths for the equivalent circuit are as follows:

$$K = Z_o \left| \tan \left(\frac{\theta}{2} + \tan^{-1} \frac{X_a}{Z_o} \right) \right|, \quad (2)$$

$$\theta = -\tan^{-1} \left(\frac{2X_b}{Z_o} + \frac{X_a}{Z_o} \right) - \tan^{-1} \frac{X_a}{Z_o}. \quad (3)$$

The relationship between the normalized characteristic impedance, K/Z_o , and the electrical length, θ , is given in Figure 5. By examining this figure, some insight can be gained as to why the K-Inverter equivalent circuit leads to a compact structure. If we compare the uniform transmission line implementation of the IIN to the proposed implementation in Figure 4b, both implementations require a phase delay of $\pi/2$ to operate as an impedance inverter. For the transmission line implementation, this requires a quarter-wave line which is lengthy at lower frequencies. However, for the proposed structure, a phase delay of $\pi/2$ is guaranteed provided the equivalent circuit elements X_a , X_b , Z_o , and θ satisfy the equations presented above. For this design, the normalized image impedance, K/Z_o , is 1.1. From Figure 5, we see that this value can be obtained using θ values ranging from 18° to 43° . The transmission line lengths used in the K-Inverter equivalent circuit are $\theta/2$; therefore, the range of electrical length values needed to implement the circuit in Figure 4b is 9° to 21.5° . Since the electrical lengths used in the equivalent model largely determine the size of the distributed realization of the broadband K-Inverter, significant reductions in the output combiner size are achieved.

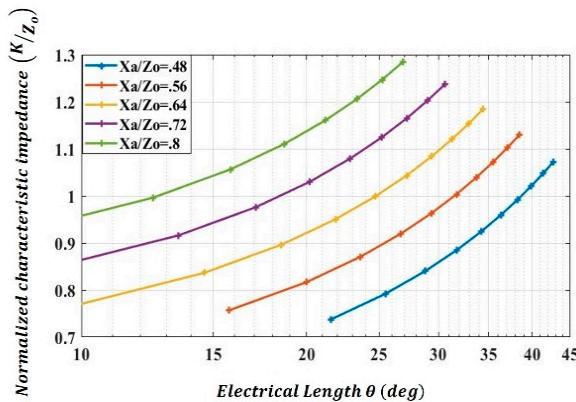


Figure 5. Normalized characteristic impedance, K/Z_0 , versus the electrical line length, θ .

The solution to the above equations uses positive values for the series reactive element, X_a , and a negative value for the shunt reactive element, X_b . This choice of element values leads to positive transmission line lengths and a more realizable circuit. However, the presence of the negative shunt reactive element is a problem when implementing the design using distributed elements. Fortunately, the Tee -Network used in the broadband K-Inverter is structurally similar to a Type-C Brune Section, which is a 2-Port network commonly used in filter design [11]. These structures are well documented and have several distributed realizations. Under certain conditions, the two reactive Tee networks are equivalent and the distributed realizations for the Brune Section can be applied. The reactive Tee-Networks for the equivalent K-Inverter and the Brune Section are given in Figure 6a,b along with the equations that link the two structures. A Coupled Inductor representation of the Brune Section, Figure 6c, is also included since the characteristic impedances for the distributed realization are given in terms of this model.

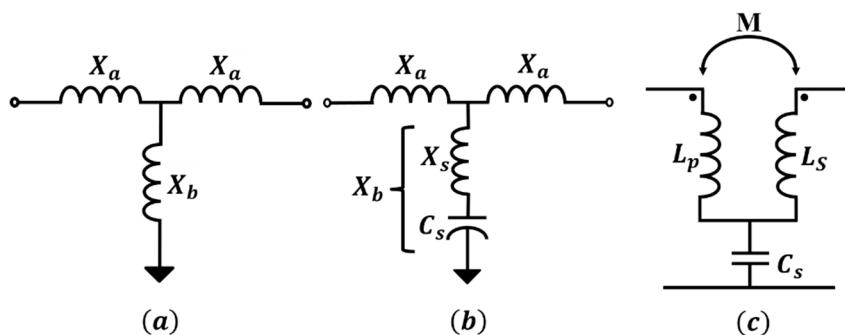


Figure 6. (a) Reactive Tee Network used in the K-Inverter equivalent from Figure 4b. (b) A Standard Brune Section. (c) Coupled Inductor representation of the Brune Section.

The Tee networks for the K-Inverter equivalent and Brune Section are similar except for the shunt elements. The shunt element for the Brune Section is the series inductor–capacitor combination, $X_s–C_s$, which determines the real frequency zero for the network. The relationship between the two shunt elements is expressed in terms of the inductances X_b , X_s , and the real frequency zero, ω_o , by

$$jX_b = jX_s \left(1 - \left(\frac{\omega_o}{\omega} \right)^2 \right), \quad (4)$$

$$\omega_o = \frac{1}{\sqrt{X_s C_s}}. \quad (5)$$

If the zero associated with the Brune Section is larger than the frequency of interest, then the effective shunt element appears negative and the series inductor–capacitor combination approximates

the negative shunt element, X_b , used in the K-Inverter network. In this frequency range, the Brune Section and the reactive tee network used in the broadband K-Inverter network are equivalent. This relationship limits the bandwidth of the proposed distributed implementation. The coupled inductor model for the Brune Section is shown in Figure 6c. The model comprises the primary and secondary windings, L_p and L_s , along with the mutual inductance, M .

$$L_p = L_s = X_a + X_s \quad (6)$$

$$M = X_s \quad (7)$$

These expressions, along with Equation (4), provide a clear link between the reactive Tee-Network and the impedance values for the distributed realization. This is illustrated in Figure 7.

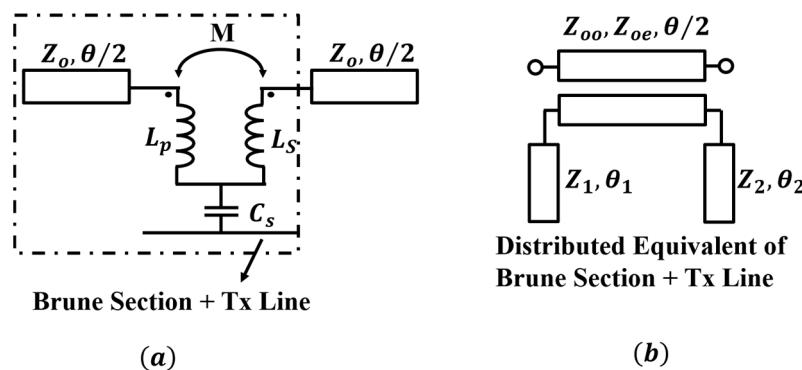


Figure 7. (a) K-Inverter equivalent circuit with Coupled Inductor Brune Section. (b) Distributed realization of the cascade connection of the Transmission Line element and the Coupled Inductor Brune element.

In Figure 7a, the equivalent circuit for the broadband K-Inverter is redrawn using the coupled inductor Brune Section model instead of the reactive tee network. The distributed realization of the outlined portion of this network is a coupled line structure loaded with open circuited stubs (Figure 7b). The equations for the even- and odd-mode characteristic impedances and the characteristic impedances of the open circuited stubs are given below [12,13]. Equations (8) and (9) are used to determine the even- and odd-mode characteristic impedances of the coupled structure. The electrical length of the coupled structure is the same as the length—the $\theta/2$ value used in the equivalent model in Figure 7a.

$$Z_b = \frac{Z_{oe} + Z_{oo}}{2} = Z_o + \frac{(L_p - M)^2}{L_p} \quad (8)$$

$$\frac{Z_{oe} - Z_{oo}}{2} = \sqrt{\frac{(L_p - M)(Z_o + L_p - M)(Z_b)}{L_p}} \quad (9)$$

The characteristic impedances for the open circuited stubs are given in Equations (9) and (10). The lengths for the stubs are adjusted to give the optimal performance over the desired bandwidth.

$$Z_1 = \frac{Z_o}{(L_p - M)} Z_b \quad (10)$$

$$Z_2 = \frac{(L_p - M - MC_s Z_o)}{L_p C_s (L_p - M + Z_o)} Z_b \quad (11)$$

3.2. Main Amplifier Matching

The initial design of the Main Amplifier portion of the power combiner starts with the half circuit equivalent presented in Figure 8. The amplifier is presented as a voltage-controlled current source with an output impedance and parasitic drain capacitance. Z_{opt_OPBO} and Z_{opt_Sat} are the desired impedances presented to the drain of the amplifier and Z_{out_Main} is the impedance looking into the Main Amplifier OMN. A reflection coefficient at the device–OMN interface was defined using the two impedances. The parameters which define the Main OMN were obtained by minimizing this reflection coefficient over the frequency band of interest. Referring to Figure 8, the output impedance, Z_{out_Main} , is defined in terms of Z_{Load_Main} , K, and the ABCD parameters associated with the Main OMN.

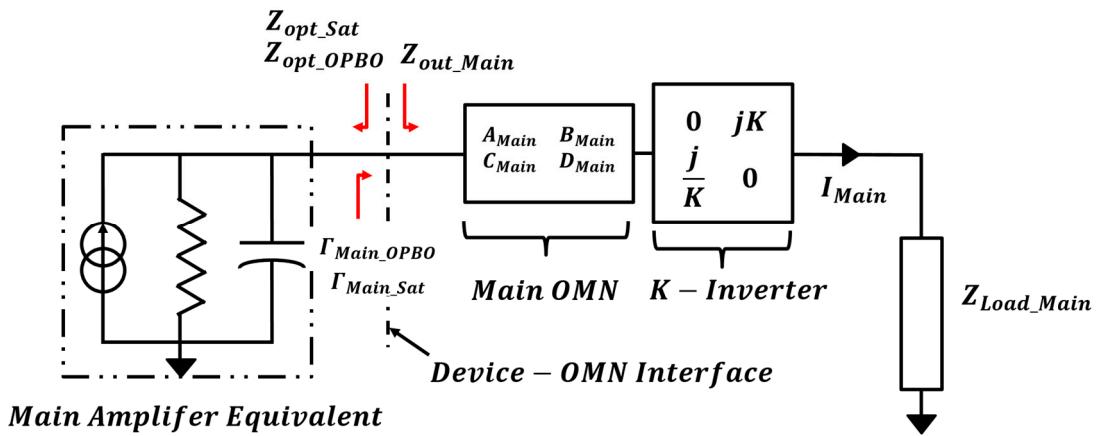


Figure 8. The half circuit equivalent for the Main Amplifier section of the Doherty Amplifier.

$$Z_{out_Main} = \frac{A_{Main} \left(\frac{K^2}{Z_{Load_Main}} \right) + B_{Main}}{C_{Main} \left(\frac{K^2}{Z_{Load_Main}} \right) + D_{Main}} \quad (12)$$

In Equation (12), Z_{Load_Main} is defined as

$$Z_{Load_Main} = R_{Load} \left(1 + \frac{I_{Aux}(\theta_{Aux})}{I_{Main}(\theta_{Main})} \right). \quad (13)$$

For the initial design, it was assumed that I_{Aux} and I_{Main} are in phase and the active load impedances are purely real. The Main OMN used in this design is a simple L-Network which provides compensation for the parasitic drain capacitance and DC bias for the device. The transmission matrix for this network is given as

$$\begin{bmatrix} A_{Main} & B_{Main} \\ C_{Main} & D_{Main} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-j \cot(\theta_4)}{Z_4} & 1 \end{bmatrix} \begin{bmatrix} \cos(\theta_3) & jZ_3 \sin(\theta_3) \\ \frac{j}{Z_3} \sin(\theta_3) & \cos(\theta_3) \end{bmatrix}. \quad (14)$$

These transmission matrix elements can be substituted into Equation (12) and used to define Z_{out_Main} .

$$Z_{out_Main} = \frac{Z_4 Z_3 K^2 \cos \theta_3 + j Z_4 Z_3^2 Z_{Load_Main} \sin \theta_3}{Z_{Load_Main} (Z_4 Z_3 \cos \theta_3 + Z_3^2 \sin \theta_3 \cot \theta_4) + j K^2 (Z_4 \sin \theta_3 + Z_3 \cos \theta_3 \cot \theta_4)} \quad (15)$$

The reflection coefficients at the device–Main OMN interface are defined in Equation (16) for the OPBO and output power saturation cases. These reflection coefficients are a function of the optimum impedances, Z_{opt_OPBO} and Z_{opt_Sat} , along with the output impedance Z_{out_Main} . Γ_{Main_OPBO}

and Γ_{Main_Sat} are minimized by selecting the proper output impedance values, which are influenced by the L-Network variables Z_3 , θ_3 , Z_4 , and θ_4 .

$$\Gamma_{Main_OPBO} = \frac{Z_{opt_OPBO} - Z_{out_Main}}{Z_{opt_OPBO} + Z_{out_Main}}; \quad \Gamma_{Main_Sat} = \frac{Z_{opt_Sat} - Z_{out_Main}}{Z_{opt_Sat} + Z_{out_Main}} \quad (16)$$

The initial implementation of the Main Amplifier portion of the output combiner is given in Figure 9 and the simulated output impedances for this structure are given in Figure 10.

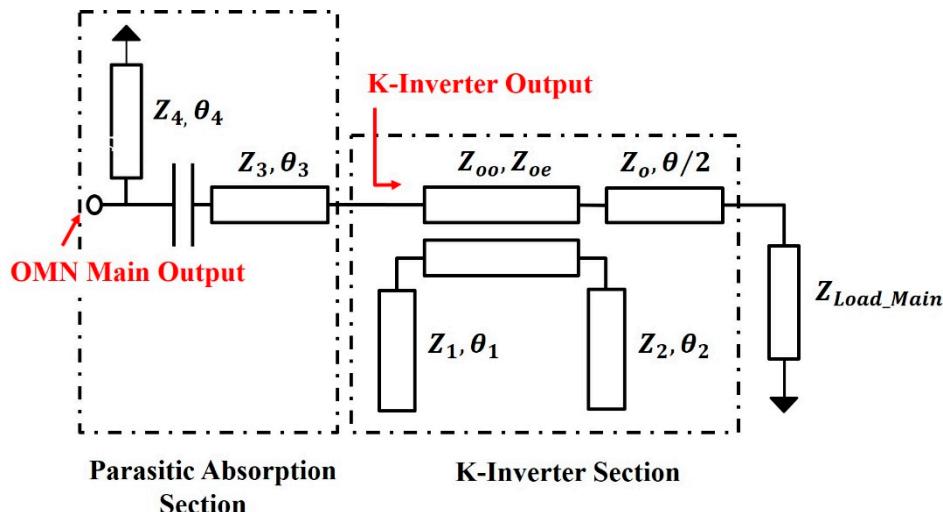


Figure 9. Main Amplifier portion of the output power combiner.

These impedance values were generated by simulating the response of the structure in Figure 9 to the discrete Z_{Load_Main} values of 50Ω , 67Ω , 85Ω , and 100Ω ; these discrete load values represent the active load values at 6 dB OPBO , 3.5 dB OPBO , 1.5 dB OPBO , and output power saturation, respectively.

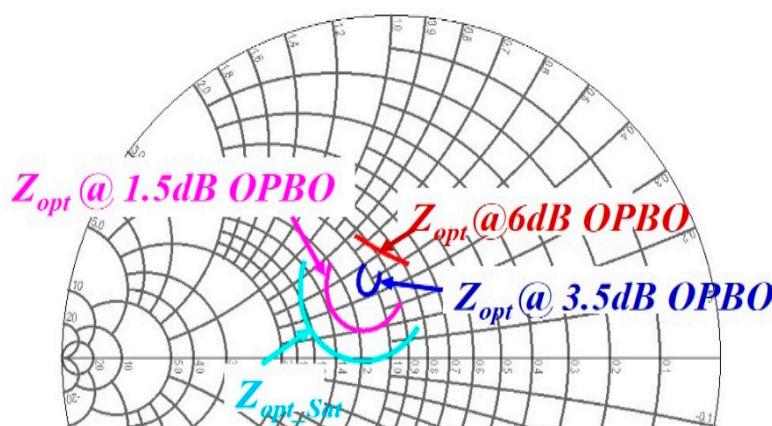


Figure 10. Simulated response of the Main Amplifier portion of the output combiner.

The simulated load values at the output of the OMN can be compared to the range of simulated loadpull values at each of the output power back-off points (Table 1a). The Simulated Loadpull Results table consists of the min and max values for the real and imaginary parts of the load admittance which produce acceptable efficiency at each of the OPBO levels. The load definitions are given below.

$$Y_{Load} = G_L + jB_L \quad (17)$$

$$G_{Min} \leq G_L \leq G_{Max} \quad (18)$$

$$B_{Min} \leq B_L \leq B_{Max} \quad (19)$$

These values were determined by noting the intersection of the Power and Efficiency contours at the discrete OPBO points and were further restricted by limiting the load Q to values corresponding to the desired bandwidth of the DPA. The range of simulated load values generated at the output of the matching network is displayed on the Smith Chart in Figure 10 and presented in Table 1b. The comparison of the two tables validates the design of the Main Amplifier portion of the output combiner.

Table 1. Min and Max values for the load admittance, $Y_{Load} = G_L + jB_L$. (a) Load limits extracted from simulated Loadpull. (b) Min and Max load values for the circuit in Figure 9.

(a)				
Simulated Loadpull Results				
6 dB OPBO	G_{Min}	G_{Max}	B_{Min}	B_{Max}
6 dB OPBO	0.014	0.018	0.0064	0.0136
3.5 dB OPBO	0.016	0.022	0.006	0.014
1.5 dB OPBO	0.02	0.022	0.002	0.014
P_{sat}	0.024	0.03	0.002	0.014

(b)				
Simulate Results for Main Amplifier				
6 dB OPBO	G_{Min}	G_{Max}	B_{Min}	B_{Max}
6 dB OPBO	0.016	0.018	0.008	0.014
3.5 dB OPBO	0.019	0.022	0.008	0.01
1.5 dB OPBO	0.018	0.028	0.006	0.008
P_{sat}	0.017	0.028	0.002	0.0144

3.3. Auxiliary Amplifier Matching

The half circuit equivalent for the Auxiliary Amplifier is given in Figure 11. The process of determining the impedance transformations for the Auxiliary amplifier at OPBO and output power saturation is described below. First, a reflection coefficient was defined at the device–OMN interface and used to determine the network values for the Aux OMN.

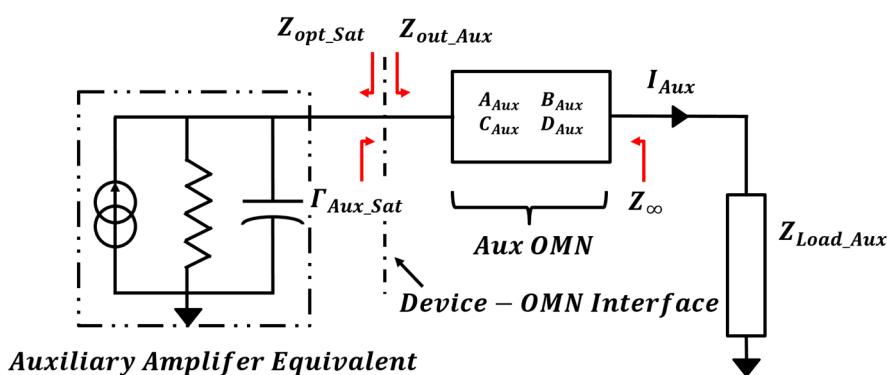


Figure 11. The half circuit equivalent for the Auxiliary Amplifier section of the Doherty Amplifier.

The proposed matching network must meet the load requirements for the Auxiliary amplifier at OBPO and output power saturation. At OPBO levels, the Auxiliary amplifier is off and should appear as an open circuit at the summing node. At output power saturation levels, the load impedance is matched

to the optimum load value. The impedance looking into the OMN was defined as Z_{out_Aux} and the equation is given in terms of the modulated load and the ABCD parameters for the matching network.

$$Z_{out_Aux} = \frac{A_{Aux}(Z_{Load_Aux}) + B_{Aux}}{C_{Aux}(Z_{Load_Aux}) + D_{Aux}} \quad (20)$$

The modulated load impedance for the Auxiliary Amplifier is given in terms of the current ratio at the junction node and the system load impedance.

$$Z_{Load_Aux} = R_{Load} \left(1 + \frac{I_{Main}}{I_{Aux}} \right) \quad (21)$$

Finally, the reflection coefficient at the Auxiliary device–OMN interface is defined. Proper choice of the transmission matrix elements minimizes this function and meets the load requirements at output power saturation.

$$\Gamma_{Aux_Sat} = \frac{Z_{opt_Sat} - Z_{out_Aux}}{Z_{opt_Sat} + Z_{out_Aux}} \quad (22)$$

To meet the load requirements at OPBO, the impedance looking into Aux OMN at the Z_{Load_Aux} end of the network must appear as an open circuit. This impedance is denoted as Z_∞ and can be expressed in terms of the transmission matrix element for Aux OMN and cold-fet impedance of the Auxiliary device, Z_{Aux_Cold} .

$$Z_\infty = \frac{D_{Aux}Z_{Aux_Cold} - B_{Aux}}{A_{Aux} - C_{Aux}Z_{Aux_Cold}} \quad (23)$$

The network parameters for Aux OMN were determined by satisfying Equations (22) and (23) simultaneously. A shunt transmission line and a stepped impedance network were used to implement this matching network, Figure 12.

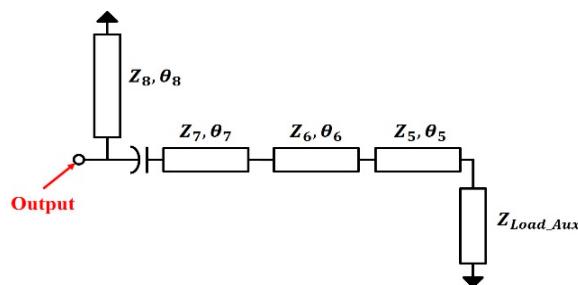


Figure 12. Auxiliary Amplifier portion of the output combiner.

3.4. Optimization of the Complete Power Combiner

The design process described above assumes that the Main and Auxiliary currents are in phase. However, joining the matching networks changes the phase of the two currents at the junction node, which, in turn, changes the modulated loads Z_{Load_Main} and Z_{Load_Aux} by introducing an imaginary component. The half circuit equivalents for the Main and Auxiliary amplifiers can be used to generate expressions for the junction currents in terms of phase. The drain voltage and current for the main device was defined by introducing the total transmission matrix.

$$\begin{bmatrix} V_{drain} \\ I_{drain} \end{bmatrix} = \begin{bmatrix} A_{Tot_Main} & B_{Tot_Main} \\ C_{Tot_Main} & D_{Tot_Main} \end{bmatrix} \begin{bmatrix} R_{Load}(I_{Main} + I_{Aux}) \\ I_{Main} \end{bmatrix} \quad (24)$$

The total transmission matrix was constructed from the K-Inverter, OMN for the Main amplifier, and the parasitic drain capacitance and output impedance blocks.

$$\begin{bmatrix} A_{Tot_Main} & B_{Tot_Main} \\ C_{Tot_Main} & D_{Tot_Main} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1+j\omega RC}{R} & 1 \end{bmatrix} \begin{bmatrix} A_{Main} & B_{Main} \\ C_{Main} & D_{Main} \end{bmatrix} \begin{bmatrix} 0 & jK \\ \frac{j}{K} & 0 \end{bmatrix} \quad (25)$$

The expression for the junction current, I_{Main} , was obtained from Equation (24) and is given below. By examining Equation (26), it is clear that the phase dependency of I_{Main} is a function of the network elements and the parasitic drain capacitance.

$$I_{Main}(\theta) = \frac{I_{Drain} - C_{Tot_Main} R_{Load} I_{Aux}(\theta)}{C_{Tot_Main} R_{Load} + D_{Tot_Main}} \quad (26)$$

Similar results are presented for the Auxiliary amplifier, and the expression for the junction current, I_{Aux} is given.

$$\begin{bmatrix} V_{Drain} \\ I_{Drain} \end{bmatrix} = \begin{bmatrix} A_{Tot_Aux} & B_{Tot_Aux} \\ C_{Tot_Aux} & D_{Tot_Aux} \end{bmatrix} \begin{bmatrix} R_{Load}(I_{Main} + I_{Aux}) \\ I_{Aux} \end{bmatrix} \quad (27)$$

$$\begin{bmatrix} A_{Tot_Aux} & B_{Tot_Aux} \\ C_{Tot_Aux} & D_{Tot_Aux} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1+j\omega RC}{R} & 1 \end{bmatrix} \begin{bmatrix} A_{Aux} & B_{Aux} \\ C_{Aux} & D_{Aux} \end{bmatrix} \quad (28)$$

$$I_{Aux}(\theta) = \frac{I_{Drain} - C_{Tot_Aux} R_{Load} I_{Main}(\theta)}{C_{Tot_Aux} R_{Load} + D_{Tot_Aux}} \quad (29)$$

By examining Equations (26) and (29), it is reasonable to conclude that the phase difference between the junction currents is produced by the difference in electrical lengths between the main and auxiliary portions of the output power combiner. The phase difference was minimized in the final design by simulating the entire output power combiner and optimizing the characteristic impedances and electrical lengths of the transmission line elements. The synthesized matching networks, along with a simplified schematic of the Main and Auxiliary devices, were used as part of the final optimization schematic (Figure 13). The output impedance, drain capacitance, and drain current make up the output equivalent circuits for the Main and Auxiliary devices. A Data Acquisition Component provides the equivalent circuit values at each OPBO point and at discrete frequencies. Current probes were placed at the summing junction to monitor I_{Main} and I_{Aux} . The ratio of the two currents was added to the list of parameters to optimize. The network parameters were adjusted to minimize the imaginary part of this ratio while still maintaining the proper current ratios and the impedance requirements for the Main and Auxiliary amplifiers over the frequency of interest and at each OPBO level.

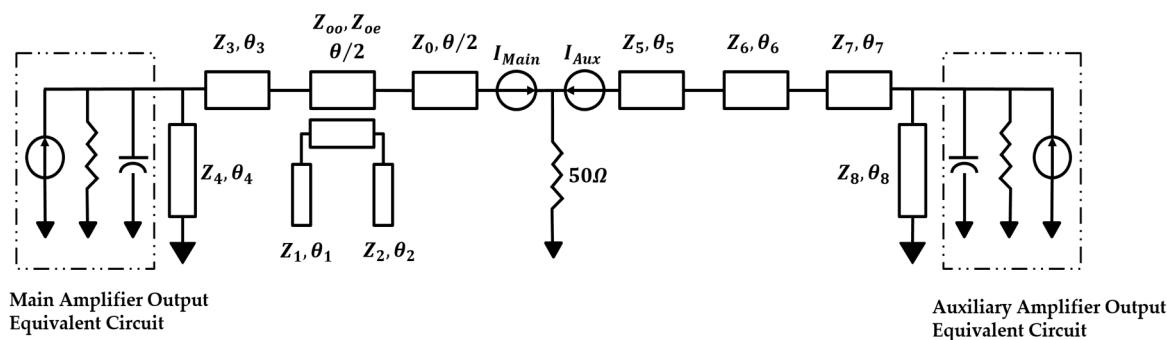


Figure 13. Final schematic used to optimize the complete output power combiner.

4. Measurement Results

The final schematic for the proposed output combiner and a photo of the fabricated Doherty PA are given in Figures 14 and 15. The dimensions of the final output power combiner are $\lambda/12$ by $\lambda/4$. This size represents a 67% reduction in size when compared to the standard broadband configuration.

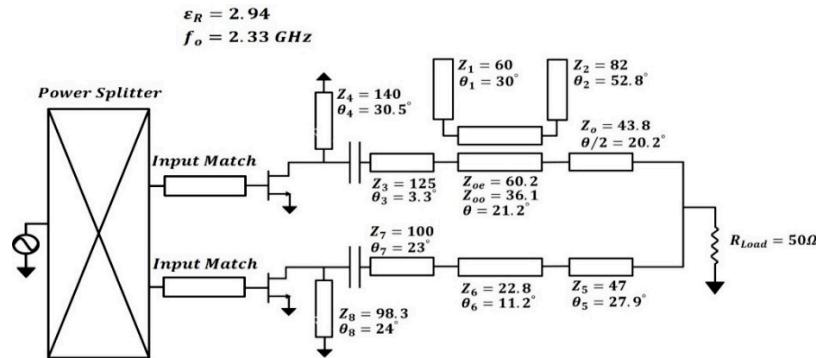


Figure 14. Schematic for the proposed Doherty output power combiner.

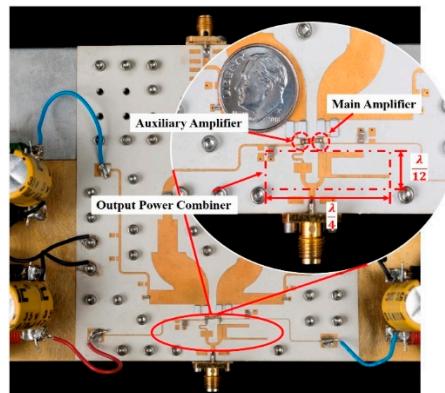


Figure 15. Photo of the fabricated Doherty Amplifier.

The simulated and measured results for the drain and power-added efficiency (PAE) were taken from 1.7 GHz to 3.4 GHz. The results show good drain efficiency and PAE between 1.7 GHz and 3.4 GHz for a fractional bandwidth of approximately 70%. The simulated PAE versus P_{out} results are presented in Figure 16. The results at 6 dB OPBO range from 44% to 52% and the peak PAE values range from 60% to 68% over the frequency of interest.

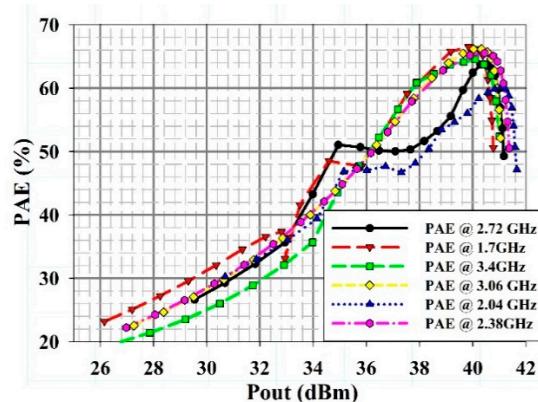


Figure 16. Simulated power-added efficiency (PAE) versus P_{out} for the proposed Doherty output combiner.

The noticeable lack of an efficiency peak at OPBO is a result of the tradeoff made between bandwidth extension for the DPA and achieving maximum PAE in the OPBO region. The lower Q loads at OPBO are necessary for extending the bandwidth of DPAs; however, they result in the disappearance of a pronounced PAE peak at OPBO. The measured PAE versus P_{out} values are given in Figure 17 and show values ranging from 37.4% to 44.3% at OPBO and 57.5% to 66% at saturation.

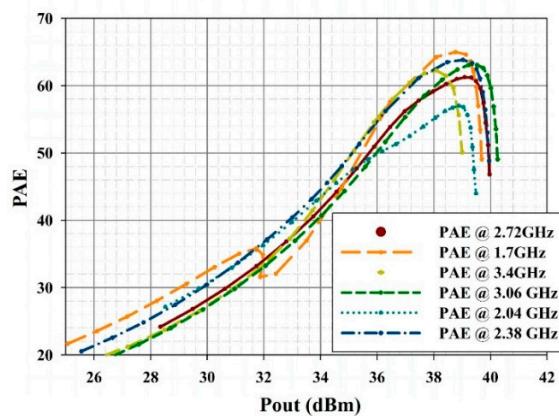


Figure 17. Measured PAE versus P_{out} for the final Doherty Power Amplifier.

The measured output power ranges from 39.2 dBm to 40.4 dBm. Figure 18 shows the drain efficiency results at 6 dB OPBO and output power saturation over the operating bandwidth for the DPA. At 6 dB OPBO, the drain efficiency average is 40.89% and its range is 37.4% to 45%. At output power saturation, the drain efficiency range is 58% to 66%.

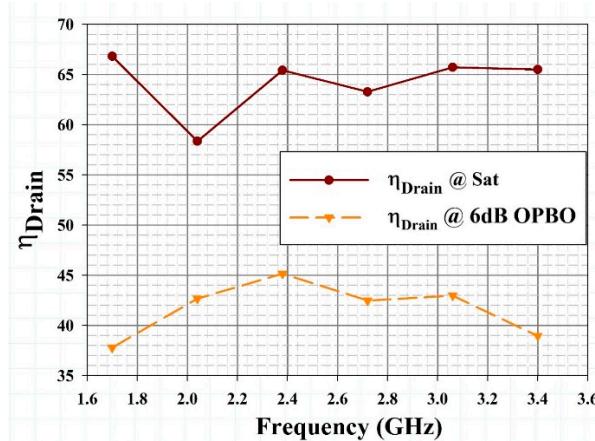


Figure 18. Measured drain efficiency at 6 dB OPBO and output power saturation for frequencies between 1.7 GHz and 3.4 GHz.

The power amplifier gain and input reflection coefficient curves are included in Figures 19 and 20 and show that the power amplifier exhibits broadband characteristics.

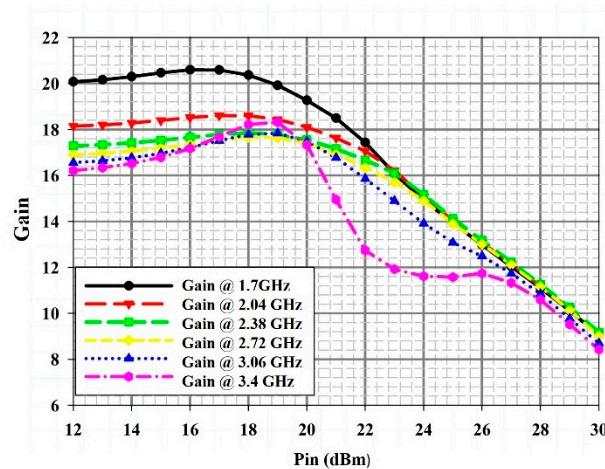


Figure 19. Measured Gain (dB) versus P_{in} (dBm) for the Doherty Amplifier in Figure 16.

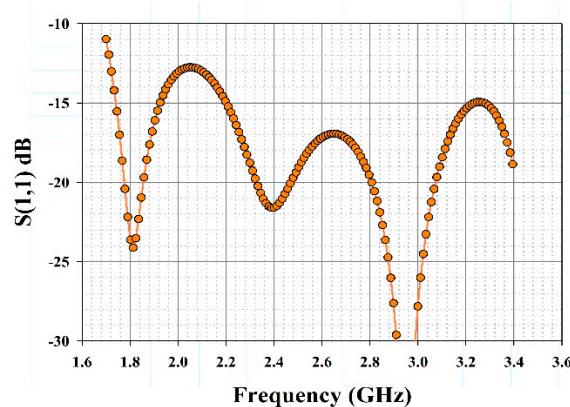


Figure 20. Input reflection coefficient for the fabricated Doherty Amplifier.

Finally, Adjacent Channel Power Ratio (ACPR) measurements were performed at carrier frequencies of 1.7 GHz, 2.38 GHz, and 3.4 GHz. A 16 QAM WCDMA signal with a 40 MHz bandwidth and a 6.5 dB Peak to Average Power Ratio (PAPR) was used. An EXG Vector Signal Generator (N5172B) and a Digital Signal Analyzer (DSA90404A) were used to make the measurements. The results of the measurement are shown in Figure 21.

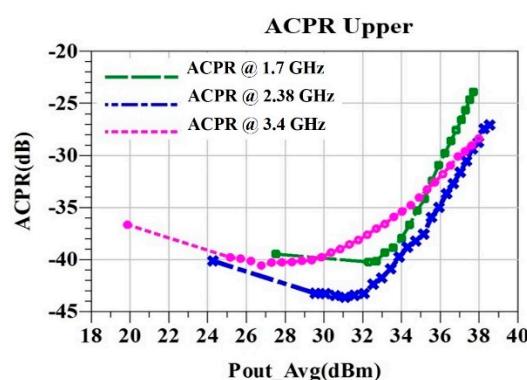


Figure 21. Adjacent Channel Power Ratio (ACPR) measurements for the fabricated Doherty Amplifier. The amplifier is driven by a 16 QAM WCDMA signal with a 40 MHz bandwidth and a Peak to Average Power Ratio (PAPR) of 6.5 dB.

Table 2 is a comparison of the DPA performances presented in the reference list. The designs reported in references [2] and [7] are the closest in fractional bandwidth and provide the best comparison. The design present in reference [2] has a larger fractional bandwidth of 83% and slightly higher efficiency at 6 dB OPBO. The efficiency at output power saturation levels is comparable. However, the structure combining output power in this design is a coupler-like structure employing four $\lambda/4$ transmission lines and is quite large. The design presented in reference [7] is an implementation of the standard broadband Doherty structure shown in Figure 1 which utilizes two $\lambda/4$ structures. The efficiency at back-off and saturation are slightly better. The operating frequency for this design is much lower and would account for the better device performance and improved efficiency. The proposed DPA achieves comparable fractional bandwidth and efficiency performance while using a significantly smaller output combining structure.

Table 2. Performance comparison.

Ref	Frequency(GHz)	Power (dBm)	Saturation DE (%)	6 dB OPBO DE (%)
[2]	1.0–2.5	40–41	45–83	35–58
[3]	0.7–0.95	43	48–56	38–45
[4]	1.4–2.6	41.5–44	58–72	40–51
[7]	0.55–1.1	42–43.5	56–72	40–52
[8]	1.6–2.6	≥ 41.7	50.8–54	41.5–45
This work	1.7–3.4	39.2–40.4	57.5–66	37.4–44.3

5. Conclusions

A compact output combiner for broadband Doherty Amplifiers was presented in this paper. The design and distributed realization of the compact structure was discussed. Finally, the proposed output combiner was verified by using it in the design of a broadband Doherty Power Amplifier. A drain efficiency ranging from 38% to 45% was achieved at OPBO for an octave bandwidth. The final size of the output power combiner is $\lambda^2/48$, which is an approximate reduction in size of 67% when compared to the standard broadband structure.

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