Article

Analysis, Design, and Experimental Validation of a Primary Side Current-Sensing Flyback Converter for Use in a Battery Management System

Borislav Dimitrov [1],*, Muthu Krishna [1], Andrew Cruden [1], Suleiman Sharkh [1] and Ahmad Elkhateb [2] (ID)

[1] Faculty of Engineering and the Environment, University of Southampton, Southampton SO17 1BJ, UK; m.k.krishna91@gmail.com (M.K.); A.J.Cruden@soton.ac.uk (A.C.); S.M.Abu-Sharkh@soton.ac.uk (S.S.)

[2] School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast, Belfast BT7 1NN, UK; A.Elkhateb@qub.ac.uk

* Correspondence: B.H.Dimitrov@soton.ac.uk

check for updates

Abstract: The purpose of the presented flyback converter is to equalise the voltage between the cells in a series string within a battery pack providing an active cell-balancing system. This would be an important part of a battery management system (BMS) for charging li-ion batteries in electric vehicles. The converter is based on primary side current sensing, where the conventional feedback circuit is omitted. The purpose of this converter is to improve efficiency by decreasing losses and to increase battery power density by decreasing the number of elements which constitute the power electronics; these are important factors for the future development of electric vehicle battery packs. Analysis of the circuit and the design procedure of the DC-DC flyback converter with primary current sensing is presented in this paper. Finally, several experimental converters have been built and tested to validate the authors' approach.

Keywords: flyback; converter; battery management system; primary side current sensing; active cell balancing

1. Introduction

Electric vehicles are gaining significant interest as part of the solution for mitigating anthropogenic climate change and poor air quality in cities. The batteries to power these vehicles are the object of significant research [1–4] as multinational automobile manufacturers seek to grow their electric/hybrid vehicle range.

The battery management system (BMS) is an essential component of the on-board power electronics. Their primary purpose is safety, where the battery pack is prevented from over-charging or over-discharging. Additionally, they can be designed to ensure the long life of the battery pack by balancing the energy amongst the individual cells, and to provide information about the battery charge level or State of Charge (SoC).

Over the course of many charge/discharge cycles, the SoC of cells, and hence their respective voltages, connected in series within a string will become imbalanced [1–3]. This is caused by many unavoidable factors, such as slight differences during manufacture (i.e., no two cells are exactly alike), battery aging, temperature variations, and sudden changes in the energy. Eventually, such a mismatch causes an overall reduction in the battery capacity. It has been shown in [1] that for n cells connected in series, the overall string capacity depends on the cell with the lowest SoC. Active cell balancing is the term used to describe the process of transferring energy between the cells. In [5], a BMS with such balancing, based on a microcontroller and buck converter, is presented for two lead-acid batteries.

Several network communication systems used in different BMSs are given in [6–8] and important functional and thermal analysis, respectively, in [9,10].

An electronic DC-DC converter is necessary for the active cell-balancing schematic proposed in this paper. The purpose of this converter is to charge a single cell separately from the string when its voltage is under a defined threshold. The basic schematic is shown in Figure 1. This schematic is based on a specialised BMS circuit [4], which is used for the voltage measurement of each cell within a series string. When one cell has a lower voltage than the others within the same string (e.g., cell 4 in Figure 1), the DC-DC converter, controlled by the BMS, charges that cell separately from the rest of the string.

A flyback DC-DC converter with primary side current sensing was chosen due to these unique features: the feedback circuit is omitted, resulting in a system with fewer elements; good efficiency (75–85%) for this class of converters; galvanic electrical isolation between the primary and secondary side, which makes it possible for the converter to be powered from the vehicle battery; good power density, which is a basic requirement of the electric vehicle's on-board electronics; and it does not suffer from the current transfer ratio degradation that arises from the temperature rise found in low-cost optocouplers. Based on these advantages, this particular flyback converter has been the object of significant research. A primary side current regulation flyback converter used as a battery charger is shown in [11]. The design procedure is well-explained and the experimental results from the charging process are shown. However, the converter is proposed to work with only one separate battery and it is not part of a BMS.

Another highly efficient AC-DC converter is given in [12], but its function as a DC-DC converter is not considered in this research. Several control systems based on Application-Specific Integrated Circuits (ASICs), fuzzy logic, and digital control systems are given, respectively, in [13–15]. These sources offer good explanation of the basic control concepts without connection to the specific load. Several applicable design procedures are shown in the manufacturers' design specifications [16–21]. Sophisticated approaches for the design of flyback converters with primary side current sensing are given, but they are based on off-line AC-DC schematics where the basic application is as LED lamp power supplies. Usually, their overall efficiency is around 75–78% for low output voltage (3.3–12 V) and 80–82% for high output voltage (12–24V) applications. In the developed converter, the input rectifier, the boost capacitor, and the input common mode filter must be excluded from the schematic for the DC-DC on-board charger, and this improves the efficiency for a flyback low (3.3 ÷ 5 V) output voltage converter. Another problem is how the constant current (CC) and constant voltage (CV) modes of operation of the primary side sensing converter will match the battery CC and CV charging. Currently, comprehensive research about the design of flyback primary current sensing working as an electric vehicle on-board battery charger is not available in the literature.

This paper proposes a flyback converter with primary side current sensing used as part of an electric vehicle battery management system. This requires the design procedures [16,17,19,20] to be altered according to the necessary DC-DC converter schematic. The analysed and designed converter is verified experimentally and the achieved efficiency is shown.
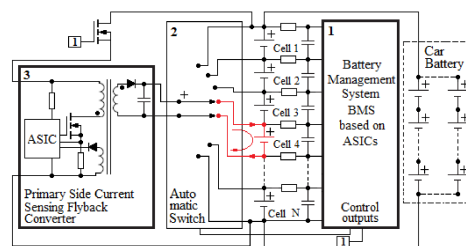

Figure 1. The basic schematic of the battery management system (BMS) and the DC-DC converter for battery voltage equalisation. (1) BMS based on an Application Specialised Integrated Circuit (ASIC); (2) automatic switch; (3) primary side current-sensing flyback converter based on the ASIC.

2. Analysis

The proposed schematic shown in Figure 1 contains the following elements:

- The Battery Management System can be based on one of the ASICs LTC6802-2, MAX1894, MAX11068, MAX11080, DS2726, BQ29330, AD7280, and ATA6870 [22–24]. This system monitors the overall battery voltage and controls the automatic switch (2) and the flyback converter (3). The BMS is not the object of research in this paper.
- The automatic switch system. This provides mechanical switching between the cells of the battery, and is also not the object of research in this paper.
- Primary side current flyback converter. The schematic is based on ASICs, for example AP3706, FAN104W, FL103, or MP020-5 [16,17,19,20]. This converter is used for the charging of a single cell (within a series string within a battery pack) if its voltage is lower than that of the other cells in the string. The charging process is conducted according to the CC (constant current) and CV (constant voltage) procedure shown in Figure 2.
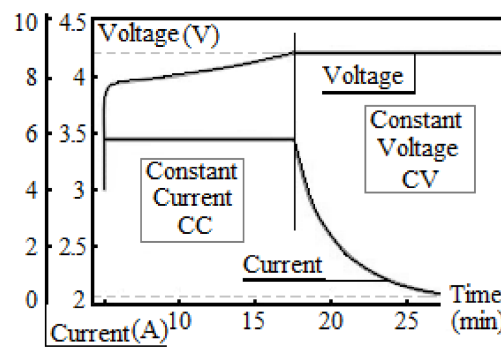

Figure 2. Li-ion battery charge diagram. CC: Constant Current charge; CV: constant voltage charge.

Figure 3 shows the schematic of the proposed converter (Figure 3B) and its derivation from a classical flyback converter (Figure 3A) with a feedback circuit. In the former, the omitted feedback schematic requires information about the output voltage to be taken from the auxiliary winding (L_3) and about the output current from the current sense resistor (R_5).

Figure 3C–E show the discontinuous conduction mode of operation (DCM), the V-I characteristic of the converter, and the time sequence of operation required for the DCM, respectively. The secondary voltage measurement is based on the oscillation process occurring over the transistor Q_1 (Drain-Source) during the current pause, t_{OFF}. It can be seen in Figure 3C that the voltage across Q_1 (the Drain-Source), V_{DS}, is the sum of the input voltage, V_{in}, the output reflecting voltage, $V_{R.out}$, and the over voltage, $V_{DS.over}$. The output voltage reference can be obtained through the auxiliary winding (L_3), which is normally used as a power supply for the ASIC (Figure 3A). The voltage from the winding L_3 and the divider $R_{11} - R_{12}$ must meet the ASIC range, which is usually between 2 and 5 V depending on the manufacturer's requirements. In this way, a reference for the output voltage is given to the control system without the classical feedback circuit shown in Figure 3A.
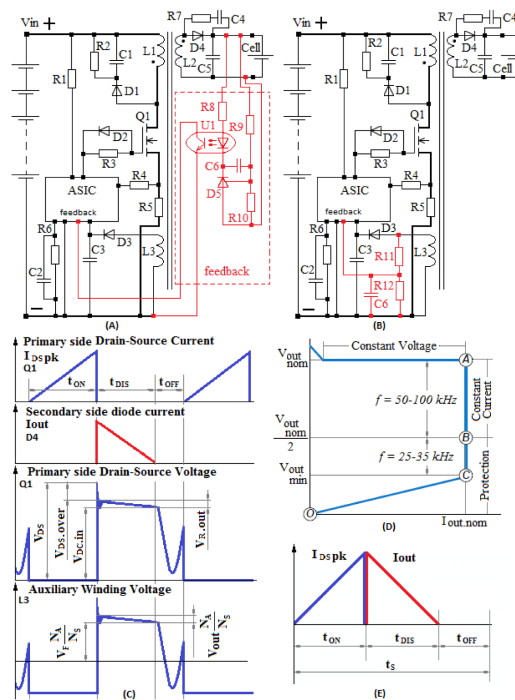
Figure 3. (**A**,**B**) Development of the flyback converter with primary current sensing from the classical flyback converter with optocoupler-based feedback; (**C**) Current-time and voltage-time diagrams of the primary and secondary side currents, primary side voltage over MOSFET Q_1, and primary side voltage on the auxiliary winding L_3; (**D**) Output V-I diagram of the converter during CC (constant current), CV (constant voltage) operation mode; (**E**) Lengths of the operating cycle.

The operation of the converter follows the next time sequence (Figure 3E):

- Time t_{ON}: the input voltage $V_{DC.in}$ is applied across the primary side of the transformer (L_1, Figure 3B), which increases the primary side current from zero to the peak value ($I_{DC.pk}$).

- Time t_{DIS}: the primary side transistor (Q_1) is turned off and the rectifier on the secondary side (D_4) is turned on. The secondary side current decreases linearly to zero. At its zero point, the accumulated energy in the transformer is depleted.

- The time t_{OFF}: the primary side voltage across Q_1 and the voltage across L_3 begins to oscillate on the resonance frequency between the primary side inductance and the parasitic output capacitor.

Figure 3D shows the Constant Voltage (CV) and Constant Current (CC) operational area described earlier in Figure 2. Assuming that the converter works only as an additional charger for SoC equalisation, this suggests that an entire cycle of charging from 0% to 100% will not be done from this charger. It can be proposed that the operation mode coincides with point A where fast charging is possible. This means that the converter must operate with higher efficiency at that point. The other two points, point B 50% of nominal output voltage and point C minimum output voltage, are also an important part of the calculation procedure.

3. Design Procedure

The design procedure depends on the parameters of the specific ASIC [16,17,19,20], which vary depending on the manufacturer. Because of this, the design procedure suggested here shows the common application of a DC-DC flyback converter with primary side sensing. The design procedure is now described in detail.

3.1. Input Parameters

The successful design requires precise input parameters: $V_{in.nom}$ is the nominal input voltage. In this case, this is the voltage from the vehicle battery where the minimum and maximum tolerances must also be given as $V_{in.min}$ and $V_{in.max}$. $V_{out.nom}$ and $I_{out.nom}$ are the nominal output voltage and current, respectively, considered according to the cell parameters shown in Figure 2. The output power is defined as $P_{out.nom} = I_{out.nom} \times V_{out.nom}$. Other parameters, such as temperature tolerances, size, weight, power density, and price, currently are not under consideration.

3.2. Estimation of the Efficiency

The input nominal power $P_{in.nom}$ is given as:

$$P_{in.nom} = \frac{V_{out.nom} \times I_{out.nom}}{\eta}. \tag{1}$$

The overall nominal efficiency at the beginning can be assumed to be within a wide range $\eta_{overall} \approx 75 - 85\%$. Although there is no input rectifier and filter due to the relatively low output voltage, a greater efficiency than 85% for this class of converter cannot be expected.

From Equation (1), the input power at point B ($P_{in.B}$) and point C ($P_{in.C}$) can be derived according to the next assumption: at point B, the output voltage drops to 50% of the nominal voltage and the overall efficiency falls to $\eta_{overall.B} = 50\%$; at point C, the efficiency and the input power depend on the minimum output voltage. With these assumptions, Equation (1) can be written for $P_{in.nom.B}$ efficiency at point B, $\eta_{overall.B}$, as follows:

$$P_{in.nom.B} = \frac{0.5 \times V_{out.nom} \times I_{out.nom}}{\eta_{overall.B}} \tag{2}$$

where the efficiency at point B, $\eta_{overall.B}$, can be calculated from the overall efficiency, $\eta_{overall}$, and the secondary side diode forward-voltage drop, V_F, as:

$$\eta_{overall.B} \cong \eta_{overall} \times \frac{0.5 \times V_{out.nom}}{(0.5 \times V_{out.nom} + V_F)} \times \frac{(V_{out.nom} + V_F)}{V_{out.nom}}. \tag{3}$$

At point C, the converter works at the minimum output voltage, $V_{out.min}$, where the input power and the efficiency at this point, $\eta_{overall.C}$, are respectively:

$$P_{in.C} = \frac{V_{out.min} \times I_{out.nom}}{\eta_{overall.C}} \tag{4}$$

$$\eta_{overall.C} \cong \eta_{overall} \times \frac{V_{out.min}}{(V_{out.min} + V_F)} \times \frac{(V_{out.nom} + V_F)}{V_{out.nom}}. \tag{5}$$

Point A is the working point for the converter if it works on fast charge mode. The input power at that point will be:

$$P_{in.A} = \frac{V_{out.out} \times I_{out.nom}}{\eta_{overall}} = \frac{V_{out.out} \times I_{out.nom}}{75 - 85\%} \tag{6}$$

where as a first assumption 80% overall efficiency can be accepted.

3.3. Determination of the Transformer Turns Ratio

The suggested design procedure begins with transformer turns ratio determination as opposite to the established flyback design procedures [25,26] with optical feedback connections (Figure 3A). The transformer turn ratio parameter represents the ratio between the primary and secondary turns N_P/N_S. It must be chosen as a compromise between the primary and secondary voltage stress, respectively, over the transistor (Q_1, Figure 3B) and the diode (D_4, Figure 3B).

As can be seen in Figure 3C, when the transistor is turned off, the voltage drain-source (V_{DS}) will be the sum of the input voltage ($V_{DC.in}$) and the reflected output voltage ($V_{R.out}$):

$$V_{DS} = V_{DC.in} + V_{R.out} + V_{DS.over} \tag{7}$$

where the reflected output voltage ($V_{R.out}$) can be calculated according to the transformer turn ratio (N_S/N_P), i.e., secondary, N_S, and primary, N_P:

$$V_{R.out} = \frac{N_S}{N_P} \times (V_{out} + V_F). \tag{8}$$

$V_{DS.over}$ is the overvoltage caused by the leakage inductance. In this design, N_P/N_S is estimated according to the desired MOSFET type with respect to its nominal voltage drain-source. The calculation algorithm and the primary side voltage stress over Q_1 are shown in Figure 4 according to the parameters assumed in Figure 3C.

The overvoltage $V_{DS.over}$ and the entire oscillating process depend on several parameters, including random factors, such as primary side and leakage inductance, transistor output capacitance, and PCB (Printed Circuit Board) layout issues, which cannot be precisely determined. This means that the overvoltage must be verified experimentally.

The transformer turns ratio between the auxiliary winding L_3 and the secondary winding L_2 (N_A/N_S) depends on the ASIC voltage supply range. Because fast charging is a heavy load, a relatively high overvoltage $V_{DS.over}$ can be expected, and this must be taken into consideration. With the minimum, $V_{DD.min}$, and maximum, $V_{DD.max}$, voltages the auxiliary winding can be calculated from:

$$V_{DD.min} = \frac{N_A}{N_S} \times \left(V_{out.min} + V_F + \frac{N_S}{N_P} \times V_{DS.over} \right) - V_{F.aux} \tag{9}$$

$$V_{DD.max} = \frac{N_A}{N_S} \times \left(V_{out.nom} + V_F + \frac{N_S}{N_P} \times V_{DS.over} \right) - V_{F.aux} \tag{10}$$

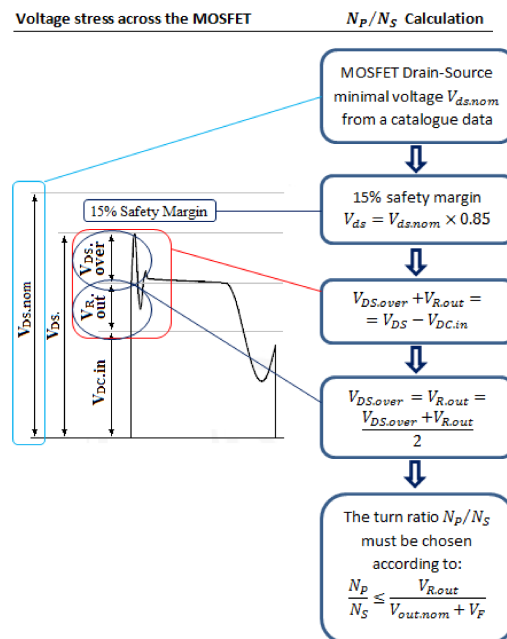where $V_{F.aux}$ is the forward voltage drop across the diode (D_4, Figure 3B).

Figure 4. Algorithm for calculating the turn ratio N_P/N_S.

3.4. Design of the Transformer

According to the time periods shown in Figure 3E, the sum of the primary side (transistor Q_1) and the secondary side (rectifier D_4) conduction time at point B (Figure 3D), i.e., 50% of the output voltage $V_{out.nom}$, is given by:

$$t_{ON.B} + t_{DIS.B} = \frac{\frac{1}{f_S} - t_{OFF.B}}{\left(1 + \frac{N_S}{N_P} \times \frac{V_{DC.min.B}}{0.5 \times V_{out.min} + V_{F.aux}}\right)} \times \left(1 + \frac{N_S}{N_P} \times \frac{V_{DC.min.B}}{0.5 \times V_{out.min} + V_{F.aux}}\right) \tag{11}$$

where $V_{DC.min.B}$ is the minimum input voltage at point B.

From here, the sum of $t_{ON.B} + t_{DIS.B}$ is derived as:

$$t_{ON.B} + t_{DIS.B} = \frac{1}{f_S} - t_{OFF.B} \tag{12}$$

where f_s is the switching frequency. The primary transformer inductance, L_m, is given by:

$$L_m = \frac{(V_{in.B} \times t_{ON.B})^2 \times f_S}{2 \times P_{in.nom.B}}. \tag{13}$$

The maximum primary side peak current, $I_{DS.pk}$, (Drain-Source) is given by:

$$I_{DS.pk} = \sqrt{\frac{2 \times P_{in.nom}}{L_m \times f_s}}. \tag{14}$$

The minimum number of turns required to avoid core saturation is given by:

$$N_{p.min} = \frac{L_m \times I_{DS.pk}}{B_{sat} \times A_e} \tag{15}$$

where B_{sat} is the flux density (T), and A_e is the cross-sectional area (m^2).

At point C, the converter operates in discontinuous conducting mode and the ON $(t_{ON.C})$ and OFF $(t_{OFF.C})$ times at this point must be checked according to:

$$t_{ON.C} = \frac{1}{V_{bus.min.C}} \times \sqrt{\frac{2 \times P_{in.C} \times L_m}{f_{s.r}}} \tag{16}$$

$$t_{OFF.C} = \frac{1}{f_{s.r}} - t_{ON.C} \left(1 + \frac{N_P}{N_S} \times \frac{V_{in.min.C}}{V_{out.min} + V_F}\right) \tag{17}$$

where $f_{s.r}$ is the switching frequency after its reduction (Figure 3B).

The transformer turns ratio between the auxiliary winding N_A and the secondary winding N_S depends on the supply voltage (V_{DD}) of the ASIC used. As the voltage on the auxiliary winding varies with the output load, it is important to operate within the permissible voltage range. In the case that the voltage V_{DD} drops down below the minimum threshold, $V_{DD.min}$, the converter must stop working. The following condition must be satisfied:

$$V_{DD.min} = \left(\frac{N_A}{N_S}(V_o + V_F) - V_{F.aux}\right) > V_{DD.max} + (2 - 3V) \tag{18}$$

where $V_{DD.max}$ is the maximum allowable voltage and $(2 - 3V)$ is a safety merging.

The transformer core, usually ferrite for flyback converters [18,19], must be selected according to the output power. Its selection can be made from the product parameter $A_E A_W$:

$$A_E A_W = \left(\frac{L_m \times I_{DS.pk} \times I_{DS.rms} \times 10^4}{B_{max} \times K_u \times K_j \times f_{S.min}} \right) \quad (19)$$

where A_E is the core cross-sectional area, A_W the window area available for winding, K_u the winding factor (0.25–0.3), K_j the current density coefficient (400–600), B_{max} the maximum flux density or saturation flux density of the core material, and $f_{S.min}$ the minimum frequency.

With a given core size, the primary winding turns, N_p, is given by:

$$N_p = \frac{L_m \times I_{DS.pk}}{A_E \times B_{max}}. \quad (20)$$

The wire size can be chosen according to the RMS (Root Mean Square) primary current $2.5 - 3 \, A/mm^2$. Multiple strands with diameters Δd depend on the frequency:

$$\Delta d = \sqrt{\frac{1}{\pi . f_s . \mu_0 . \sigma}} \quad (21)$$

where: $\mu_0 = 4 \times \pi \times 10^{-7}$ H/m is the permeability in vacuum and $\sigma = 6 \times 10^7$ S/m is the conductivity of the copper. The magnetic air gap length in the core is:

$$l_{gap} = \mu_o . A_E . \frac{N_p^2}{L_m} - \frac{l_c}{\mu_r} \approx \mu_o . A_E . \frac{N_p^2}{L_m} \quad (22)$$

where μ_r is the relative magnetic permeability of the core material and l_c the core magnetic length.

The stored energy, E_{st}, in the flyback transformer is given from:

$$E_{st} = \frac{1}{2} . L_m . I_{DC.pk}^2 . f_s. \quad (23)$$

3.5. Current Sense Resistor

The current sense resistor (R_5) value is calculated by:

$$R_5 = \frac{N_p}{K \times I_{out} \times N_s} \quad (24)$$

where K is the design parameter of the ASIC. The voltage divider $R_{11} - R_{12}$ can be calculated from:

$$\frac{R_{11}}{R_{12}} = \frac{V_{out.nom}}{V_{ref}} \times \frac{N_A}{N_s} - 1. \quad (25)$$

The capacitor C6 must be chosen in the range $22 \div 68$ pF [19].

3.6. Calculating the Parameters of the Primary Side MOSFET Transistor

The voltage stress of the primary side transistor is given in Figure 4. The Drain-Source primary RMS current, $I_{DS.rms}$, is calculated from:

$$I_{DS.rms} = I_{DS.pk} \times \sqrt{\frac{t_{ON} \times f_s}{3}}. \quad (26)$$

3.7. Calculating the Parameters of the Secondary Side Rectifier

The maximum reverse voltage and the RMS current of the secondary side rectifier are given from:

$$V_F = V_{out.nom} \times \frac{N_S}{N_P} \times V_{in.max} \tag{27}$$

$$I_{F.rms} = I_{DS.rms} \times \sqrt{\frac{V_{DC.in.min}}{V_{R.out}}} \times \frac{N_P}{N_S}. \tag{28}$$

Equation (28) is based on $I_{DS.rms}$ and the transformer turn ratio.

The relationship between the primary and the secondary side peak current is:

$$I_{DS.pk} = \frac{I_{F.pk}}{N_p} \tag{29}$$

where $I_{F.pk}$ is the secondary side peak current. The dependence between the ideal output current, I_{out}, and $I_{F.pk}$ is given by:

$$I_{out} = \frac{1}{2} \times I_{F.pk} \times \frac{t_{ON}}{t_s}. \tag{30}$$

3.8. Design of the Clamping Systems

The parasitic components, such as leakage inductance L_{LK}, secondary leakage inductance L_{LKS}, output MOSFETs capacitance C_{oss}, and secondary rectifier capacitance C_{DS}, are analysed [26–28] and included in this design procedure.

The primary side RCD clamping circuit (R_2, C_1, D_1) prevents the excessive voltage spike which results from the transformer leakage inductance (L_{LK}). The maximum voltage stress of the MOSFET is given by Equation (7). The previously considered safety voltage margin of 15% shows that the clamping system must restrict the voltage spike in this range. The peak clamping current is given from:

$$I_{CL.pk} = \sqrt{\left(\frac{2.P_{IN.A}}{L_m.f_s}\right)^2 - \frac{C_{oss}}{L_{LK}}V_{DC.over}^2} \tag{31}$$

where C_{oss} is the output capacitance of the transistor Q_1 taken from the manufacturer's catalog.

The dissipated power from the RCD network, P_{RCD}, is given by:

$$P_{RCD} = \frac{1}{2}f_S.L_{LK}.I_{CL.pk}^2 \cdot \frac{V_{R.out} + V_{DC.over}}{V_{DC.over}}. \tag{32}$$

The resistance R_2 and the capacitor C_1 are given by:

$$R_2 = \frac{(V_{R.out} + V_{DS.over})^2}{P_{RCD}} \tag{33}$$

$$C_1 > \frac{V_{R.out} + V_{DS.over}}{V_{rip}.R_{RCD}.f_s}. \tag{34}$$

3.9. Design of the Output Filter

The peak-to-peak ripple, $\Delta I_{C.rip}$, of the output capacitor (C_5) is calculated from:

$$\Delta I_{C.rip} = \frac{N_p}{N_s}I_{DS.pk}, \tag{35}$$

and the voltage ripple on the output from:

$$\Delta V_{out.rip} = \frac{t_{DIS.A}}{2.C_5} \times \frac{(\Delta I_{C.rip} - I_{out.nom})^2}{\Delta I_{C.rip}} + \Delta I_{C.rip} \times R_{ESR} \tag{36}$$

where R_{ESR} is the equivalent series resistor of C_5.

3.10. Design of the RC Snubber

The resistor R_7 is given by:

$$R_7 = \sqrt{\frac{L_{LKS}}{C_{DS}}} \tag{37}$$

where L_{LKS} is the secondary leakage inductance and C_{DS} is the secondary side rectifier parasitic capacitance.

Normally C_4 is 2–3 times C_{DS}.

4. Experimental Results

Based on the presented design procedure, an experimental converter was designed, built, and tested. Its parameters are presented in Table 1.

The experimental results are presented as follows:

- Figure 5. The oscillogram shows the primary side of the converter, where: (1) is the voltage Drain-Source, V_{DS}, across the MOSFET with specific oscillation after full energy transfer; (2) is the primary side current, I_{pk}, through L_1, Q_1, and R_5; (3) is the secondary side current through the rectifier, which represents the energy transfer at the zero point; and (4) is the voltage on the auxiliary winding, which repeats the shape of (1) but with a smaller amplitude.
- Figure 6 shows the secondary side of the converter, where (1) and (2) are the secondary side current and voltage, respectively, over D_4; (3) is the voltage on the auxiliary winding; and (4) is the output voltage.
- Figure 7 shows the primary side of the converter under an open circuit. Although the tested battery charger is not supposed to work under this condition, this experiment shows the process of reducing the switching frequency from 50–100 kHz to 20–35 kHz (Figure 3D).
- The maximum obtained efficiency of the converter is 84% as shown in Figure 8.
- Some specific parameters are given in Figure 9. The primary side current has a peak value immediately after the transistor is turned on. When it is turned off, its process has a typical oscillation in V_{DS}. Although these features are assumed to be normal, they have to be considered alongside the control system parameters. Two delay times are necessary for its correct operation, respectively, in ranges 100–200 ns and 300–400 ns as Figure 10 shows.

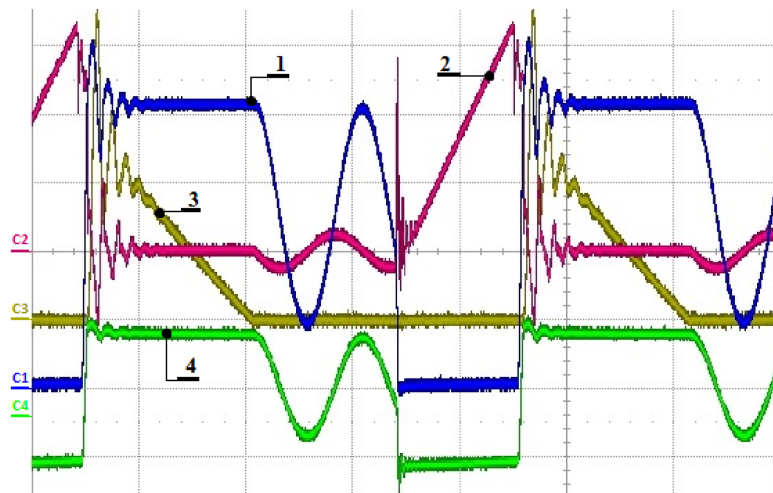A photo of the experimental converter and a battery string is shown in Figure 10.

Figure 5. Primary side of the converter: (1) Voltage Drain-Source V_{DS} over the transistor (150.00 V/div); (2) Primary side current I_{pk} (0.5 A/div); (3) Secondary side current through the rectifier (1.00 A/div); and (4) Voltage on the auxiliary winding (5.00 V/div). Time scale: 2.5 µs/div, 100 kHz.
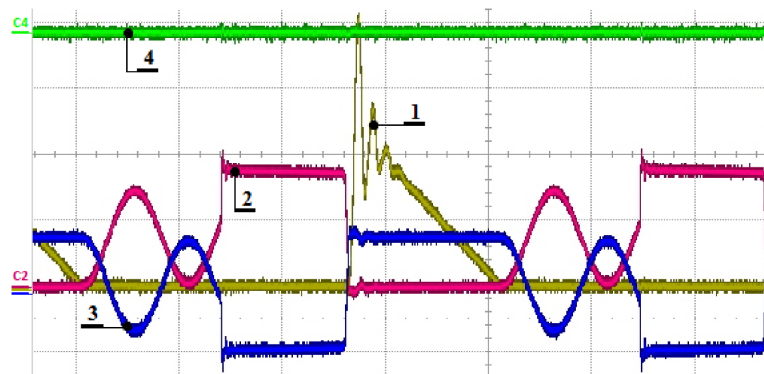

Figure 6. Secondary side of the converter: (1) Secondary side current through the rectifier (2.00 A/div); (2) Voltage over the secondary side rectifier (5.00 V/div); (3) Voltage on the secondary side of the transformer L_2 5.00 V/div; and (4) Output DC voltage (20.00 mV/div). Time scale: 2.50 µs/div, 100 kHz.

Table 1. Parameters of the experimentally tested converter.

Parameter	Value
$V_{in.min}$	350 V
$V_{in.max}$	400 V
$V_{in.nom}$	380 V
$V_{out.max}$	5 V
$I_{out.max}$	10 A
f_s	66 kHz

5. Conclusions

In this paper, the essential points of the design procedure of a flyback converter with primary current sensing is presented. The same converter can be used as part of a BMS for active cell balancing. From the obtained results, the following conclusions can be formulated:

- The presented design procedure for a DC-DC flyback converter is correct and it can be used as part of the overall design of the converter.
- The schematic of the flyback converter with primary current sensing (Figure 3B) can be used as a battery charger and is particularly suitable for battery equalisation as part of a BMS. The schematic works under constant current and constant voltage (Figure 3D) and meets the battery charging requirements (Figure 2).
- The efficiency of the circuit reaches 82–84% for a low-voltage output converter (Figure 8). If fast charging of a cell is necessary, the converter must be designed to work at the working point A from the output V-I characteristic (Figure 3 D).
- The experimental verification shown in Figures 5–7 entirely meets the theoretical analysis shown in Figure 3.
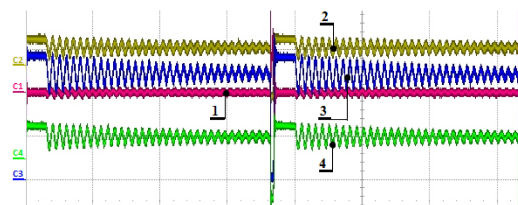- As Figure 9 shows, the two delay times in the turn-on and turn-off processes are necessary.

Figure 7. Primary side of the converter under an open circuit: (1) Primary side current I_{pk} (0.5 A/div); (2) Voltage on the auxiliary winding (10.00 V/div); (3) Voltage Drain-Source V_{DS} over the transistor (200.00 V/div); and (4) Voltage after the auxiliary winding divider R_{11}, R_{12}, and C_6 (Figure 3B) (2.00 V/div); Time scale: 10 µs/div, 25 kHz.
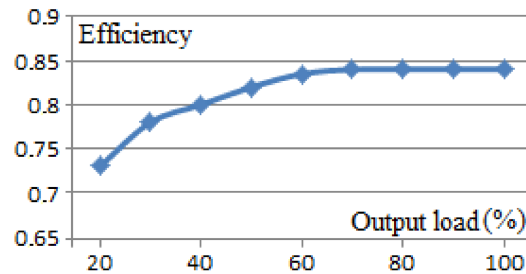

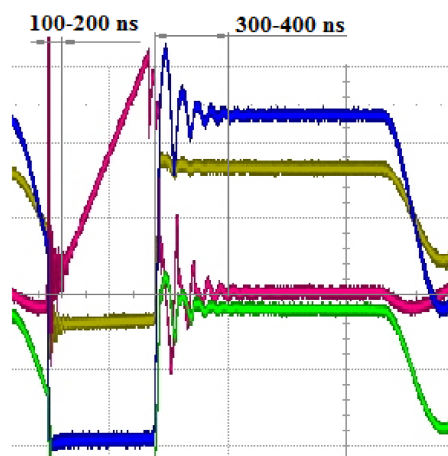**Figure 8.** Efficiency of the experimentally tested converter.

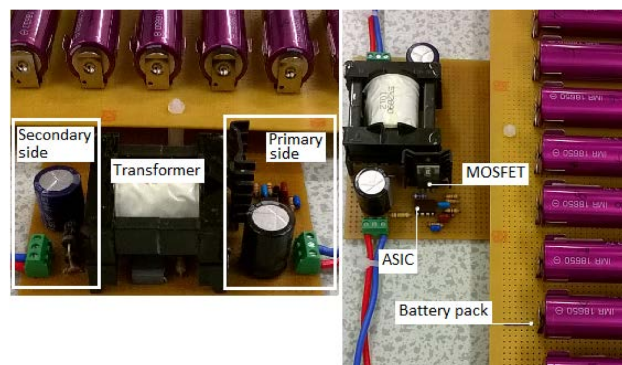**Figure 9.** The delay times during the transient processes when turning on and off.

Figure 10. The Experimental converter with a battery string.

Author Contributions: Borislav Dimitrov and Andrew Cruden conceived and designed the experiments; Borislav Dimitrov and Muthu Krishna performed the experiments; Borislav Dimitrov, Andrew Cruden and Suleiman Sharkh analysed the data; Borislav Dimitrov, Andrew Cruden, Muthu Krishna and Ahmad Elkhateb contributed to the circuit design, design procedure and analysis; Borislav Dimitrov and Andrew Cruden wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Jang, J.; Zhang, C. *Fundamentals and Applications of Lithium-ion Batteries in Electric Drive Vehicles*; John Wiley & Sons: Singapore, 2015; ISBN 978-1-118-41478-1.
2. Link, A.; O'Connor, A.; Scott, T. *Battery Technology for Electric Vehicles*; Swales & Willis Ltd.: Devon, UK, 2015; ISBN 978-1-138-81110-2.
3. Brec, E.; Muller, B. *Electric Vehicle Batteries: Moving from Research Towards Innovation*; Springer International Publishing: Cham, Switzerland, 2015; ISBN 978-3-319-12705-7.
4. Andrea, D. *Battery Management System for Large Lithium-Ion Battery Packs*; Artech House: Boston, MA, USA; London, UK, 2010; ISBN 978-1-60807-104-3.
5. Namith, T.; Shankpal, P. Design and Development of Efficient Battery Charging and Cell Balancing for Battery Management System. *SASTech J.* **2012**, *11*, 15–22.
6. Douglass, J. *Battery Management for High-Power Battery Stacks*. CAN Newsletter 4/2010; 2010; pp. 34–38. Available online: https://can-newsletter.org (accessed on 15 August 2017).
7. Hoog, J.; Alpcan, T.; Brazil, M.; Thomas, D.; Mareels, I. Optimal Charging of Electric Vehicles Taking Distribution Network Constraints into Account. *IEEE Trans. Power Syst.* **2014**, *30*, 365–375. [CrossRef]
8. Li, L.; Lu, X.; He, J.; Sun, Z.; Yang, G. Design of New-generation Electric Vehicle Terminal. *Energy Power Eng.* **2013**, *5*, 1362–1366. [CrossRef]
9. Barreras, J.; Swierczynski, M.; Schaltz, E.; Andreasen, J.; Christian, F.; Sauer, D.; Dirk, U. Christensen Functional Analysis of Battery Management Systems Using Multi-Cell HIL Simulator. In Proceedings of the 10th International Conference on Ecological Vehicles and Renewable Energies (EVER), Monte-Carlo, Monaco, 31 March–2 April 2015.
10. Gi-Heon, K.; Jeffrey, G.; Lustbader, J.; Pesaran, A. Thermal Management of Batteries in Advanced Vehicles Using Phase-Change Materials. *World Electr. Veh. J.* **2008**, *2*, 137–147.
11. Paul, C.; Chao, P.; Chen, W.; Wu, R. A Battery Charge Controller Realized by a Flyback Converter with Digital Primary Side Regulation for Mobile Phones. *Microsyst. Technol.* **2014**, *20*, 1689–1703.
12. Mayuri, R.; Purushotham, K.; Rao, B. High Efficient AC/DC Converter. *Elect. Electron. Eng.* **2017**, *7*, 43–47.
13. Qiu, J.; He, L.; Wang, Y. A Multimode Digital Controller IC for Flyback Converter with High Accuracy Primary-Side Feedback. *Comput. Electron.* **2013**, *14*, 652–662. [CrossRef]
14. Lian, K.; Hong, C. Current-Sensorless Flyback Converters Using Integral T-S Fuzzy Approach. *Int. J. Fuzzy Syst.* **2013**, *15*, 66–74.

15. Chang, C.; Lin, Y.; Tzou, Y. Digital Primary-Side Sensing Control for Flyback Converters. In Proceedings of the International Conference on Power Electronics and Drive Systems, Taipei, Taiwan, 2–5 November 2009; pp. 689–694.

16. Monolithic Power Systems (MPS). Application Note AN062 Rev.12, Flyback Converter Using the Primary-Side Regulator, 2012, MP020-5. Available online: https://www.monolithicpower.com/ (accessed on 15 August 2017).

17. Qinghua, S.; Wengui, D. Basic Steps to Design a PSR Flyback Converter Using AP3706/08N, 2009, BCD Semiconductor Manufacturing Limited Application Note 1028, Rev 1.1. Available online: https://www.diodes.com/ (accessed on 15 August 2017).

18. Fairchild Semiconductor Corporation Design Guideline for Flyback Charger Using FAN104WMX, 2012, Application Note AN-6093 Rev. 1.0.1. Available online: https://www.fairchildsemi.com (accessed on 15 August 2017).

19. Fairchild Semiconductor Corporation, Design Guideline for LED Lamp Control Using Primary-Side Regulated Flyback Converter, FL103M, 2011, Application Note AN-9741 Rev. 1.0.0. Available online: https://www.fairchildsemi.com (accessed on 15 August 2017).

20. ST Datasheet Production Data. Off-Line All-Primary-Sensing Switching Regulator. 2014. Available online: https://www.st.com (accessed on 15 August 2017).

21. Ayachit, A.; Reatti, A.; Kazimierczuk, M.K. Magnetising Inductance of Multiple-Output Flyback DC-DC Convertor for Discontinuous-Conduction Mode. *IET Power Electron.* **2016**, *10*, 451–461. [CrossRef]

22. Analog Devices Inc. Lithium Ion Battery Monitoring System AD7280. 2008. Available online: https://www.analog.com (accessed on 15 August 2017).

23. Maxim Integrated Products, Inc. 5-Cell to 10-Cell Li+ Protector with Cell Balancing. 2010. Available online: https://www.maxim-ic.com (accessed on 15 August 2017).

24. Maxim Integrated Products, Inc. 12-Channel, High-Voltage Battery-Pack Fault Monitors. 2010. Available online: https://www.maxim-ic.com (accessed on 15 August 2017).

25. Saliva, A. Design Guide for Off-Line Fixed Frequency DCM Flyback Converter, Infineon Technologies North America, Design Note DN 2013-01. Available online: https://www.infineon.com (accessed on 15 August 2017).

26. Saini, D.; Ayachit, A.; Reatti, A.; Kazimierczuk, M.K. Analysis and Design of Choke Inductors for Switched-Mode Power Inverters. *IEEE Trans. Ind. Electron.* **2018**, *65*, 2234–2244. [CrossRef]

27. Luchetta, A.; Manetti, S.; Piccirilli, M.; Reatti, A.; Kazimierczuk, M. Effects of Parasitic Components on Diode Duty Cycle and Small-Signal Model of PWM DC-DC Buck Converter in DCM. In Proceedings of the IEEE 15th International Conference on Environment and Electrical Engineering, Rome, Italy, 10–13 June 2015; pp. 772–777.

28. Luchetta, A.; Manetti, S.; Piccirilli, M.; Reatti, A.; Kazimierczuk, M. Derivation of Network Functions for PWM DC-DC Buck Converter in DCM Including Effects of Parasitic Components on Diode Duty-Cycle. In Proceedings of the IEEE 15th International Conference on Environment and Electrical Engineering, Rome, Italy, 10–13 June 2015; pp. 778–783.