

# Implementing a CNN in TensorFlow for HLS

This notebook will walk you through the process of creating a Convolutional Neural Network that performs object classification using TensorFlow and the HLS4ML flow in Catapult AI NN. There are three phases to this process

- Defining the network model in TensorFlow
- Configuring Catapult AI NN and generating the C++ model
- Synthesizing the C++ into hardware with Catapult AI NN

Note: To load and execute this Jupyter Notebook from a shell, do the following:

```
sh $MGC_HOME/shared/pkgs/ccs_hls4ml/create_env.sh
$MGC_HOME/bin/python3 $HOME/ccs_venv
(The previous step need only be executed once)
bash
source $HOME/ccs_venv/bin/activate
jupyter notebook --ip="127.0.0.1" --browser=firefox
$MGC_HOME/shared/examples/cat_ai_nn/Tutorial/notebook.ipynb
```

## Defining the network model in TensorFlow

First we need to configure the Python environment

### Import the Catapult AI NN Python module

```
In [1]: import catapult_ai_nn
import os

import ssl
ssl._create_default_https_context = ssl._create_stdlib_context
### Note: Targeting ASIC using the SAED32 library and power estimation/optimization r
try:
    pdk_var = os.environ['SAED32_EDK']
except KeyError:
    print('WARNING: Environment variable SAED32_EDK was not found. You will not be ab

script_file = os.path.basename(__session__)
script_name = os.path.splitext(script_file)
step = script_name[0]
```

```
2024-12-13 14:14:36.751072: E external/local_xla/xla/stream_executor/cuda/cuda_dnn.cc:9261] Unable to register cuDNN factory: Attempting to register factory for plugin cuDNN when one has already been registered
2024-12-13 14:14:36.751117: E external/local_xla/xla/stream_executor/cuda/cuda_fft.cc:607] Unable to register cuFFT factory: Attempting to register factory for plugin cuFFT when one has already been registered
2024-12-13 14:14:36.752537: E external/local_xla/xla/stream_executor/cuda/cuda_blas.cc:1515] Unable to register cuBLAS factory: Attempting to register factory for plugin cuBLAS when one has already been registered
2024-12-13 14:14:36.760841: I tensorflow/core/platform/cpu_feature_guard.cc:182] This TensorFlow binary is optimized to use available CPU instructions in performance-critical operations.
To enable the following instructions: AVX2 AVX512F FMA, in other operations, rebuild TensorFlow with the appropriate compiler flags.
2024-12-13 14:14:38.905514: W tensorflow/compiler/tf2tensorrt/utils/py_utils.cc:38] TF-TRT Warning: Could not find TensorRT
```

## Download the MNIST dataset

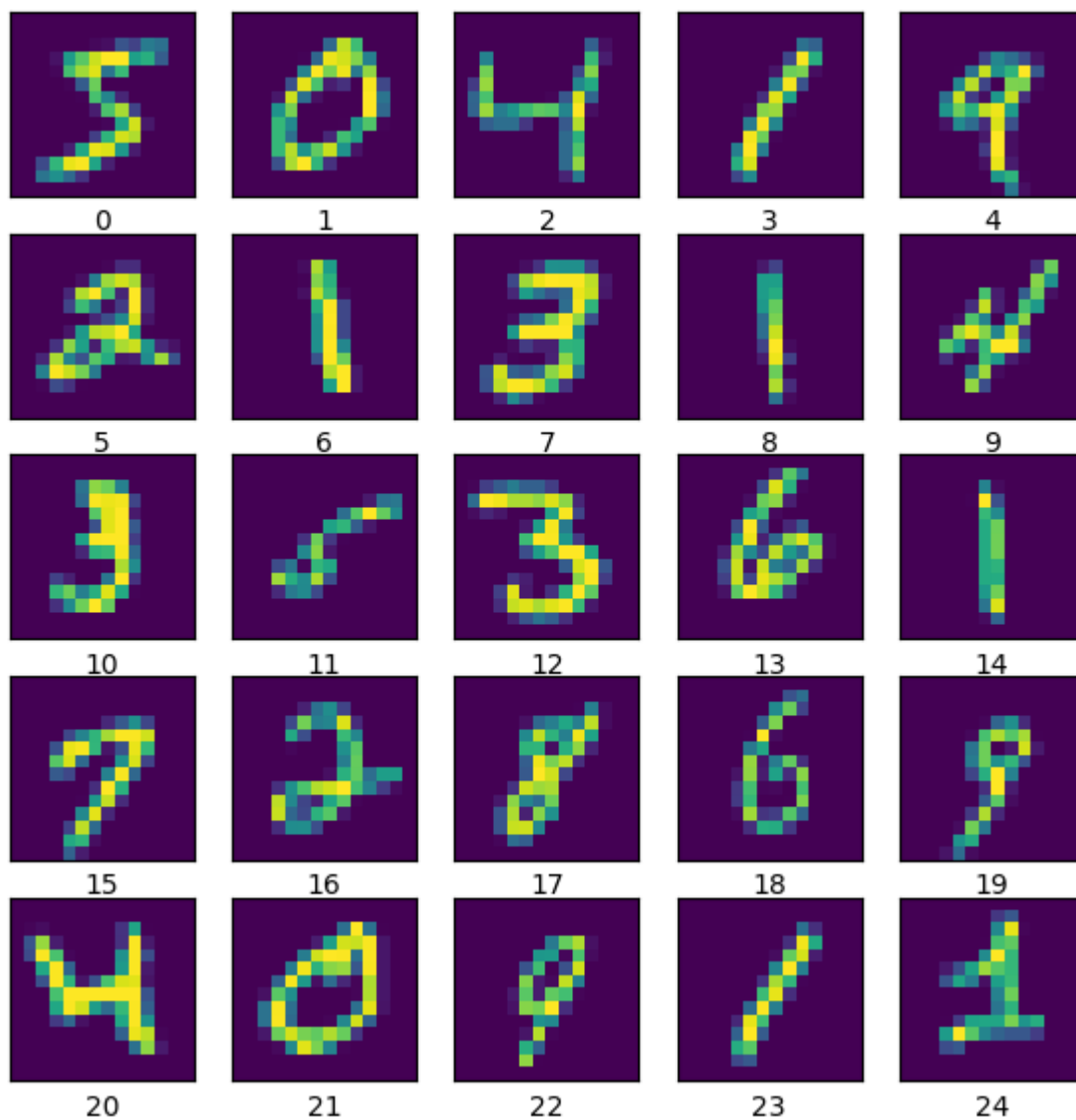
Download the MNIST dataset (contains 28x28 pixel images), reshape (potentially) to a smaller resolution, and normalize the pixel values to values between 0 and 1 (8bit resolution)

```
In [2]: import tensorflow as tf
from tensorflow.keras.models import Sequential
from tensorflow.keras import layers, Model, Input
from tensorflow.keras.models import load_model
import numpy as np
# Dataset is 28x28 images
(x_train, y_train), (x_test, y_test) = tf.keras.datasets.mnist.load_data()
Fw = 14
# Reshape images from 28x28 down to Fw x Fw
x_train = tf.image.resize(x_train[...], np.newaxis, size=(Fw, Fw)).numpy()
x_test = tf.image.resize(x_test[...], np.newaxis, size=(Fw, Fw)).numpy()
x_train = x_train.reshape(-1, Fw, Fw, 1) / 255.0
x_test = x_test.reshape(-1, Fw, Fw, 1) / 255.0
y_train = tf.keras.utils.to_categorical(y_train, num_classes=10)
y_test = tf.keras.utils.to_categorical(y_test, num_classes=10)
```

## Plot the Dataset

Generate a plot of the first 25 images in the dataset along with their labels to confirm the data

```
In [3]: from IPython.display import Image
import matplotlib.pyplot as plt
# View the first 25 images from the dataset
plt.figure(figsize=(7,7))
for i in range(25):
    plt.subplot(5,5,i+1)
    plt.xticks([])
    plt.yticks([])
    plt.grid(True)
    plt.imshow(x_train[i])
    plt.xlabel(i)
plt.show()
```



## Define the CNN model in TensorFlow

This notebook contains several different neural network architectures for MNIST to explore:

- Conv2D, Batchnorm and Dense



- Conv2D and MaxPool



For each architecture there is a pure Keras implementation, which results in post-training quantization (PTQ) and a QKeras implementation which allows quantization-aware training (QAT) resulting in smaller bitwidth operators. Use the two variables below to select the model architecture and quantization mode.

```
In [4]: model_arch = 1
#model_arch = 2
quant_mode = 'ptq'
#quant_mode = 'qat'
```

```
In [5]: if model_arch == 1 and quant_mode == 'ptq':
    ## Neural Network Architecture 1 - Conv2D, BatchNorm and Dense
    # Note we are applying names to the top model and to each of the layers
    model = Sequential(name='mnist_'+step)
    model.add(layers.Input(shape=(Fw,Fw, 1), name='input1'))
    model.add(layers.Conv2D(filters=5, kernel_size=5, strides=3, name='conv2d1'))
    model.add(layers.BatchNormalization(name='batchnorm1'))
    model.add(layers.Activation('relu', name='relu1'))
    model.add(layers.Flatten(name='flatten1'))
```

```
model.add(layers.Dense(10, name='dense1'))
model.add(layers.Activation('softmax', name='softmax1'))
```

```
In [6]: if model_arch == 1 and quant_mode == 'qat':
        ## Neural Network Architecture 1 - Conv2D, BatchNorm and Dense
        # Note we are applying names to the top model and to each of the layers
        model = Sequential(name='mnist_'+step)
        model.add(layers.Input(shape=(Fw,Fw, 1), name='input1'))
        model.add(QConv2D(filters=5, kernel_size=5, strides=3,
            kernel_quantizer=quantized_bits(8, 1, 1, alpha=1),
            bias_quantizer=quantized_bits(8, 1, alpha=1),
            name='conv2d1'))
        model.add(layers.BatchNormalization(name='batchnorm1'))
        model.add(layers.Activation('relu', name='relu1'))
        model.add(layers.Flatten(name='flatten1'))
        model.add(QDense(
            units=10,
            kernel_quantizer=quantized_bits(8, 1, alpha=1),
            bias_quantizer=quantized_bits(8, 1, alpha=1),
            kernel_regularizer=tf.keras.regularizers.L1L2(0.0001),
            activity_regularizer=tf.keras.regularizers.L2(0.0001),
            name='dense1',
        ))
        model.add(layers.Activation('softmax', name='softmax1'))
```

```
In [7]: if model_arch == 2 and quant_mode == 'ptq':
        ## Neural Network Architecture 2 - Conv2D and MaxPool
        # Note we are applying names to the top model and to each of the layers
        model = Sequential(name='mnist_'+step)
        model.add(layers.Input(shape=(Fw,Fw, 1), name='input1'))
        model.add(layers.Conv2D(filters=32, kernel_size=3, strides=1, name='conv2d1'))
        model.add(layers.Activation('relu', name='relu1'))
        model.add(layers.MaxPooling2D(name='maxpool1', pool_size=2))
        model.add(layers.Conv2D(filters=64, kernel_size=3, strides=1, name='conv2d2'))
        model.add(layers.Activation('relu', name='relu2'))
        model.add(layers.MaxPooling2D(name='maxpool2', pool_size=2))
        model.add(layers.Flatten(name='flatten1'))
        model.add(layers.Dense(10, name='dense1'))
        model.add(layers.Activation('softmax', name='softmax1'))
```

```
In [8]: if model_arch == 2 and quant_mode == 'qat':
        ## Neural Network Architecture 2 - Conv2D and MaxPool
        # Note we are applying names to the top model and to each of the layers
        model = Sequential(name='mnist_'+step)
        model.add(layers.Input(shape=(Fw,Fw, 1), name='input1'))
        model.add(QConv2D(filters=32, kernel_size=3, strides=1,
            kernel_quantizer=quantized_bits(8, 1, 1, alpha=1),
            bias_quantizer=quantized_bits(8, 1, alpha=1),
            name='conv2d1'))
        model.add(layers.Activation('relu', name='relu1'))
        model.add(layers.MaxPooling2D(name='maxpool1', pool_size=2))
        model.add(QConv2D(filters=64, kernel_size=3, strides=1,
            kernel_quantizer=quantized_bits(8, 1, 1, alpha=1),
            bias_quantizer=quantized_bits(8, 1, alpha=1),
            name='conv2d2'))
        model.add(layers.Activation('relu', name='relu2'))
        model.add(layers.MaxPooling2D(name='maxpool2', pool_size=2))
        model.add(layers.Flatten(name='flatten1'))
        model.add(layers.Dense(10, name='dense1'))
        model.add(layers.Activation('softmax', name='softmax1'))
```

Show the structure of the network model

Note the 'Param #' column - this specifies the number of parameters (weights/biases) required by that layer.

```
In [9]: # Show the model textually
model.summary()
```

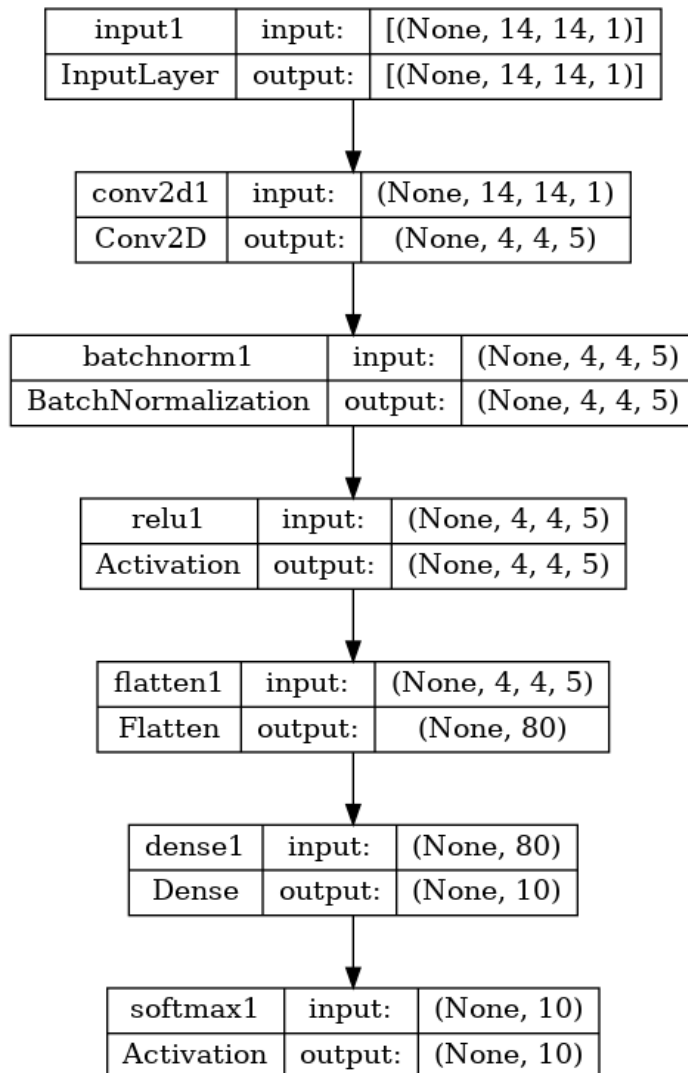
Model: "mnist\_notebook"

Layer (type)	Output Shape	Param #
conv2d1 (Conv2D)	(None, 4, 4, 5)	130
batchnorm1 (BatchNormalization)	(None, 4, 4, 5)	20
relu1 (Activation)	(None, 4, 4, 5)	0
flatten1 (Flatten)	(None, 80)	0
dense1 (Dense)	(None, 10)	810
softmax1 (Activation)	(None, 10)	0

=====  
Total params: 960 (3.75 KB)  
Trainable params: 950 (3.71 KB)  
Non-trainable params: 10 (40.00 Byte)

```
In [10]: from tensorflow.keras.utils import plot_model
# Show the model graphically
plot_model(model, to_file=model.name+'_model.png', show_shapes=True, show_layer_names=True)
Image(model.name+'_model.png', width=350)
```

Out[10]:



## Compile and train the model with the MNIST dataset

```
In [11]: # Compile and train the model
model.compile(optimizer='adam', loss='categorical_crossentropy', metrics=['accuracy'])
history = model.fit(x_train, y_train, epochs=10)
```

```

Epoch 1/10
1875/1875 [=====] - 3s 1ms/step - loss: 0.5885 - accuracy: 0.8305
Epoch 2/10
1875/1875 [=====] - 3s 2ms/step - loss: 0.2948 - accuracy: 0.9146
Epoch 3/10
1875/1875 [=====] - 3s 2ms/step - loss: 0.2495 - accuracy: 0.9280
Epoch 4/10
1875/1875 [=====] - 3s 2ms/step - loss: 0.2237 - accuracy: 0.9355
Epoch 5/10
1875/1875 [=====] - 3s 1ms/step - loss: 0.2065 - accuracy: 0.9398
Epoch 6/10
1875/1875 [=====] - 3s 1ms/step - loss: 0.1955 - accuracy: 0.9422
Epoch 7/10
1875/1875 [=====] - 3s 2ms/step - loss: 0.1868 - accuracy: 0.9445
Epoch 8/10
1875/1875 [=====] - 3s 1ms/step - loss: 0.1808 - accuracy: 0.9465
Epoch 9/10
1875/1875 [=====] - 3s 1ms/step - loss: 0.1751 - accuracy: 0.9477
Epoch 10/10
1875/1875 [=====] - 3s 2ms/step - loss: 0.1703 - accuracy: 0.9490

```

## Print the overall accuracy of the trained model

```

In [12]: from sklearn.metrics import accuracy_score
# Measure the accuracy of the model
test_loss, test_acc = model.evaluate(x_test, y_test)
print(f"Test Accuracy: {test_acc}")

```

```

313/313 [=====] - 1s 1ms/step - loss: 0.1468 - accuracy: 0.9551
Test Accuracy: 0.9550999999046326

```

# Configuring Catapult AI NN and generating the C++ model

## Configure Catapult AI NN

Create the configuration object that controls the Python to C++ translation. This step will save the model as a .json file, the weights and biases as an .h5 file, and the input feature data and output predictions as text files for use by the C++ testbench.

```

In [13]: # General project settings
config_ccs = catapult_ai_nn.config_for_dataflow(model=model, x_test=x_test, y_test=y_test,
default_precision='ac_fixed<16,6>', max_precision=1,
default_reuse_factor=1,
output_dir='my-' + model.name + '-Catapult-test',
tech='asic',
asiclibs='saed32rvt_tt0p78v125c_beh',
clock_period=10,
io_type='io_stream',
csim=0, SCVerify=0, Synth=1)

```

```

# Specific architecture settings
# Configure input feature precision since it is known
config_ccs['HLSConfig']['LayerName']['input1']['Precision'] = 'ac_fixed<8,1,true>'
# Performance strategy is set to latency mode
config_ccs['HLSConfig']['Model']['Strategy'] = 'Latency'

```

Warning: output directory "my-mnist\_notebook-Catapult-test" already exists  
 Saving neural network model "mnist\_notebook" as JSON file "my-mnist\_notebook-Catapult-test/mnist\_notebook.json"  
 Saving neural network model weights as H5 file "my-mnist\_notebook-Catapult-test/mnist\_notebook\_weights.h5"  
 Saving C++ testbench data files as "my-mnist\_notebook-Catapult-test/tb\_input\_features.dat" and "my-mnist\_notebook-Catapult-test/tb\_output\_predictions.dat"  
 2/2 [=====] - 0s 3ms/step  
 Interpreting Sequential  
 Topology:  
 Layer name: input1, layer type: InputLayer, input shapes: [[None, 14, 14, 1]], output shape: [None, 14, 14, 1]  
 Layer name: conv2d1, layer type: Conv2D, input shapes: [[None, 14, 14, 1]], output shape: [None, 4, 4, 5]  
 Layer name: batchnorm1, layer type: BatchNormalization, input shapes: [[None, 4, 4, 5]], output shape: [None, 4, 4, 5]  
 Layer name: relu1, layer type: Activation, input shapes: [[None, 4, 4, 5]], output shape: [None, 4, 4, 5]  
 Layer name: flatten1, layer type: Reshape, input shapes: [[None, 4, 4, 5]], output shape: [None, 80]  
 Layer name: dense1, layer type: Dense, input shapes: [[None, 80]], output shape: [None, 10]  
 Layer name: softmax1, layer type: Softmax, input shapes: [[None, 10]], output shape: [None, 10]

## Refinements to the HLS4ML configuration

There are several branches in the cells below based on the model architecture chosen at the top of this notebook

```

In [14]: # Potentially make refinements to the configuration
enable_customization = False
if enable_customization:
    if model_arch == 1:
        config_ccs['HLSConfig']['LayerName']['conv2d1']['ReuseFactor'] = 25
        config_ccs['HLSConfig']['LayerName']['dense1']['ReuseFactor'] = 10
    if model_arch == 2:
        config_ccs['HLSConfig']['LayerName']['conv2d1']['ReuseFactor'] = 25
        config_ccs['HLSConfig']['LayerName']['maxpool1']['ReuseFactor'] = 2
        config_ccs['HLSConfig']['LayerName']['conv2d2']['ReuseFactor'] = 25
        config_ccs['HLSConfig']['LayerName']['maxpool2']['ReuseFactor'] = 2
        config_ccs['HLSConfig']['LayerName']['dense1']['ReuseFactor'] = 2

```

```

In [15]: import json
# Print out the final HLS4ML configuration
print(json.dumps(config_ccs, indent=4))

```

```

{
  "OutputDir": "my-mnist_notebook-Catapult-test",
  "ProjectName": "myproject",
  "Backend": "Catapult",
  "Version": "1.0.0",
  "Technology": "asic",
  "ASICLibs": "saed32rvttt0p78v125c_beh",
  "FIFO": "Xilinx_FIFO.FIFO_SYNC",
  "ASICFIFO": "hls4ml_lib.mgc_pipe_mem",
  "ClockPeriod": 10,
  "IOType": "io_stream",
  "ProjectDir": "Catapult",
  "HLSConfig": {
    "Model": {
      "Precision": {
        "default": "ac_fixed<16,6>",
        "maximum": "ac_fixed<16,6>"
      },
      "ReuseFactor": 1,
      "Strategy": "Latency",
      "BramFactor": 1000000000,
      "TraceOutput": false
    },
    "LayerName": {
      "input1": {
        "LayerClassName": "InputLayer",
        "Trace": false,
        "Precision": "ac_fixed<8,1,true>"
      },
      "conv2d1": {
        "LayerClassName": "Conv2D",
        "Trace": false,
        "Precision": {
          "result": "auto",
          "weight": "auto",
          "bias": "auto"
        },
        "NonConfigurable": {
          "in_height": 14,
          "in_width": 14,
          "n_chan": 1,
          "n_filt": 5,
          "filt_height": 5,
          "filt_width": 5,
          "stride_height": 3,
          "stride_width": 3,
          "pad_top": 0,
          "pad_bottom": 0,
          "pad_left": 0,
          "pad_right": 0
        }
      },
      "conv2d1_linear": {
        "LayerClassName": "linear",
        "Trace": false,
        "Precision": {
          "result": "auto"
        },
        "NonConfigurable": {
          "in_height": 4,
          "in_width": 4,
          "n_chan": 5
        }
      },
      "batchnorm1": {
        "LayerClassName": "BatchNormalization",

```

```

        "Trace": false,
        "Precision": {
            "result": "auto",
            "scale": "auto",
            "bias": "auto"
        },
        "NonConfigurable": {
            "n_filt": 5
        }
    },
    "relu1": {
        "LayerClassName": "relu",
        "Trace": false,
        "Precision": {
            "result": "auto"
        },
        "NonConfigurable": {
            "in_height": 4,
            "in_width": 4,
            "n_chan": 5
        }
    },
    "flatten1": {
        "LayerClassName": "Reshape",
        "Trace": false,
        "Precision": {
            "result": "auto"
        }
    },
    "dense1": {
        "LayerClassName": "Dense",
        "Trace": false,
        "Precision": {
            "result": "auto",
            "weight": "auto",
            "bias": "auto"
        }
    },
    "dense1_linear": {
        "LayerClassName": "linear",
        "Trace": false,
        "Precision": {
            "result": "auto"
        }
    },
    "softmax1": {
        "LayerClassName": "Softmax",
        "Trace": false,
        "Precision": {
            "result": "auto"
        }
    }
},
"WriterConfig": {
    "Namespace": null,
    "WriteWeightsTxt": 1,
    "WriteTar": 0
},
"ROMLocation": "Local",
"MemType": null,
"PortType": null,
"CopyNNET": false,
"CModelDefaultThreshold": 0.0,
"BuildOptions": {
    "csim": 0,

```

```

        "SCVerify": 0,
        "Synth": 1,
        "vhdl": 1,
        "verilog": 1,
        "RTLSynth": 0,
        "RandomTBFrames": 2,
        "PowerEst": 0,
        "PowerOpt": 0,
        "BuildBUP": 0,
        "BUPWorkers": 0,
        "LaunchDA": 0
    },
    "InputData": "my-mnist_notebook-Catapult-test/tb_input_features.dat",
    "OutputPredictions": "my-mnist_notebook-Catapult-test/tb_output_predictions.dat",
    "KerasJson": "my-mnist_notebook-Catapult-test/mnist_notebook.json",
    "KerasH5": "my-mnist_notebook-Catapult-test/mnist_notebook_weights.h5"
}

```

## Generate the Catapult AI NN model view

Use the Catapult AI NN configuration object to construct an HLS4ML representation of the model

```

In [16]: # Finally, generate the C++ model and HLS script
hls_model_ccs = catapult_ai_nn.generate_dataflow(model=model, config_ccs=config_ccs)

```

Creating HLS model

WARNING: Layer conv2d1 requires "dataflow" pipeline style. Switching to "dataflow" pipeline style.

## Write and Compile the C++

Compile the C++ model into a shared object that can be called from Python. Note that the compile() method forces HLS4ML to write the C++ design and script to disk

```

In [17]: # Compile the C++ model
hls_model_ccs.compile()

```

Writing HLS project

```

... skipping copy of NNET headers from /user/dgb/sb/sif/aol/Mgc_home/shared/include/nn
et_utils/
... skipping copy of ac_types headers - assumed to located in Catapult install tree
... skipping copy of ac_math headers - assumed to located in Catapult install tree
... skipping copy of ac_simutils headers - assumed to located in Catapult install tree
Done

```

## Measure the accuracy of the C++ model

Run the test images through the C++ model and measure the accuracy

```

In [18]: # Measure the accuracy of the C++ model against the Python model
ccs_hls_model_predictions = hls_model_ccs.predict(x_test)
print('QKeras Model Accuracy : {}'.format(accuracy_score(np.argmax(y_test, axis=1), n
print('C++      Model Accuracy : {}'.format(accuracy_score(np.argmax(y_test, axis=1), n

```

313/313 [=====] - 0s 992us/step

QKeras Model Accuracy : 0.9551

C++ Model Accuracy : 0.8927

# Synthesizing the C++ into hardware with Catapult

Now synthesize the C++ model into hardware with Catapult

```
In [19]: # Run HLS to generate the RTL  
hls_model_ccs.build()
```

```

Catapult backend build() option overrides: "reset=False"
/user/dgb/sb/sif/aol/Mgc_home/bin/catapult -product ultra -shell -f build_prj.tcl -eval
'set ::argv "reset=False"'
// Catapult Ultra Synthesis 2025.1/1149870 (Nightly Build) Fri Dec 13 09:29:58 PST 20
24
//
// Copyright (c) Siemens EDA, 1996-2024, All Rights Reserved.
// UNPUBLISHED, LICENSED SOFTWARE.
// CONFIDENTIAL AND PROPRIETARY INFORMATION WHICH IS THE
// PROPERTY OF SIEMENS EDA OR ITS LICENSORS.
//
// Running on Linux dgb@orw-dgb-rk8:3000869 4.18.0-553.22.1.el8_10.x86_64 x86_64 aol
//
// Package information: SIFLIBS v28.1_0.0, HLS_PKGS v28.1_0.0,
// SIF_TOOLKITS v28.1_0.0, SIF_XILINX v28.1_0.0,
// SIF_ALTERA v28.1_0.0, CCS_LIBS v28.1_0.0,
// CDS_PPRO v2024.1_3, CDS_DesignChecker v2024.2_1,
// CDS_OASYS v21.1_3.1, CDS_PSR v24.2_0.4,
// DesignPad v2.78_1.0, DesignAnalyzer 2025.1/1145558
//
# Connected to license server 1700@orw-csd-lic-00 (LIC-13)
# Catapult product license successfully checked out, elapsed time 00:02 (LIC-14)
# Custom Startup HOME/catapult.tcl
# Working Directory: '/home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tutorial/my-mnist_
notebook-Catapult-test'
do file ./build_prj.tcl
# > array set BuildOptions {
# > reset 0
# > csim 0
# > SCVerify 0
# > Synth 1
# > vhdl 1
# > verilog 1
# > RTLSynth 0
# > RandomTBFrames 2
# > PowerEst 0
# > PowerOpt 0
# > BuildBUP 0
# > BUPWorkers 0
# > LaunchDA 0
# > }
# > set sfd [file dirname [info script]]
# .
# > if { [info exists ::argv] } {
# > foreach arg $::argv {
# > foreach {optname optval} [split $arg '='] {}
# > set mapping {"cosim" "SCVerify" "validation" "SCVerify" "synth" "Synth" "vsynt
h" "RTLSynth" "ran_frame" "RandomTBFrames" "sw_opt" "PowerEst" "power" "PowerOpt" "da"
"LaunchDA" "bup" "BuildBUP"}
# > set pos [lsearch -exact $mapping $optname]
# > if { ($pos != -1) && ([expr $pos % 2] == 0) } {
# > set oldoptname $optname
# > set optname [lindex $mapping [expr $pos + 1]]
# > logfile message "HLS4ML build() option '$oldoptname' is being depricated. Us
e '$optname'\n" warning
# > }
# > if { [info exists BuildOptions($optname)] } {
# > if {[string is integer -strict $optval]} {
# > set BuildOptions($optname) $optval
# > } else {
# > set BuildOptions($optname) [string is true -strict $optval]
# > }
# > } else {
# > logfile message "Unknown argv switch '$optname'\n" error
# > }
# > }

```

```

# > }
# > puts "***** INVOKE OPTIONS *****"
# ***** INVOKE OPTIONS *****
# > foreach x [lsort [array names BuildOptions]] {
# >   puts "[format {   %-20s %s} $x $BuildOptions($x)]"
# > }
#   BUPWorkers           0
#   BuildBUP             0
#   LaunchDA             0
#   PowerEst             0
#   PowerOpt             0
#   RTLSynth            0
#   RandomTBFrames       2
#   SCVerify            0
#   Synth               1
#   csim                0
#   reset               0
#   verilog             1
#   vhdl                1
# > puts ""
#
# > proc report_time { op_name time_start time_end } {
# >   set time_taken [expr $time_end - $time_start]
# >   set time_s [expr ($time_taken / 1000) % 60]
# >   set time_m [expr ($time_taken / (1000*60)) % 60]
# >   set time_h [expr ($time_taken / (1000*60*60)) % 24]
# >   puts "***** ${op_name} COMPLETED IN ${time_h}h${time_m}m${time_s}s *****"
# > }
# > proc setup_xilinx_part { part } {
# >   global env
# >
# >   set part_sav $part
# >   set libname [lindex [library get /CONFIG/PARAMETERS/Vivado/PARAMETERS/Xilinx/PARAMETERS/*/PARAMETERS/*/PARAMETERS/$part/LIBRARIES/*/NAME -match glob -ret v] 0]
# >   puts "Library Name: $libname"
# >   if { [llength $libname] == 1 } {
# >     set libpath [library get /CONFIG/PARAMETERS/Vivado/PARAMETERS/Xilinx/PARAMETERS/*/PARAMETERS/*/PARAMETERS/$part/LIBRARIES/*/NAME -match glob -ret p]
# >     puts "Library Path: $libpath"
# >     if { [regexp {/CONFIG/PARAMETERS/(\S+)/PARAMETERS/(\S+)/PARAMETERS/(\S+)/PARAMETERS/(\S+)/PARAMETERS/(\S+)/PARAMETERS/(\S+)/.*} $libpath dummy rtltool vendor family speed part] } {
# >       solution library add $libname -- -rtlsyntool $rtltool -vendor $vendor -family $family -speed $speed -part $part_sav
# >     } else {
# >       solution library add $libname -- -rtlsyntool Vivado
# >     }
# >   } else {
# >     logfile message "Could not find specific Xilinx base library for part '$part'. Using KINTEX-u\n" warning
# >     solution library add mgc_Xilinx-KINTEX-u-2_beh -- -rtlsyntool Vivado -manufacturer Xilinx -family KINTEX-u -speed -2 -part xcku115-flvb2104-2-i
# >   }
# >   solution library add Xilinx_RAMs
# >   solution library add Xilinx_ROMs
# >   solution library add Xilinx_FIFO
# >   if { [info exists env(XILINX_PCL_CACHE)] } {
# >     options set /Flows/Vivado/PCL_CACHE $env(XILINX_PCL_CACHE)
# >     solution options set /Flows/Vivado/PCL_CACHE $env(XILINX_PCL_CACHE)
# >   }
# > }
# > proc setup_asic_libs { args } {
# >   set do_saed 0
# >   foreach lib $args {
# >     solution library add $lib -- -rtlsyntool DesignCompiler
# >     if { [lsearch -exact {saed32hvt_tt0p78v125c_beh saed32lvt_tt0p78v125c_beh saed32rvt_tt0p78v125c_beh} $lib] != -1 } {

```

```

# > set do_saed 1
# > }
# > }
# > solution library add ccs_sample_mem
# > solution library add ccs_sample_rom
# > solution library add hls4ml_lib
# > go libraries
# >
# > if { $do_saed } {
# >     source [application get /SYSTEM/ENV_MGC_HOME]/pkgs/siflibs/saed/setup_saedlib.tcl
# > }
# > }
# > options set Input/CppStandard {c++17}
# c++17
# > options set Input/CompilerFlags -DRANDOM_FRAMES=$BuildOptions(RandomTBFrames)
# -DRANDOM_FRAMES=2
# > options set Input/SearchPath {$MGC_HOME/shared/include/nnet_utils} -append
# {$MGC_HOME/shared/include/nnet_utils}
# > options set ComponentLibs/SearchPath {$MGC_HOME/shared/pkgs/ccs_hls4ml} -append
# {$MGC_HOME/pkgs/siflibs} {$MGC_HOME/shared/include/calypso_mem} {$MGC_HOME/pkgs/siflibs/nangate} {$MGC_HOME/pkgs/siflibs/saed} {$MGC_HOME/pkgs/siflibs/dware} {$MGC_HOME/pkgs/ccs_altera} {$MGC_HOME/pkgs/ccs_xilinx} {$MGC_HOME/pkgs/ccs_achronix} {$MGC_HOME/pkgs/siflibs/origami} {$MGC_HOME/pkgs/siflibs/microsemi} {$MGC_HOME/pkgs/ccs_lattice} {$MGC_HOME/pkgs/ccs_nx} {$MGC_HOME/pkgs/ccs_libs/interfaces/amba} {$MGC_HOME/pkgs/siflibs/ccs_fpga} {$MGC_HOME/pkgs/siflibs_inhouse} {$MGC_HOME/shared/pkgs/ccs_hls4ml}
# > if {$BuildOptions(reset)} {
# >     project load Catapult.ccs
# >     go new
# > } else {
# >     project new -name Catapult
# > }
# > options set Message/ErrorOverride HIER-10 -remove
# ASM-11 ASM-48 ASM-63 ASM-69 ASSERT-1 CIN-8 CIN-17 CIN-46 CIN-48 CIN-49 CIN-50 CIN-54 CIN-84 CIN-87 CIN-109 CIN-110 CIN-111 CIN-112 CIN-188 CIN-214 CIN-243 CIN-244 CLUSTER-3 CNS-9 CRAAS-21 DIR-24 DIR-32 HIER-2 HIER-20 HIER-45 IFSYN-6 INCR-13 INCR-14 INCR-15 LIB-194 LIB-204 LIB-211 LIB-224 LOOP-21 MEM-65 MEM-78 MEM-82 MEM-83 MEM-88 MGEN-16 NL-21 NL-26 NL-30 NL-35 OPT-25 READ-8 READ-9 SCHD-37 SCHD-54 SCHD-55 SIF-6 SIF-17 SIF-20
# > solution options set Message/ErrorOverride HIER-10 -remove
# ASM-11 ASM-48 ASM-63 ASM-69 ASSERT-1 CIN-8 CIN-17 CIN-46 CIN-48 CIN-49 CIN-50 CIN-54 CIN-84 CIN-87 CIN-109 CIN-110 CIN-111 CIN-112 CIN-188 CIN-214 CIN-243 CIN-244 CLUSTER-3 CNS-9 CRAAS-21 DIR-24 DIR-32 HIER-2 HIER-20 HIER-45 IFSYN-6 INCR-13 INCR-14 INCR-15 LIB-194 LIB-204 LIB-211 LIB-224 LOOP-21 MEM-65 MEM-78 MEM-82 MEM-83 MEM-88 MGEN-16 NL-21 NL-26 NL-30 NL-35 OPT-25 READ-8 READ-9 SCHD-37 SCHD-54 SCHD-55 SIF-6 SIF-17 SIF-20
# > options set Message/Hide HIER-10 -append
# LIB-207 LIB-217 CRD-177 HIER-10
# > if {$BuildOptions(vhdl)} {
# >     options set Output/OutputVHDL true
# > } else {
# >     options set Output/OutputVHDL false
# > }
# true
# > if {$BuildOptions(verilog)} {
# >     options set Output/OutputVerilog true
# > } else {
# >     options set Output/OutputVerilog false
# > }
# true
# > if { [info exists ::env(XILINX_PCL_CACHE)] } {
# >     options set /Flows/Vivado/PCL_CACHE $::env(XILINX_PCL_CACHE)
# >     solution options set /Flows/Vivado/PCL_CACHE $::env(XILINX_PCL_CACHE)
# > }
# /wv/hlstools/lib/2023.2/vivado_2023.2/xilinx_cache
# > catch {flow package require /HLS4ML}
# 0
# > flow package require /SCVerify

```

```

# 10.4
# > flow package option set /SCVerify/INVOKE_ARGS "$sfd/firmware/weights $sfd/tb_data/
tb_input_features.dat $sfd/tb_data/tb_output_predictions.dat 0.0"
# ./firmware/weights ./tb_data/tb_input_features.dat ./tb_data/tb_output_predictions.d
at 0.0
# > set design_top myproject
# myproject
# > solution file add $sfd/firmware/myproject.cpp
# /INPUTFILES/1
# > solution file add $sfd/myproject_test.cpp -exclude true
# /INPUTFILES/2
# > set Strategy latency
# latency
# > set IOType io_stream
# io_stream
# > if { ![file exists $sfd/hls4ml_config.yml] } {
# >   logfile message "Could not locate HLS4ML configuration file '$sfd/hls4ml_config.
yml'. Unable to determine network configuration.\n" warning
# > } else {
# >   set pf [open "$sfd/hls4ml_config.yml" "r"]
# >   while {![eof $pf]} {
# >     gets $pf line
# >     if { [regexp {\s+Strategy: (\w+)} $line all value] }      { set Strategy [strin
g tolower $value] }
# >     if { [regexp {IOType: (\w+)} $line all value] }          { set IOType [string
tolower $value] }
# >   }
# >   close $pf
# > }
# > if { $IOType == "io_stream" } {
# > solution options set Architectural/DefaultRegisterThreshold 2050
# > }
# 2050
# > directive set -RESET_CLEAR_ALL_REGS no
# /RESET_CLEAR_ALL_REGS no
# > directive set -MEM_MAP_THRESHOLD [expr 2048 * 16 + 1]
# /MEM_MAP_THRESHOLD 32769
# > set hls_clock_period 10
# 10
# > go analyze
# Info: Starting transformation 'analyze' on solution 'solution.v1' (SOL-8)
# Creating project directory '/home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tutorial/m
y-mnist_notebook-Catapult-test/Catapult/'. (PRJ-1)
# Moving session transcript to file "/home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tut
orial/my-mnist_notebook-Catapult-test/catapult.log"
# Front End called with arguments: -I/user/dgb/sb/sif/aol/Mgc_home/shared/include/nnet
_utils -- /home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tutorial/my-mnist_notebook-Cat
apult-test/firmware/myproject.cpp (CIN-69)
# Edison Design Group C++/C Front End - Version 6.6 (CIN-1)
# Warning: $PROJECT_HOME/firmware/parameters.h(118): integer conversion resulted in a
change of sign (CRD-68)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(120): Pragma 'hls_design<>'
detected on routine 'nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>' (CIN-6)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(59): Pragma 'hls_design
<>' detected on routine 'nnet::relu<conv2d1_result_t, layer5_t, relu_config5>' (CIN-6)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(82): Pragma 'hls_design<>' d
etected on routine 'nnet::dense<layer5_t, densel_result_t, config7>' (CIN-6)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(416): Pragma 'hls_desig
n<>' detected on routine 'nnet::softmax<densel_result_t, result_t, softmax_config9>'
(CIN-6)
# $PROJECT_HOME/firmware/myproject.cpp(17): Pragma 'hls_design<top>' detected on routi
ne 'myproject' (CIN-6)
# $MGC_HOME/shared/include/ac_std_float.h(192): Pragma 'hls_design<>' detected on rout
ine 'ac::fx_div<8>' (CIN-6)
# Warning: $MGC_HOME/shared/include/ac_math/ac_softmax_pwl.h(136): Cannot bind pragma
'hls_waive APT' to any valid construct. Please check if a valid construct follows the

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pragma. (CIN-319)
# Warning: $MGC_HOME/shared/include/ac_math/ac_shift.h(345): Cannot bind pragma 'hls_w
aive ISE' to any valid construct. Please check if a valid construct follows the pragn
a. (CIN-319)
# Warning: $MGC_HOME/shared/include/ac_math/ac_shift.h(184): Cannot bind pragma 'hls_w
aive ISE' to any valid construct. Please check if a valid construct follows the pragn
a. (CIN-319)
# Source file analysis completed (CIN-68)
# Info: Completed transformation 'analyze' on solution 'solution.v1': elapsed time 6.7
9 seconds, memory usage 1664596kB, peak memory usage 1664596kB (SOL-9)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno
=24 (DAPM-15)
# > if { $IOType == "io_parallel" } {
# >   set inlines {}
# >   set pooling2d_used 0
# >   foreach fn [solution get /SOURCEHIER/FUNC_HBS/* -match glob -ret l -checkpath 0]
# >   {
# >     if { [string match {nnet::*} $fn] } { lappend inlines $fn }
# >     if { [string match {nnet::pooling2d_cl*} $fn] } { set pooling2d_used 1 }
# >     if { [string match {ac::fx_div*} $fn] } { lappend inlines $fn }
# >   }
# >   foreach fn $inlines {
# >     set old [solution design get $fn]
# >     logfile message "solution design set $fn -inline\n" warning
# >     solution design set $fn -inline
# >   }
# >   if { $pooling2d_used } {
# >     directive set -SCHED_USE_MULTICYCLE true
# >   }
# > }
# > if { ! $BuildOptions(BuildBUP) } {
# >
# > go compile
# >
# > if { $BuildOptions(csim) } {
# >   puts "***** C SIMULATION *****"
# >   set time_start [clock clicks -milliseconds]
# >   flow run /SCVerify/launch_make ./scverify/Verify_orig_cxx_osc_i.mk {} SIMT00L=osc
i sim
# >   set time_end [clock clicks -milliseconds]
# >   report_time "C SIMULATION" $time_start $time_end
# > }
# >
# > puts "***** SETTING TECHNOLOGY LIBRARIES *****"
# > setup_asic_libs {saed32rvt_tt0p78v125c_beh}
# >
# > directive set -CLOCKS [list clk [list -CLOCK_PERIOD $hls_clock_period -CLOCK_EDGE
rising -CLOCK_OFFSET 0.000000 -CLOCK_UNCERTAINTY 0.0 -RESET_KIND sync -RESET_SYNC_NAM
E rst -RESET_SYNC_ACTIVE high -RESET_ASYNC_NAME arst_n -RESET_ASYNC_ACTIVE low -ENABLE
_NAME {} -ENABLE_ACTIVE high]]
# >
# > if { $BuildOptions(Synth) } {
# >   puts "***** C/RTL SYNTHESIS *****"
# >   set time_start [clock clicks -milliseconds]
# >
# >   go assembly
# >
# >   go architect
# >
# >   go allocate
# >
# >   go schedule
# >
# >   go extract
# >   set time_end [clock clicks -milliseconds]
# >   report_time "C/RTL SYNTHESIS" $time_start $time_end

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# > }
# >
# > } else {
# >   go analyze
# >
# >   directive set -CLOCKS [list clk [list -CLOCK_PERIOD $hls_clock_period -CLOCK_EDGE rising -CLOCK_OFFSET 0.000000 -CLOCK_UNCERTAINTY 0.0 -RESET_KIND sync -RESET_SYNC_NAME rst -RESET_SYNC_ACTIVE high -RESET_ASYNC_NAME arst_n -RESET_ASYNC_ACTIVE low -ENABLE_NAME {} -ENABLE_ACTIVE high]]
# >
# >   set blocks [solution get /HIERCONFIG/USER_HBS/*/RESOLVED_NAME -match glob -rec 1 -ret v -state analyze]
# >   set bu_mappings {}
# >   set top [lindex $blocks 0]
# >   foreach block [lreverse [lrange $blocks 1 end]] {
# >     if { [string match {nnet::*} $block] == 0 } { continue }
# >     go analyze
# >     solution design set $block -top
# >     go compile
# >     solution library remove *
# >     puts "***** SETTING TECHNOLOGY LIBRARIES *****"
# > setup_asic_libs {saed32rvt_tt0p78v125c_beh}
# >     go extract
# >     set block_soln "[solution get /TOP/name -checkpath 0].[solution get /VERSION -checkpath 0]"
# >     lappend bu_mappings [solution get /CAT_DIR] /$top/$block "[Block\] $block_soln"
# >   }
# >
# >   go analyze
# >   solution design set $top -top
# >   go compile
# >
# >   if {$BuildOptions(csim)} {
# >     puts "***** C SIMULATION *****"
# >     set time_start [clock clicks -milliseconds]
# >     flow run /SCVerify/launch_make ./scverify/Verify_orig_cxx_osci.mk {} SIMTOOL=osci sim
# >     set time_end [clock clicks -milliseconds]
# >     report_time "C SIMULATION" $time_start $time_end
# >   }
# >   foreach {d i l} $bu_mappings {
# >     logfile message "solution options set ComponentLibs/SearchPath $d -append\n" info
# >     solution options set ComponentLibs/SearchPath $d -append
# >   }
# >
# >   puts "***** SETTING TECHNOLOGY LIBRARIES *****"
# >   solution library remove *
# > setup_asic_libs {saed32rvt_tt0p78v125c_beh}
# >   go compile
# >   foreach {d i l} $bu_mappings {
# >     logfile message "solution library add [list $l]\n" info
# >     eval solution library add [list $l]
# >   }
# >   go libraries
# >
# >   foreach {d i l} $bu_mappings {
# >     set cnt [directive get $i/* -match glob -checkpath 0 -ret p]
# >     if { $cnt != {} } {
# >       logfile message "directive set $i -MAP_TO_MODULE [list $l]\n" info
# >       eval directive set $i -MAP_TO_MODULE [list $l]
# >     }
# >   }
# >
# >   go assembly
# >   set design [solution get -name]

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# > logfile message "Adjusting FIFO_DEPTH for top-level interconnect channels\n" warning
# > foreach ch_fifo_m2m [directive get -match glob -checkpath 0 -ret p $design/*_out:cns/MAP_TO_MODULE] {
# >     set ch_fifo [join [lrange [split $ch_fifo_m2m '/'] 0 end-1] /]/FIFO_DEPTH
# >     logfile message "directive set -match glob $ch_fifo 1\n" info
# >     directive set -match glob "$ch_fifo" 1
# > }
# > foreach ch_fifo_m2m [directive get -match glob -checkpath 0 -ret p $design/*_cnp*:cns/MAP_TO_MODULE] {
# >     set ch_fifo [join [lrange [split $ch_fifo_m2m '/'] 0 end-1] /]/FIFO_DEPTH
# >     logfile message "Bypass FIFO '$ch_fifo' depth set to 1 - larger value may be required to prevent deadlock\n" warning
# >     logfile message "directive set -match glob $ch_fifo 1\n" info
# >     directive set -match glob "$ch_fifo" 1
# > }
# > go architect
# > go allocate
# > go schedule
# > go dpfsm
# > go extract
# > }
# Info: Starting transformation 'compile' on solution 'myproject.v1' (SOL-8)
# Generating synthesis internal form... (CIN-3)
# $MGC_HOME/shared/include/ac_std_float.h(196): Found design routine 'ac::fx_div<8>' specified by directive (CIN-52)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Found design routine 'nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>' specified by directive (CIN-52)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Found design routine 'nnet::relu<conv2d1_result_t, layer5_t, relu_config5>' specified by directive (CIN-52)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Found design routine 'nnet::dense<layer5_t, densel_result_t, config7>' specified by directive (CIN-52)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Found design routine 'nnet::softmax<densel_result_t, result_t, softmax_config9>' specified by directive (CIN-52)
# $PROJECT_HOME/firmware/myproject.cpp(21): Found top design routine 'myproject' specified by directive (CIN-52)
# $PROJECT_HOME/firmware/myproject.cpp(21): Synthesizing routine 'myproject' (CIN-13)
# $PROJECT_HOME/firmware/myproject.cpp(21): Inlining routine 'myproject' (CIN-14)
# $PROJECT_HOME/firmware/myproject.cpp(69): Pragma 'hls_resource<layer7_out:cns>' detected, variable = 'layer7_out', module = 'hls4ml_lib.mgc_pipe_mem FIFO_DEPTH = 1' (CIN-341)
# $PROJECT_HOME/firmware/myproject.cpp(69): Pragma 'hls_resource<layer7_out:cns>' detected, variables = 'layer7_out', module = 'hls4ml_lib.mgc_pipe_mem' (CIN-9)
# $PROJECT_HOME/firmware/myproject.cpp(63): Pragma 'hls_resource<layer5_out:cns>' detected, variable = 'layer5_out', module = 'hls4ml_lib.mgc_pipe_mem FIFO_DEPTH = 1' (CIN-341)
# $PROJECT_HOME/firmware/myproject.cpp(63): Pragma 'hls_resource<layer5_out:cns>' detected, variables = 'layer5_out', module = 'hls4ml_lib.mgc_pipe_mem' (CIN-9)
# $PROJECT_HOME/firmware/myproject.cpp(58): Pragma 'hls_resource<layer2_out:cns>' detected, variable = 'layer2_out', module = 'hls4ml_lib.mgc_pipe_mem FIFO_DEPTH = 1' (CIN-341)
# $PROJECT_HOME/firmware/myproject.cpp(58): Pragma 'hls_resource<layer2_out:cns>' detected, variables = 'layer2_out', module = 'hls4ml_lib.mgc_pipe_mem' (CIN-9)
# $PROJECT_HOME/firmware/myproject.cpp(20): Pragma 'hls_resource<layer9_out:rsc>' detected, variable = 'layer9_out', module = 'ccs_ioport.ccs_out_wait' (CIN-341)
# $PROJECT_HOME/firmware/myproject.cpp(20): Pragma 'hls_resource<layer9_out:rsc>' detected, variables = 'layer9_out', module = 'ccs_ioport.ccs_out_wait' (CIN-9)
# $PROJECT_HOME/firmware/myproject.cpp(19): Pragma 'hls_resource<input1:rsc>' detected, variable = 'input1', module = 'ccs_ioport.ccs_in_wait' (CIN-341)
# $PROJECT_HOME/firmware/myproject.cpp(19): Pragma 'hls_resource<input1:rsc>' detected, variables = 'input1', module = 'ccs_ioport.ccs_in_wait' (CIN-9)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Found design routine 'nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>' specified by directive (CIN-52)

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2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Found design routine
'nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>' specified by directive (CIN-5
2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Synthesizing routine
'nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>' (CIN-13)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Inlining routine 'nne
t::conv_2d_cl<input_t, conv2d1_result_t, config2>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(68): Inlining routine 'nne
t::conv_2d_buffer_cl<input_t, conv2d1_result_t, config2>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/ap_shift_reg.h(84): Inlining member function 'ap
_shift_reg<nnet::array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::value_type, 14U>::a
p_shift_reg' on object 'line_buffer' (CIN-64)
# $MGC_HOME/shared/include/nnet_utils/ap_shift_reg.h(85): Pragma 'hls_unroll<yes>' det
ected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/ap_shift_reg<nnet::
array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::value_type, 14U>::ap_shift_reg:for' (CIN-2
03)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(80): Pragma 'hls_pipeline_i
nit_interval<1>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/cor
e/ReadInputHeight' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(273): Inlining routine 'nne
t::compute_output_buffer_2d<input_t, conv2d1_result_t, config2>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(234): Inlining routine 'nne
t::shift_line_buffer<input_t, config2>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(246): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/UpdateBuffer'
(CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(19): Inlining member function 'nne
t::array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::operator[]' on object 'data' (CIN
-64)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(255): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/LineBufferDat
aIn' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(259): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/LineBufferShi
ft' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/ap_shift_reg.h(110): Inlining member function 'a
p_shift_reg<nnet::array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::value_type, 14U>::
shift' on object 'line_buffer' (CIN-64)
# $MGC_HOME/shared/include/nnet_utils/ap_shift_reg.h(116): Pragma 'hls_unroll<yes>' de
tected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/ap_shift_reg<nne
t::array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::value_type, 14U>::shift:if:for' (CIN-20
3)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(196): Inlining routine 'nne
t::kernel_shift_2d<input_t, config2>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(203): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/KernelShiftWi
dth' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(207): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/KernelShiftHe
ight' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(210): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/KernelShiftCh
annel' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(222): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/KernelPushHei
ght' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(225): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/KernelPushCha
nnel' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(14): Inlining routine 'nne
t::dense_latency<nnet::array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::value_type, n
net::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::value_type, config2::mult_conf
ig>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(57): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t, conv2d1_result_t, config2>/core/ResetAccum'

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(CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(64): Pragma 'hls_unroll<25
>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/Compute' (CIN
-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(69): Pragma 'hls_unroll<5>'
detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/MultAndAccum' (C
IN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(79): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/Result' (CIN-
203)
# $MGC_HOME/shared/include/nnet_utils/nnet_mult.h(121): Inlining routine 'nnet::cast<n
net::array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::value_type, nnet::array<ac_fixe
d<16, 6, true, AC_TRN, AC_WRAP>, 5U>::value_type, config2::mult_config>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(319): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/CastLoop' (CI
N-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(17): Inlining member function 'nne
t::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::operator[]' on object 'res_pack'
(CIN-64)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(31): Inlining routine 'nne
t::conv_2d_encoded_cl<input_t, conv2d1_result_t, config2>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(50): Pragma 'hls_pipeline_i
nit_interval<1>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/cor
e/ReadInputHeight#1' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(13): Inlining routine 'nne
t::compute_scaled_indices_2d<input_t, config2>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(60): Inlining method 'nnet::s
cale_index_regular<5U, 3U, 14U>::scale_index' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(16): Inlining routine 'nnet::
scale_index_K_gte_S<5U, 3U, 14U>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(19): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/ComputeIndex'
(CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(60): Inlining method 'nnet::s
cale_index_regular<5U, 3U, 14U>::scale_index' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(16): Inlining routine 'nnet::
scale_index_K_gte_S<5U, 3U, 14U>' (CIN-14)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(26): Instantiating
global variable 'pixels' which may be accessed outside this scope (CIN-18)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(131): Inlining routine 'nne
t::compute_output_encoded<input_t, conv2d1_result_t, config2>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(141): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/MultLoop' (CI
N-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(140): Pragma 'hls_pipeline_in
it_interval<1>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/
MultLoop' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(19): Inlining member function 'nne
t::array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::operator[]' on object 'data' (CIN
-64)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(80): Inlining routine 'nnet::
mult_buffer<input_t, conv2d1_result_t, config2>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(91): Pragma 'hls_unroll<yes>'
detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/InitData' (CIN-2
03)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(14): Inlining routine 'nne
t::dense_latency<nnet::array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::value_type, n
net::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::value_type, config2::mult_conf
ig>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(57): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/ResetAccum#1'
(CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(64): Pragma 'hls_unroll<25
>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/Compute#1' (C
IN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(69): Pragma 'hls_unroll<5>'

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detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/MultAndAccum#1'
(CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(79): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/Result#1' (CI
N-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_mult.h(121): Inlining routine 'nnet::cast<n
net::array<ac_fixed<8, 1, true, AC_TRN, AC_WRAP>, 1U>::value_type, nnet::array<ac_fixe
d<16, 6, true, AC_TRN, AC_WRAP>, 5U>::value_type, config2::mult_config>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(107): Pragma 'hls_unroll<yes
>' detected on '/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/CastLoop#1'
(CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(17): Inlining member function 'nne
t::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::operator[]' on object 'res_pack'
(CIN-64)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Optimizing block '/nn
et::conv_2d_cl<input_t,conv2d1_result_t,config2>' ... (CIN-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(123): INOUT port 'data' is
only used as an input. (OPT-10)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(123): INOUT port 'res' is o
nly used as an output. (OPT-11)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(124): INOUT port 'weights'
is only used as an input. (OPT-10)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(125): INOUT port 'biases' i
s only used as an input. (OPT-10)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window' is never driven.
(OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(0)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(1)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(2)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(3)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(4)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(5)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(6)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(7)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(8)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(9)' is never drive
n. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(10)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(11)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(12)' is never driv
en. (OPT-3)

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# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(13)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(14)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(15)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(16)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(17)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(18)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(19)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(20)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(21)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(22)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(23)' is never driv
en. (OPT-3)
# Warning: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(38): Channel 'nne
t::conv_2d_encoded_cl<input_t,conv2d1_result_t,config2>:data_window(24)' is never driv
en. (OPT-3)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(248): Loop '/nnet::conv_2d_cl
<input_t,conv2d1_result_t,config2>/core/UpdateBuffer' iterated at most 1 times. (LOOP-
2)
# $MGC_HOME/shared/include/nnet_utils/ap_shift_reg.h(117): Loop '/nnet::conv_2d_cl<inp
ut_t,conv2d1_result_t,config2>/core/ap_shift_reg<nnet::array<ac_fixed<8,1,true,AC_TRN,
AC_WRAP>,1U>::value_type,14U>::shift:if:for' iterated at most 13 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(261): Loop '/nnet::conv_2d_cl
<input_t,conv2d1_result_t,config2>/core/LineBufferShift' iterated at most 4 times. (LO
OP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(257): Loop '/nnet::conv_2d_cl
<input_t,conv2d1_result_t,config2>/core/LineBufferDataIn' iterated at most 1 times. (L
OOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(212): Loop '/nnet::conv_2d_cl
<input_t,conv2d1_result_t,config2>/core/KernelShiftChannel' iterated at most 1 times.
(LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(209): Loop '/nnet::conv_2d_cl
<input_t,conv2d1_result_t,config2>/core/KernelShiftHeight' iterated at most 5 times.
(LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(205): Loop '/nnet::conv_2d_cl
<input_t,conv2d1_result_t,config2>/core/KernelShiftWidth' iterated at most 4 times. (L
OOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(227): Loop '/nnet::conv_2d_cl
<input_t,conv2d1_result_t,config2>/core/KernelPushChannel' iterated at most 1 times.
(LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(224): Loop '/nnet::conv_2d_cl
<input_t,conv2d1_result_t,config2>/core/KernelPushHeight' iterated at most 5 times. (L
OOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(59): Loop '/nnet::conv_2d_c
l<input_t,conv2d1_result_t,config2>/core/ResetAccum' iterated at most 5 times. (LOOP-
2)

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# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(71): Loop '/nnet::conv_2d_c
l<input_t,conv2d1_result_t,config2>/core/MultAndAccum' iterated at most 5 times. (LOOP
-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(66): Loop '/nnet::conv_2d_c
l<input_t,conv2d1_result_t,config2>/core/Compute' iterated at most 25 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(81): Loop '/nnet::conv_2d_c
l<input_t,conv2d1_result_t,config2>/core/Result' iterated at most 5 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(321): Loop '/nnet::conv_2d_cl
<input_t,conv2d1_result_t,config2>/core/CastLoop' iterated at most 5 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(84): Loop '/nnet::conv_2d_c
l<input_t,conv2d1_result_t,config2>/core/ReadInputWidth' iterated at most 14 times. (L
OOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(82): Loop '/nnet::conv_2d_c
l<input_t,conv2d1_result_t,config2>/core/ReadInputHeight' iterated at most 14 times.
 (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Found design routi
ne 'nnet::relu<conv2d1_result_t, layer5_t, relu_config5>' specified by directive (CIN-
52)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Found design routi
ne 'nnet::relu<conv2d1_result_t, layer5_t, relu_config5>' specified by directive (CIN-
52)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Synthesizing routi
ne 'nnet::relu<conv2d1_result_t, layer5_t, relu_config5>' (CIN-13)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Inlining routine
'nnet::relu<conv2d1_result_t, layer5_t, relu_config5>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(61): Pragma 'hls_pipeli
ne_init_interval<1>' detected on '/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/
core/ReLUActLoop' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(70): Pragma 'hls_unroll
<yes>' detected on '/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core/ReLUPackL
oop' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(17): Inlining member function 'nne
t::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::operator[]' on object 'in_data'
 (CIN-64)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(17): Inlining member function 'nne
t::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::operator[]' on object 'out_data'
 (CIN-64)
# $MGC_HOME/shared/include/ac_math/ac_relu.h(111): Inlining routine 'ac_math::ac_relu<
16, 6, true, AC_TRN, AC_WRAP, 16, 6, true, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_fixed.h(1383): Inlining routine 'operator<><16, 6, true,
AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Optimizing block
'/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>' ... (CIN-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): INOUT port 'data'
is only used as an input. (OPT-10)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): INOUT port 'res' i
s only used as an output. (OPT-11)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(72): Loop '/nnet::relu<
conv2d1_result_t,layer5_t,relu_config5>/core/ReLUPackLoop' iterated at most 5 times.
 (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(63): Loop '/nnet::relu<
conv2d1_result_t,layer5_t,relu_config5>/core/ReLUActLoop' iterated at most 16 times.
 (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Found design routine 'n
net::dense<layer5_t, dense1_result_t, config7>' specified by directive (CIN-52)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Found design routine 'n
net::dense<layer5_t, dense1_result_t, config7>' specified by directive (CIN-52)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Synthesizing routine 'n
net::dense<layer5_t, dense1_result_t, config7>' (CIN-13)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(83): Pragma 'hls_pipeline_in
it_interval<1>' detected on '/nnet::dense<layer5_t,dense1_result_t,config7>/core/main'
 (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Inlining routine 'nne
t::dense<layer5_t, dense1_result_t, config7>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(83): Pragma 'hls_pipeline_in
it_interval<1>' detected on '/nnet::dense<layer5_t, dense1_result_t, config7>' (CIN-20

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# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Pragma 'hls_pipeline_in
it_interval<1>' detected on routine 'nnet::dense<layer5_t, dense1_result_t, config7>'
(CIN-329)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(70): Pragma 'hls_pipeli
ne_init_interval<1>' detected on '/nnet::dense<layer5_t,dense1_result_t,config7>/core/
DataPrepare' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(103): Pragma 'hls_unroll<yes
>' detected on '/nnet::dense<layer5_t,dense1_result_t,config7>/core/DataPack' (CIN-20
3)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(17): Inlining member function 'nne
t::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::operator[]' on object 'data_pac
k' (CIN-64)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(14): Inlining routine 'nne
t::dense_wrapper<nnet::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::value_type,
nnet::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 10U>::value_type, config7>' (CIN-
14)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(14): Inlining routine 'nne
t::dense_latency<nnet::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::value_type,
nnet::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 10U>::value_type, config7>' (CIN-
14)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(57): Pragma 'hls_unroll<yes
>' detected on '/nnet::dense<layer5_t,dense1_result_t,config7>/core/ResetAccum' (CIN-2
03)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(64): Pragma 'hls_unroll<80
>' detected on '/nnet::dense<layer5_t,dense1_result_t,config7>/core/Compute' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(69): Pragma 'hls_unroll<10
>' detected on '/nnet::dense<layer5_t,dense1_result_t,config7>/core/MultAndAccum' (CIN
-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(79): Pragma 'hls_unroll<yes
>' detected on '/nnet::dense<layer5_t,dense1_result_t,config7>/core/Result' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_mult.h(121): Inlining routine 'nnet::cast<n
net::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 5U>::value_type, nnet::array<ac_fix
ed<16, 6, true, AC_TRN, AC_WRAP>, 10U>::value_type, config7>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(123): Pragma 'hls_unroll<yes
>' detected on '/nnet::dense<layer5_t,dense1_result_t,config7>/core/ResPack' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(17): Inlining member function 'nne
t::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 10U>::operator[]' on object 'res_pac
k' (CIN-64)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Optimizing block '/nne
t::dense<layer5_t,dense1_result_t,config7>' ... (CIN-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): INOUT port 'data_strea
m' is only used as an input. (OPT-10)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): INOUT port 'res_stream'
is only used as an output. (OPT-11)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(86): INOUT port 'weights' is
only used as an input. (OPT-10)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(87): INOUT port 'biases' is
only used as an input. (OPT-10)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(105): Loop '/nnet::dense<lay
er5_t,dense1_result_t,config7>/core/DataPack' iterated at most 5 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(98): Loop '/nnet::dense<laye
r5_t,dense1_result_t,config7>/core/DataPrepare' iterated at most 16 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(59): Loop '/nnet::dense<lay
er5_t,dense1_result_t,config7>/core/ResetAccum' iterated at most 10 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(71): Loop '/nnet::dense<lay
er5_t,dense1_result_t,config7>/core/MultAndAccum' iterated at most 10 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(66): Loop '/nnet::dense<lay
er5_t,dense1_result_t,config7>/core/Compute' iterated at most 80 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(81): Loop '/nnet::dense<lay
er5_t,dense1_result_t,config7>/core/Result' iterated at most 10 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(125): Loop '/nnet::dense<lay
er5_t,dense1_result_t,config7>/core/ResPack' iterated at most 10 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(117): Loop '/nnet::dense<lay
er5_t,dense1_result_t,config7>/core/ResWrite' iterated at most 1 times. (LOOP-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Found design rout

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line 'nnet::softmax<dense1_result_t, result_t, softmax_config9>' specified by directive
(CIN-52)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Found design rout
ine 'nnet::softmax<dense1_result_t, result_t, softmax_config9>' specified by directive
(CIN-52)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Synthesizing rout
ine 'nnet::softmax<dense1_result_t, result_t, softmax_config9>' (CIN-13)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Inlining routine
'nnet::softmax<dense1_result_t, result_t, softmax_config9>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(420): Pragma 'hls_pipel
ine_init_interval<1>' detected on '/nnet::softmax<dense1_result_t,result_t,softmax_con
fig9>/core/SoftmaxInitLoop' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(425): Pragma 'hls_unrol
l<yes>' detected on '/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/Sof
tmaxInitPackLoop' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(17): Inlining member function 'nne
t::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 10U>::operator[]' on object 'in_pack'
(CIN-64)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation.h(560): Inlining routine 'nnet::
ac_softmax_pwl_wrapper<10U, 16, 6, true, AC_TRN, AC_WRAP, 16, 6, true, AC_TRN, AC_WRAP
>' (CIN-14)
# $MGC_HOME/shared/include/ac_math/ac_softmax_pwl.h(118): Inlining routine 'ac_math::a
c_softmax_pwl<AC_TRN, false, 0, 0, AC_TRN, AC_WRAP, false, 0, 0, AC_TRN, AC_WRAP, 10U,
16, 6, true, AC_TRN, AC_WRAP, 16, 6, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_math/ac_pow_pwl.h(277): Inlining routine 'ac_math::ac_ex
p_pwl<0, AC_TRN, 16, 6, true, AC_TRN, AC_WRAP, 65, 47, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_math/ac_pow_pwl.h(144): Inlining routine 'ac_math::ac_po
w2_pwl<AC_TRN, 19, 7, true, AC_TRN, AC_WRAP, 65, 47, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_math/ac_shift.h(337): Inlining routine 'ac_math::ac_shif
t_left<21, 1, AC_TRN, AC_WRAP, 65, 47, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_fixed.h(1383): Inlining routine 'operator<<<67, 47, fals
e, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_math/ac_reciprocal_pwl.h(155): Inlining routine 'ac_mat
h::ac_reciprocal_pwl<AC_TRN, 69, 51, false, AC_TRN, AC_WRAP, 89, 19, false, AC_TRN, AC
_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_math/ac_normalize.h(123): Inlining routine 'ac_math::ac_
normalize<69, 51, false, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_fixed.h(1383): Inlining routine 'operator<==<69, 0, fals
e, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_fixed.h(1383): Inlining routine 'operator!=<69, 51, fals
e, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_fixed.h(1383): Inlining routine 'operator!=<69, 51, fals
e, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_math/ac_shift.h(176): Inlining routine 'ac_math::ac_shif
t_right<21, 1, AC_TRN, AC_WRAP, 89, 19, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/ac_fixed.h(1383): Inlining routine 'operator>><89, 19, fals
e, AC_TRN, AC_WRAP>' (CIN-14)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(435): Pragma 'hls_unrol
l<yes>' detected on '/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/Sof
tmaxResPackLoop' (CIN-203)
# $MGC_HOME/shared/include/nnet_utils/nnet_types.h(17): Inlining member function 'nne
t::array<ac_fixed<16, 6, true, AC_TRN, AC_WRAP>, 10U>::operator[]' on object 'out_pac
k' (CIN-64)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Optimizing block
'/nnet::softmax<dense1_result_t,result_t,softmax_config9>' ... (CIN-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): INOUT port 'data'
is only used as an input. (OPT-10)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): INOUT port 'res'
is only used as an output. (OPT-11)
# Warning: $MGC_HOME/shared/include/ac_math/ac_pow_pwl.h(174): Reducing the number of
bits used to represent array elements of 'ac_math::ac_pow2_pwl<AC_TRN,19,7,true,AC_TR
N,AC_WRAP,65,47,AC_TRN,AC_WRAP>:c_lut.rom', from '12' bits to '11' bits. (MEM-87)
# Warning: To disable array compaction optimization, please use 'directive set -DA_DIS
ABLE_RESIZE_MEM true'. Disabling the optimization can have QoF implications. (MEM-99)
# Warning: If the array is transformed at later stages using WORD_WIDTH, BLOCK_SIZE, I
NTERLEAVE directive, the new array dimensions will be used.The num_byte_enables (if u

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may be incompatible. Please review the applicable constraint settings to get the desired RAM/ROM layout. (MEM-100)

# Warning: \$MGC\_HOME/shared/include/ac\_math/ac\_reciprocal\_pwl.h(181): Reducing the number of bits used to represent array elements of 'ac\_math::ac\_reciprocal\_pwl<AC\_TRN,69,51,false,AC\_TRN,AC\_WRAP,89,19,false,AC\_TRN,AC\_WRAP>;c\_lut.rom', from '12' bits to '11' bits. (MEM-87)

# Warning: To disable array compaction optimization, please use 'directive set -DA\_DISABLE\_RESIZE\_MEM true'. Disabling the optimization can have QofR implications. (MEM-99)

# Warning: If the array is transformed at later stages using WORD\_WIDTH, BLOCK\_SIZE, INTERLEAVE directive, the new array dimensions will be used. The num\_byte\_enables (if used) may be incompatible. Please review the applicable constraint settings to get the desired RAM/ROM layout. (MEM-100)

# Warning: \$MGC\_HOME/shared/include/ac\_math/ac\_pow\_pwl.h(173): Reducing the number of bits used to represent array elements of 'ac\_math::ac\_pow2\_pwl<AC\_TRN,19,7,true,AC\_TRN,AC\_WRAP,65,47,AC\_TRN,AC\_WRAP>;m\_lut.rom', from '10' bits to '8' bits. (MEM-87)

# Warning: To disable array compaction optimization, please use 'directive set -DA\_DISABLE\_RESIZE\_MEM true'. Disabling the optimization can have QofR implications. (MEM-99)

# Warning: If the array is transformed at later stages using WORD\_WIDTH, BLOCK\_SIZE, INTERLEAVE directive, the new array dimensions will be used. The num\_byte\_enables (if used) may be incompatible. Please review the applicable constraint settings to get the desired RAM/ROM layout. (MEM-100)

# Warning: \$MGC\_HOME/shared/include/ac\_math/ac\_reciprocal\_pwl.h(180): Reducing the number of bits used to represent array elements of 'ac\_math::ac\_reciprocal\_pwl<AC\_TRN,69,51,false,AC\_TRN,AC\_WRAP,89,19,false,AC\_TRN,AC\_WRAP>;m\_lut.rom', from '10' bits to '8' bits. (MEM-87)

# Warning: To disable array compaction optimization, please use 'directive set -DA\_DISABLE\_RESIZE\_MEM true'. Disabling the optimization can have QofR implications. (MEM-99)

# Warning: If the array is transformed at later stages using WORD\_WIDTH, BLOCK\_SIZE, INTERLEAVE directive, the new array dimensions will be used. The num\_byte\_enables (if used) may be incompatible. Please review the applicable constraint settings to get the desired RAM/ROM layout. (MEM-100)

# Warning: \$MGC\_HOME/shared/include/ac\_math/ac\_reciprocal\_pwl.h(181): Reducing the number of bits used to represent array elements of 'ac\_math::ac\_reciprocal\_pwl<AC\_TRN,69,51,false,AC\_TRN,AC\_WRAP,89,19,false,AC\_TRN,AC\_WRAP>;c\_lut.rom#1', from '11' bits to '10' bits. (MEM-87)

# Warning: To disable array compaction optimization, please use 'directive set -DA\_DISABLE\_RESIZE\_MEM true'. Disabling the optimization can have QofR implications. (MEM-99)

# Warning: If the array is transformed at later stages using WORD\_WIDTH, BLOCK\_SIZE, INTERLEAVE directive, the new array dimensions will be used. The num\_byte\_enables (if used) may be incompatible. Please review the applicable constraint settings to get the desired RAM/ROM layout. (MEM-100)

# \$MGC\_HOME/shared/include/nnet\_utils/nnet\_activation\_stream.h(427): Loop '/nnet::softmax<dense1\_result\_t,result\_t,softmax\_config9>/core/SoftmaxInitPackLoop' iterated at most 10 times. (LOOP-2)

# \$MGC\_HOME/shared/include/ac\_math/ac\_softmax\_pwl.h(153): Loop '/nnet::softmax<dense1\_result\_t,result\_t,softmax\_config9>/core/CALC\_EXP\_LOOP' iterated at most 10 times. (LOOP-2)

# \$MGC\_HOME/shared/include/ac\_math/ac\_softmax\_pwl.h(157): Loop '/nnet::softmax<dense1\_result\_t,result\_t,softmax\_config9>/core/SUM\_EXP\_LOOP' iterated at most 10 times. (LOOP-2)

# \$MGC\_HOME/shared/include/ac\_math/ac\_softmax\_pwl.h(165): Loop '/nnet::softmax<dense1\_result\_t,result\_t,softmax\_config9>/core/CALC\_SOFTMAX\_LOOP' iterated at most 10 times. (LOOP-2)

# \$MGC\_HOME/shared/include/nnet\_utils/nnet\_activation.h(564): Loop '/nnet::softmax<dense1\_result\_t,result\_t,softmax\_config9>/core/nnet::ac\_softmax\_pwl\_wrapper<10U,16,6,true,AC\_TRN,AC\_WRAP,16,6,true,AC\_TRN,AC\_WRAP>;for' iterated at most 10 times. (LOOP-2)

# \$MGC\_HOME/shared/include/nnet\_utils/nnet\_activation\_stream.h(437): Loop '/nnet::softmax<dense1\_result\_t,result\_t,softmax\_config9>/core/SoftmaxResPackLoop' iterated at most 10 times. (LOOP-2)

# \$MGC\_HOME/shared/include/nnet\_utils/nnet\_activation\_stream.h(422): Loop '/nnet::softmax<dense1\_result\_t,result\_t,softmax\_config9>/core/SoftmaxInitLoop' iterated at most 1 times. (LOOP-2)

# \$PROJECT\_HOME/firmware/myproject.cpp(21): Optimizing block '/myproject' ... (CIN-4)

# \$PROJECT\_HOME/firmware/myproject.cpp(22): INOUT port 'input1' is only used as an input. (OPT-10)

# \$PROJECT\_HOME/firmware/myproject.cpp(23): INOUT port 'layer9\_out' is only used as an

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output. (OPT-11)
# Design 'myproject' was read (SOL-1)
# Makefile for Original Design + Testbench written to file './scverify/Verify_orig_cxx_
_osci.mk'
# Warning: Hierarchical design detected - Design analysis will be done at block level
# Info: CDesignChecker Shell script written to '/home/dgb/sb/sif/subprojs/hls4ml/src/t
oolkits/tutorial/my-mnist_notebook-Catapult-test/Catapult/myproject.v1/CDesignChecker/
design_checker.sh'
# Info: Completed transformation 'compile' on solution 'myproject.v1': elapsed time 1
1.66 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'compile': Total ops = 788, Real ops = 331, Vars =
149 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno
=24 (DAPM-15)
# ***** SETTING TECHNOLOGY LIBRARIES *****
# Info: Starting transformation 'libraries' on solution 'myproject.v1' (SOL-8)
# Info: Please set ComponentLibs/TechLibSearchPath to enable flows that use downstream
synthesis tools (LIB-220)
# Reading component library '$MGC_HOME/pkgs/siflibs/mgc_busdefs.lib' [mgc_busdefs]...
(LIB-49)
# Reading component library '$MGC_HOME/pkgs/siflibs/stdops.lib' [STDOPS]... (LIB-49)
# Reading component library '$MGC_HOME/pkgs/siflibs/fpops.lib' [FPOPS]... (LIB-49)
# Reading component library '$MGC_HOME/pkgs/siflibs/ccs_dw_ops.lib' [CCS_DW_OPS]... (L
IB-49)
# Reading component library '$MGC_HOME/pkgs/siflibs/ccs_ioport.lib' [ccs_ioport]... (L
IB-49)
# Reading component library '$MGC_HOME/pkgs/siflibs/mgc_ioport.lib' [mgc_ioport]... (L
IB-49)
# Reading component library '$MGC_HOME/pkgs/cds_assert/assert_ops.lib' [ASSERT_OPS]...
(LIB-49)
# Reading component library '$MGC_HOME/pkgs/cds_assert/assert_mods.lib' [assert_mod
s]... (LIB-49)
# Reading component library '$MGC_HOME/pkgs/siflibs/ccs_connections.lib' [ccs_connecti
ons]... (LIB-49)
# Reading component library '$MGC_HOME/pkgs/siflibs/saed/saed32rvt_tt0p78v125c_beh.li
b' [saed32rvt_tt0p78v125c_beh]... (LIB-49)
# Reading component library '$MGC_HOME/pkgs/siflibs/ccs_sample_mem.lib' [ccs_sample_me
m]... (LIB-49)
# Reading component library '$MGC_HOME/pkgs/siflibs/ccs_sample_rom.lib' [ccs_sample_ro
m]... (LIB-49)
# Reading component library '$MGC_HOME/shared/pkgs/ccs_hls4ml/hls4ml.lib' [hls4ml_li
b]... (LIB-49)
# Info: Completed transformation 'libraries' on solution 'myproject.v1': elapsed time
0.50 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'libraries': Total ops = 788, Real ops = 331, Vars
= 149 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno
=24 (DAPM-15)
# Info: SAED32 EDK library set to /wv/hlstools/hlsqa_p4/hlslibs/bitcoin_v1.1_lib
# ***** C/RTL SYNTHESIS *****
# Info: Starting transformation 'assembly' on solution 'myproject.v1' (SOL-8)
# Info: $PROJECT_HOME/firmware/myproject.cpp(21): Partition '/myproject/core' is found
empty and is optimized away. (OPT-12)
# Info: Completed transformation 'assembly' on solution 'myproject.v1': elapsed time
3.29 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'assembly': Total ops = 796, Real ops = 337, Vars
= 156 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno
=24 (DAPM-15)
# Info: Starting transformation 'loops' on solution 'myproject.v1' (SOL-8)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(427): Loop '/myproject/
nnet::softmax<densel_result_t,result_t,softmax_config9>/core/SoftmaxInitPackLoop' is b
eing fully unrolled (10 times). (LOOP-7)
# $MGC_HOME/shared/include/ac_math/ac_softmax_pwl.h(153): Loop '/myproject/nnet::softm
ax<densel_result_t,result_t,softmax_config9>/core/CALC_EXP_LOOP' is left rolled. (LOOP
-4)

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# $MGC_HOME/shared/include/ac_math/ac_softmax_pwl.h(157): Loop '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/SUM_EXP_LOOP' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/ac_math/ac_softmax_pwl.h(165): Loop '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/CALC_SOFTMAX_LOOP' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation.h(564): Loop '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/nnet::ac_softmax_pwl_wrapper<10U,16,6,true,AC_TRN,AC_WRAP,16,6,true,AC_TRN,AC_WRAP>;for' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(437): Loop '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/SoftmaxResPackLoop' is being fully unrolled (10 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Loop '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/main' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(105): Loop '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core/DataPack' is being fully unrolled (5 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(59): Loop '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core/ResetAccum' is being fully unrolled (10 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(71): N_UNROLL parameter 10 is equal to the total number of loop iterations; loop fully unrolled. (LOOP-5)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(71): Loop '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core/MultAndAccum' is being fully unrolled (10 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(81): Loop '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core/Result' is being fully unrolled (10 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(125): Loop '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core/ResPack' is being fully unrolled (10 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(98): Loop '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core/DataPrepare' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(66): N_UNROLL parameter 80 is equal to the total number of loop iterations; loop fully unrolled. (LOOP-5)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(66): Loop '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core/Compute' is being fully unrolled (80 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Loop '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core/main' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(72): Loop '/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core/ReLUActLoop' is being fully unrolled (5 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(63): Loop '/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core/ReLUActLoop' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Loop '/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core/main' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/nnet_utils/ap_shift_reg.h(117): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/ap_shift_reg<nnet::array<ac_fixed<8,1,true,AC_TRN,AC_WRAP>,1U>;value_type,14U>;shift;if:for' is being fully unrolled (13 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(209): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/KernelShiftHeight' is being fully unrolled (5 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(224): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/KernelPushHeight' is being fully unrolled (5 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(59): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/ResetAccum' is being fully unrolled (5 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(71): N_UNROLL parameter 5 is equal to the total number of loop iterations; loop fully unrolled. (LOOP-5)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(71): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/MultAndAccum' is being fully unrolled (5 times). (LOOP-7)

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lled (5 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(81): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/Result' is being fully unrolled (5 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(321): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/CastLoop' is being fully unrolled (5 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(261): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/LineBufferShift' is being fully unrolled (4 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv_stream.h(205): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/KernelShiftWidth' is being fully unrolled (4 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(66): N_UNROLL parameter 25 is equal to the total number of loop iterations; loop fully unrolled. (LOOP-5)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(66): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/Compute' is being fully unrolled (25 times). (LOOP-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(84): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/ReadInputWidth' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(82): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/ReadInputHeight' is left rolled. (LOOP-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/main' is left rolled. (LOOP-4)
# Loop '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/SUM_EXP_LOOP' is merged and folded into Loop 'CALC_EXP_LOOP' (LOOP-9)
# Loop '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/nnet::ac_softmax_pwl_wrapper<10U,16,6,true,AC_TRN,AC_WRAP,16,6,true,AC_TRN,AC_WRAP>;for' is merged and folded into Loop 'CALC_SOFTMAX_LOOP' (LOOP-9)
# Info: Completed transformation 'loops' on solution 'myproject.v1': elapsed time 9.41 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'loops': Total ops = 6871, Real ops = 2001, Vars = 171 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno=24 (DAPM-15)
# Info: Starting transformation 'memories' on solution 'myproject.v1' (SOL-8)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(124): I/O-Port Resource '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/weights:rsc' (from var: weights) mapped to 'ccs_ioport.ccs_in' (size: 2000). (MEM-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(125): I/O-Port Resource '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/biases:rsc' (from var: biases) mapped to 'ccs_ioport.ccs_in' (size: 80). (MEM-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(86): I/O-Port Resource '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/weights:rsc' (from var: weights) mapped to 'ccs_ioport.ccs_in' (size: 12800). (MEM-2)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(87): I/O-Port Resource '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/biases:rsc' (from var: biases) mapped to 'ccs_ioport.ccs_in' (size: 160). (MEM-2)
# Info: Completed transformation 'memories' on solution 'myproject.v1': elapsed time 6.25 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'memories': Total ops = 4095, Real ops = 1396, Vars = 360 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno=24 (DAPM-15)
# Info: Starting transformation 'cluster' on solution 'myproject.v1' (SOL-8)
# Warning: ROM clustering skipped Technology Library(ies) required for Prototyping not found (CLUSTER-24)
# CCORE synthesis starting: pending=1 maximum_workers=1 workers=0
# CCORE synthesis has been reconfigured the maximum required number of workers, which is set to 1
# Reading solution library '/home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tutorial/mymnist_notebook-Catapult-test/Catapult/td_ccore_solutions/leading_sign_69_0_82b89553a53ce3c07b5a7cac2ad0f6a0ce82_0/.sif/solIndex_3_9514c3be-8e87-46ac-8b34-b338b3b9c06c.xml' ... (LIB-129)

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# Module 'leading_sign_69_0_82b89553a53ce3c07b5a7cac2ad0f6a0ce82_0' in the cache is va
lid & accepted for CCORE 'leading_sign_69_0_82b89553a53ce3c07b5a7cac2ad0f6a0ce82' (TD-
3)
# Module for CCORE 'leading_sign_69_0' has been successfully synthesized (TD-4)
# Reading solution library '/home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tutorial/my-
mnist_notebook-Catapult-test/Catapult/td_ccore_solutions/leading_sign_69_0_e84e02bf576
73318c5ed4a484f617a80ce81_0/.sif/solIndex_3_bf6e2107-da1f-4b12-b70e-166bf2bfc9a2.xml'
... (LIB-129)
# Module 'leading_sign_69_0_e84e02bf57673318c5ed4a484f617a80ce81_0' in the cache is va
lid & accepted for CCORE 'leading_sign_69_0_e84e02bf57673318c5ed4a484f617a80ce81' (TD-
3)
# Module for CCORE 'leading_sign_69_0' has been successfully synthesized (TD-4)
# Reading solution library '/home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tutorial/my-
mnist_notebook-Catapult-test/Catapult/td_ccore_solutions/leading_sign_69_0_634083feadb
ecfce40b4651795a0fc7ace81_0/.sif/solIndex_3_e41fd540-ba88-42c8-8e3d-547348d57ae8.xml'
... (LIB-129)
# Module 'leading_sign_69_0_634083feadbecfce40b4651795a0fc7ace81_0' in the cache is va
lid & accepted for CCORE 'leading_sign_69_0_634083feadbecfce40b4651795a0fc7ace81' (TD-
3)
# Module for CCORE 'leading_sign_69_0' has been successfully synthesized (TD-4)
# Reading solution library '/home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tutorial/my-
mnist_notebook-Catapult-test/Catapult/td_ccore_solutions/leading_sign_69_0_f52dd1794db
733e66c942d0db29a57b7ce81_0/.sif/solIndex_3_6ba88243-583f-4ac1-8dd3-f978e64d4ef0.xml'
... (LIB-129)
# Module 'leading_sign_69_0_f52dd1794db733e66c942d0db29a57b7ce81_0' in the cache is va
lid & accepted for CCORE 'leading_sign_69_0_f52dd1794db733e66c942d0db29a57b7ce81' (TD-
3)
# Module for CCORE 'leading_sign_69_0' has been successfully synthesized (TD-4)
# CCORE Task - Summary - running=0 available=0 launching=0 scheduled=0 pending=0 inco
mplete=0 complete=4 elapsed=00:01
# CCORE Task - Complete - peak_running=0 max_parallel=1
# Info: Completed transformation 'cluster' on solution 'myproject.v1': elapsed time 1.
90 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'cluster': Total ops = 3764, Real ops = 1188, Vars
= 305 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno
=24 (DAPM-15)
# Info: Starting transformation 'architect' on solution 'myproject.v1' (SOL-8)
# Design 'myproject' contains '2191' real operations. (SOL-11)
# Warning: Extrapolation detected. Script '/home/dgb/sb/sif/subprojs/hls4ml/src/toolki
ts/tutorial/my-mnist_notebook-Catapult-test/Catapult/myproject.v1/adjust_char_library.
tcl' generated. (LIB-142)
# Info: Completed transformation 'architect' on solution 'myproject.v1': elapsed time
6.80 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'architect': Total ops = 5526, Real ops = 2191, Va
rs = 577 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno
=24 (DAPM-15)
# Info: Starting transformation 'allocate' on solution 'myproject.v1' (SOL-8)
# Performing concurrent resource allocation and scheduling on '/myproject/nnet::softma
x<dense1_result_t,result_t,softmax_config9>/core' (CRAAS-1)
# Info: Select qualified components for data operations ... (CRAAS-3)
# Info: Apply resource constraints on data operations ... (CRAAS-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(422): Prescheduled LOOP
'/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/SoftmaxInitLo
op' (3 c-steps) (SCHD-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Prescheduled LOOP
'/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/main' (1 c-st
eps) (SCHD-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Prescheduled LOOP
'/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/core:rlp' (0
c-steps) (SCHD-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Prescheduled SEQU
ENTIAL '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core' (tota
l length 61 c-steps) (SCHD-8)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Initial sch
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chedule of SEQUENTIAL '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9
>/core': Latency = 21, Area (Datapath, Register, Total) = 57199.75, 13902.68, 71102.43
(CRAAS-11)
# At least one feasible schedule exists. (CRAAS-9)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Final sched
ule of SEQUENTIAL '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/
core': Latency = 21, Area (Datapath, Register, Total) = 44058.16, 10242.00, 54300.16
(CRAAS-12)
# Resource allocation and scheduling done. (CRAAS-2)
# Performing concurrent resource allocation and scheduling on '/myproject/nnet::dense<
layer5_t,dense1_result_t,config7>/core' (CRAAS-1)
# Info: Select qualified components for data operations ... (CRAAS-3)
# Info: Apply resource constraints on data operations ... (CRAAS-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Prescheduled LOOP '/myp
roject/nnet::dense<layer5_t,dense1_result_t,config7>/core/main' (2 c-steps) (SCHD-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Prescheduled LOOP '/myp
roject/nnet::dense<layer5_t,dense1_result_t,config7>/core/core:rlp' (1 c-steps) (SCHD-
7)
# $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Prescheduled SEQUENTIAL
'/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core' (total length 3 c-step
s) (SCHD-8)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Initial schedule
of SEQUENTIAL '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core': Latenc
y = 16, Area (Datapath, Register, Total) = 2029714.61, 7968.93, 2037683.54 (CRAAS-11)
# At least one feasible schedule exists. (CRAAS-9)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Final schedule of
SEQUENTIAL '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core': Latency =
17, Area (Datapath, Register, Total) = 1182517.04, 30170.94, 1212687.98 (CRAAS-12)
# Resource allocation and scheduling done. (CRAAS-2)
# Performing concurrent resource allocation and scheduling on '/myproject/nnet::relu<c
onv2d1_result_t,layer5_t,relu_config5>/core' (CRAAS-1)
# Info: Select qualified components for data operations ... (CRAAS-3)
# Info: Apply resource constraints on data operations ... (CRAAS-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(63): Prescheduled LOOP
'/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core/ReLUActLoop' (2 c
-steps) (SCHD-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Prescheduled LOOP
'/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core/main' (1 c-steps)
(SCHD-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Prescheduled LOOP
'/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core/core:rlp' (0 c-st
eps) (SCHD-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Prescheduled SEQUE
NTIAL '/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core' (total leng
th 33 c-steps) (SCHD-8)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Initial sche
dule of SEQUENTIAL '/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/cor
e': Latency = 16, Area (Datapath, Register, Total) = 577.69, 66.08, 643.77 (CRAAS-11)
# At least one feasible schedule exists. (CRAAS-9)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(60): Final schedu
le of SEQUENTIAL '/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core':
Latency = 16, Area (Datapath, Register, Total) = 453.12, 66.08, 519.19 (CRAAS-12)
# Resource allocation and scheduling done. (CRAAS-2)
# Performing concurrent resource allocation and scheduling on '/myproject/nnet::conv_2
d_cl<input_t,conv2d1_result_t,config2>/core' (CRAAS-1)
# Info: Select qualified components for data operations ... (CRAAS-3)
# Info: Apply resource constraints on data operations ... (CRAAS-4)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(82): Prescheduled LOOP '/my
project/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/ReadInputHeight' (2 c-
steps) (SCHD-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Prescheduled LOOP '/m
yproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/main' (2 c-steps) (SC
HD-7)
# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Prescheduled LOOP '/m
yproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/core:rlp' (0 c-steps)
(SCHD-7)

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# $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Prescheduled SEQUENTIAL
AL '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core' (total length
394 c-steps) (SCHD-8)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Initial schedul
e of SEQUENTIAL '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core':
Latency = 196, Area (Datapath, Register, Total) = 219541.70, 9032.78, 228574.48 (CRAA
S-11)
# At least one feasible schedule exists. (CRAAS-9)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(122): Final schedule
of SEQUENTIAL '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core': L
atency = 198, Area (Datapath, Register, Total) = 107254.50, 15455.50, 122710.00 (CRAAS
-12)
# Resource allocation and scheduling done. (CRAAS-2)
# Info: Applying user-supplied FIFO_DEPTH constraint of 1 to channel 'layer2_out' (HIE
R-22)
# Info: Applying user-supplied FIFO_DEPTH constraint of 0 to channel 'layer5_out' over
riding computed fifo_depth of 2 (HIER-35)
# Info: Applying user-supplied FIFO_DEPTH constraint of 0 to channel 'layer7_out' over
riding computed fifo_depth of 2 (HIER-35)
# Netlist written to file 'schedule.gnt' (NET-4)
# Info: Completed transformation 'allocate' on solution 'myproject.v1': elapsed time 1
2.34 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'allocate': Total ops = 5526, Real ops = 2191, Var
s = 577 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno
=24 (DAPM-15)
# Info: Starting transformation 'schedule' on solution 'myproject.v1' (SOL-8)
# Performing concurrent resource allocation and scheduling on '/myproject/nnet::softma
x<dense1_result_t,result_t,softmax_config9>/core' (CRAAS-1)
# Performing concurrent resource allocation and scheduling on '/myproject/nnet::dense<
layer5_t,dense1_result_t,config7>/core' (CRAAS-1)
# Performing concurrent resource allocation and scheduling on '/myproject/nnet::relu<c
onv2d1_result_t,layer5_t,relu_config5>/core' (CRAAS-1)
# Performing concurrent resource allocation and scheduling on '/myproject/nnet::conv_2
d_cl<input_t,conv2d1_result_t,config2>/core' (CRAAS-1)
# Global signal 'data:rsc.rdy' added to design 'nnet::conv_2d_cl<input_t,conv2d1_resul
t_t,config2>' for component 'data:rsci' (LIB-3)
# Global signal 'data:rsc.vld' added to design 'nnet::conv_2d_cl<input_t,conv2d1_resul
t_t,config2>' for component 'data:rsci' (LIB-3)
# Global signal 'data:rsc.dat' added to design 'nnet::conv_2d_cl<input_t,conv2d1_resul
t_t,config2>' for component 'data:rsci' (LIB-3)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(90): Creating buffer
for wait controller for component 'data:rsc' (SCHD-46)
# Global signal 'res:rsc.rdy' added to design 'nnet::conv_2d_cl<input_t,conv2d1_result
_t,config2>' for component 'res:rsci' (LIB-3)
# Global signal 'res:rsc.vld' added to design 'nnet::conv_2d_cl<input_t,conv2d1_result
_t,config2>' for component 'res:rsci' (LIB-3)
# Global signal 'res:rsc.dat' added to design 'nnet::conv_2d_cl<input_t,conv2d1_result
_t,config2>' for component 'res:rsci' (LIB-3)
# Global signal 'weights:rsc.dat' added to design 'nnet::conv_2d_cl<input_t,conv2d1_re
sult_t,config2>' for component 'weights:rsci' (LIB-3)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(74): Creating buffer
for wait controller for component 'weights:rsc' (SCHD-46)
# Global signal 'biases:rsc.dat' added to design 'nnet::conv_2d_cl<input_t,conv2d1_res
ult_t,config2>' for component 'biases:rsci' (LIB-3)
# Info: $MGC_HOME/shared/include/ac_fixed.h(339): Creating buffer for wait controller
for component 'biases:rsc' (SCHD-46)
# Global signal 'weights.triosy.lz' added to design 'nnet::conv_2d_cl<input_t,conv2d1_
result_t,config2>' for component 'weights.triosy:obj' (LIB-3)
# Global signal 'biases.triosy.lz' added to design 'nnet::conv_2d_cl<input_t,conv2d1_r
esult_t,config2>' for component 'biases.triosy:obj' (LIB-3)
# Global signal 'data:rsc.rdy' added to design 'nnet::relu<conv2d1_result_t,layer5_t,r
elu_config5>' for component 'data:rsci' (LIB-3)
# Global signal 'data:rsc.vld' added to design 'nnet::relu<conv2d1_result_t,layer5_t,r
elu_config5>' for component 'data:rsci' (LIB-3)
# Global signal 'data:rsc.dat' added to design 'nnet::relu<conv2d1_result_t,layer5_t,r

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elu_config5>' for component 'data:rsci' (LIB-3)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(66): Creating buffer for wait controller for component 'data:rsc' (SCHD-46)
# Global signal 'res:rsc.rdy' added to design 'nnet::relu<conv2d1_result_t,layer5_t,relu_config5>' for component 'res:rsci' (LIB-3)
# Global signal 'res:rsc.vld' added to design 'nnet::relu<conv2d1_result_t,layer5_t,relu_config5>' for component 'res:rsci' (LIB-3)
# Global signal 'res:rsc.dat' added to design 'nnet::relu<conv2d1_result_t,layer5_t,relu_config5>' for component 'res:rsci' (LIB-3)
# Global signal 'data_stream:rsc.rdy' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'data_stream:rsci' (LIB-3)
# Global signal 'data_stream:rsc.vld' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'data_stream:rsci' (LIB-3)
# Global signal 'data_stream:rsc.dat' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'data_stream:rsci' (LIB-3)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(102): Creating buffer for wait controller for component 'data_stream:rsc' (SCHD-46)
# Global signal 'res_stream:rsc.rdy' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'res_stream:rsci' (LIB-3)
# Global signal 'res_stream:rsc.vld' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'res_stream:rsci' (LIB-3)
# Global signal 'res_stream:rsc.dat' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'res_stream:rsci' (LIB-3)
# Global signal 'weights:rsc.dat' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'weights:rsci' (LIB-3)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_dense_latency.h(74): Creating buffer for wait controller for component 'weights:rsc' (SCHD-46)
# Global signal 'biases:rsc.dat' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'biases:rsci' (LIB-3)
# Info: $MGC_HOME/shared/include/ac_fixed.h(339): Creating buffer for wait controller for component 'biases:rsc' (SCHD-46)
# Global signal 'weights.triosy.lz' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'weights.triosy:obj' (LIB-3)
# Global signal 'biases.triosy.lz' added to design 'nnet::dense<layer5_t,dense1_result_t,config7>' for component 'biases.triosy:obj' (LIB-3)
# Global signal 'data:rsc.rdy' added to design 'nnet::softmax<dense1_result_t,result_t,softmax_config9>' for component 'data:rsci' (LIB-3)
# Global signal 'data:rsc.vld' added to design 'nnet::softmax<dense1_result_t,result_t,softmax_config9>' for component 'data:rsci' (LIB-3)
# Global signal 'data:rsc.dat' added to design 'nnet::softmax<dense1_result_t,result_t,softmax_config9>' for component 'data:rsci' (LIB-3)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(423): Creating buffer for wait controller for component 'data:rsc' (SCHD-46)
# Global signal 'res:rsc.rdy' added to design 'nnet::softmax<dense1_result_t,result_t,softmax_config9>' for component 'res:rsci' (LIB-3)
# Global signal 'res:rsc.vld' added to design 'nnet::softmax<dense1_result_t,result_t,softmax_config9>' for component 'res:rsci' (LIB-3)
# Global signal 'res:rsc.dat' added to design 'nnet::softmax<dense1_result_t,result_t,softmax_config9>' for component 'res:rsci' (LIB-3)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(422): Loop '/myproject/nnet::softmax<dense1_result_t,result_t,softmax_config9>/core/SoftmaxInitLoop' is pipelined with initiation interval 1 and no flushing (SCHD-43)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_dense_stream.h(85): Loop '/myproject/nnet::dense<layer5_t,dense1_result_t,config7>/core/main' is pipelined with initiation interval 1 and no flushing (SCHD-43)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(63): Loop '/myproject/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core/ReLUActLoop' is pipelined with initiation interval 1 and no flushing (SCHD-43)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_conv2d_stream.h(82): Loop '/myproject/nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>/core/ReadInputHeight' is pipelined with initiation interval 1 and no flushing (SCHD-43)
# $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(63): Loop '/myproject/myproject.struct/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/nnet::relu<conv2d1_result_t,layer5_t,relu_config5>/core/core/ReLUActLoop' iterated at most 17 times. (L00 P-2)
# Info: Running transformation 'schedule' on solution 'myproject.v1': elapsed time 29.

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31 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-15)  
# Info: Running transformation 'schedule' on solution 'myproject.v1': elapsed time 51.12 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-15)  
# Info: Running transformation 'schedule' on solution 'myproject.v1': elapsed time 73.19 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-15)  
# Report written to file 'cycle.rpt'  
# Info: Completed transformation 'schedule' on solution 'myproject.v1': elapsed time 92.70 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)  
# Info: Design complexity at end of 'schedule': Total ops = 5973, Real ops = 2294, Var s = 1505 (SOL-21)  
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno =24 (DAPM-15)  
# Info: Starting transformation 'dpfsm' on solution 'myproject.v1' (SOL-8)  
# Performing FSM extraction... (FSM-1)  
# Creating shared register 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pX(3:0).lpi#2' for variables 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pX(3:0).lpi#2, nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pX(3:0).sva, nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pX(3:0).lpi#2.dfm' (2 registers deleted). (FSM-3)  
# Creating shared register 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(0)(0)(0).lpi#2' for variables 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(0)(0)(0).lpi#2, nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(0)(0)(1).sva, nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(0)(0)(13).sva#1.1' (2 registers deleted). (FSM-3)  
# Creating shared register 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(1)(0)(0).lpi#2' for variables 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(1)(0)(0).lpi#2, nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(1)(0)(1).sva, nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(1)(0)(13).sva#1.1' (2 registers deleted). (FSM-3)  
# Creating shared register 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(1)(0)(1).lpi#2' for variables 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(1)(0)(1).lpi#2, nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(1)(0)(2).sva' (1 register deleted). (FSM-2)  
# Creating shared register 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(2)(0)(0).lpi#2' for variables 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(2)(0)(0).lpi#2, nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(2)(0)(1).sva, nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(2)(0)(13).sva#1.1' (2 registers deleted). (FSM-3)  
# Creating shared register 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(3)(0)(0).lpi#2' for variables 'nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(3)(0)(0).lpi#2, nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(3)(0)(1).sva, nnet::conv\_2d\_buffer\_cl<input\_t,conv2d1\_result\_t,config2>:line\_buffer.Array(3)(0)(13).sva#1.1' (2 registers deleted). (FSM-3)  
# Creating shared register 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:sY.lpi#2' for variables 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:sY.lpi#2, nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:sY.lpi#2.dfm#1, nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:sY.sva' (2 registers deleted). (FSM-3)  
# Creating shared register 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.lpi#2(0)' for variables 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.lpi#2(0), nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.lpi#2.dfm#1(0), nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.sva(0)' (2 registers deleted). (FSM-3)  
# Creating shared register 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.lpi#2(31:4)' for variables 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.lpi#2(31:4), nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.lpi#2.dfm#1(31:4), nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.sva(31:4)' (2 registers deleted). (FSM-3)  
# Creating shared register 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.lpi#2(3:1)' for variables 'nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.lpi#2(3:1), nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.lpi#2(3:1), nnet::compute\_output\_buffer\_2d<input\_t,conv2d1\_result\_t,config2>:pY.sva(3:1)' (2 registers deleted). (FSM-3)

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t,config2>:pY.lpi#2.dfm#1(3:1), nnet::compute_output_buffer_2d<input_t,conv2d1_result_t,config2>:pY.sva(3:1)' (2 registers deleted). (FSM-3)
# Creating shared register 'nnet::compute_output_buffer_2d<input_t,conv2d1_result_t,config2>:sX(2:0).lpi#2' for variables 'nnet::compute_output_buffer_2d<input_t,conv2d1_result_t,config2>:sX(2:0).lpi#2, nnet::compute_output_buffer_2d<input_t,conv2d1_result_t,config2>:sX(2:0).sva, nnet::compute_output_buffer_2d<input_t,conv2d1_result_t,config2>:sX(2:0).lpi#2.dfm' (2 registers deleted). (FSM-3)
# Info: Completed transformation 'dpfsm' on solution 'myproject.v1': elapsed time 7.44 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'dpfsm': Total ops = 7292, Real ops = 3490, Vars = 1264 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno =24 (DAPM-15)
# Info: Starting transformation 'instance' on solution 'myproject.v1' (SOL-8)
# Info: Running transformation 'instance' on solution 'myproject.v1': elapsed time 29.85 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-15)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation.h(565): Optimizing constant bits for register 'reg(nnet::ac_softmax_pwl_wrapper<10U,16,6,true,AC_TRN,AC_WRAP,16,6,true,AC_TRN,AC_WRAP>:for:and#18.psp)(const bits:all)' in module 'nnet::softmax<dense1_result_t,result_t,softmax_config9>:core' (DEADCODE-1)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation.h(565): Optimizing constant bits for register 'reg(nnet::ac_softmax_pwl_wrapper<10U,16,6,true,AC_TRN,AC_WRAP,16,6,true,AC_TRN,AC_WRAP>:for:and#17.psp)(const bits:all)' in module 'nnet::softmax<dense1_result_t,result_t,softmax_config9>:core' (DEADCODE-1)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation.h(565): Optimizing constant bits for register 'reg(nnet::ac_softmax_pwl_wrapper<10U,16,6,true,AC_TRN,AC_WRAP,16,6,true,AC_TRN,AC_WRAP>:for:and#16.psp)(const bits:all)' in module 'nnet::softmax<dense1_result_t,result_t,softmax_config9>:core' (DEADCODE-1)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation.h(565): Optimizing constant bits for register 'reg(nnet::ac_softmax_pwl_wrapper<10U,16,6,true,AC_TRN,AC_WRAP,16,6,true,AC_TRN,AC_WRAP>:for:and#15.psp)(const bits:all)' in module 'nnet::softmax<dense1_result_t,result_t,softmax_config9>:core' (DEADCODE-1)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation.h(565): Optimizing constant bits for register 'reg(nnet::ac_softmax_pwl_wrapper<10U,16,6,true,AC_TRN,AC_WRAP,16,6,true,AC_TRN,AC_WRAP>:for:and#14.psp)(const bits:all)' in module 'nnet::softmax<dense1_result_t,result_t,softmax_config9>:core' (DEADCODE-1)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation.h(565): Optimizing constant bits for register 'reg(nnet::ac_softmax_pwl_wrapper<10U,16,6,true,AC_TRN,AC_WRAP,16,6,true,AC_TRN,AC_WRAP>:for:and#13.psp)(const bits:all)' in module 'nnet::softmax<dense1_result_t,result_t,softmax_config9>:core' (DEADCODE-1)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation.h(565): Optimizing constant bits for register 'reg(nnet::ac_softmax_pwl_wrapper<10U,16,6,true,AC_TRN,AC_WRAP,16,6,true,AC_TRN,AC_WRAP>:for:and#12.psp)(const bits:all)' in module 'nnet::softmax<dense1_result_t,result_t,softmax_config9>:core' (DEADCODE-1)
# Info: $MGC_HOME/shared/include/nnet_utils/nnet_activation_stream.h(417): Deadcode-cleaning: in module 'nnet::softmax<dense1_result_t,result_t,softmax_config9>:core' out of 139 observations points, 7 have been proven to be totally constant and 0 have been proven to be partially constant. (DEADCODE-3)
# Netlist written to file 'schematic.nlv' (NET-4)
# Info: Completed transformation 'instance' on solution 'myproject.v1': elapsed time 44.42 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'instance': Total ops = 6525, Real ops = 3314, Vars = 6457 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno =24 (DAPM-15)
# Info: Starting transformation 'extract' on solution 'myproject.v1' (SOL-8)
# Warning: connected DA instance failed to respond (ignoring) (DAPM-16)
# Warning: connected DA instance failed to respond (ignoring) (DAPM-16)
# Report written to file 'rtl.rpt'
# Generating scverify_top.cpp
# Generating SCVerify ccs_wrapper_myproject.vhdl
# Netlist written to file 'rtl.vhdl' (NET-4)
# generate concat
# order file name is: rtl.vhdl_order.txt
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_in_wait_v1.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_out_wait_v1.vhd

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# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/hls_pkgs/src/funcs.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_comps_v5.vh
d
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_bl_beh_v5.v
hd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_br_beh_v5.v
hd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_l_beh_v5.vh
d
# Add dependent file: ../td_ccore_solutions/leading_sign_69_0_82b89553a53ce3c07b5a7cac
2ad0f6a0ce82_0/rtl.vhdl
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_io_sync_v2.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_in_v1.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_register-file_rst
_v4.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/hls_pkgs/mgc_comps_src/mgc_co
mps.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/hls_pkgs/mgc_comps_src/mgc_ge
neric_reg_beh.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_sync_separateRW_r
st_generic_v3.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_sync_separateRW_c
dc_generic_v2.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_wrapper_
generic_v3.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_core_v1
1.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_v11.vhd
# Add dependent file: ./rtl.vhdl
# Finished writing concatenated file: /home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tu
torial/my-mnist_notebook-Catapult-test/Catapult/myproject.v1/concat_rtl.vhdl
# order file name is: rtl.vhdl_order_sim.txt
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_in_wait_v1.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_out_wait_v1.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/hls_pkgs/src/funcs.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_comps_v5.vh
d
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_bl_beh_v5.v
hd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_br_beh_v5.v
hd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_l_beh_v5.vh
d
# Add dependent file: ../td_ccore_solutions/leading_sign_69_0_82b89553a53ce3c07b5a7cac
2ad0f6a0ce82_0/rtl.vhdl
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_io_sync_v2.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_in_v1.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_register-file_rst
_v4.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/hls_pkgs/mgc_comps_src/mgc_co
mps.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/hls_pkgs/mgc_comps_src/mgc_ge
neric_reg_beh.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_sync_separateRW_r
st_generic_v3.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_sync_separateRW_c
dc_generic_v2.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_wrapper_
generic_v3.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_core_v1
1.vhd
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_v11.vhd
# Add dependent file: ./rtl.vhdl
# Finished writing concatenated simulation file: /home/dgb/sb/sif/subprojs/hls4ml/src/
toolkits/tutorial/my-mnist_notebook-Catapult-test/Catapult/myproject.v1/concat_sim_rt
l.vhdl

```

```

# Generating SCVerify testbench files
# Makefile for RTL VHDL output 'rtl.vhdl' vs Untimed C++ written to file './scverify/V
erify_rtl_vhdl_msim.mk'
# Makefile for Concat RTL VHDL output 'concat_sim_rtl.vhdl' vs Untimed C++ written to
file './scverify/Verify_concat_sim_rtl_vhdl_msim.mk'
# Generating SCVerify ccs_wrapper_myproject.v
# Netlist written to file 'rtl.v' (NET-4)
# generate concat
# order file name is: rtl.v_order.txt
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_in_wait_v1.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_out_wait_v1.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_bl_beh_v5.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_br_beh_v5.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_l_beh_v5.v
# Add dependent file: ../td_ccore_solutions/leading_sign_69_0_82b89553a53ce3c07b5a7cac
2ad0f6a0ce82_0/rtl.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_io_sync_v2.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_in_v1.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_register-file_rst
_v4.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/hls_pkgs/mgc_comps_src/mgc_ge
neric_reg_beh.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_sync_separateRW_r
st_generic_v3.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_sync_separateRW_c
dc_generic_v2.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_wrapper_
generic_v3.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_core_v1
1.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_v11.v
# Add dependent file: ./rtl.v
# Finished writing concatenated file: /home/dgb/sb/sif/subprojs/hls4ml/src/toolkits/tu
torial/my-mnist_notebook-Catapult-test/Catapult/myproject.v1/concat_rtl.v
# order file name is: rtl.v_order_sim.txt
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_in_wait_v1.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_out_wait_v1.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_bl_beh_v5.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_br_beh_v5.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_shift_l_beh_v5.v
# Add dependent file: ../td_ccore_solutions/leading_sign_69_0_82b89553a53ce3c07b5a7cac
2ad0f6a0ce82_0/rtl.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_io_sync_v2.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ccs_in_v1.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_register-file_rst
_v4.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/hls_pkgs/mgc_comps_src/mgc_ge
neric_reg_beh.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_sync_separateRW_r
st_generic_v3.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/ram_sync_separateRW_c
dc_generic_v2.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_wrapper_
generic_v3.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_core_v1
1.v
# Add dependent file: /user/dgb/sb/sif/aol/Mgc_home/pkgs/siflibs/mgc_pipe_mem_v11.v
# Add dependent file: ./rtl.v
# Finished writing concatenated simulation file: /home/dgb/sb/sif/subprojs/hls4ml/src/
toolkits/tutorial/my-mnist_notebook-Catapult-test/Catapult/myproject.v1/concat_sim_rt
l.v
# Makefile for RTL Verilog output 'rtl.v' vs Untimed C++ written to file './scverify/V
erify_rtl_v_msim.mk'
# Makefile for Concat RTL Verilog output 'concat_sim_rtl.v' vs Untimed C++ written to
file './scverify/Verify_concat_sim_rtl_v_msim.mk'
# Info: Completed transformation 'extract' on solution 'myproject.v1': elapsed time 1

```

```

5.79 seconds, memory usage 1730132kB, peak memory usage 1795668kB (SOL-9)
# Info: Design complexity at end of 'extract': Total ops = 6524, Real ops = 3313, Vars
= 1220 (SOL-21)
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno
=24 (DAPM-15)
# ***** C/RTL SYNTHESIS COMPLETED IN 0h3m59s *****
# > project save
# Warning: Unable to start connect folder watch - failed to initialize inotify - errno
=24 (DAPM-15)
# > if {$BuildOptions(SCVerify)} {
# >   if {$BuildOptions(verilog)} {
# >     flow run /SCVerify/launch_make ./scverify/Verify_rtl_v_msim.mk {} SIMTOOL=msim
sim
# >   }
# >   if {$BuildOptions(vhdl)} {
# >     flow run /SCVerify/launch_make ./scverify/Verify_rtl_vhdl_msim.mk {} SIMTOOL=m
sim sim
# >   }
# > }
# > if {$BuildOptions(PowerEst)} {
# >   puts "***** Pre Power Optimization *****"
# >   go switching
# >   if {$BuildOptions(verilog)} {
# >     flow run /PowerAnalysis/report_pre_pwropt_Verilog
# >   }
# >   if {$BuildOptions(vhdl)} {
# >     flow run /PowerAnalysis/report_pre_pwropt_VHDL
# >   }
# > }
# > if {$BuildOptions(PowerOpt)} {
# >   puts "***** Power Optimization *****"
# >   go power
# > }
# > if {$BuildOptions(RTLSynth)} {
# >   set launch {}
# >   foreach {p v} [solution get /OUTPUTFILES/.../FILETYPE -match glob -rec 1 -ret p
v] {
# >     if { $v == "SYNTHESIS" } {
# >       set p1 [file dirname $p]
# >       set nettype [string tolower [solution get $p1/DEPENDENCIES/1/FILETYPE -check
path 0]]
# >       if { [info exists BuildOptions($nettype)] && $BuildOptions($nettype) } {
# >         set launch [lindex [lindex [solution get $p1/FLAWS] 0] 1]
# >       }
# >     }
# >   }
# >   if { $launch != {} } {
# >     puts "***** RTL SYNTHESIS *****"
# >     set time_start [clock clicks -milliseconds]
# >     eval flow run $launch
# >     set time_end [clock clicks -milliseconds]
# >     report_time "RTL SYNTHESIS" $time_start $time_end
# >   } else {
# >     logfile message "RTL Synthesis flow lookup failed\n" warning
# >   }
# > }
# > if {$BuildOptions(LaunchDA)} {
# >   puts "***** Launching DA *****"
# >   flow run /DesignAnalyzer/launch
# > }
# > if { [catch {flow package present /HLS4ML}] == 0 } {
# >   flow run /HLS4ML/collect_reports
# > }
# Info: Generated HLS4ML nnet layer post-HLS report '/home/dgb/sb/sif/subprojs/hls4ml/
src/toolkits/tutorial/my-mnist_notebook-Catapult-test/Catapult/myproject.v1/nnet_layer
_results.txt'

```

```

# Info: =====
# Info: HLS4ML 'nnet' Layer Results
# Info:
# Info: Layer                                Area          La
tency          Thruput          TotalPwr          DynPwr          LeakPwr
# Info: -----
-----
# Info: nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>          115253
198              201              NaN              NaN              NaN
# Info: nnet::relu<conv2d1_result_t,layer5_t,relu_config5>          1749
16              18              NaN              NaN              NaN
# Info: nnet::dense<layer5_t,dense1_result_t,config7>          1214771
17              16              NaN              NaN              NaN
# Info: nnet::softmax<dense1_result_t,result_t,softmax_config9>          51284
21              23              NaN              NaN              NaN
# Info:
# Info:
# Info: FIFO Interconnect
# Info: C++ Variable          Instance          Component
Width          Depth          Area
# Info: -----
- -----
# Info: layer2_out          layer2_out_cns_pipe          hls4ml_lib.mgc_pipe_mem
80              1          1031
# Info: layer5_out          layer5_out_cns_pipe          hls4ml_lib.mgc_pipe_mem
80              1          1031
# Info: layer7_out          layer7_out_cns_pipe          hls4ml_lib.mgc_pipe_mem
160              1          2054
# Info:
# Info:
# Info: Weight/Bias Value ROM Constants
# Info: Layer          Variable          Size (bits)
# Info: -----
# Info: 2              b2              80
# Info: 2              w2              2000
# Info: 7              b7              160
# Info: 7              w7              12800
# Info:
# > end dofile ./build_prj.tcl
Utilization report not found.
Timing report not found.
Results in nnet_layer_results.txt from: my-mnist_notebook-Catapult-test/Catapult/mypro
ject.v1/nnet_layer_results.txt

```

```
Out[19]: {'PerLayerQ0FR': ['====='],
          "HLS4ML 'nnet' Layer Results",
          '',
          'Layer',
          'Thruput', 'TotalPwr', 'DynPwr', 'LeakPwr', 'Area', 'Laten
cy',
          '-----',
          '-----',
          'nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>',
          115253, 1
98      201      NaN      NaN      NaN',
          'nnet::relu<conv2d1_result_t,layer5_t,relu_config5>',
          1749
16      18      NaN      NaN      NaN',
          'nnet::dense<layer5_t,dense1_result_t,config7>',
          1214771
17      16      NaN      NaN      NaN',
          'nnet::softmax<dense1_result_t,result_t,softmax_config9>',
          51284
21      23      NaN      NaN      NaN',
          '',
          'FIFO Interconnect',
          'C++ Variable', 'Instance', 'Component',
          'Width', 'Depth', 'Area',
          '-----',
          '-----',
          'layer2_out', 'layer2_out_cns_pipe', 'hls4ml_lib.mgc_pipe_mem',
          80      1      1031',
          'layer5_out', 'layer5_out_cns_pipe', 'hls4ml_lib.mgc_pipe_mem',
          80      1      1031',
          'layer7_out', 'layer7_out_cns_pipe', 'hls4ml_lib.mgc_pipe_mem',
          160      1      2054',
          '',
          'Weight/Bias Value ROM Constants',
          'Layer', 'Variable', 'Size (bits)',
          '-----',
          '2', 'b2', 80',
          '2', 'w2', 2000',
          '7', 'b7', 160',
          '7', 'w7', 12800'}}]
```

Print reports from Catapult

```
In [20]: summary_file = 'my-' + model.name + '-' + config_ccs['Backend'] + '-test/firmware/lay
print('Layer summary report: '+summary_file)
with open(summary_file,'r') as f:
    print(f.read())
```

Layer summary report: my-mnist\_notebook-Catapult-test/firmware/layer\_summary.txt

Layer Name	Layer Class	Input Type	Input Shape	Output Type
Output Shape	Weight Type	Bias Type	Filter Shape	Stride
IOType	Reuse			
conv2d1	Conv2D	ac_fixed<8,1,true>	[14][14][1]	ac_fixed<16,6,true>
[4][4][5]			[5][5]	3
relu1	relu	ac_fixed<16,6,true>	[4][4][5]	io_stream
[4][4][5]				1
flatten1	Reshape	ac_fixed<16,6,true>	[4][4][5]	ac_fixed<16,6,true>
[80]				io_stream
dense1	Dense	ac_fixed<16,6,true>	[80]	ac_fixed<16,6,true>
[10]				io_stream
softmax1	Softmax	ac_fixed<16,6,true>	[10]	ac_fixed<16,6,true>
[10]				io_stream
				1

```
In [21]: import glob
```

```

#Show the contents of the last report generated
print('my-' + model.name + '-' + config_ccs['Backend'] + '-test/Catapult*/myproject.v
rpt_files = glob.glob('my-' + model.name + '-' + config_ccs['Backend'] + '-test/Catap
print('Latest report: ' + rpt_files[-1])
with open(rpt_files[-1], 'r') as f:
    print(f.read())

```

my-mnist\_notebook-Catapult-test/Catapult\*/myproject.v1/nnet\_layer\_results.txt  
Latest report: my-mnist\_notebook-Catapult-test/Catapult/myproject.v1/nnet\_layer\_results.txt

=====  
HLS4ML 'nnet' Layer Results

Layer				Area	Latency
Thruput	TotalPwr	DynPwr	LeakPwr		
-----					
nnet::conv_2d_cl<input_t,conv2d1_result_t,config2>				115253	198
201	NaN	NaN	NaN		
nnet::relu<conv2d1_result_t,layer5_t,relu_config5>				1749	16
18	NaN	NaN	NaN		
nnet::dense<layer5_t,dense1_result_t,config7>				1214771	17
16	NaN	NaN	NaN		
nnet::softmax<dense1_result_t,result_t,softmax_config9>				51284	21
23	NaN	NaN	NaN		

FIFO Interconnect

C++ Variable			Instance	Component	Wi
dth	Depth	Area			
-----					
layer2_out			layer2_out_cns_pipe	hls4ml_lib.mgc_pipe_mem	
80	1	1031			
layer5_out			layer5_out_cns_pipe	hls4ml_lib.mgc_pipe_mem	
80	1	1031			
layer7_out			layer7_out_cns_pipe	hls4ml_lib.mgc_pipe_mem	
160	1	2054			

Weight/Bias Value ROM Constants

Layer	Variable	Size (bits)
-----		
2	b2	80
2	w2	2000
7	b7	160
7	w7	12800