# Computational Science on Many-Core Architectures

**360.252**

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Zoom Channel 95028746244
Wednesday, January 20, 2021

# Agenda for Today

Exercise 10 Recap

Grading and Oral Exam

CSE on FPGAs

Possible Next Steps

# Exercise 9 Recap

## Takeaways

- Issue with atomicAdd in HIP (fixed)
- SyCL still in its infancy

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How was your experience?

## Exercise Grades

- Provided by end of the week

# Grading (cf. Lecture 1)

## Part 1: Hands-On Exercises

- approx. 100 points over 10 exercises (excl. bonus points)
- approx. 40 percent of overall grade
- minimum of 50 percent of total points

## Part 2: Oral exam

- oral exam (most likely virtual because of COVID-19)
- approx. 60 percent of overall grade
- “Fail” on oral exam means “Fail” on course

# Oral Exam

## Oral Exam

- Arrange appointment via email (suggest time slot)
- Oral exam via Zoom
- Video for identification required
- Not recorded
- Public

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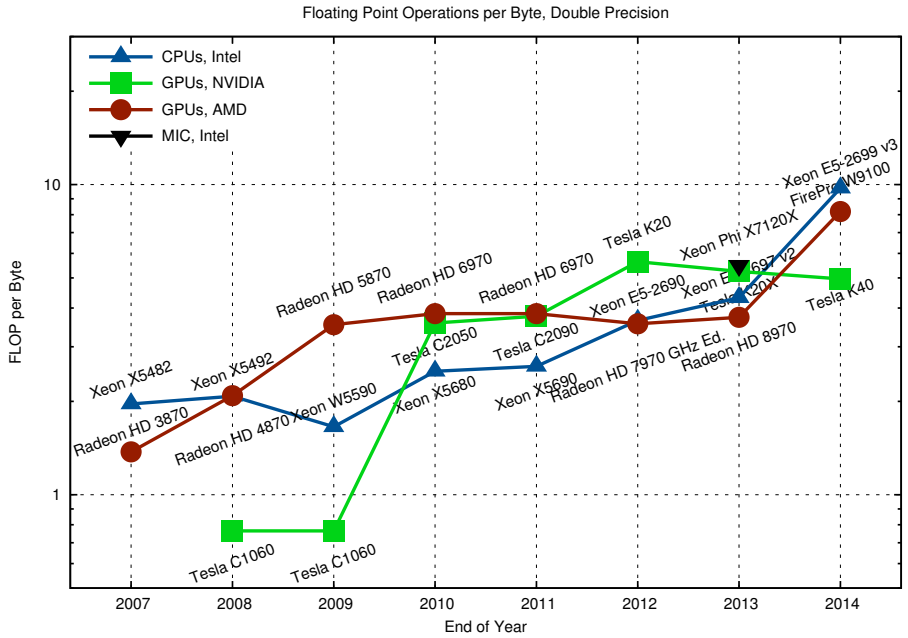
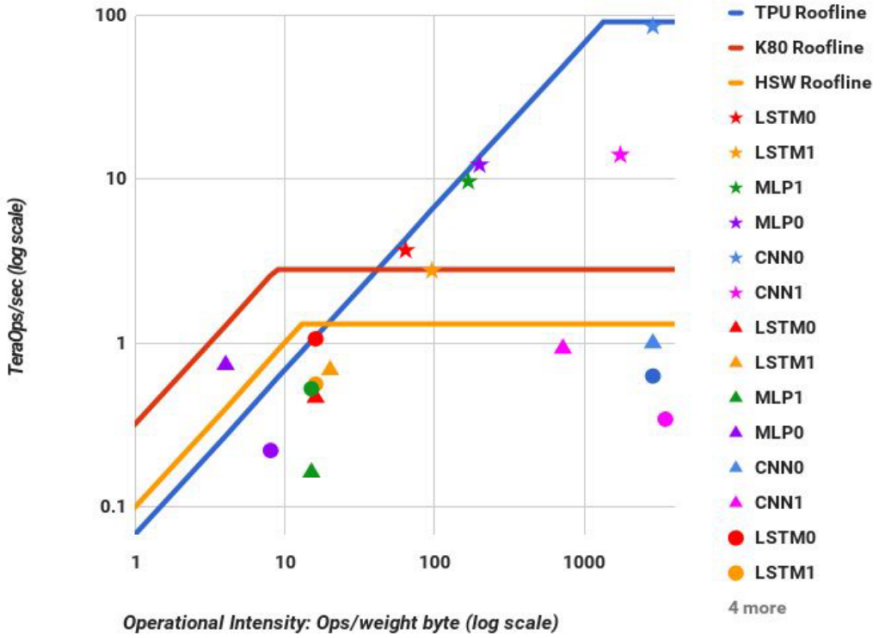
## Topics

- Everything covered in the lecture and the exercises
- Emphasis on high-level understanding (“Tell me about the different ways of summing a vector on the GPU and their pros and cons”)
- No low-level details (“What is the second parameter of `clEnqueueNDRangeKernel()`?”)

## Reminder: Hardware Trend

- Compute power grows faster than memory bandwidth
- More and more applications tend to be bandwidth-bound



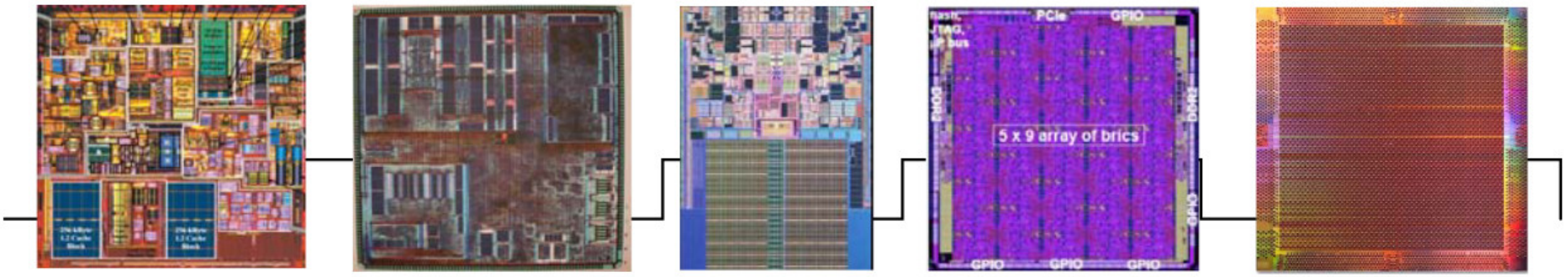




https://arxiv.org/ftp/arxiv/papers/1704/1704.04760.pdf

# FPGAs

## Why

- General purpose hardware is complex ...
- ... and relatively energy-hungry
- For more power per Watt, use stripped-down hardware



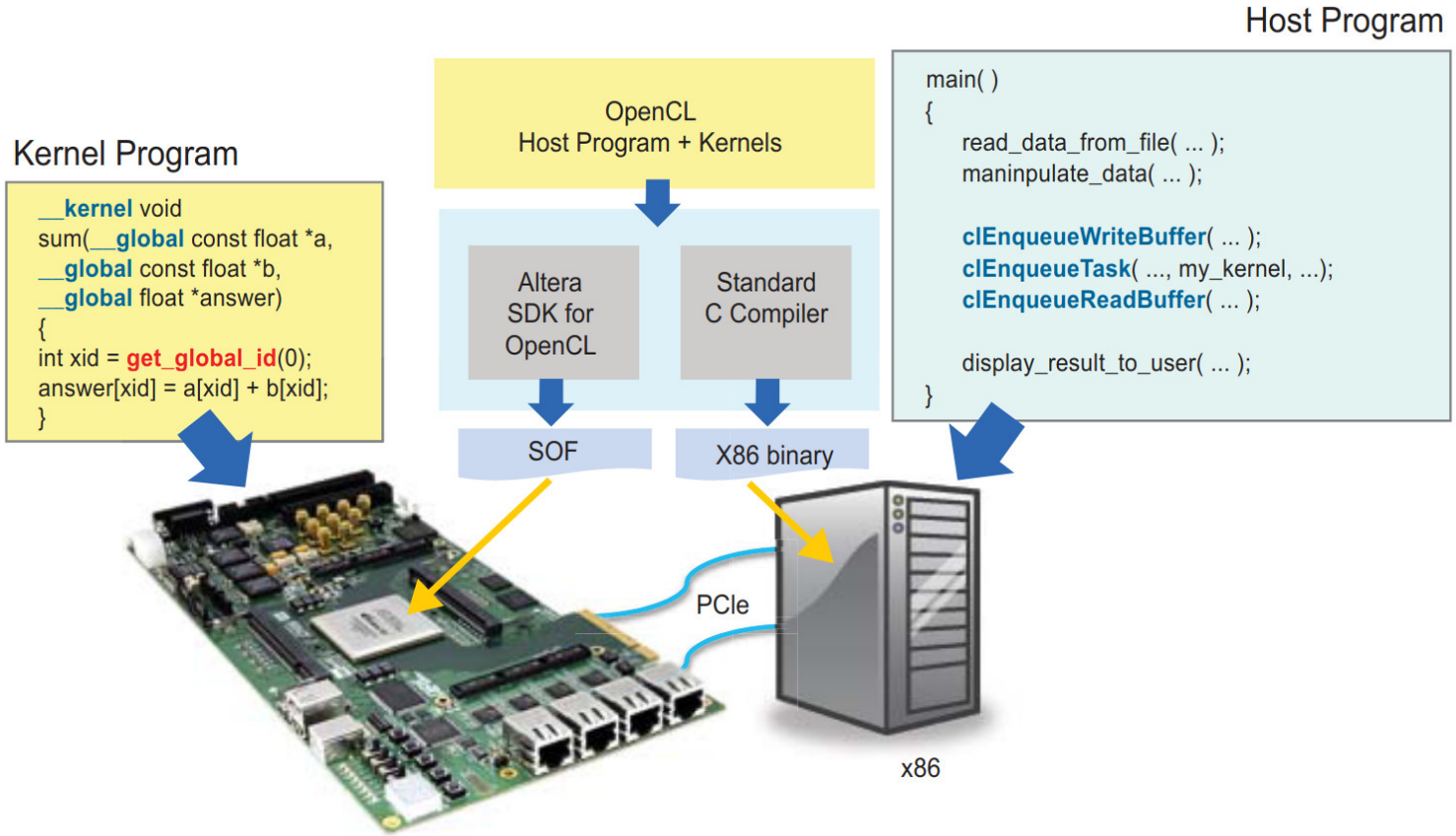

Implementing FPGA Design with theOpenCL Standard. Altera Whitepaper WP-01173-3.0

https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/wp/wp-01173-opencl.pdf

# FPGAs

## How

- VHDL and Verilog as bare-metal synthesis languages (bottom-up)
- OpenCL (SYCL?) to describe the operations to perform (top-down)

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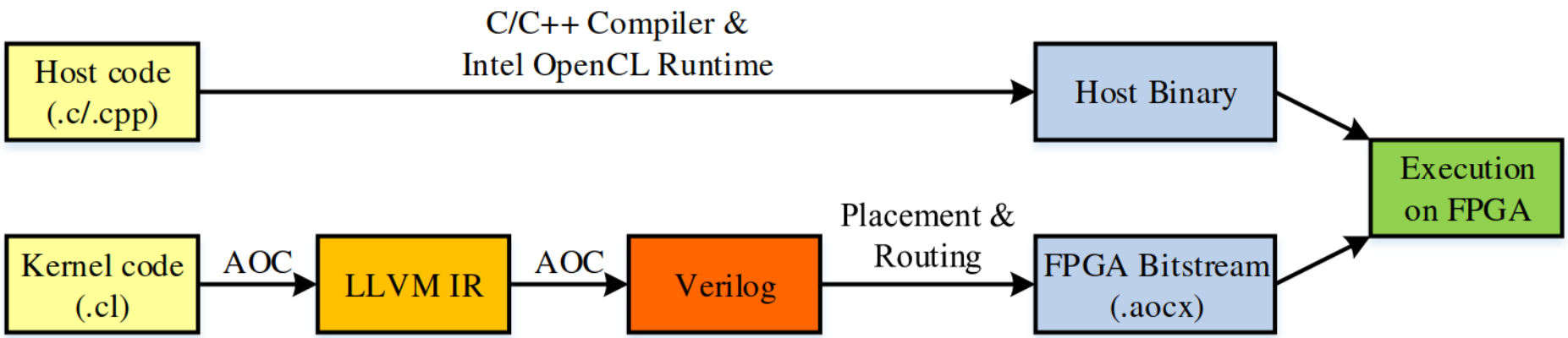
## OpenCL Compilation

- Host code compiled via normal compiler toolchain
- OpenCL kernels fed to hardware synthesizer (slow!)




Hamid Reza Zohouri: High Performance Computing with FPGAs and OpenCL `https://arxiv.org/pdf/1810.09773.pdf`

# FPGAs

## Fundamental Limitations

- Memory-bound applications do not benefit!
- Compute-bound applications can benefit if programmed efficiently
- Special purpose hardware is expensive

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### 6.2 Insights

Even though FPGAs are very old devices, they are at the beginning of their path to large-scale adoption in HPC. The role of the FPGA manufacturers is very crucial at this time since if FPGAs are to be able to compete with existing HPC accelerators, especially GPUs, significant improvements in both hardware and software capabilities are required. Among hardware features, the following improvements could prove valuable in HPC:

- The main source of performance bottleneck in current-generation FPGAs is external memory bandwidth. Even though the upcoming Stratix 10 MX series is the first step in addressing this issue, the higher memory bandwidth comes at the cost of less FPGA area and hence, lower peak compute performance compared to the Stratix 10 GX series. On

# FPGAs

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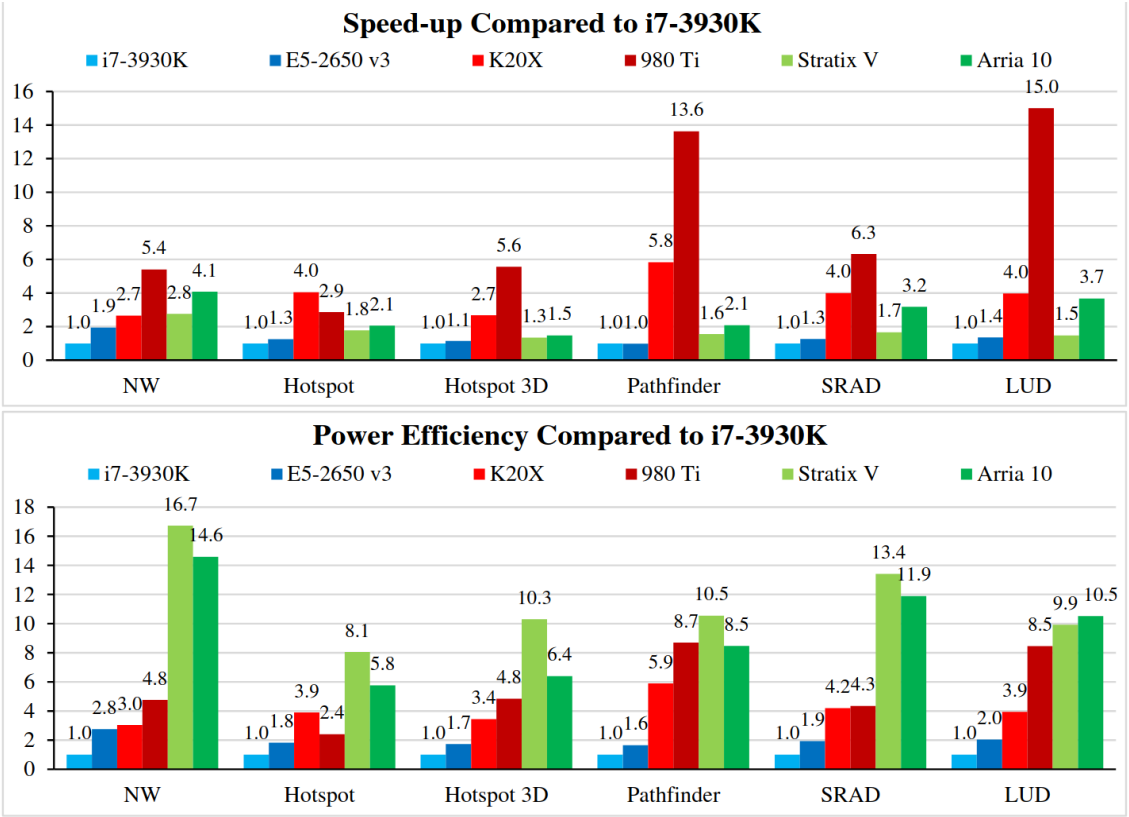

# Feedback

## TISS

- Please use TISS for regular term evaluation

## Additional Feedback

- Form `feedback.txt` in lecture notes folder
- Anonymous upload of feedback:
  `https://owncloud.tuwien.ac.at/index.php/s/Vwd0PoZEiK2oSZp`
- Zotter chocolate bar for each submission (until Feb 7)
  (anonymous handover via post office)

# Possible Next Steps

## Master Thesis

- Several offerings at the Institute for Microelectronics
- “Diplomarbeitenbörse”

## Projects

- Available
- Discuss details via phone/email/Zoom/etc.

# Bonus Lecture

## Starting Your Own Company - Lessons Learned

- Wednesday, January 27, 10:00-11:00 (approx.), this Zoom channel
- Feel free to invite anyone who might be interested
- Not part of 360.252

## Topics

- When and how to found?
- Funding
- Product development
- Good technology is not enough (sales, marketing, etc.)