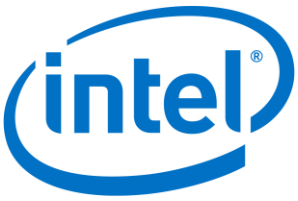

Intel® Curie™ Platform
Customer Reference Board (CRB)

Hardware User Guide

December 2015

Revision 005

Document Number: 333187-005

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Revision History

Revision	Description	Date
001	Initial release.	September 2015
002	Changed codenames to official product names.	October 1, 2015
003	Minor updates.	October 13, 2015
004	Added information on add-on boards.	November 2, 2015
005	Intel Software for Curie platform v2	December 2015

§

1 Introduction

This user guide describes the typical hardware set-up procedures, features, and use of the Customer Reference Board (CRB), for the Intel® Curie™ platform. This document must be read in its entirety prior to powering on the CRB.

Note: This document is relevant to the Intel® Curie™ CRB only. The references in this document correlates to reference designators and board properties of the Intel® Curie™ CRB. The CRB supports various additional interfaces through add-on boards. The details for the various add-on boards are mentioned in chapter 3.

1.1 Terminology

Table 1 Terminology

Term	Definition
A4WP	Alliance for Wireless Power
ADC	Analog-to-digital converter
ADXL	Product name from analog devices
AES	Advanced Encryption Standard
AFE	Analog front end
AOB	Add-on board
AON	Always on
APIC	Advanced programmable interrupt controller
ASIC	Application-specific integrated circuit
ATP	Intel® Quark™ SE
BDS	BeiDou navigation satellite system
BLE	Bluetooth Low Energy
CRB	Customer reference board
DAC	Digital-to-analog converter
DCP	Dedicated charging port
EAS	External architecture specifications
EEPROM	Electrically erasable programmable read-only memory
ERM	Eccentric rotating mass
ESD	Electrostatic discharge
GAL	GPS-aided lizard
GLONASS	Global navigation satellite system
GND	Ground
GPIO	General purpose input output
GPS	Global positioning system
HRM	Heart rate monitor
I2C	Inter-integrated circuit
I2S	Integrated interchip sound
ISA	International Society of Automation
JTAG	Joint Test Action Group
LDO	Low dropout
LED	Light emitting diode
LNA	Low-noise amplifier

NC	Not connected
NFC	Near Field Communications
OHRM	Optical heart rate monitor
OTP	One–time programmable
PLL	Phase-locked loop
PMIC	Power management IC
RF	Radio frequency
RISC	Reduced instruction set computer
RTC	Real-time clock
SAR	Specific absorption rate
SBAS	Satellite-based augmentation systems
SIM	Subscriber identity module
SoC	System-on-chip
SPIO	Serial peripheral interface bus
SRAM	Static random access memory
TBD	To Be Determined
TCM	Tightly-coupled memory
TFT	Thin-film transistor
UART	Universal asynchronous receiver/transmitter
UICC	Universal integrated circuit card
USB	Universal serial bus
WPC	Wireless Power Consortium

1.2 References

Table 2 Reference documents

Document name	Number/location
Curie_CRB_HW_Specification	TBD
CURIE_REF_BOARD_DESIGN	TBD
Intel® Curie™ Module Platform Design Guide (PDG)	558965
Intel® Curie™ Module External Design Specification (EDS)	559322

1.3 Block diagrams and connectors

Figure 1 Curie CRB block diagram

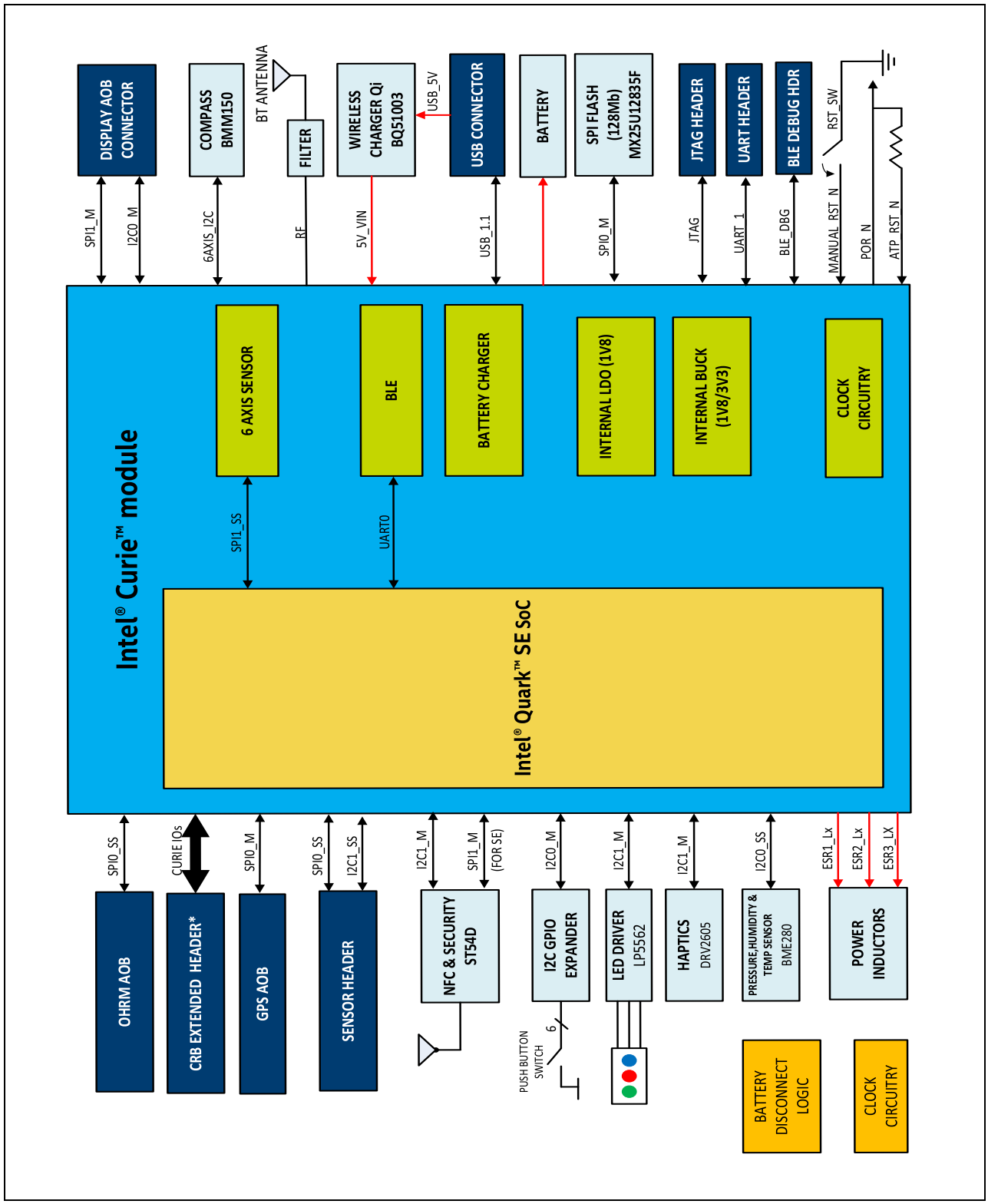


Figure 2 CRB front side showing connectors

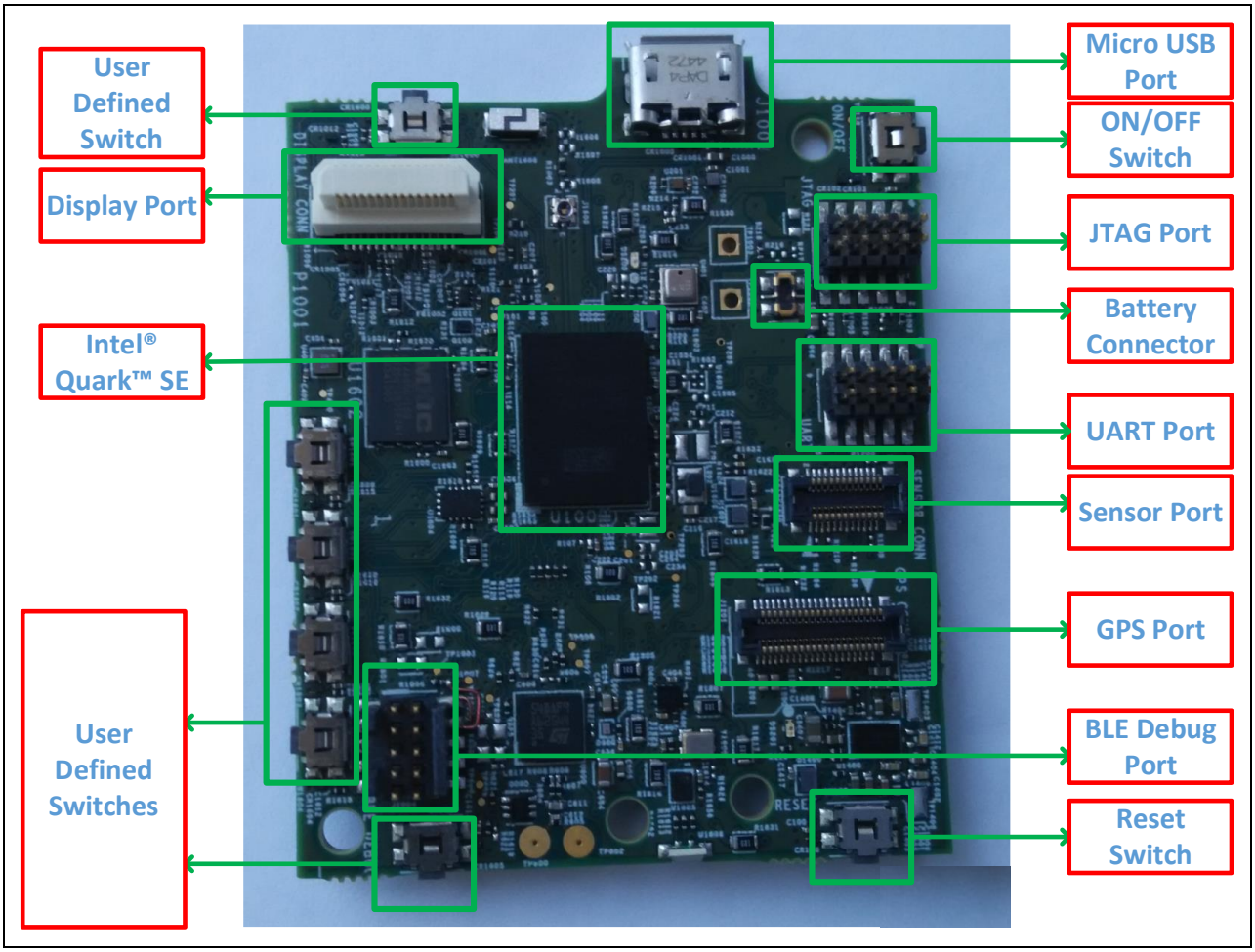


Table 3 CRB front items

Item	Description	More Info
Micro USB Port	Micro USB connection is used for both firmware flashing and charging.	N/A
ON/OFF Switch	To turn ON or OFF.	N/A
JTAG Port	It is port for JTAG connector, is dedicated debug port implementing a serial communications interface for low-overhead access without requiring direct external access to the system address and data buses.	*DebugCard*
UART Port	It is serial port for UART chip. The UART chip takes the parallel output of the computer's system bus and transforms it into serial form for transmission through the serial port.	*DebugCard*
Sensor Port	Provides interface for Sensor Connectors.	N/A
GPS Port	Provides interface for GPS Card.	*GPSAOB*
Reset Switch	Implements reset functionality.	N/A
BLE Debug Port	Interface to BLE debug connector which can be used to debug BLE on the Intel® Curie™ module. .	*DebugCard*
Intel® Quark™ SE	Atlas Peak SOC inside Curie which drives the CRB.	N/A
Display Port	Port for a digital SPI interface.	*DisplayAOB*
User defined Switches	Switches that are directly connected to Intel® Quark™ SE through the GPIO expander	N/A
Battery Connector	Port to connect external battery	N/A

Figure 3 CRB rear side showing connectors

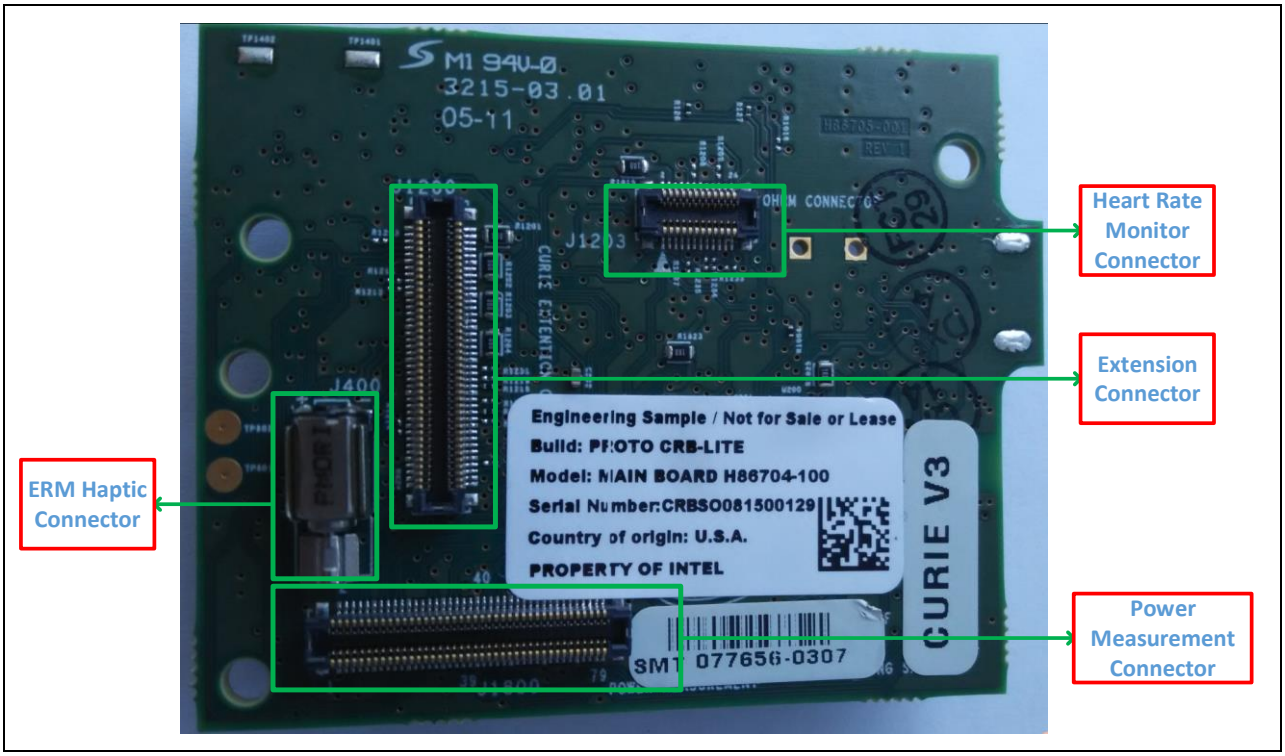


Table 4 CRB rear items

Item	Description	More Info
Heart Rate Monitor Port	Interface for external OHRM daughter card, measures individual's heart rate	*HeartRateMonitorAOB*
Extension connector	Has most of the Intel® Curie™ module's IOs, which are used for testing /probing those IOs and to connect external sensor board in future if necessary.	N/A
Power Measurement	Interface for measuring power consumption, specifically to measure individually how much current the platform devices are consuming	N/A
ERM Haptic Connector	Interface for ERM (Eccentric Rotating Mass) Haptics. Haptics-enabled system is any system that incorporates feedback via vibrations through the sense of touch.	N/A

1.4 CRB features

Table 5 CRB feature set summary

Feature	CRB implementation
SOC	• Intel architecture • 32/16/8/4MHz and 32.768KHz clock out for platform devices (from Atlas Peak SoC) • 32-bit address bus • Intel® Pentium® x86 ISA compatible without x87 floating point unit • 8 KB L1 instruction cache • Low latency data tightly coupled memory (TCM) interface to on-die SRAM • Integrated Local APIC and I/O APIC • Dimensions: 8.5 × 11mm, Weight: ~0.005 lb.
PMIC	• Integrated
Memory	• Integrated • 384 KB of on-die flash • 80 KB of on-die SRAM • 8KB OTP
Display interfaces	• Display available through SPI
Storage	• Serial flash memory through SPI is used for additional storage and its size is 128 Mb
IO	• I2C • I2S • USB • SPI • UART • JTAG • GPIO
User interface keypad/buttons	• Reset button • Power button
Sensors	• Compass/accelerometer/gyroscope • Pressure/barometer
Touch panel	• TBD
Wireless interfaces	• BLE • GPS • NFC-Security
Power/charging	• USB Based charging over micro AB connector supported for validation • TI's Single cell Li-ion battery charging unit • Qi Based Wireless Charging
Debug	• Primary JTAG • Debug Add-on Board (AOB) • USB Debug Port • Test Points, resistor pads on critical signals

1.5 Add-on boards

The CRB board modular design is achieved by various add-on boards:

Table 6 Add-on boards

Sl.No.	Name	Function
1	Display adapter	display and touch controller
2	GPS	Capable of global positioning by simultaneous reception of GPS, GLONASS, GAL, SBAS and BDS satellite system
3	Heart rate monitor	allows to measure one's heart rate in real time or record the heart rate for later study

Note: For more details on each add-on board, refer to the chapter 3.

1.6 Key I/O interfaces

1.6.1 USB 1.1 port mapping and OC mapping details

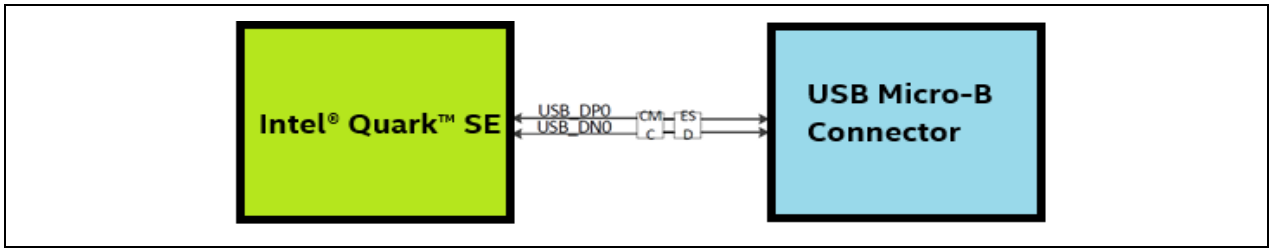
USB 1.1 port usages supported by Intel® Curie™ CRB is as below:

- USB Port0 is connected to a USB micro-B receptacle

Table 7 I/O interfaces

USB port	Reference description of mapped device port	Default/rework
USB Port 0	USB Port0 is connected to a USB micro-B receptacle	Default

Figure 4 USB 1.1 port topology

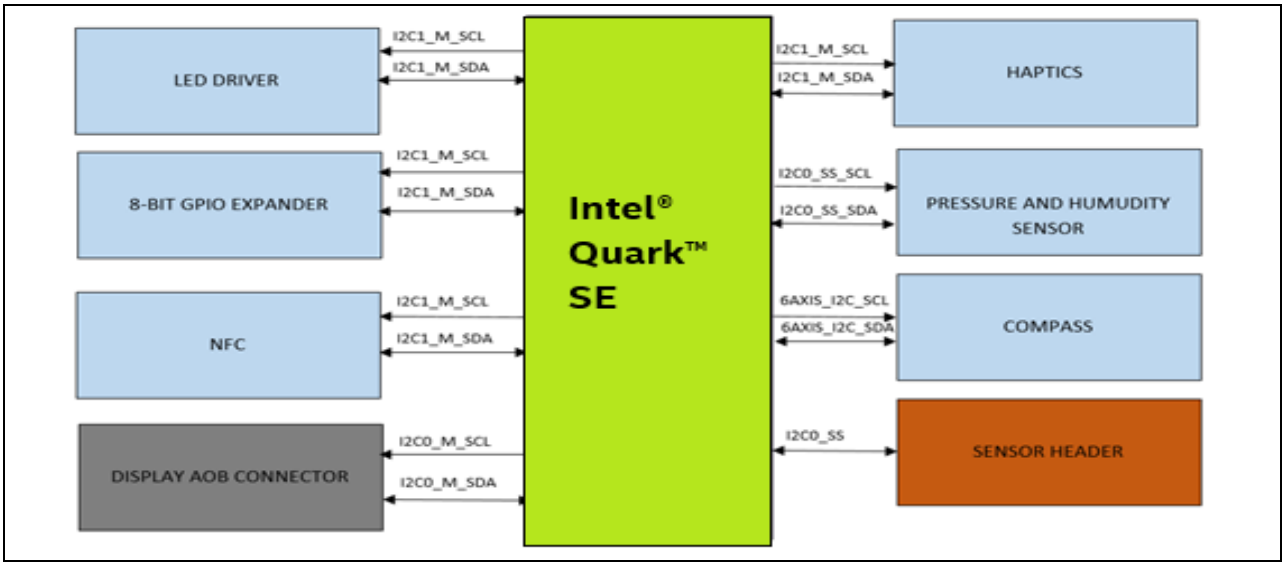


1.6.2 I²C port mapping details

Table 8 I²C port mapping

I2C	Subsystem	Device	Signal	RVP connectivity
I2C_0	Pressure, humidity and temperature sensor	BME280	I2C0_SS_SCL, I2C0_SS_SDA	Pressure, humidity and temperature sensor
	Display/touch ASIC	LS010B7DH02/CY8CTST241	I2C0_M_SCL, I2C0_M_SDA	Display / touch header
	I²C GPIO expander	PCA6408A	I2C0_SCL, I2C0_SDA	I²C GPIO expander
I2C_1	NFC	ST54D	I2C1_M_SCL, I2C1_M_SDA	NFC
	Haptics	DRV2605	I2C1_M_SCL, I2C1_M_SDA	Haptics
	LED driver	LP5562	I2C1_SCL, I2C1_SDA	LED driver

Figure 5 I2C connection block diagram on CRB

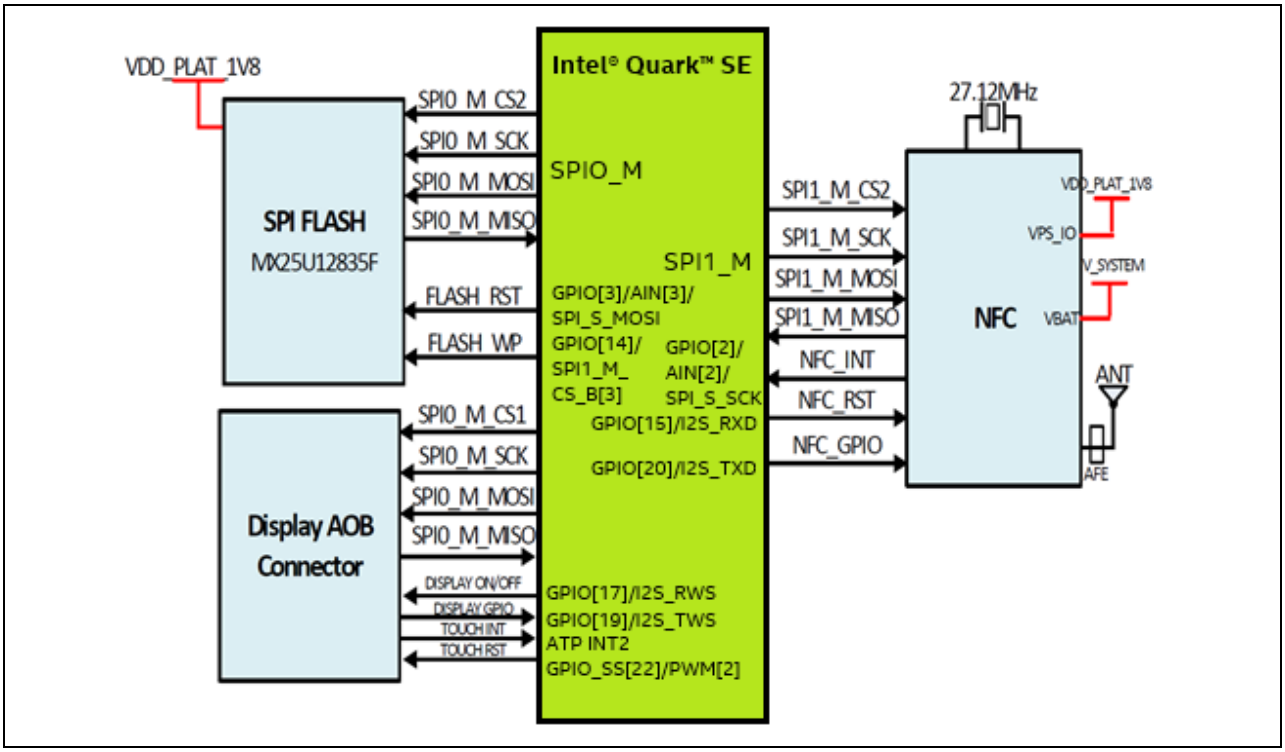


1.6.3 SPI port mapping details

Table 9 SPI port mapping

SPIO	Subsystem	Device	Signal	RVP connectivity
SPI0	GPS ASIC	BCM4774W	SPI0_M_CS1 SPI0_M_SCK SPI0_M_MOSI SPI0_M_MISO	GPS ASIC
	Heart rate monitor	H86709-001	SPI0_SS_CS3 SPI0_SS_CS1 SPI0_SS_SCK SPI0_SS_MOSI SPI0_SS_MISO SPI0_SS_CS2	Heart rate monitor
	SPI Flash	MX25U12835F	SPI0_M_CS2, SPI0_M_SCK, SPI0_M_MOSI, SPI0_M_MISO	SPI flash
SPI1	NFC	ST54D	SPI1_M_CS2 SPI1_M_SCK SPI1_M_MOSI SPI1_M_MISO	NFC
	Display ASIC	LS010B7DH02	SPI0_M_CS1 SPI0_M_SCK SPI0_M_MOSI SPI0_M_MISO	Display / touch header

Figure 6 SPI simplified topology



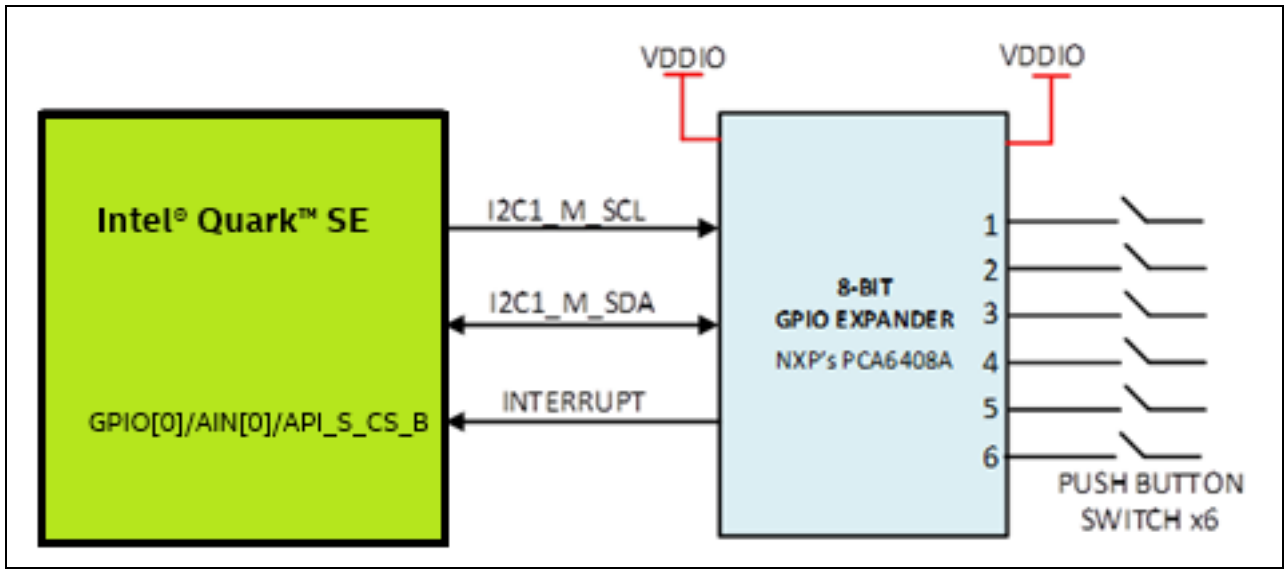
Note: Refer Figure 14 for more details on SPI signaling for GPS and OHRM.

1.6.4 I²C GPIO expander

The CRB uses an 8-bit I²C based GPIO expander. It is connected with Intel® Curie™ using I2C1_M. 6 general purpose buttons are connected to I²C GPIO expander. It features:

- Low standby current consumption of 1uA
- 400KHz fast mode I2C
- Active low reset input
- Open drain active low interrupt output
- Internal power-on reset

Figure 7 CRB-I2C GPIO expander



Note:

- Refer Intel® Curie™ EDS *[4]* for the AC and DC characteristics of accessible signals in Intel® Curie™ CRB
- Refer Intel® Curie™ PDG/EDS *[3]/[4]* for more info on connectors in Intel® Curie™ CRB

1.6.5 Power Supply Solutions, Usage, and Recommendations

There are two charging solutions for Curie CRB:

- Micro USB based charging
- Wireless Qi charging

Additional details about the power supply:

- The CRB is targeted to be configured for the 190 mAh battery by default.
- For wearable or otherwise space-constrained applications, a 40 mAh battery option is targeted with the CRB. This battery can reliably power the system, but you must budget overall battery capacity for your application and avoid high peak currents.
- The power supervisor in the Intel® Curie™ Module (Figure 9) will force a system reset if the VSYS voltage drops below 2.9 V for more than 25 micro-s. This voltage is selected so that the module cannot trip the protection circuit included in the battery itself.
- The CRB includes a wireless charging receiver based on the WPC (Qi) standard. Wireless charging based on the Rezence (A4WP) standard is possible, but this functionality is not built into the CRB. (Figure 8) shows the interface points.
- The battery system pin details depicted in (Figure 10) resides inside Intel® Curie™.

Figure 8 CRB-WPC/Qi Wireless Charging

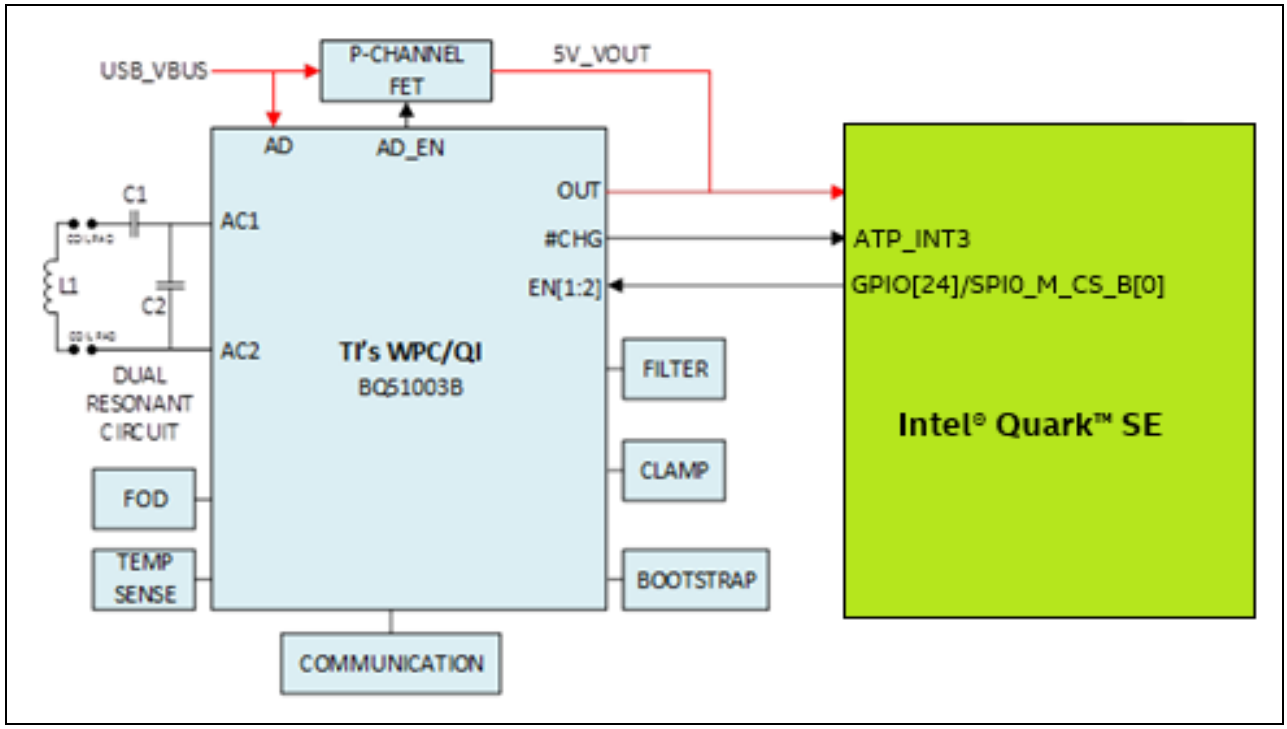


Figure 9 VSYS power supervisor in the Intel® Curie™ module

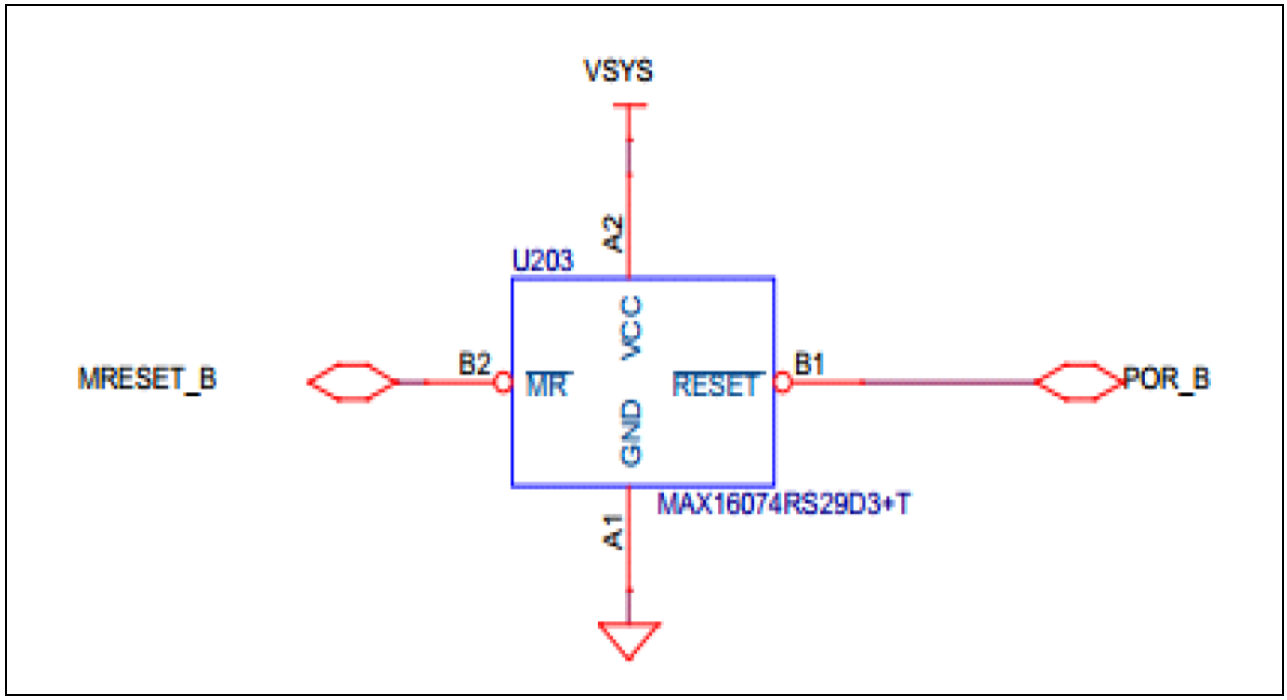
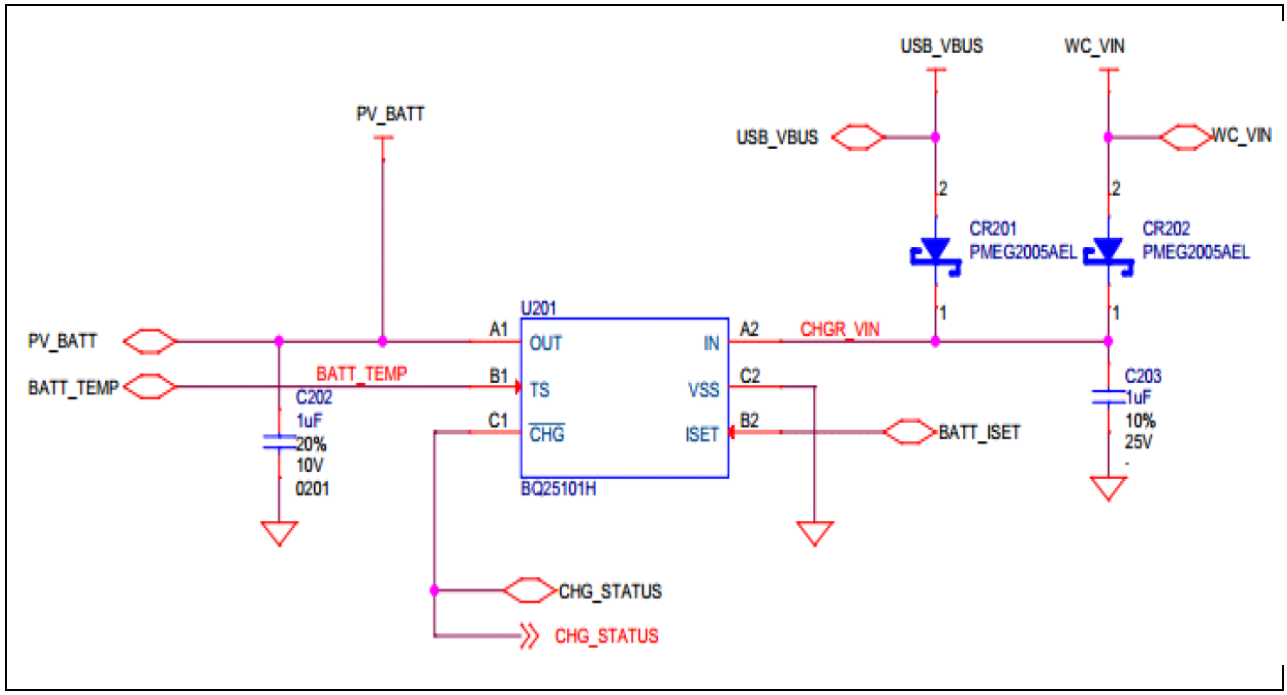


Figure 10 Battery Charging System Pin Diagram



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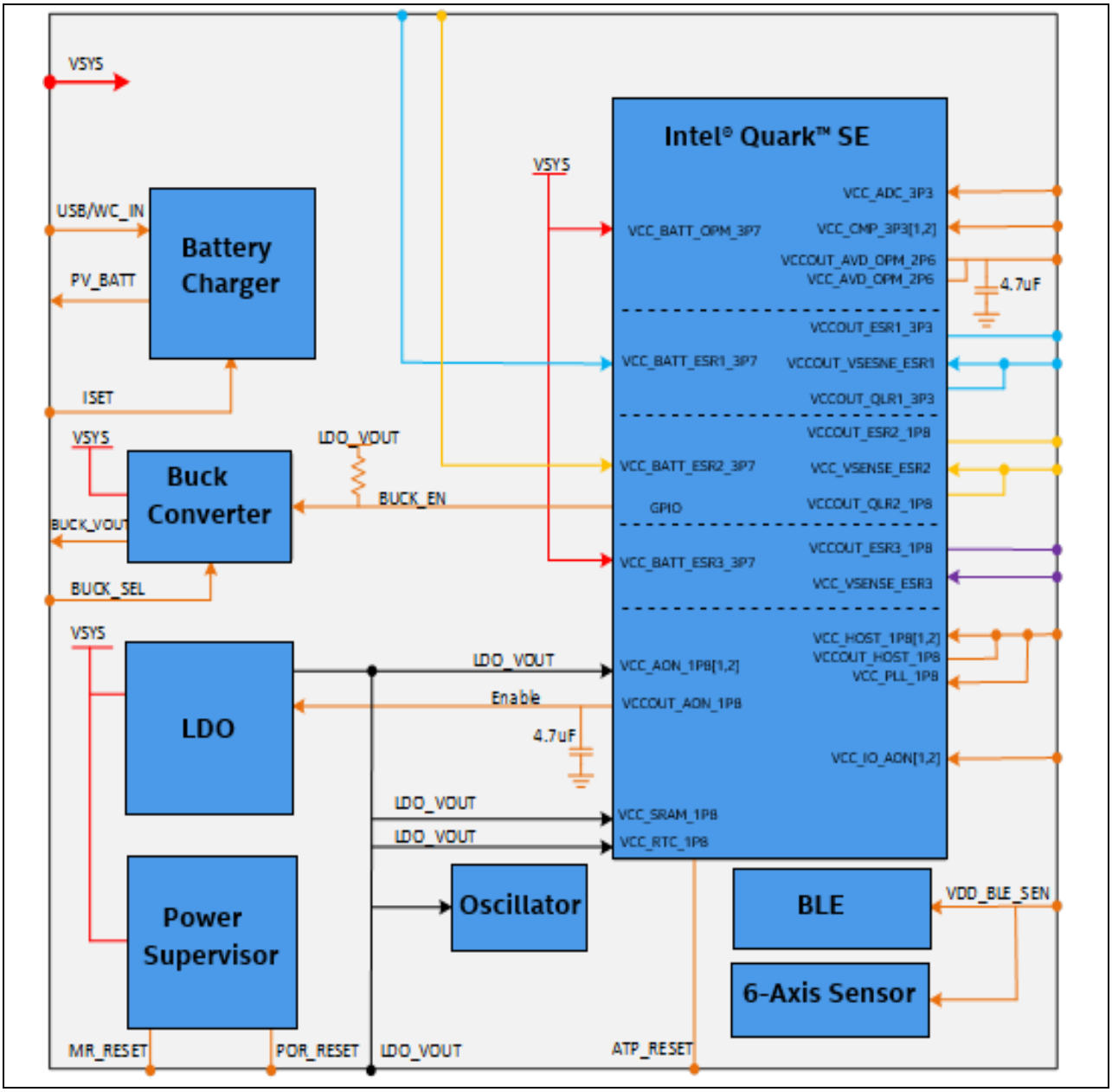
2 Power Architecture and Connectors

2.1 Power Architecture of Intel® Curie™.and CRB

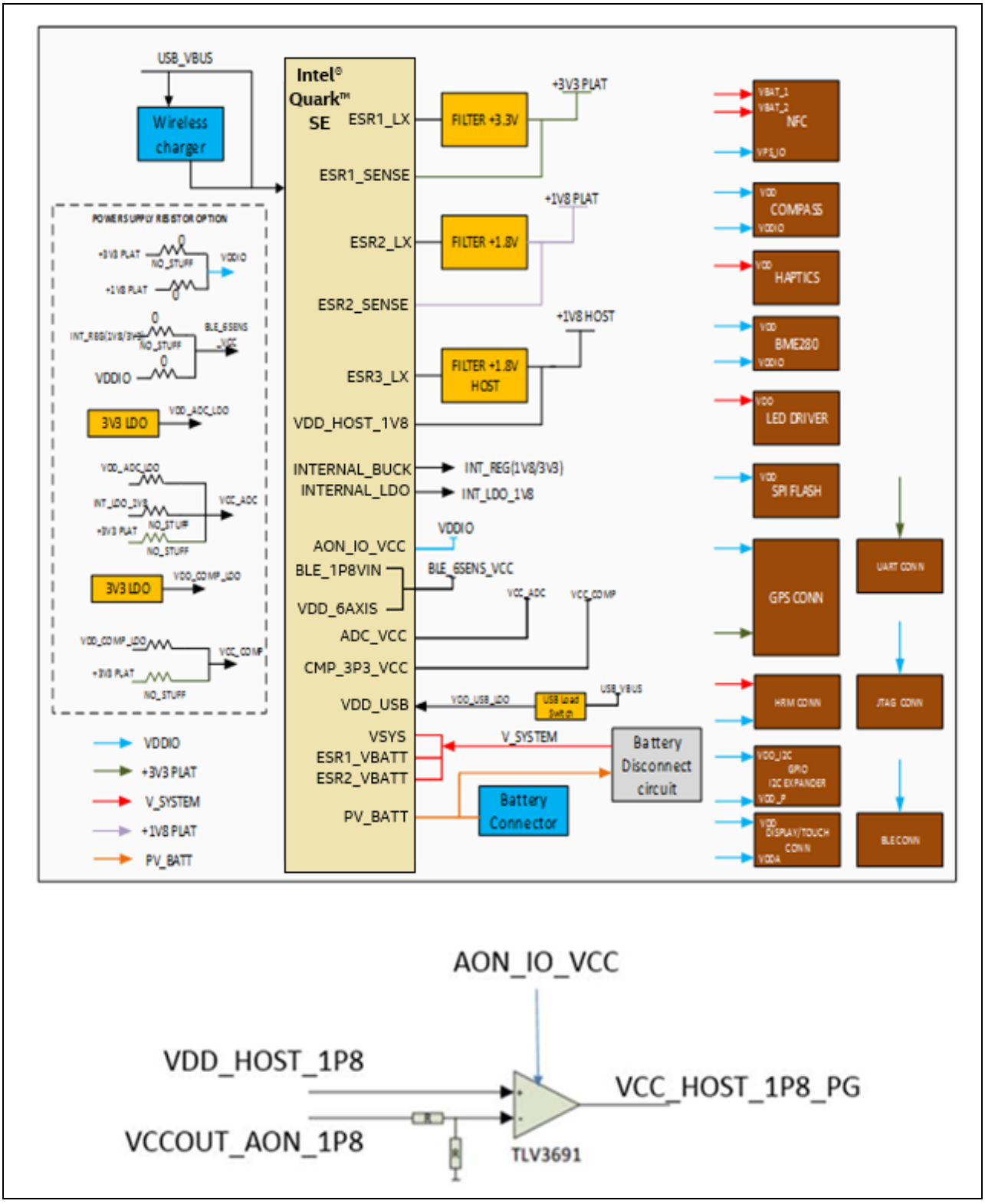
- Intel® Curie™ has power inputs, which are intended to be supplied from USB power or wireless charger device. On a priority basis, any one of those powers is fed to charger circuit located inside Intel® Curie™, which is controlled by a wireless charger. Battery will provide the required power to CRB.
- Intel® Curie™ provides power rails to their platform devices and host blocks. **Error! Not a valid bookmark self-reference.** shows the power output from Intel® Curie™ devices for host/platform devices.

Figure 11 Intel® Curie™.power architecture – I



2.1.1 CRB

Figure 12 Intel® Curie™ power architecture – II



The CRB consumes power from a batter, which is recharged through wireless charging system or USB. The battery delivers power to over voltage protection core, ESR1, ESR2, ESR3, internal switching regulator and internal LDO.

- ESR1 provides platform 3V3, which can be used by external platform devices such as sensors, GPS, display etc.
- ESR2 provides platform 1V8, which can be used by external platform devices such as sensors, GPS, display etc.
- ESR3 provides host 1V8, which is again feed in to Intel® Curie™. It is used for powering SoC's internal PLL.
- Internal LDO in Intel® Curie™ provides 1.8V to supply the SoC's AON (Always On) core, RTC and SRAM.
- Internal switching regulator in Intel® Curie™ provides 1.8/3.3 V@300 mA to platform devices.
- Intel® Curie™ has Smart Bluetooth and 6-axis chip, which has to be powered externally.
- Intel® Curie™ has separate power supplies for analog and comparator core, which has to be supplied from platform powers.

2.1.2 Intel® Curie™ Power Sequence

1. VCCOUT_AVD_OPM_2P6 starts and rises when VSYS rises above 1.9 V.
2. When VCCOUT_AVD_OPM_2P6 reaches a threshold Voltage (1.65 V), eSR 1, 2 get enabled and start raising.
3. eSR 1,2 raises at the same time as shown in Figure 13. In CRB, VCC_IO_AON is connected to any of these two rails.
   - As per ATP Power sequence requirement VCC_IO_AON, VCC_AON_1P8 should be powered before HOST_1P8.
4. VCCOUT_AON_1P8 ramps to 1.8V at T_ON_QLR0. (Final data is not available here. we have mentioned the test values)
5. Internal Intel® Curie™ LDO enable is connected to VCCOUT_AON_1P8, it starts ramping once VCCOUT_AON_1P8 reaches a threshold voltage.
   - LDO_OUT is connected to VCC_AON_1P8.
6. When VCCOUT_AON_1P8 reaches a threshold values (1.55V), eSR3 starts ramps to 1.8V at T_eSR time.
   - Once eSR3 has ramped up, VDD_HOST_1P8 will be at the same potential as VCCOUT_AON_1P8 (1.8V)
   - The comparator shown in Figure 12 pulls VCC_HOST_1P8_PG high to complete the power up sequence
7. BUCK_OUT reaches 1.8V at T_Buck_on time when proper power input applied.

Figure 13 CRB power up sequence

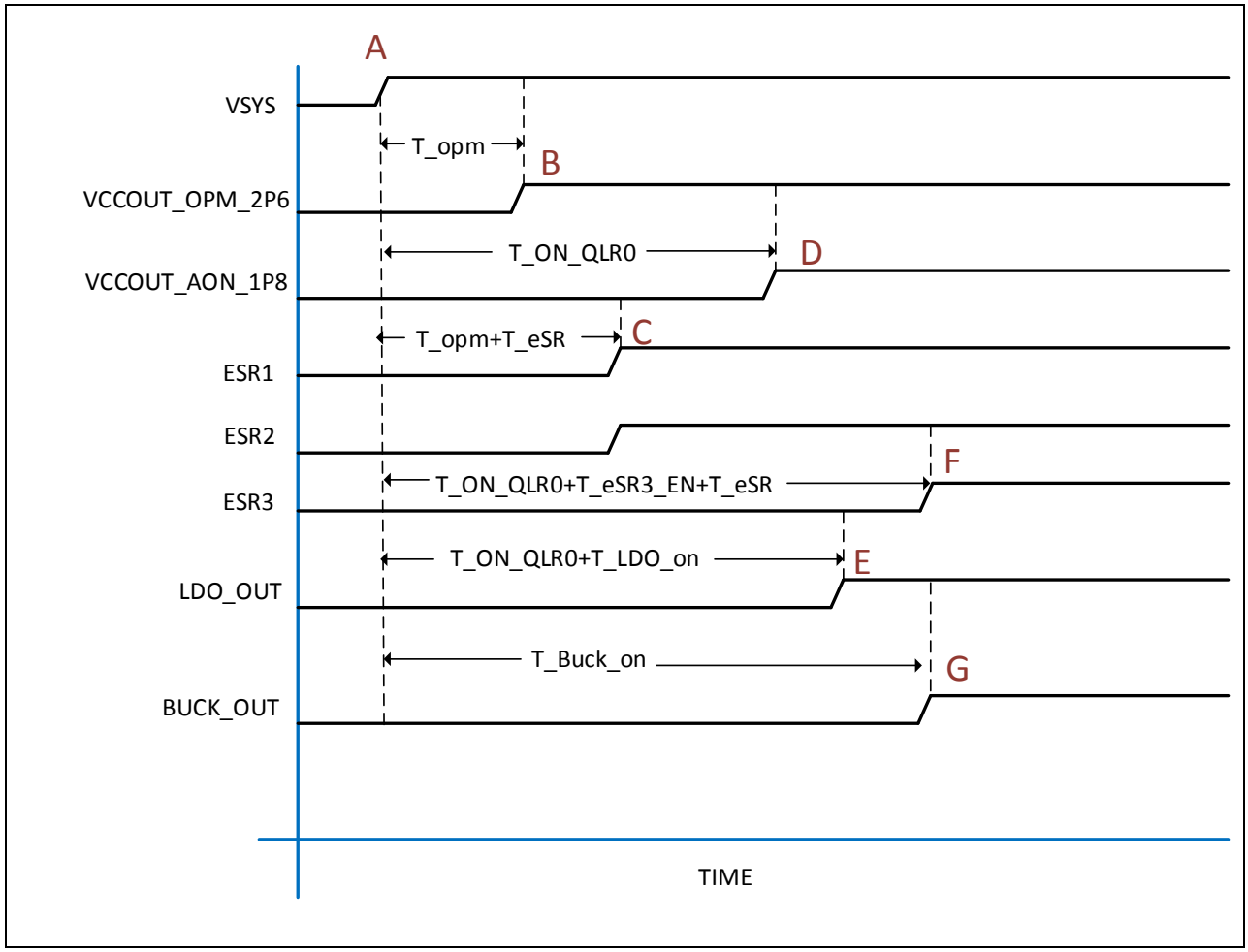
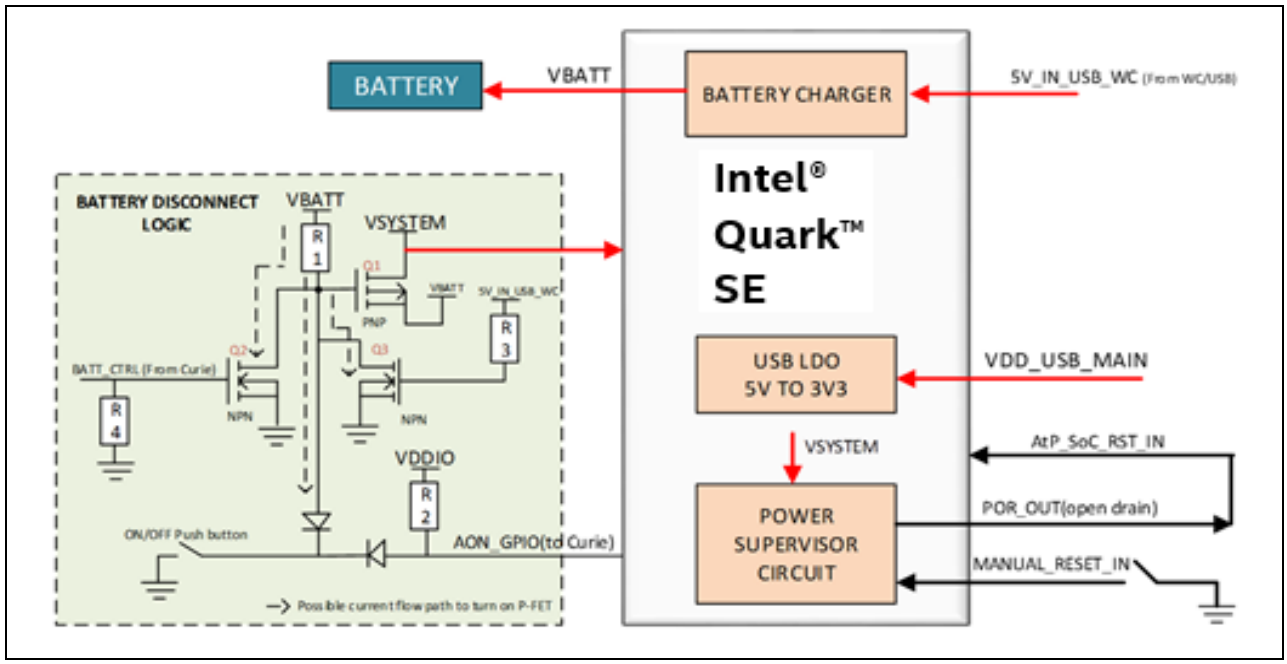


Table 10 Power-up sequence parameters

Parameter	Description	Min	Typical	Max	Remark
T_opm	Time for OPM regulator properly regulate output when main power is applied.	-	50 us	1000 us	From ATP EAS
T_ON_QLR0	Time interval for Internal qLR0 regulator to properly regulate the output.	-	6 ms	-	As per test result (need confirmation)
T_eSR	Time interval for eSR to properly regulate the voltage	-	0.15 ms	-	From ATP EAS
T_eSR3_EN	Time interval for eSR3 starts regulate the output voltage when VCCOUT_AON_1P8 reaches threshold (1.55V).	-	1.38 ms	-	As per test result (need confirmation)
T_LDO_on	Time interval for LDO properly regulate output voltage when Enable asserted.	-	~400 us	-	From datasheet
T_Buck_on	Time interval for Buck regulator properly regulate output voltage when Enable asserted.	-	10 ms	25 ms	From datasheet

2.1.3 Battery disconnect and SoC reset logic

Figure 14 CRB power supervisor



2.1.3.1 Reset logic:

To provide controlled input power to Intel® Curie™ and platform devices, system voltage is monitored for a threshold level by the power supervisor circuit, which is present inside Intel® Curie™. If system voltage falls below a threshold, the power supervisor pulls down the POR_OUT pin LOW to keep the SoC in reset state. When VSYSTEM reaches the voltage threshold (by charging the battery), the power supervisor releases the reset and SoC reset line held high.

CRB also has manual reset switch, so that reset can be provided to SoC by pressing the reset push button.

2.1.3.2 Battery disconnect logic

The CRB has battery disconnect logic, which is used to disconnect the battery from the system to avoid battery leakage during shipment and CRB OFF state. It works as follows:

- When the battery is initially inserted, Q1 gate is high due to resistor R1 and Q1 is in OFF state so that battery is disconnected from the system.
- To turn CRB on:
  - Press the ON/OFF push button, so that Q1 turns ON as its gate goes low. Hence, battery connected to V_SYSTEM and SoC is powered up. Meanwhile, under push button is in pressed state, SoC has to turn the BATT_CTRL GPIO high, so that Q1 remains in ON state permanently. Once push button released, SoC detects HIGH in push button GPIO line due to resistor R2.
    Or:
  - CRB has to be connected to charger (either USB or wireless charger), so that Q3 will turn ON due to pull-up resistor R3. Hence Q1 turns ON as its gate goes low and SoC is powered up by V_SYSTEM. Then SoC has to turn the BATT_CTRL GPIO high, so that Q1 remains in ON state permanently.
- To turn CRB off:
  - Push button has to be pressed, so that SoC detects LOW in AON_GPIO line. Immediately, SoC turns the BATT_CTRL GPIO line to LOW so that Q2 turns OFF. Once Q2 turns OFF, Q1 turns OFF due to its gate turns HIGH and battery is disconnected from V_SYSTEM.

2.2 CRB pin mapping details

Figure 15 CRB pin mapping details

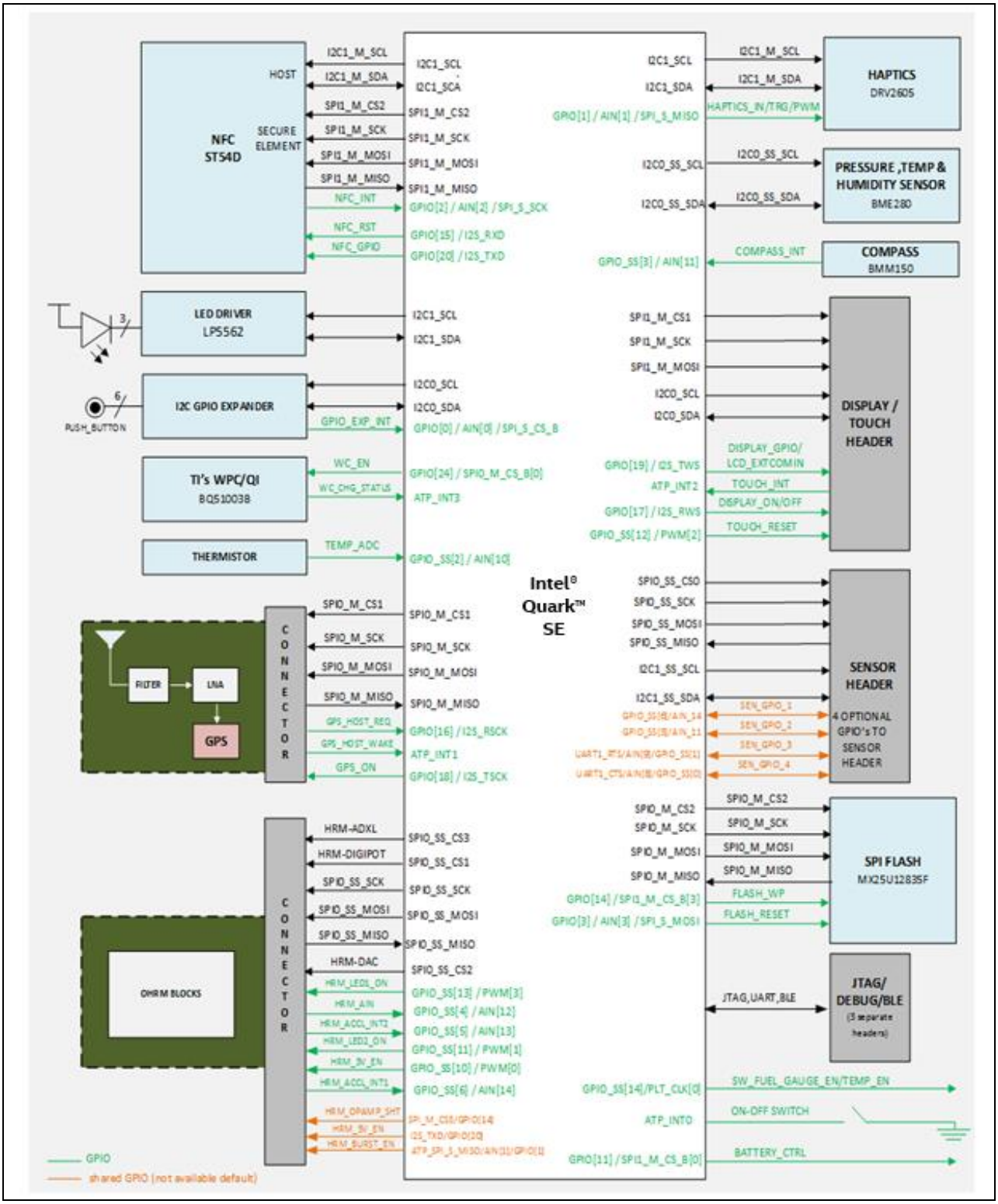


Table 11 I²C addresses

Section	Address
Pressure, humidity, temperature sensor	0x76
Magnetometer	0x10
Haptics control	0x5A
NFC	0x08
I2C_Expander	0x20
LED driver	0x30
Touch sensor	0x24

Table 12 CRB interface list

Interface	CRB
I2C0	I2C GPIO EXPANDER, TOUCH CONTROLLER
I2C1	NFC,LED DRIVER,HAPTICS
I2C0_SS	BME280
I2C1_SS	SENSOR CONNECTOR
6_AXIS_I2C	COMPASS
SPI0_M_CS0	-
SPI0_M_CS1	GPS
SPI0_M_CS2	SPI Flash
SPI0_M_CS3	-
SPI1_M_CS0	-
SPI1_M_CS1	DISPLAY
SPI1_M_CS2	NFC
SPI1_M_CS3	-
SPI0_SS_CS0	SENSOR CONNECTOR
SPI0_SS_CS1	HRM-DIGIPOT
SPI0_SS_CS2	HRM-DAC
SPI0_SS_CS3	HRM_ADXL
SPI1_SS_CS0	-
SPI1_SS_CS1	BMI160 (on Intel® Curie™ Module)
SPI1_SS_CS2	-
SPI1_SS_CS3	-
I2S	-
UART0	NRF51822 (on Intel® Curie™ Module)
UART1	UART DEBUG CONNECTOR

2.3 Connector details

2.3.1 HRM connector

Table 13 HRM connector signal list

Pin	Signal	Signal	Pin
1	GND	GND	2
3	HRM_AIN	V_SYSTEM_HRM	4
5	GND	VDD_IO_HRM	6
7	HRM_OP_AMP_SD *	GND	8
9	SPI0_SS_CLK	HRM_ADXL_INT_1 *	10
11	SPI0_SS_MOSI	HRM_5V_EN *	12
13	GND	GND	14
15	SPI0_SS_MISO	HRM_LED_ON_1	16
17	OHRM_DAC_CS	HRM_LED_ON_2	18
19	GND	HRM_BURST_EN *	20
21	OHRM_DIGIPOT_CS	HRM_3V_EN	22
23	OHRM_ACCEL_CS	HRM_ADXL_INT_2	24

* This signal is multiplexed with other signals. Refer to the CRB schematic to select the mux option.

2.3.2 GPS connector

Table 14 GPS connector signal list

Pin	Signal	Signal	Pin
1	NC	NC	2
3	GND	NC	4
5	NC	SPI0_M_SCK	6
7	NC	GND	8
9	NC	SPI0_M_MOSI	10
11	NC	SPI0_M_MISO	12
13	NC	GPS_ON *	14
15	VDD_PLAT_3V3	NC	16
17	NC	NC	18
19	NC	NC	20
21	NC	NC	22
23	NC	GPS_HOST_WAKE	24
25	SPI0_M_CS1_N	GPS_HOST_REQ *	26
27	GND	NC	28
29	NC	NC	30
31	VDD_PLAT_3V3	NC	32
33	NC	GND	34
35	NC	VDD_IO_GPS	36
37	GND	VDD_IO_GPS	38
39	NC	VDD_PLAT_3V3	40

* This signal is multiplexed with other signals. Refer to the CRB schematic to select the mux option.

2.3.3 Display connector

Table 15 Display connector signal list

Pin	Signal	Signal	Pin
1	V_SYSTEM_DISPLAY	VDD_PLAT_3V3	2
3	DISPLAY_5V_EN *	SPI1_M_MOSI	4
5	NC	DISP_SPI1_M_CS1_N	6
7	NC	DISPLAY_ON_OFF *	8
9	NC	DISPLAY_GPIO *	10
11	NC	VDD_IO_DISPLAY	12
13	NC	SPI1_M_SCK	14
15	NC	GND	16
17	GND	TOUCH_INT_N	18
19	NC	TOUCH_RST_N	20
21	NC	VDD_IO_DISPLAY	22
23	GND	GND	24
25	GND	GND	26
27	GND	I2C0_M_SCL	28
29	GND	I2C0_M_SDA	30

* This signal is multiplexed with other signals. Refer to the CRB schematic to select the mux option.

2.3.4 Sensor connector

Table 16 Sensor connector signal list

Pin	Signal	Signal	Pin
1	GND	GND	2
3	GPIO_SS_0 *	V_SYSTEM	4
5	GND	VDD_IO	6
7	GPIO_SS_1 *	GND	8
9	I2C1_SS_SCL	NC	10
11	I2C1_SS_SDA	NC	12
13	GND	GND	14
15	SPI0_SS_SCK	SPI0_SS_MOSI	16
17	SENS_CONN_SPI0_SS_CS0_N	SPI0_SS_MISO	18
19	GND	NC	20
21	GPIO_SS_3 *	GPIO_SS_6 *	22
23	NC	NC	24

* This signal is multiplexed with other signals. Refer to the CRB schematic to select the mux option.

2.3.5 Extended IO connector

Table 17 CRB Extended IO connector signal list

Pin	Signal	Signal	Pin
1	GND	GND	2
3	FLASH_SPI0_M_CS2_N	V_SYSTEM	4
5	NFC_SPI1_M_CS2_N	NC	6
7	WC_EN	NC	8
9	BATTERY_CTRL	NC	10
11	GND	GND	12

13	I2C_EXP_INT_N	NC	14
15	FLASH_RST_N	VDD_IO	16
17	GPIO_15	NC	18
19	GPIO_2	NC	20
21	GND	GND	22
23	NC	NC	24
25	I2C1_M_SDA	NC	26
27	I2C1_M_SCL	VDD_PLAT_1V8	28
29	NC	NC	30
31	GND	GND	32
33	BLE_SCL	NC	34
35	BLE_SDA	NC	36
37	ATP_RESET_N	NC	38
39	WC_STATUS	VDD_PLAT_3V3	40
41	GND	GND	42
43	BT_GPIO	NC	44
45	EXT_TEMP_MEASURE	GPIO_SS_12	46
47	COMPASS_INT_N	GPIO_17	48
49	SW_FG_TEMP_EN	GPIO_16	50
51	GND	GND	52
53	6_AXIS_INT	NC	54
55	NC	GPIO_19	56
57	I2C0_SS_SDA	GPIO_20	58
59	I2C0_SS_SCL	GPIO_18	60
61	GND	GND	62
63	GPIO_1	NC	64
65	SPI1_M_MISO	SPI0_M_MISO	66
67	SPI1_M_MOSI	SPI0_M_MOSI	68
69	SPI1_M_SCK	SPI0_M_SCK	70
71	GND	GND	72
73	I2C_6AXIS_COMPASS_SCL	EXT_GPIO_1	74
75	I2C_6AXIS_COMPASS_SDA	EXT_GPIO_2	76
77	GND	GND	78
79	GND	GND	80

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3 Add-on Boards

3.1 GPS AOB

Broadcom BCM4774W Global Navigation Satellite System (GNSS) is used in CRB, which is available as a personality module. It is connected with Intel® Curie™ using SPI0_M interface. Other blocks in the module include LNA and SAW filters to improve RF performance. It features:

- ARM-based 32-bit Cortex-M4F core
- Digital SPI interface
- Simultaneous reception of GPS, GLONASS, GAL, SBAS and BDS satellite system
- Integrated 12-bit 8-channel ADC.
- Integrated GNSS baseband and RF
- Small footprint of 2.87mm x 4.188mm x 0.5mm

Table 18 provides the power consumption details.

Table 18 Power consumption details

Power supply	Voltage range(V)		Typical current consumption (mA)
	Min	Max	
VDD_PMU_IN	1.62	3.63	60
VDD_PMU_IN_AON	1.62	3.63	5
VDD_IO	1.62	3.63	5

Figure 16 CRB-GPS header

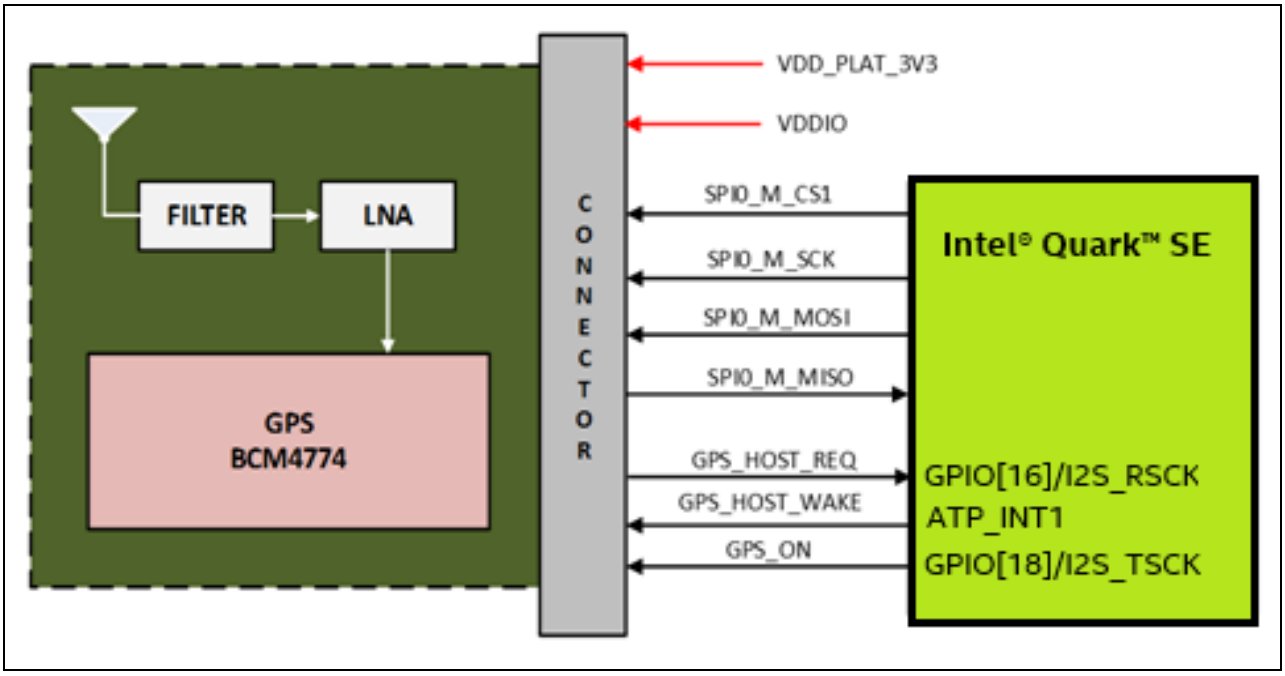
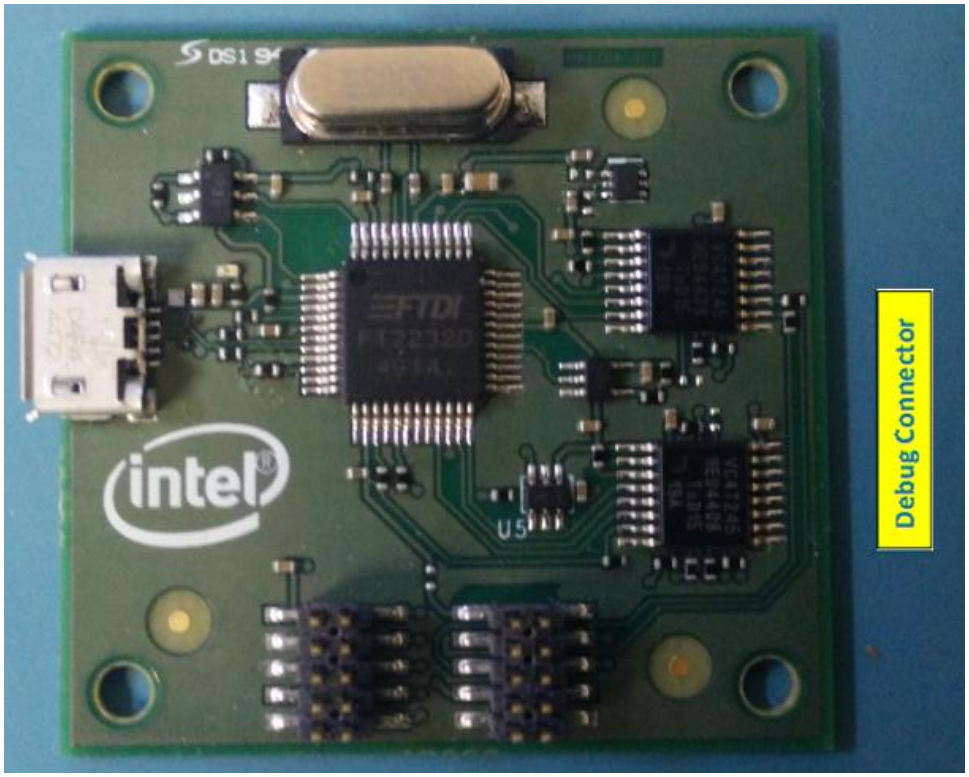


Figure 17 GPS AOB

3.1.1 Debug card

- CRB has a USB1.1 interface, which is used for communication with USB host, as well as one of the charging port. It works only in device mode. USB lines are protected with ESD diodes for safe performance. A 1.07K bleeding resistor is added in USB power line to provide an immediate discharge path for USB power.
- JTAG is provided to the JTAG connector, which is used to flash/debug Intel® Curie™. Additionally, there is a BLE debug connector and UART connector, which can be used to debug the BLE chipset and Intel® Curie™.
- JTAG and UART connectors can be mated with debug AOB for USB-UART/USB-JTAG based debugging.

Figure 18 Debug card AOB



3.2 Display AOB

CRB has a display connector, which is mated with an add-on board that has a mating connector for display and touch controllers.

A Sharp LS010B7DH02 display is used in CRB. It features:

- Transflective panel of white and black.
- Digital SPI interface.
- 1.02" screen with 96 x 150 resolution.
- 1-bit internal memory for data storage within the panel.
- Superlow power consumption TFT panel.

Table 19 provides the power consumption details.

Table 19 Power consumption details

Power supply	Voltage range (V)		Typical current consumption (mA)
	Min	Max	
VDDA	2.7	3.3	TBD
VDD	2.7	3.3	TBD

A Cypress CY8CTST241 capacitive touch screen controller is used in CRB. It is connected with Intel® Curie™ using I2C0. It features,

- Up to 32 sense pin.
- Large object detection.
- Resistant to LCD noise.
- Wide supply voltage range from 1.71V to 5.5V.
- Integrated voltage regulator.

Table 20 provides the power consumption details for touch controller.

Table 20 Power consumption details

Power supply	Voltage range(V)		Typical current consumption(mA)
	Min	Max	
VDD	1.71	5.5	2

Figure 19 CRB display connector

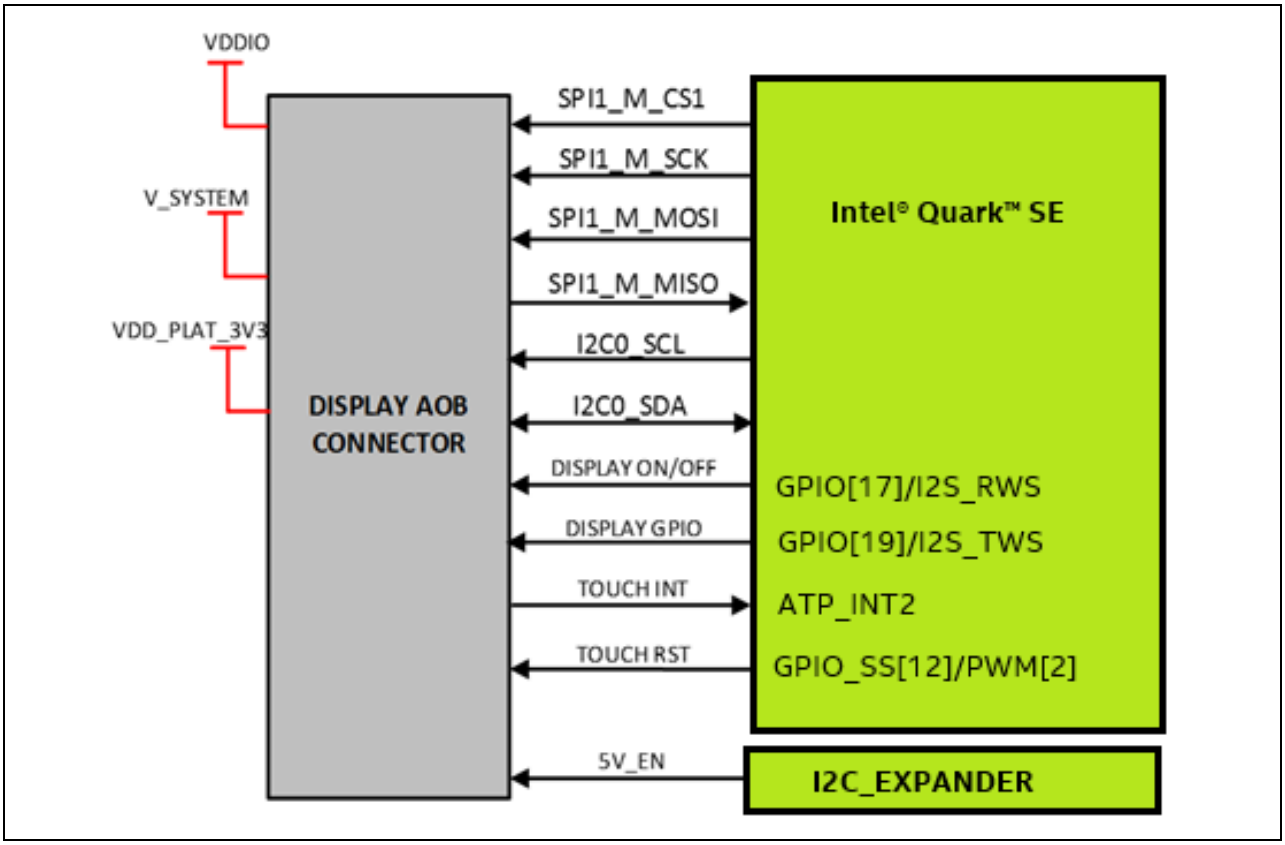
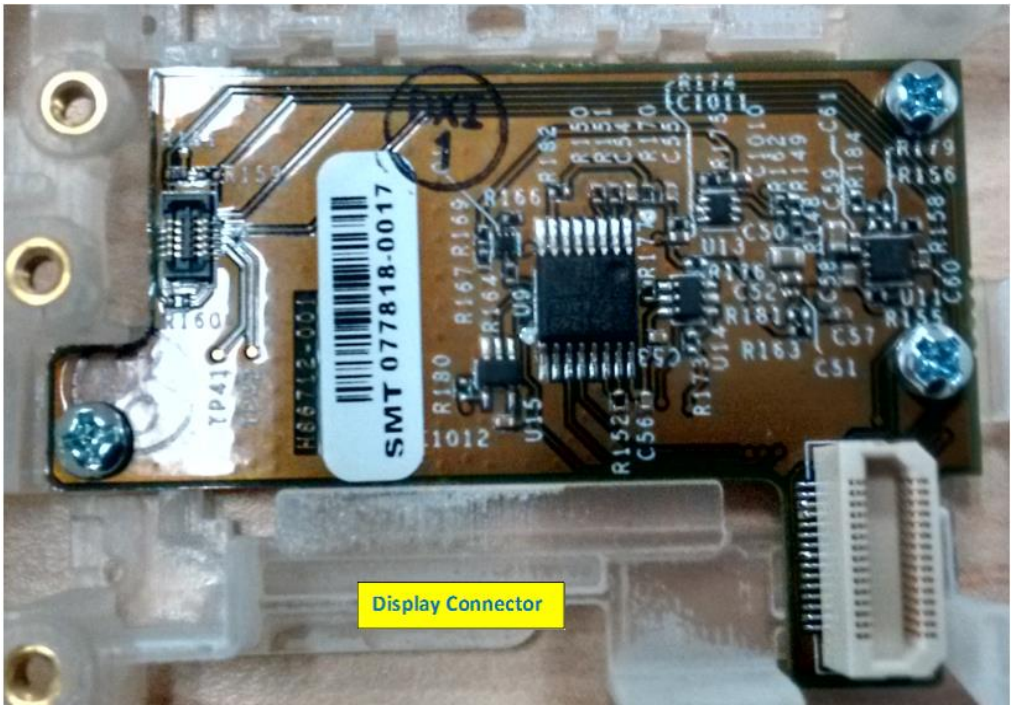


Figure 20 Display AOB

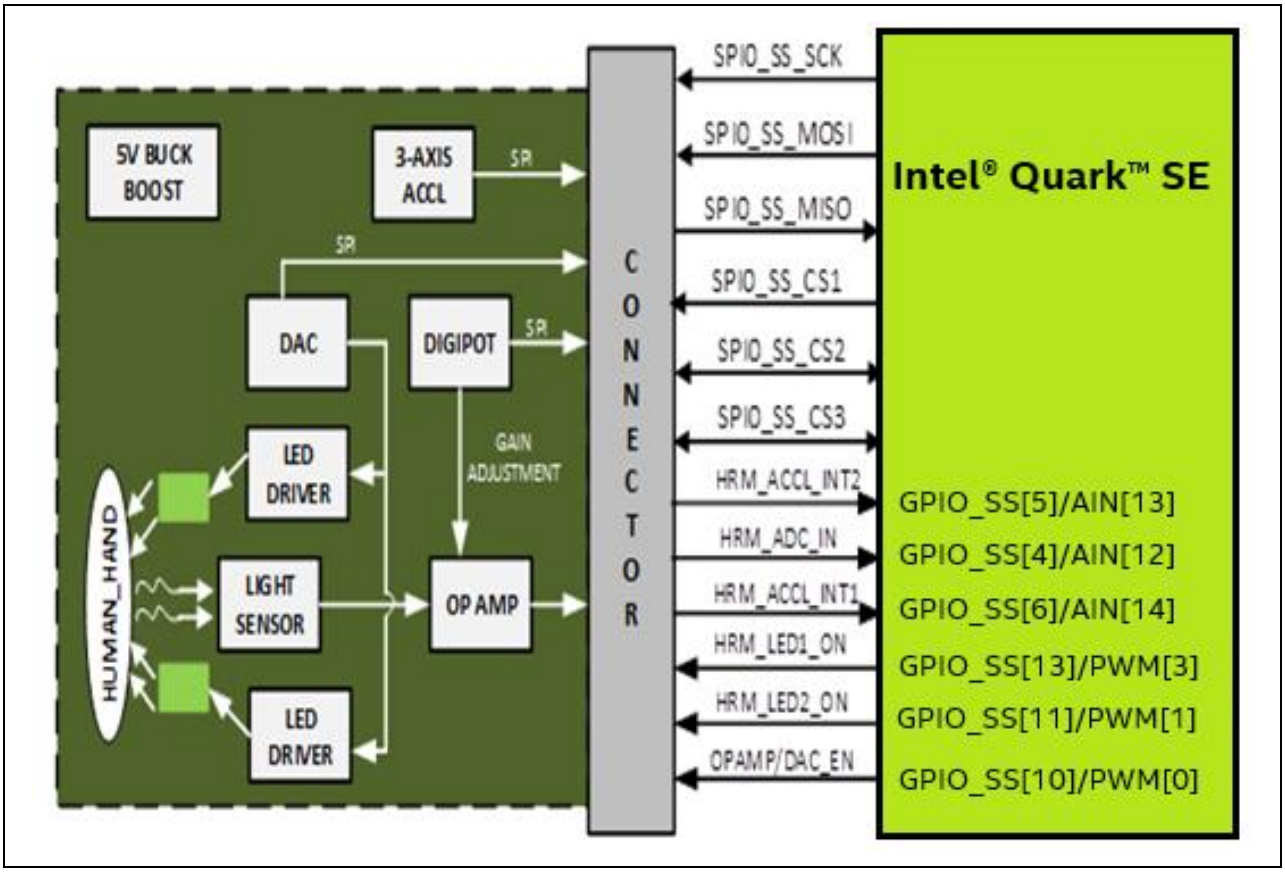


3.3 Heart rate monitor AOB

CRB has a Heart Rate Monitor (HRM) connector, which is connected to the HRM daughter board. It frequently measures an individual's heart rate and communicates with the processor. SPI0_SS is connected to the HRM connector to use with ADXL, DAC, and Digital potentiometer.

Due to very high power consumption of the LED light sources, these circuits are duty cycled to reduce the average power, typically operated at a 32 Hz rate. Upon activation, the circuits must settle and be ready in 10 us. The DAC provides a reference current for the LED driver to set LED current. A trans-impedance amplifier converts the photo diode current to a voltage which is sampled by the ADC in the Intel® Curie™ module. 5V power for the LEDs is provided by a local high efficiency boost converter.

Figure 21 CRB-HRM



3.4 OHRM data acquisition

This section describes how to control the hardware to initialize and operate the OHRM hardware to collect data samples. This same technique should be used for both normal operation of the heart beat monitor and for testing of the hardware system. In the test case, the measured samples can just be recorded for analysis. In normal operation, the heart rate algorithm shall be passed the resulting samples.

These variables will be updated by the algorithm or can be manipulated manually for testing.

- Integration time (how long LED light source is on before sampling). Typ 100-300us.
- LEDs to activate (1 or both).
- DAC voltage (LED drive current setting).
- Digipot settings for TIA.

3.4.1 Data acquisition timing

Sampling at 32Hz Rate

T = 0

Wake up DAC

- control register: PD0, PD1 = 1 (normal mode)
- Will take 600us for internal reference to stabilize

T = 600us

- BURST_EN = 1, OP_AMP_SD = 1
- Trigger accelerometer sampling
- Set DAC output voltage (variable)

T = 610us (settling time for DAC)

- Enable LED. LED_ON_1, LED_ON_2 (variable)
- Wait to allow photons to integrate in photo diode

T = 610us + integration time

- Read ADC value. Optional take 16 samples and average
- OP_AMP_SD = 0 (put op amp in to shutdown)
- Data acquisition is complete
- Do Initialization steps (below)
- Record data value for debug / test
- Send data to algorithm
- Intel® Curie™ can sleep on timer until next cycle

T = 34ms. Repeat above.

Initialization:

- LED_ON_1, LED_ON_2 = 0
- VDD_5V_EN = 1
- BURST_EN = 0
- VDD_3V_A_EN = 1
- Initialize registers of DAC via SPI. State = shutdown
- OP_AMP_SD = 0

Power Down:

- LED_ON_1, LED_ON_2 = 0
- VDD_5V_EN = 0
- BURST_EN = 0
- VDD_3V_A_EN = 0
- OP_AMP_SD = 0

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