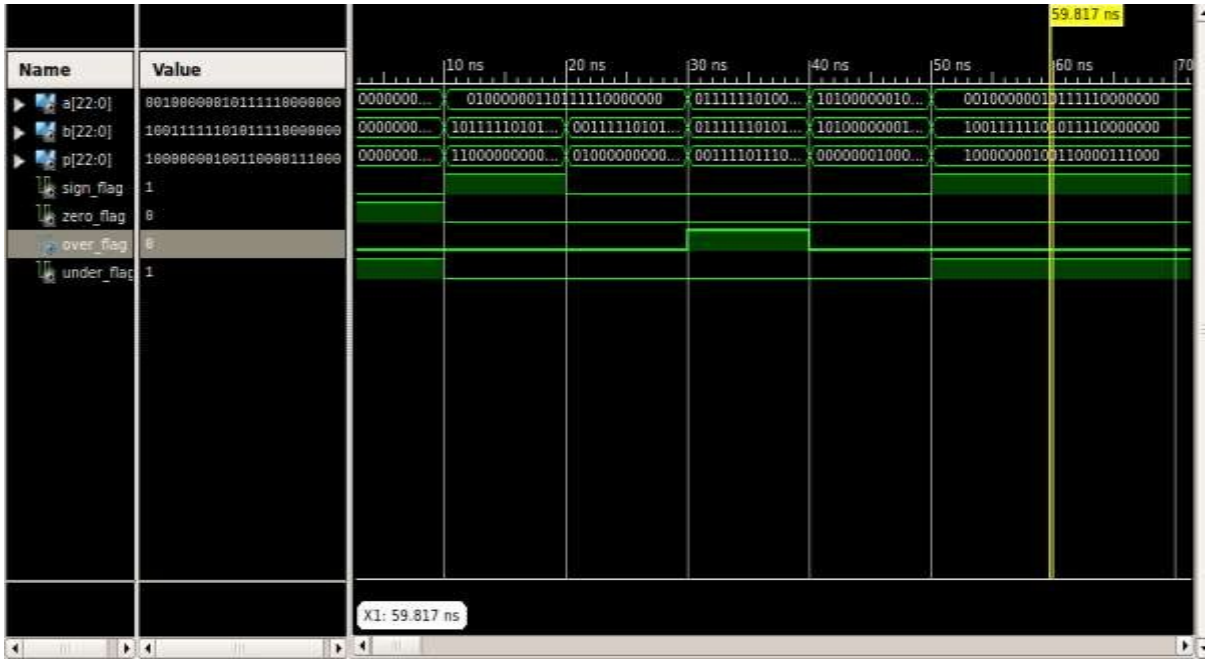
Lab 4 Report

1. Behavioral Simulation snapshots



A <= "0" & "10000001" & "10111110000000";
B <= "1" & "01111101" & "01011110000000";
sign_flag = 1; zero_flag = 0; over_flag = 0; under_flag = 0.

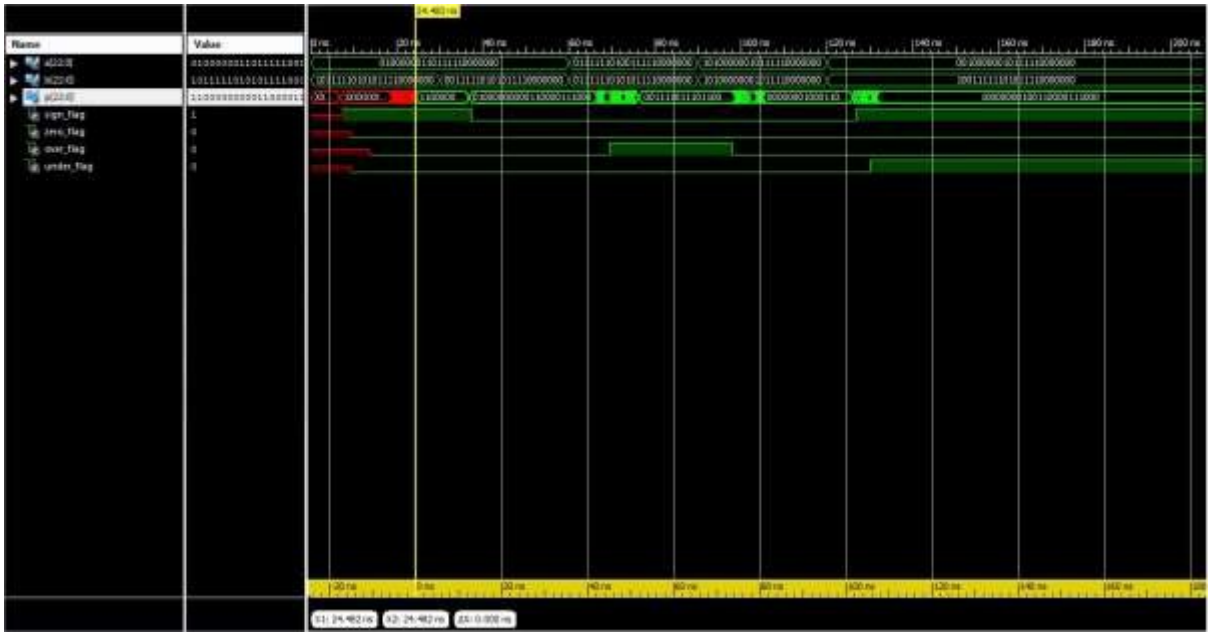
A <= "0" & "10000001" & "10111110000000";
B <= "0" & "01111101" & "01011110000000";
sign_flag = 0; zero_flag = 0; over_flag = 0; under_flag = 0.

A <= "0" & "11111101" & "00111110000000";
B <= "0" & "11111101" & "01011110000000";
sign_flag = 0; zero_flag = 0; over_flag = 1; under_flag = 0.

A <= "1" & "01000000" & "10111110000000";
B <= "1" & "01000000" & "01011110000000";
sign_flag = 0; zero_flag = 0; over_flag = 0; under_flag = 0.

A <= "0" & "01000000" & "10111110000000";
B <= "1" & "00111111" & "01011110000000";
sign_flag = 1; zero_flag = 0; over_flag = 0; under_flag = 1.

2. Post PAR simulation snapshots



A <= "0" & "10000001" & "10111110000000";
B <= "1" & "01111101" & "01011110000000";
wait for 30 ns;
sign_flag = 1; zero_flag = 0; over_flag = 0; under_flag = 0.

A <= "0" & "10000001" & "10111110000000";
B <= "0" & "01111101" & "01011110000000";
wait for 30 ns; -- OverFlow
sign_flag = 0; zero_flag = 0; over_flag = 0; under_flag = 0.

A <= "0" & "11111101" & "00111110000000";
B <= "0" & "11111101" & "01011110000000";
wait for 30 ns;
sign_flag = 0; zero_flag = 0; over_flag = 1; under_flag = 0.

A <= "1" & "01000000" & "10111110000000";
B <= "1" & "01000000" & "01011110000000";
wait for 30 ns; -- UnderFLow
sign_flag = 0; zero_flag = 0; over_flag = 0; under_flag = 0.

A <= "0" & "01000000" & "10111110000000";
B <= "1" & "00111111" & "01011110000000";
sign_flag = 1; zero_flag = 0; over_flag = 0; under_flag = 1.

3. Analysis

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Timing Summary:
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Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 47.513ns
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Combinational path delay consists 27.461ns logic and 20.052ns routing delays.
Logic delay contributes 57.8% and routing delay contributes 42.2% to combinational path delay. .
Maximum operation frequency is 21.047 MHz.

The number of LUTs and other resources:

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**N**
Number of 4 input LUTs	540	9,312	5%	
Number of occupied Slices	311	4,656	6%	
Number of Slices containing only related logic	311	311	100%	
Number of Slices containing unrelated logic	0	311	0%	
Total Number of 4 input LUTs	547	9,312	5%	
Number used as logic	540			
Number used as a route-thru	7			
Number of bonded IOBs	73	232	31%	
Average Fanout of Non-Clock Nets	2.87			