# I² C interface, 16-way breathing light, extended GPIO controller

## characteristics

- Supports 16-way common anode constant-current LED driver
- 256-step linear dimming with four current range options
- 16 expansion GPIO ports, each individually configurable as an input or output
- Changes in the state of the input port can generate interrupt outputs (INTN)
- 400kHz fast I² C interface with 1.8V communication support
- Hardware reset support, 10 μs de-jittering of reset port
- ESD protection: ±4000V HBM (MIL-STD-883H)
  (Method 3015.8 standard)
- Latch-up : ±450mA (JEDEC STANDARD NO.78C SEPTEMBER 2010 standard)
- RoHS compliant, lead-free packaging
- Low standby current (<0.1μA)
- Operating voltage: 2.4V~5.5V
- Working temperature: -40℃~85℃
- Package Type: TQFN4X4-24L

## application

- mobile
- MP3/PMP
- GPS
- digital photo frame

## summary

The AW9523B is an I² C-interface, 16-way breather with expandable GPIO controllers for each channel.

After power-up, the 16 GPIO ports default to output mode, and their output defaults are configurable via the 2-bit device address. Each GPIO port can be individually configured as an input or output. Each channel can be configured as LED-driven mode or GPIO mode separately by command.

In LED mode, the 16 LEDs are common anode low dropout constant current drivers with 256 steps of linear dimming per channel. The AW9523B enhances the dropout performance of the low 6-way LED driver to provide 20mA of LED current with a current source dropout of only 60mV, making it more suitable for driving LCD backlights.

The AW9523B includes a one-bit interrupt output pin (INTN). When the GPIO is applied in input mode and its input state is changed, it can cause an interrupt output (INTN) is changed, thus submitting an interrupt request to the processor. Interrupts can be cleared when the GPIO input status is read through the I² C interface.

The AW9523B supports hardware reset (RSTN) and soft reset functions, with 10 μs anti-jitter handling built into the hardware reset pin. The AW9523B communicates with the processor via the fast I² C interface.

## Pinout and Identification Diagram

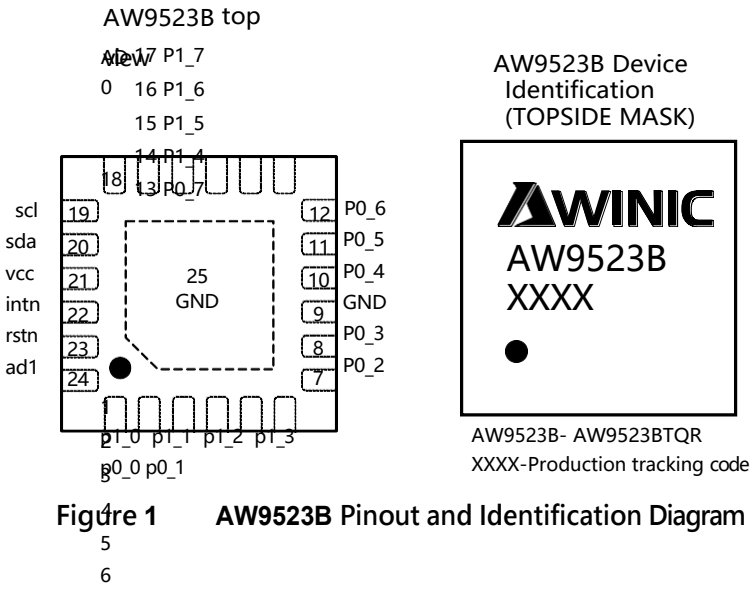
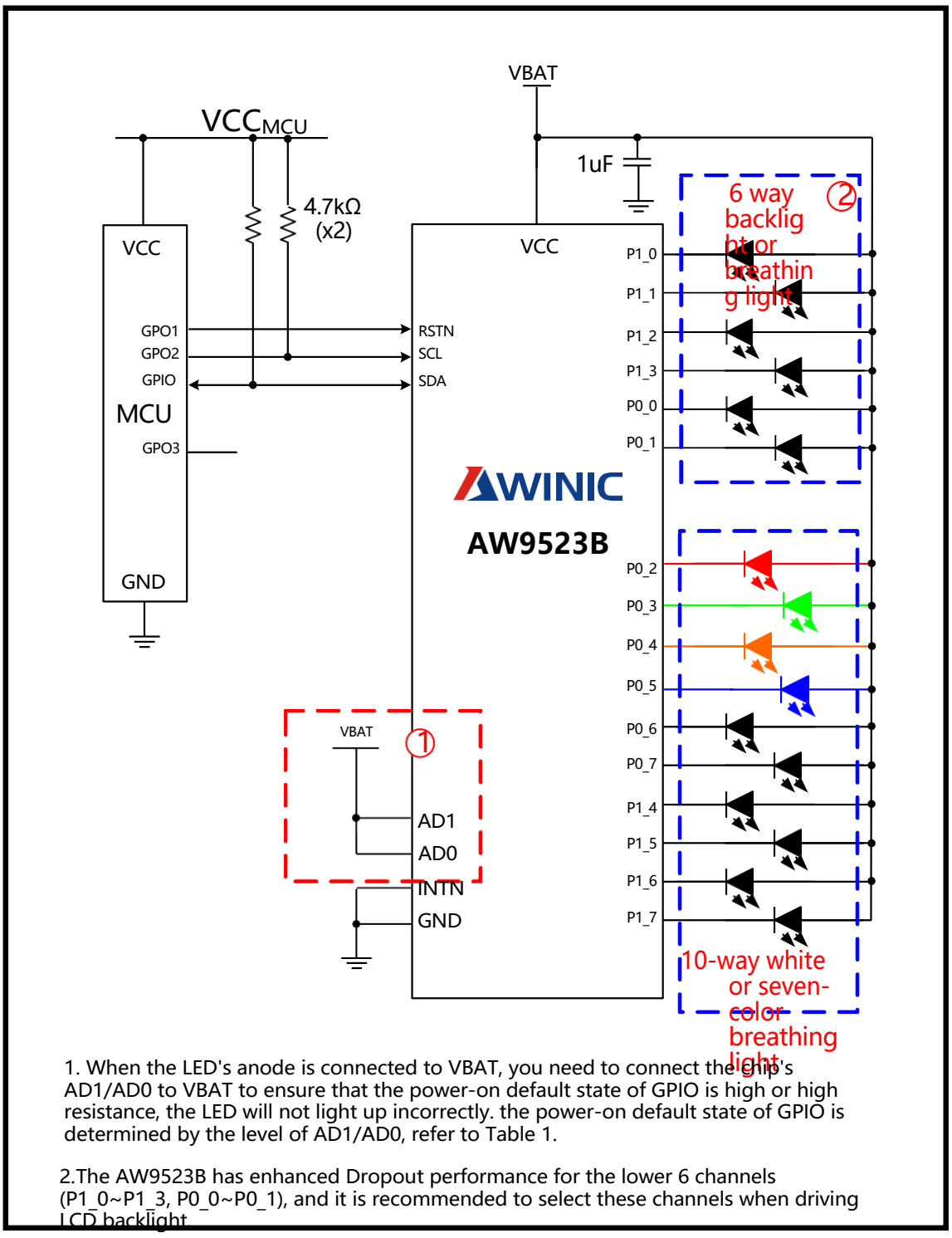



**Figure 1 AW9523B Pinout and Identification Diagram**

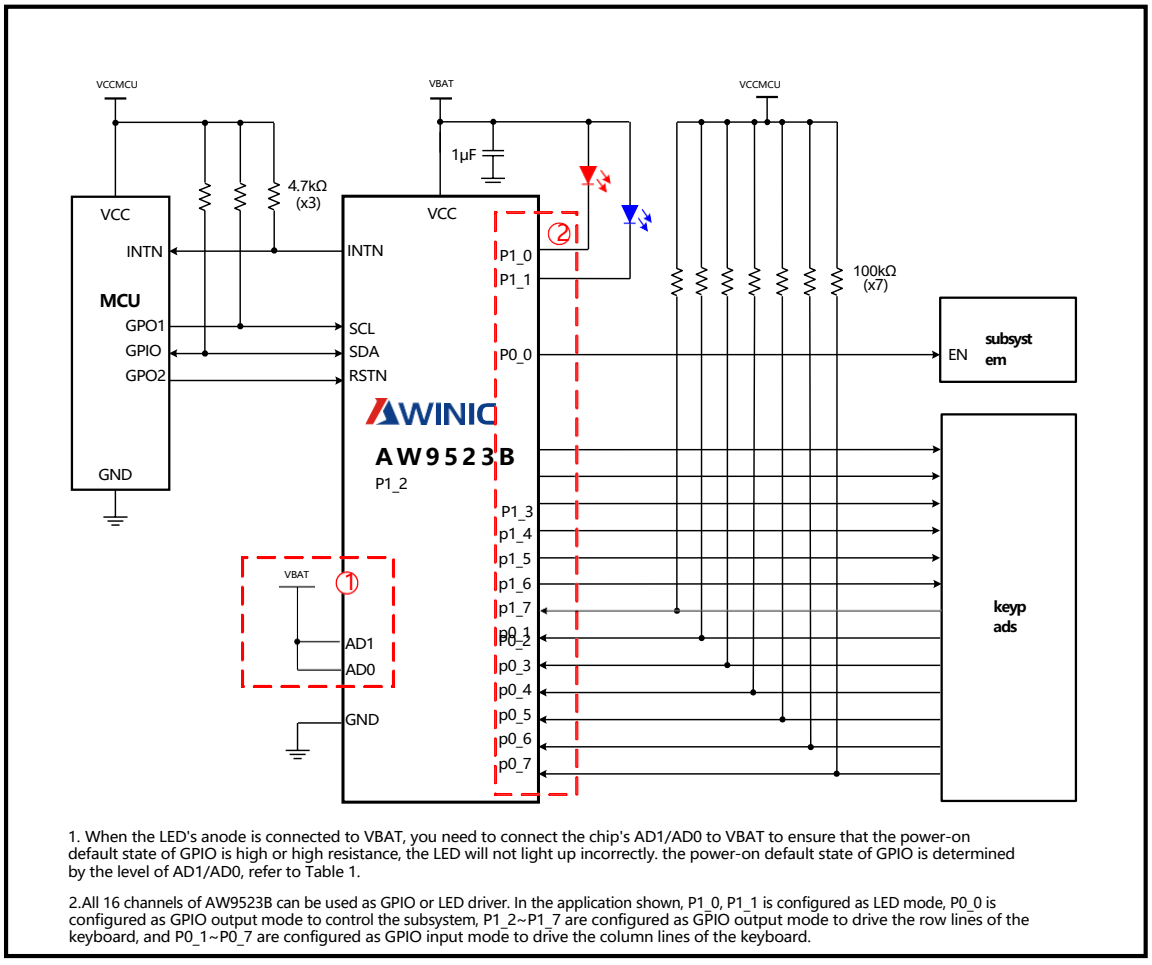
# Typical Application Diagram 1: Single chip for 16-way breathing light, of which 6 can be used as backlight




1. When the LED's anode is connected to VBAT, you need to connect the chip's AD1/AD0 to VBAT to ensure that the power-on default state of GPIO is high or high resistance, the LED will not light up incorrectly. the power-on default state of GPIO is determined by the level of AD1/AD0, refer to Table 1.

2.The AW9523B has enhanced Dropout performance for the lower 6 channels (P1_0~P1_3, P0_0~P0_1), and it is recommended to select these channels when driving LCD backlight.

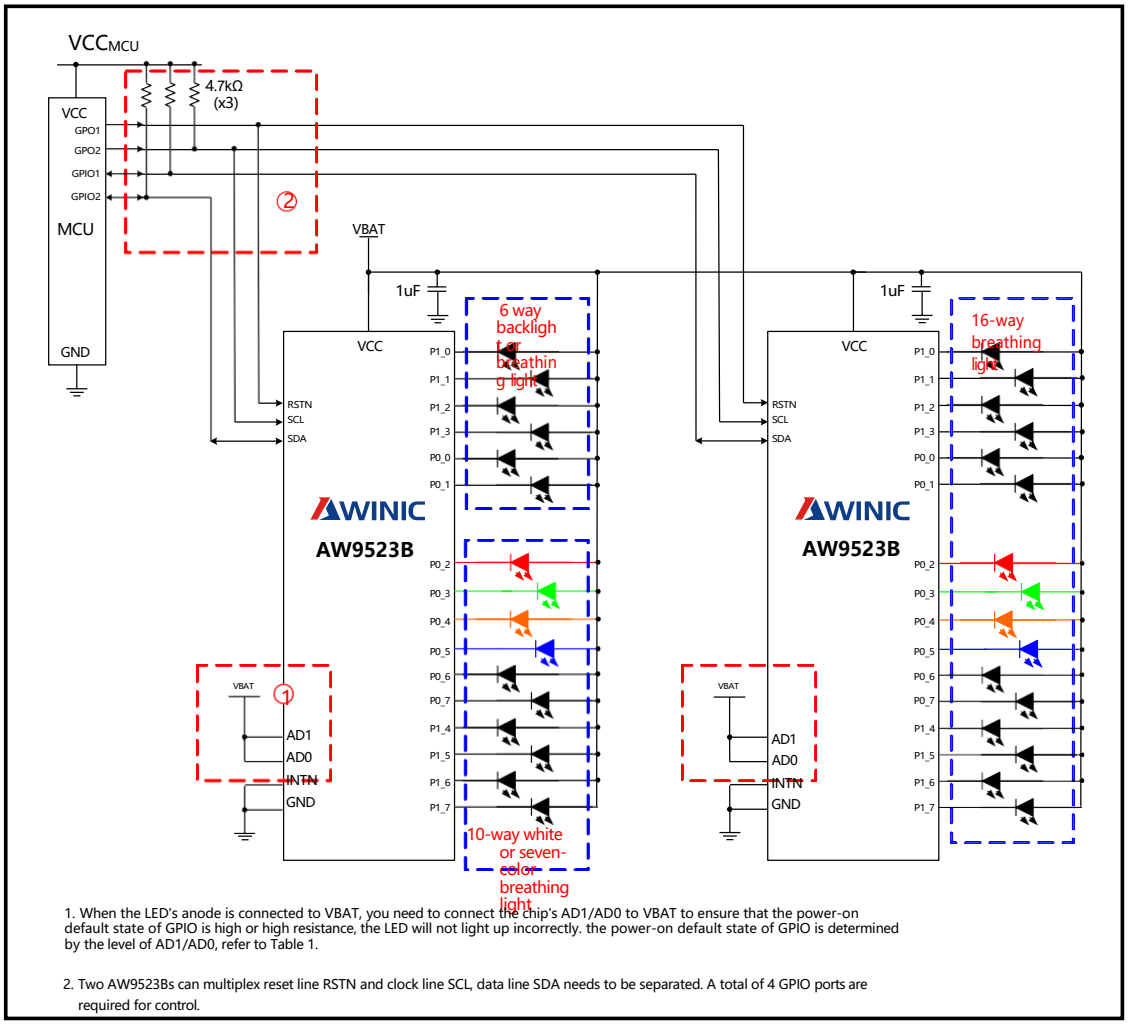
# Typical application diagram 2: single chip to achieve breathing light + keyboard extension




1. When the LED's anode is connected to VBAT, you need to connect the chip's AD1/AD0 to VBAT to ensure that the power-on default state of GPIO is high or high resistance, the LED will not light up incorrectly. the power-on default state of GPIO is determined by the level of AD1/AD0, refer to Table 1.

2.All 16 channels of AW9523B can be used as GPIO or LED driver. In the application shown, P1_0, P1_1 is configured as LED mode, P0_0 is configured as GPIO output mode to control the subsystem, P1_2~P1_7 are configured as GPIO output mode to drive the row lines of the keyboard, and P0_1~P0_7 are configured as GPIO input mode to drive the column lines of the keyboard.

# Typical Application Figure 3: Two Chips for 32-way Breathing Light

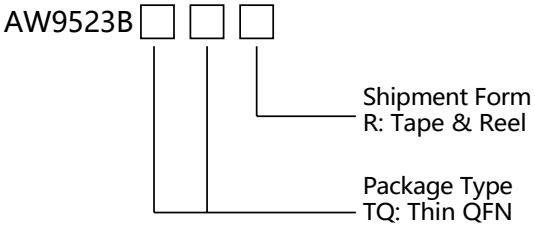



1. When the LED's anode is connected to VBAT, you need to connect the chip's AD1/AD0 to VBAT to ensure that the power-on default state of GPIO is high or high resistance, the LED will not light up incorrectly. the power-on default state of GPIO is determined by the level of AD1/AD0, refer to Table 1.

2. Two AW9523Bs can multiplex reset line RSTN and clock line SCL, data line SDA needs to be separated. A total of 4 GPIO ports are required for control.

# Ordering Information

| Product Model | Operating Temperature Range | Package form | Device Identification | Shipping Form |
|---|---|---|---|---|
| AW9523BTQR | -40℃～85℃ | TQFN4X4-24L | AW9523B | Tape and Reel Packaging 6000 tablets/tray |




# Absolute maximum rating (Note 1)

| parameters | coverage |
|---|---|
| Supply voltage VCC | -0.3 V to 6 V |
| SCL, SDA, AD0, AD1, INTN, RSTN, P0_0~P0_7, P1_0~P1_7 | -0.3V to VCC |
| Maximum power consumption (PDmax, package@ TA=25° C) | 3.2 W |
| Package thermal resistance $\theta_{JA}$ | 31°C/W |
| Maximum junction temperature $T_{Jmax}$ | 125° C |
| Storage temperature range | -65° C to 150° C |
| Pin Temperature (solder for 10 seconds) | 260° C |
| ESD Range (Note 2) | |
| HBM, all pins | ±4000V |
| Latch-up | |

| | |
|---|---|
| Test standard: JEDEC STANDARD NO.78C SEPTEMBER 2010 | +IT: +450mA<br>-IT: -450mA |

**Note 1:** If the operating conditions of the device exceed the above limits, permanent damage may be caused to the device. The above parameters are only the limit values of the operating conditions and it is not recommended to operate the device under conditions other than those recommended. The reliability and lifetime of the device may be affected if the device is operated under extreme operating conditions for a long time.

**Note 2:** HBM tests by discharging the charge stored on a 100pF capacitor through a 1.5 kΩ resistor against the pin. Test standard.
MIL-STD-883H Method 3015.8

# Electrical Characteristics

Test conditions: $T_A$ = 25° C, VCC = 3.8V (unless otherwise noted).

| parameters | | conditions | minimum | typical | largest | unit |
|---|---|---|---|---|---|---|
| **Supply voltage and current** | | | | | | |
| VCC | Input supply voltage | $T_A$ = -40° C~85° C | 2.4 | | 5.5 | V |
| VPOR | Power-on reset voltage | $T_A$ = -40° C~85° C | | 1.8 | 2.3 | V |
| ISTB | Shutdown current | RSTN = GND | | 0.1 | 2 | μA |
| **digital output** | | | | | | |
| VOH | Output high level (P0_7 to P0_0. (P1_7~P1_0) | VCC=2.5V, ISOURCE=10mA | VCC-170 | | | mV |
| | | VCC=3.6V, ISOURCE=20mA | VCC-250 | | | mV |
| | | VCC=5V, ISOURCE=20mA | VCC-200 | | | mV |
| VOL | Output low level (P0_7 to P0_0. (P1_7~P1_0) | VCC=2.5V, ISINK=20mA | | 90 | | mV |
| | | VCC=3.6V, ISINK=20mA | | 70 | | mV |
| | | VCC=5V, ISINK=20mA | | 60 | | mV |
| | Output low level (SDA, INTN) | VCC=2.5V, ISINK=6mA | | 150 | | mV |
| | | VCC=3.6V, ISINK=6mA | | 100 | | mV |
| | | VCC=5V, ISINK=6mA | | 75 | | mV |
| **Digital Inputs** | | | | | | |
| VIH | Logic High (SCL. SDA, RSTN, AD0. AD1, P0_7~P0_0, P1_7~P1_0) | | 1.4 | | | V |
| VIL | Logic Low (SCL. SDA, RSTN, AD0. AD1, P0_7~P0_0, P1_7~P1_0) | | | | 0.4 | V |
| IIH, IIL | Input Current (SCL, SDA. AD0, AD1. (P0_7~P0_0, P1_7~P1_0) | $V_I$ = VCC or GND | -0.2 | | +0.2 | μA |
| R_RSTN | Built-in pull-down resistor for RSTN pin | | | 100k | | Ω |
| CI | Input Capacitance (SCL, SDA. RSTN, AD0, AD1. (P0_7~P0_0, P1_7~P1_0) | $V_I$ = VCC or GND | | 3 | | pF |
| tSP_RSTN | Low burr pulse width that can be filtered by the RSTN pin | RSTN = VCC | | 10 | | μs |

| LED Driver | | | | |
|---|---|---|---|---|
| ILED | LED current size per circuit | ISEL<1:0>=0, DIMx=FFH | 37 | mA |
| Vdrop1 | Low 6 way (P1-0 to P1_3. (P0_0~P0_1) Output voltage drop | IOUT=21mA, ISEL<1:0>=01, DIMx=C0H | 60 | mV |

| | | | | |
|---|---|---|---|---|
| Vdrop2 | High 10-way (P0-2 to P0_7. (P1_4~P1_7) Output voltage drop | IOUT=21mA, ISEL<1:0>=01, DIMx=C0H | 80 | mV |

## I² C Interface Timing Parameters

| parameters | symbolic | minimum | typical | maximum | unit |
|---|---|---|---|---|---|
| SCL clock frequency | fSCL | | | 400 | kHz |
| (Repeat) Hold time of the start condition (time between the falling edge of SDA and the falling edge of SCL) | tHD:STA | 0.6 | | | μS |
| Low cycle of the SCL clock | tLOW | 1.3 | | | μS |
| High level period of the SCL clock | tHIGH | 0.6 | | | μS |
| Repeat start condition build time | tSU:STA | 0.6 | | | μS |
| Data retention time | tHD:DAT | 0 | | | μS |
| Data creation time | tSU:DAT | 0.1 | | | μS |
| Rise time of SDA and SCL signals | $t_R$ | | | 0.3 | μS |
| SDA and SCL signal fall times | $t_F$ | | | 0.3 | μS |
| Stop condition establishment time | tSU:STO | 0.6 | | | μS |
| Bus idle time between stop condition and start condition | tBUF | 1.3 | | | |
| Maximum width of noise (burr) that can be filtered at the input | tSP | 0 | 140 | 240 | nS |
| Load capacitance of the bus | $C_b$ | | | 400 | pF |

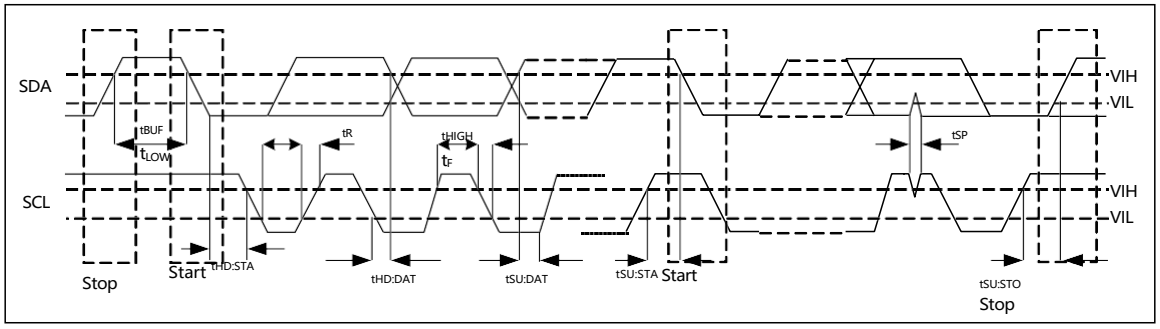



**Figure 2 I² C Interface Timing**

# Typical characteristic curves

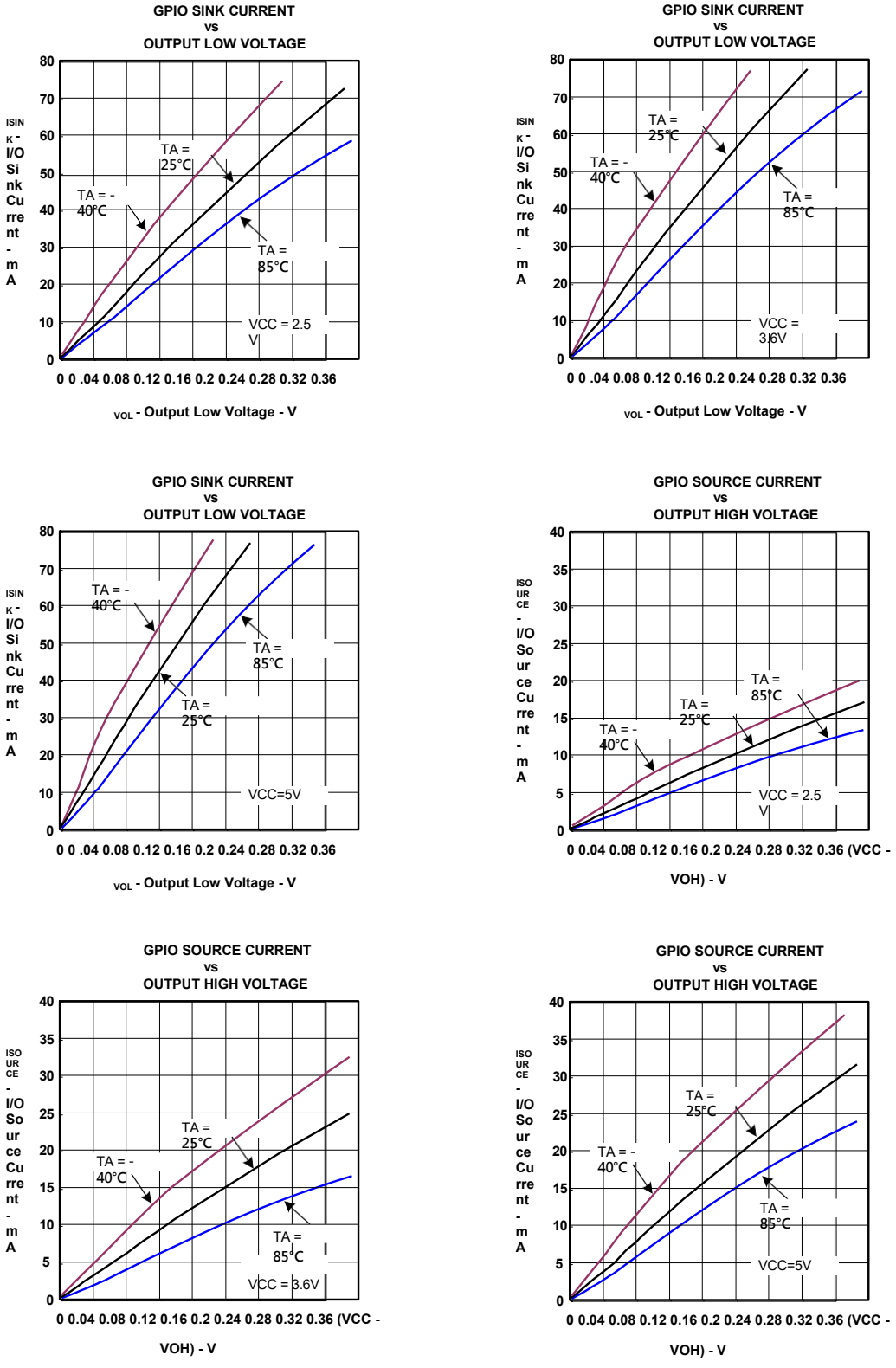



**Figure 3 Typical characteristic curve**

## Pin Description

| Pin Serial Number | Pin Name | description |
|---|---|---|
| 1 | P1_0 | Default is GPIO mode, input or output port, Push-Pull driven output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 2 | P1_1 | Default is GPIO mode, input or output port, Push-Pull driven output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 3 | P1_2 | Default is GPIO mode, input or output port, Push-Pull driven output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 4 | P1_3 | Default is GPIO mode, input or output port, Push-Pull driven output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 5 | P0_0 | GPIO input or output port, Open-Drain (default) or Push-Pull drive output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 6 | P0_1 | GPIO input or output port, Open-Drain (default) or Push-Pull drive output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 7 | P0_2 | GPIO input or output port, Open-Drain (default) or Push-Pull drive output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 8 | P0_3 | GPIO input or output port, Open-Drain (default) or Push-Pull drive output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 9 | GND | Ground pin. This pin must be connected directly to the ground level on the PCB. |
| 10 | P0_4 | GPIO input or output port, Open-Drain (default) or Push-Pull drive output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 11 | P0_5 | GPIO input or output port, Open-Drain (default) or Push-Pull drive output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 12 | P0_6 | GPIO input or output port, Open-Drain (default) or Push-Pull drive output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 13 | P0_7 | GPIO input or output port, Open-Drain (default) or Push-Pull drive output. Configurable to LED-driven mode. The power-up default state is related to the level of AD1\AD0 |
| 14 | P1_4 | GPIO input or output port, Push-Pull drive output. Configurable to LED drive mode. The power-up default state is the same as the The level of AD1/AD0 is related |
| 15 | P1_5 | GPIO input or output port, Push-Pull drive output. Configurable to LED drive mode. The power-up default state is the same as the The level of AD1/AD0 is related |
| 16 | P1_6 | GPIO input or output port, Push-Pull drive output. Configurable to LED drive mode. The power-up default state is the same as the The level of AD1/AD0 is related |
| 17 | P1_7 | GPIO input or output port, Push-Pull drive output. Configurable to LED drive mode. The power-up default state is the same as the The level of AD1/AD0 is related |
| 18 | AD0 | $I^2C$ Interface device address selection, connected to VBAT or GND, and controls the power-up default state of the output port, refer to Table 1. |
| 19 | SCL | $I^2C$ Interface Clock Bus |
| 20 | SDA | $I^2C$ Interface Data Bus |
| 21 | VCC | Power input pins |
| 22 | INTN | Interrupt output pin, open-drain output, external pull-up resistor required; |

## System Block Diagram

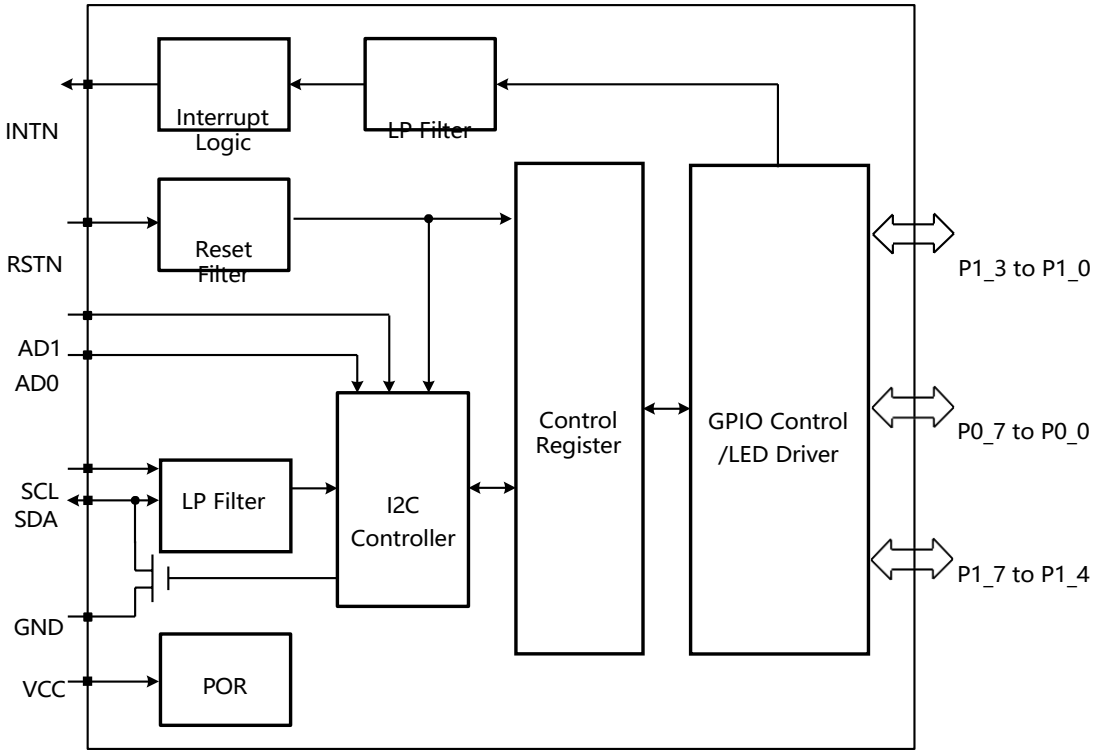



**Figure 4 AW9523B System Block Diagram**

## Function Description

The AW9523B is an $I^2C$ interface, 16-way breather and 16-way expansion GPIO controller that contains 16 bi-directional GPIO ports, each of which can be configured to LED drive mode by command. In GPIO mode, each GPIO can be individually configured as an input or output. In LED drive mode, the output ports are common-positive constant-current type control with 256 levels adjustable for each channel, while the global control bits ISEL[1:0] can select 4 different levels of maximum drive current $I_{MAX}$ .

## GPIO Output Driver

After power-on, the 16 GPIO ports are in GPIO mode by default and are in output state, and their output defaults can be configured by the 2-bit device address (AD1, AD0) as shown in Table 1. P1 port is Push-Pull driver; P0 port is Open-Drain driver by default and can be set to Push-Pull driver by configuring global control register. When P0 port is Open-Drain mode, external pull-up resistor is required.

Table *1.* Default logic for ***AW9523B*** output port after power-up, ***AD1/AD0*** vs. ***P0_x/P1_x***

| AD1 | AD0 | P1_7 | P1_6 | P1_5 | P1_4 | P1_3 | P1_2 | P1_1 | P1_0 | P0_7 | P0_6 | P0_5 | P0_4 | P0_3 | P0_2 | P0_1 | P0_0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | GND | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GND | VBAT | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| VBAT | GND | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | 0 | 0 | 0 | 0 |
| VBAT | VBAT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

## GPIO input and output direction selection

Config_Port0 and Config_Port 1 set the port as input and output state. Each bit of the register corresponds to a GPIO port, the position '1' represents the input state, set '0' represents the output state. The default value is 0 for the output state.

## GPIO Input Status

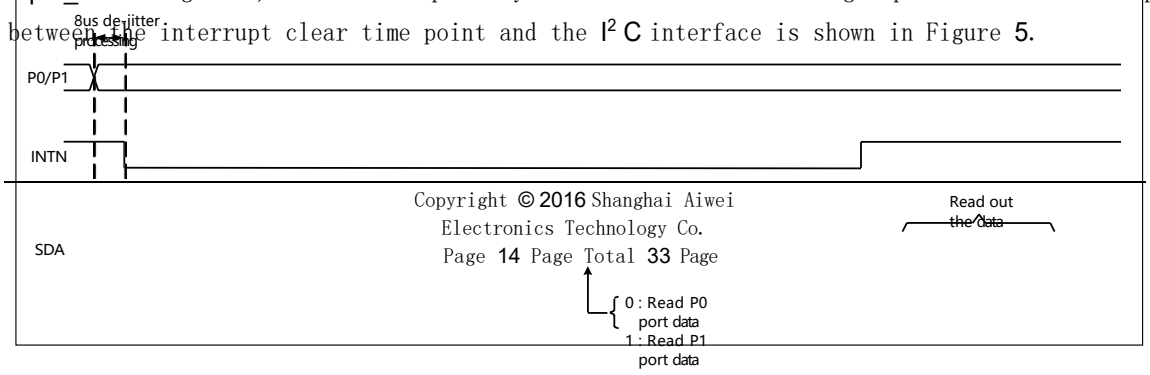
The current GPIO port logic state can be obtained by reading Input_Port0 and Input_Port1 through the I² C interface. AW9523B GPIO

The 1.8V logic input is supported by the port.

## Interrupt function

When the GPIO port is configured in input mode and the interrupt function is enabled, a change in its input state can cause a change in the interrupt output (INTN), which submits an interrupt request to the processor. Interrupts can be cleared when the GPIO input state is read through the I² C interface. By default, the 16 GPIO port interrupts are enabled. The AW9523B monitors the input state at all times, and when a change in the GPIO port logic level is detected, the internal circuitry first performs 8μs of de-jittering; if the change in state is confirmed after 8μs, the interrupt pin level is pulled low. The interrupt is generated whether the GPIO port level changes from low to high or from high to low. If a GPIO port is configured in output mode or its interrupt enable is turned off, the change in state will not generate an interrupt.

Interrupts can be cleared by reading the Input_Port0 and Input_Port1 registers so that the interrupt pin is pulled high by an external pull-up resistor. Interrupts generated by a change in the P0 port must be cleared by reading the Input_Port0 register; interrupts generated by a change in the P1 port must be cleared by reading the Input_Port1 register, and interrupts may not be cleared across groups. The relationship between the interrupt clear time point and the I² C interface is shown in Figure 5.



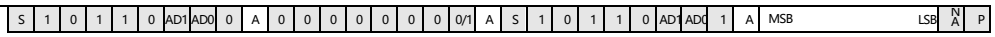


Figure 5 Interrupt generation and clearing interrupts

When a GPIO port state change generates an interrupt, changing its input or output state or turning off the interrupt enable for that IO port will not clear the interrupt; the interrupt cannot be cleared until it is read through the I² C interface, or cleared through the reset function.

## LED Driver

The AW9523B integrates a 16-way common-positive constant-current LED driver, and the P0 and P1 ports can be configured to LED drive mode by commanding the 12H and 13H registers. The chip's built-in resistor sets the maximum value of the drive current ($I_{MAX}$) to 37mA (typical). Meanwhile, setting ISEL[1:0] can limit the dimming range to 0~$I_{MAX}$, 0~($I_{MAX}$ ×3/4), 0~($I_{MAX}$ ×2/4) or 0~($I_{MAX}$ ×1/4), see Table 9 for ISEL[1:0] configuration.

Each LED can be linearly dimmable in 256 steps via the DIM register on the basis of a defined maximum drive current. DIMx (x=0~3) Word length 8bits, see Table 2 for specific dimming levels.

The AW9523B enhances the dropout performance of the low 6-way LED driver, requiring only 60mV of current source dropout to provide The 20mA LED current makes it more suitable for driving LCD backlighting. These are the recommended choices when driving LCD backlighting.

Table 2. 256 step dimming level configurations

| DIMx bit | | | | | | | | Corresponding dimming level |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1/255 x $I_{MAX}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2/255 x $I_{MAX}$ |
| ..... | | | | | | | | ..... |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 253/255 x $I_{MAX}$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254/255 x $I_{MAX}$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255/255 x $I_{MAX}$ |

## I² C Interface

The AW9523B communicates with the MCU via the I² C interface and supports two modes: standard mode (100 kHz), and fast mode

(The AW9523B is connected to the I² C network as a slave. SCL is a unidirectional input port; SDA is a bidirectional input/output port. When the SDA is an output, it is an open-drain output mode and requires an external pull-up resistor.

### Starting and stopping conditions

A switch from high to low on the SDA line while the SCL line is high indicates the start condition of the I²C interface. All transmissions start at the start condition or repeat the start condition.

A toggle from low to high on the SDA line while the SCL line is high indicates a stop condition for the I²C interface. All transmissions are terminated by a stop condition or a repeat start condition.

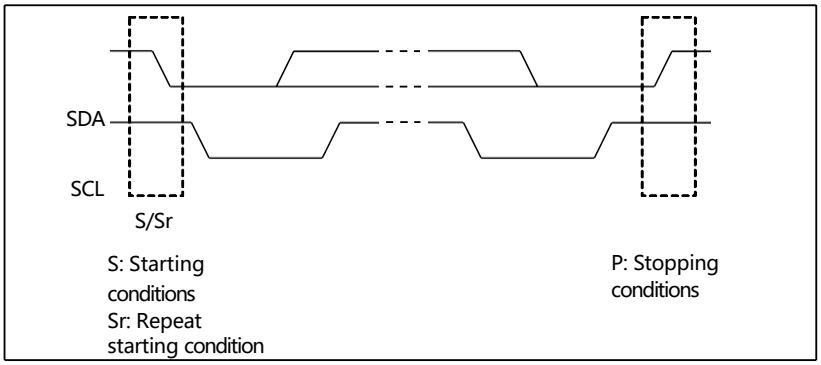



**Figure 6 Start and stop conditions**

### data transmission

After the start condition is generated, the I²C bus will send a slave address. After the AW9523B has recognized the start condition, it waits to receive the slave address. If the address sent on the SDA line is the same as a slave address, that slave device will pull the SDA line low in response (answer).

### Data validity

When the clock line (SCL) is high, the data on the SDA line must remain stable. Except for the start and stop conditions, the level on the SDA line must only change when SCL is low.

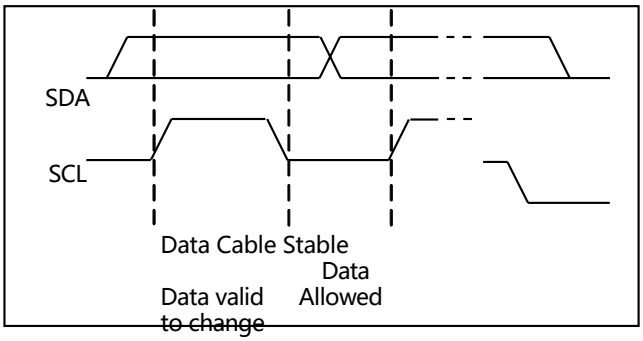



**Figure 7 Bit Transfer**

### respondent

The answer is used to indicate the successful transmission of data. After the sender (master) has sent 8bits of data, the SDA line must be released. The receiver (slave)

must pull the SDA line low during the answer clock pulse. The AW9523B generates an answer after every byte of data received.

In read mode, the slave AW9523B sends 8 bits of data first, then releases the SDA line and detects an answer on the SDA line. If an answer is detected and the host does not send a stop condition, the slave will continue to send data. If no answer is detected, the slave will stop sending data and wait for a stop condition.

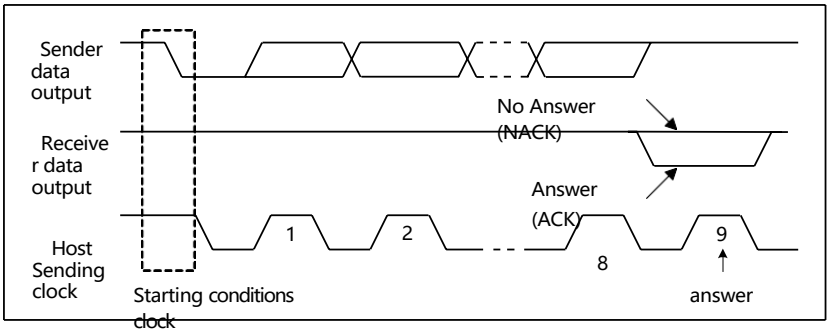



**Figure 8 I² C Interface Answer**

### address byte

The AW9523B provides 2 bits address pins AD1,AD0, which allows up to four AW9523B devices to be used simultaneously on one I² C bus. The 8-bit address consists of the 7-bit slave address plus a read/write judgment bit (R/W), which is transmitted first after the start condition. If the transmitted slave address matches the address of a device on the bus, the addressed receiver pulls the SDA line low (Answering).

The high five bits of the slave address are fixed to "10110". The sixth and seventh bits are AD1 and AD0 in that order, and their values are determined by the values of hardware pins AD1 and AD0. The eighth bit (LSB) is the read/write flag bit, which defines whether the next operation is a read or write operation. A '1' indicates a read and a '0' indicates a write.

| 1 | 0 | 1 | 1 | 0 | AD1 | AD0 | R/W |
|---|---|---|---|---|---|---|---|

(The values of AD1 and AD0 must not be the same as the values of the AD1 and AD0 pins)

**Figure 9 AW9523B Address Bytes**

### write operation

Figure 10 shows the timing diagram of the AW9523B write operation. The host sends the start condition first, followed by the 7-bit slave address plus a read/write bit '0'; when the sent slave address matches an AW9523B device address, the AW9523B answers; then the host sends the 8-bit AW9523B register address in the format of high significant bit (MSB) first and low significant bit (LSB) second; after the AW9523B answers, the host then sends the 8-bit register data, still MSB first and low significant bit (LSB) second; the AW9523B answers. first and the low significant bit (LSB) second; after the AW9523B answers, the host then sends the 8-bit register data, still MSB first and LSB second. Next, the AW9523B answers; the host sends a stop condition to end the transmission.

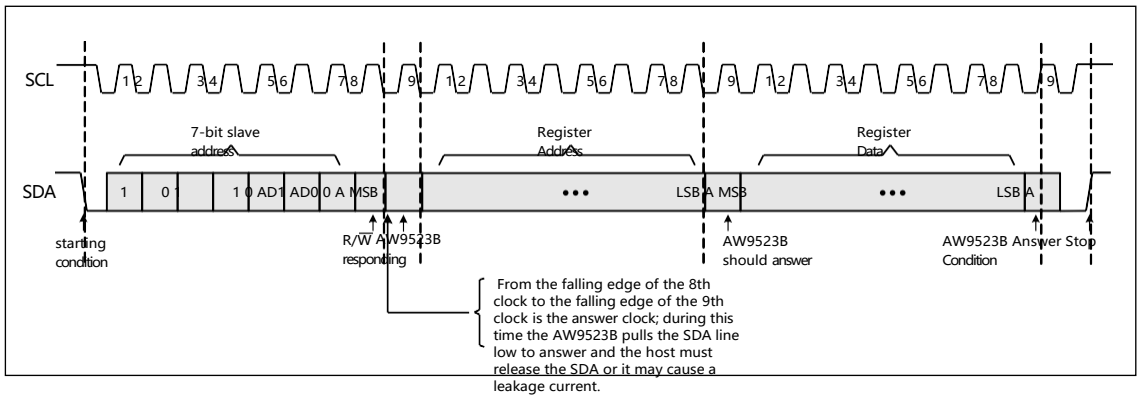



**Figure 10 AW9523B Write Operation**

### read operation

Figure 11 shows the timing diagram of the AW9523B read operation. The host sends the start condition first, followed by the 7-bit slave address plus a read/write bit '0'; when the slave address sent matches an AW9523B device address, the AW9523B answers; then the host sends the 8-bit AW9523B register address in the format of high significant bit (MSB) is sent first, followed by the low significant bit (LSB), and the AW9523B answers; then, the host sends the stop condition and repeats the start condition, followed by the 7-bit slave address plus a read/write bit '1', and the AW9523B answers; after answering, the AW9523B sends the 8-bit register data, which is still sent in the format MSB before, LSB after; at the next answer clock, the host does not answer, then the host sends a stop condition to end this transmission.

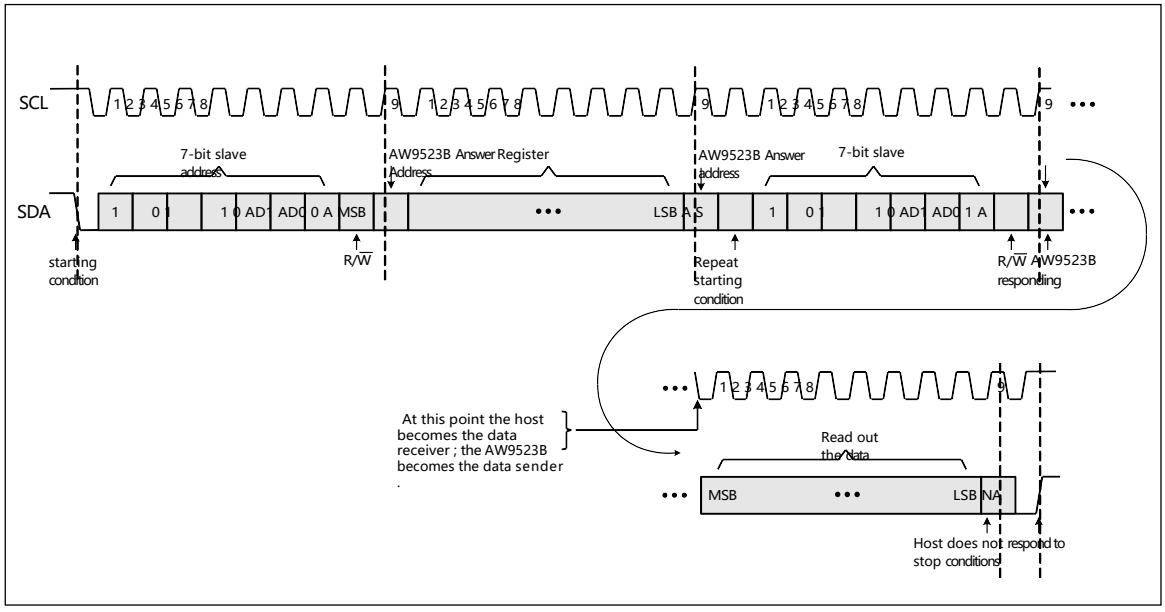



**Figure 11 AW9523B Read Operation**

## Reset function

The AW9523B supports three reset modes: power-on reset, hardware reset, and soft reset. All three reset modes can reset the registers to their default values.

### Hardware Reset

The hardware reset timings are shown in Figure 12.

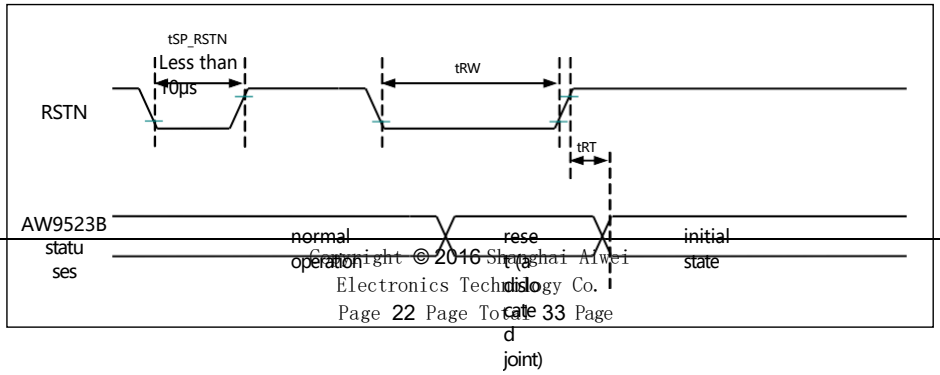


Figure 12 Hardware Reset Timing

Table 3. Hardware Reset Parameters Table

| parameters | | conditions | minimum | typical | largest | unit |
|---|---|---|---|---|---|---|
| $t_{RW}$ | Reset signal low pulse width | VSS = 0V, VCC = 2.4V~5.5V, T = -40° C~85° C | 20 | | | μs |
| $t_{RT}$ | Reset recovery time | | 1 | | | μs |

Notes.

1. The hardware reset pin (RSTN) has built-in anti-jitter circuitry. Spike pulses caused by electrostatic discharge (ESD) or other disturbances will not cause the system to reset. The reset relationships are listed in the following table.

| Reset pulse (RSTN) | AW9523B Operation |
|---|---|
| Less than 10μs (typical) | non-reset |
| Greater than 20μs | reset (a dislocated joint) |

2. After reset, the AW9523B is in its default state. At this time, all GPIO ports are configured as outputs, and their output values are determined by the 2-bit device addresses (AD1, AD0), refer to Table 1 for specific values; the interrupt state (INTN) is cleared and pulled high by an external pull-up resistor.

3. During the low level of the reset pulse, the anti-jitter circuit will also function and high pulses less than 10ns will be filtered out, as shown in Figure 13 As indicated.

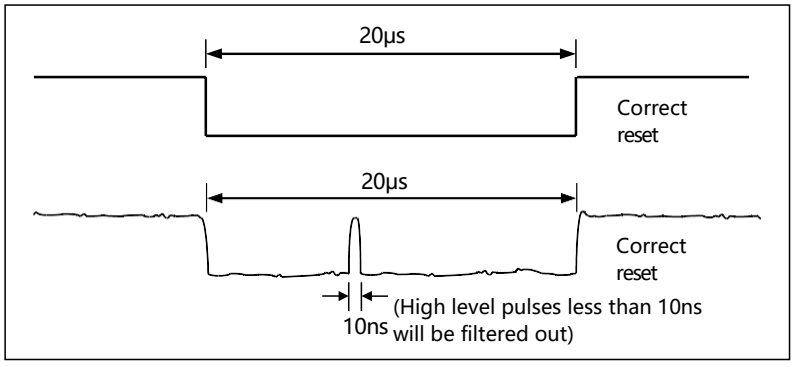



Figure 13 Anti-jitter handling during reset pulse low

## soft reset

The AW9523B also supports soft reset mode. Each time data 00H is written to the

soft reset register (7FH) via the I² C interface, a reset pulse is generated. After a soft reset, the AW9523B is in the default state, which is the same as a hardware reset. The soft reset timing is shown in Figure 14.

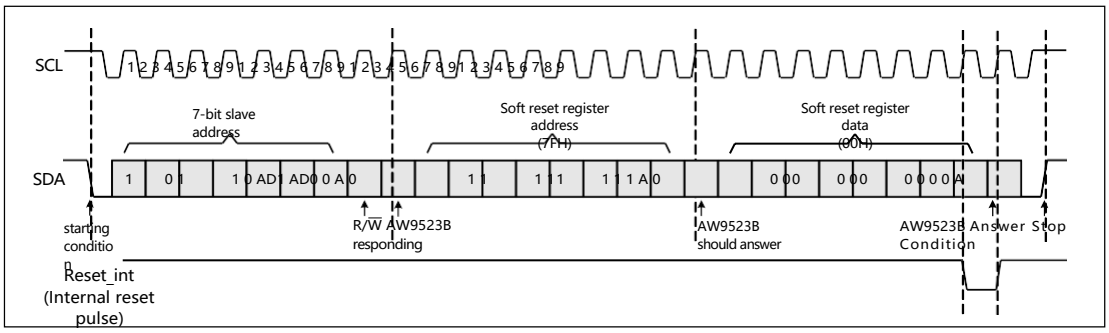



**Figure 14 Soft Reset Timing**

# Register List

Table *4: AW9523B* Register List

| Register Address | W/R | default value | functionalities | description |
|---|---|---|---|---|
| 00H | R | Equal to P0 port level | Input_Port0 | P0 port input status |
| 01H | R | Equal to P1 port level | Input_Port1 | P1 port input status |
| 02H | W/R | Refer to Table 1 | Output_Port0 | P0 port output status |
| 03H | W/R | Refer to Table 1 | Output_Port1 | P1 port output status |
| 04H | W/R | 00H | Config_Port0 | P0 port input or output configuration |
| 05H | W/R | 00H | Config_Port1 | P1 port input or output configuration |
| 06H | W/R | 00H | Int_Port0 | P0 port interrupt enable |
| 07H | W/R | 00H | Int_Port1 | P1 port interrupt enable |
| 10H | R | 23H | ID | ID register (read-only) |
| 11H | W/R | 00H | CTL | Global Control Register |
| 12H | W/R | FFH | LED Mode Switch | P0_7~P0_0 Operating mode switching |
| 13H | W/R | FFH | LED Mode Switch | P1_7~P1_0 Operating mode switching |
| 20H | W | 00H | DIM0 | P1_0 port LED current control |

| | | | | |
|---|---|---|---|---|
| 21H | W | 00H | DIM1 | P1_1 port LED current control |
| 22H | W | 00H | DIM2 | P1_2 port LED current control |
| 23H | W | 00H | DIM3 | P1_3 port LED current control |
| 24H | W | 00H | DIM4 | P0_0 port LED current control |

| | | | | |
|---|---|---|---|---|
| 25H | W | 00H | DIM5 | P0_1 port LED current control |
| 26H | W | 00H | DIM6 | P0_2 port LED current control |
| 27H | W | 00H | DIM7 | P0_3 port LED current control |
| 28H | W | 00H | DIM8 | P0_4 port LED current control |
| 29H | W | 00H | DIM9 | P0_5 port LED current control |
| 2AH | W | 00H | DIM10 | P0_6 port LED current control |
| 2BH | W | 00H | DIM11 | P0_7 port LED current control |
| 2CH | W | 00H | DIM12 | P1_4 port LED current control |
| 2DH | W | 00H | DIM13 | P1_5 port LED current control |
| 2EH | W | 00H | DIM14 | P1_6 port LED current control |
| 2FH | W | 00H | DIM15 | P1_7 port LED current control |
| 7FH | W | 00H | SW_RSTN | Software Reset Control |
| other than it | - | - | - | Reserved register, user does not operate |

# Detailed description of the registers

**Table *5.* Input Status Registers (*00H, 01H*)**

| address | name (of a thing) | description | default value |
|---|---|---|---|
| 00H | Input_Port0 | Current logic state of P0 port pin. 0-Low; 1-High | X |
| 01H | Input_Port1 | Current logic state of P1 port pin. 0-Low; 1-High | X |

The Input Status Register (00H, 01H) is used to reflect the current logic state of the GPIO port, regardless of whether the GPIO port is configured in input or output mode. This register supports read operations only; write operations are disabled. Its default value is determined by the external pin level.

Reading 00H through the I²C interface clears the interrupt caused by the P0 port; reading 01H clears the interrupt caused by P1

Interrupts caused by the port. The address of the register to be read must be written via the I²C interface before the read operation.

Bits 7 to 0 of register 00H correspond to the input status of P0_7 to P0_0, and bits 7 to 0 of register 01H correspond to the input status of P1_7 to P1_0, in that order.

**Table *6.* Output Status Registers (*02H, 03H*)**

| address | name (of a thing) | description | default value |
|---|---|---|---|
| 02H | Output_Port0 | Sets the P0 port pin output value. 0-Output low; 1-Output high | Refer to Table 1 |
| 03H | Output_Port1 | Set the P1 port pin output value. 0 - output low; 1 - output high | Refer to Table 1 |

The Output Status Register (02H, 03H) is used to set the output value of the GPIO port. For GPIO ports configured in input mode, the corresponding bit is invalid; similarly, reading the value of this register only reads the value of the register itself, not the status on the corresponding port.

Bits 7 to 0 of register 02H correspond to the output status of P0_7 to P0_0, and bits 7 to 0 of register 03H correspond to the output status of P1_7 to P1_0, in that order.

**Table *7.* configuration registers (*04H, 05H*)**

| address | name (of a thing) | description | default value |
|---|---|---|---|
| 04H | Config_Port0 | P0 port input/output mode selection. 0-output mode; 1-input mode | 00H |
| 05H | Config_Port1 | P1 port input/output mode selection. 0 - output mode; 1 - input mode | 00H |

The configuration registers (04H, 05H) are used to set the GPIO port to be in input mode or output mode. Each bit of the GPIO port can be individually configured as input or output mode. If a bit is set to 1, the corresponding port is configured as input mode; if a bit is set to 0, the corresponding port is configured as output mode.

Bits 7 to 0 of register 04H correspond to the configuration control of P0_7 to P0_0, and bits 7 to 0 of register 05H correspond to the configuration control of P1_7 to P1_0, in that order.

Table *8:* Interrupt Enable Registers (*06H*, *07H*)

| address | name (of a thing) | description | default value |
|---|---|---|---|
| 06H | Int_Port0 | P0 port interrupt enable. 0 - interrupt enable; 1 - interrupt not enable | 00H |
| 07H | Int_Port1 | P1 port interrupt enable. 0 - interrupt enable; 1 - interrupt not enable | 00H |

The interrupt enable registers (05H, 06H) are used to set the interrupt enable of the GPIO port. If a bit is set to 0, the interrupt function of the corresponding port will be enabled; if a bit is set to 1, the interrupt function of the corresponding port will be disabled.

Bits 7 to 0 of register 06H correspond to the interrupt enable of P0_7 to P0_0, and bits 7 to 0 of register 07H correspond to the interrupt enable of P1_7 to P1_0, in that order.

**Table *9. ID* registers (*10H*)**

| address | name (of a thing) | description | default value |
|---|---|---|---|
| 10H | ID | ID register, read-only, readout value 23H | 23H |

The ID register (10H) is a read-only register to read the device ID. the default value for the AW9523B ID read is 23H.

**Table *10.* Global Control Register (*11H*)**

| location | name (of a thing) | description | default value |
|---|---|---|---|
| D[7:5] | retain | - | - |
| D[4] | GPOMD | Set the P0 port drive mode. If D[4]=0, P0 port is Open-Drain mode; if D[4]=1, P0 port is Push-Pull mode. | 0 |
| D[3:2] | retain | - | - |
| D[1:0] | ISEL | 256 step dimming range selection<br>00:0~$I_{MAX}$<br>01: 0~($I_{MAX}$ × 3/4)<br>10:0~($I_{MAX}$ × 2/4)<br>11:0~($I_{MAX}$ × 1/4) | 00 |

D[4] is used to configure the P0 output mode as Open-Drain or Push-Pull. When the P0 port is used as an output, an external pull-up resistor is required if the open-drain mode is used; if the push-pull mode is used, no pull-up resistor is required.

D[1:0] is used to configure the maximum current of the LED driver. By default, the chip's built-in resistor sets the maximum current to 37mA (typical value), which can be further set to $I_{MAX}$ × 1/4, $I_{MAX}$ × 2/4, $I_{MAX}$ × 3/4, and $I_{MAX}$ via ISEL[1:0], so that the range of 256-step dimming is changed as well.

This register is configurable except D4, D[1:0], other bits (D[7:5], D[3:2]) are for test use and the default value is 0; if user needs to configure register 11H, its D[7:5], D[3:2] must be configured to 0, otherwise it may cause system function error.

**Table *11. LED* mode switching registers (*12H[7:0]*)**

| address | name (of a thing) | description | default value |
|---|---|---|---|
| 12H | LED Mode Switch | Configure P0_7~P0_0 as LED or GPIO mode.<br>1: GPIO Mode<br>0: LED mode | FFH |

LED mode switching register 12H[7:0] can configure P0_7~P0_0 ports as LED drive mode or GPIO mode respectively. After reset, the default is GPIO mode. If a bit of 12H[7:0] is configured to 0, the corresponding port is in LED mode, and if it is configured to 1, the corresponding port is in GPIO mode. Bits 7 to 0 of the register correspond to the mode control of P0_7~P0_0 in turn.

Table *12. LED* Mode Switching Register (*13H[7:0]*)

| address | name (of a thing) | description | default value |
|---|---|---|---|
| 13H | LED Mode Switch | Configure P1_7~P1_0 as LED or GPIO mode.<br>1: GPIO Mode<br>0: LED mode | FFH |

LED mode switching register 13H[3:0] can configure P1_7~P1_0 ports as LED drive mode or GPIO mode respectively. After reset, the default is GPIO mode. If a bit of 13H[7:0] is configured to 0, the corresponding port is in LED mode, and if it is configured to 1, the corresponding port is in GPIO mode. Bits 7 to 0 of the register correspond to the mode control of P1_7~P1_0 in turn.

**Table *13. 256* Step Dimmer Configuration Registers (*20H~2FH*)**

| address | name (of a thing) | description | default value |
|---|---|---|---|
| 20H | DIM0 | P1_0 port LED drive current configuration | 00H |
| 21H | DIM1 | P1_1 port LED drive current configuration | 00H |
| 22H | DIM2 | P1_2 port LED drive current configuration | 00H |
| 23H | DIM3 | P1_3 port LED drive current configuration | 00H |
| 24H | DIM4 | P0_0 port LED drive current configuration | 00H |
| 25H | DIM5 | P0_1 port LED drive current configuration | 00H |
| 26H | DIM6 | P0_2 port LED drive current configuration | 00H |
| 27H | DIM7 | P0_3 port LED drive current configuration | 00H |
| 28H | DIM8 | P0_4 port LED drive current configuration | 00H |
| 29H | DIM9 | P0_5 port LED drive current configuration | 00H |
| 2AH | DIM10 | P0_6 port LED drive current configuration | 00H |
| 2BH | DIM11 | P0_7 port LED drive current configuration | 00H |
| 2CH | DIM12 | P1_4 port LED drive current configuration | 00H |
| 2DH | DIM13 | P1_5 port LED drive current configuration | 00H |
| 2EH | DIM14 | P1_6 port LED drive current configuration | 00H |
| 2FH | DIM15 | P1_7 port LED drive current configuration | 00H |

The dimming configuration registers(20H~2FH) are used to configure the LED drive current of P0 and P1 ports. Each LED can support 256 Step dimming. Refer to Table 2 for the specific configuration.

**Table *13.* Soft Reset Register (*7FH*)**

| address | name (of a thing) | description | default value |
|---|---|---|---|
| 7FH | Software Reset | Write 00H to generate a reset pulse | X |

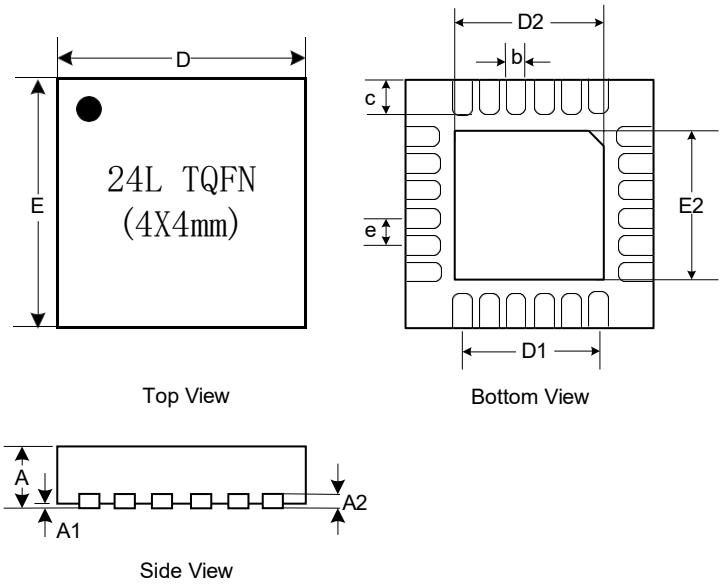
The Soft Reset Register (7FH) provides a soft reset function for the convenience of software debuggers. Each time 00H is written to this register, a reset pulse is generated. The soft reset timing is shown in Figure 14.

**Table *14.* Reserved Registers**

| address | description | default value |
|---|---|---|
| 08H~0FH<br>14H~1FH<br>30H~7EH<br>80H~FFH | Reserved register, test use or undefined | X |

The reserved registers (08H~10H, 14H~1FH, 30H~7EH, 80H~FFH) are for test use or undefined, and the user must not operate on them, otherwise a function error may be generated.

# Package Description




| Unit:mm | TQFN-24L | | |
|---|---|---|---|
| Symbol | Min | Typ | Max |
| A | 0.700 | 0.750 | 0.800 |
| A1 | 0.000 | | 0.050 |
| A2 | 0.203 (Ref.) | | |
| b | 0.200 | 0.250 | 0.300 |
| c | 0.350 | 0.400 | 0.450 |
| D | 3.950 | 4.000 | 4.050 |
| D1 | 2.500 (Ref.) | | |
| D2 | 2.650 | 2.700 | 2.750 |
| e | 0.500 (BSC) | | |
| E | 3.950 | 4.000 | 4.050 |
| E2 | 2.650 | 2.700 | 2.750 |