Computer Architecture (2024-2025) **Assignment** 2 December 2, 2024

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INSTRUCTIONS

1. Submission is only via Brightspace. Deadlines are strict.
2. The exercises in this assignment add up to 100 points. To calculate your grade simply divide the number of points by 10.
3. You must submit a pdf typeset in (La)TeX (no handwritten solutions) using **this** template.
4. Seeking solutions from the internet, from any external resource, or from any other person is prohibited.
5. Please note that the course lecturer reserves the right to ask the student submitting the assignment to explain the answers to any or all questions. If the student is unable to provide a satisfactory answer then that question may receive partial/no credit.
6. Of course, university policies on plagiarism always apply. In particular, any suspected plagiarism will be reported to the Board of Examiners.

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1. Design an FSM for a simple calculator that performs addition, subtraction, multiplication, and division based on user input. **(15 points)**

   The calculator has the following keys on its keypad:

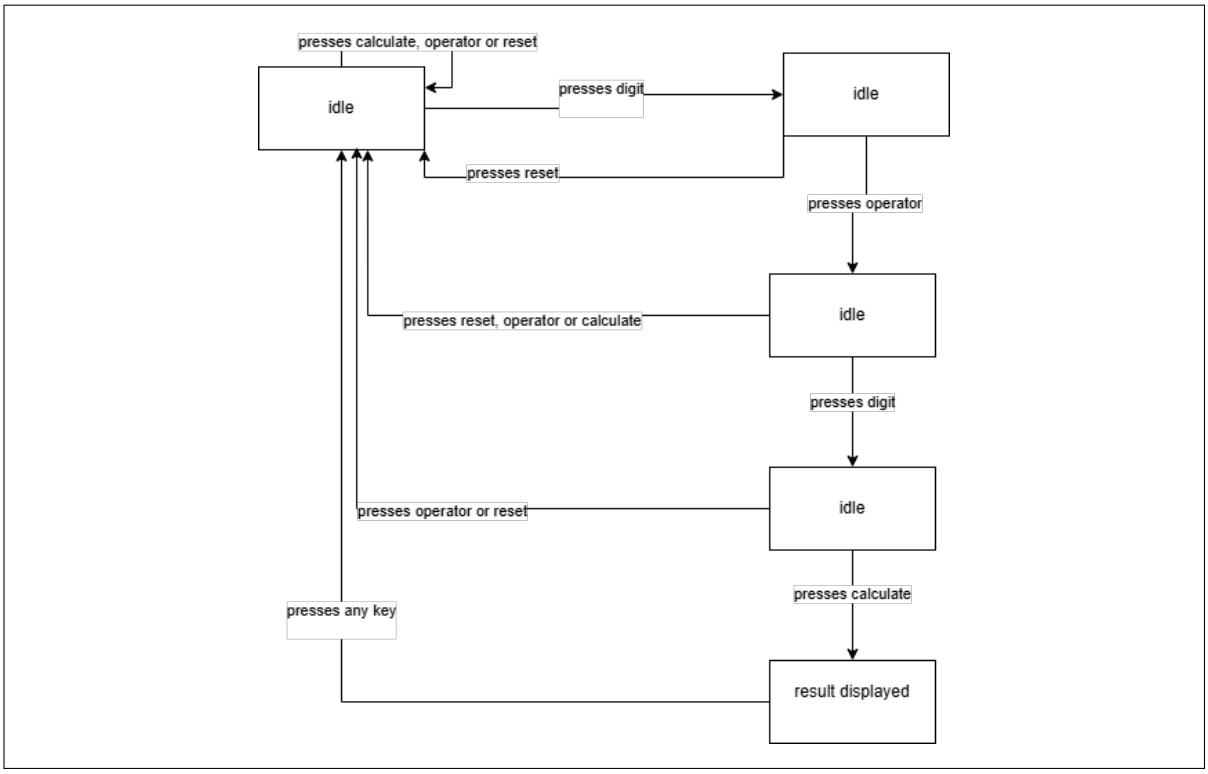
   - **Digits:** 0–9
   - **Operators:** +, -, *, /
   - **Calculate:** =
   - **Reset:** C

   The calculator starts in an *idle* state. The user enters the first number (any number of digits), followed by an operator, and then the second number. They press the *Calculate* key to display the result, after which any additional key press will return the calculator to the *idle* state. Pressing the *Reset* key takes the calculator to the *idle* state.

   Incorrect inputs: Any incorrect input takes the calculator to the *idle* state. Incorrect inputs include:

   - Pressing the *Calculate* button before entering the second number.
   - Entering an operator before the first number.
   - Entering multiple operators.

   Solution:

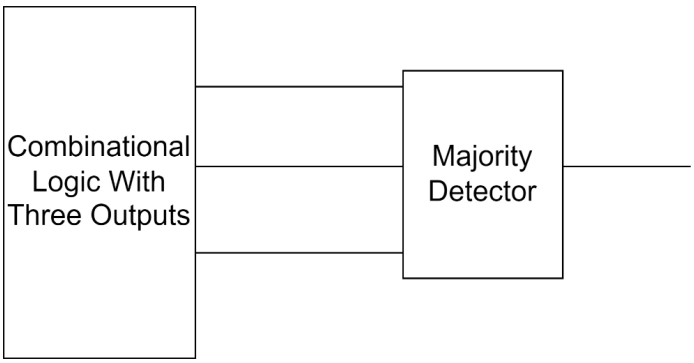


2. Assume a combinational logic circuit includes 3 inputs. Use logic gates to design a circuit to determine if the majority of the inputs are 1 or 0. **(10 points)**

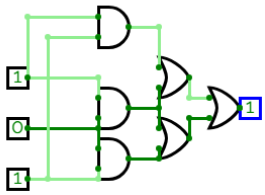
   Example:

   - **Majority 1:** 101, 110
   - **Majority 0:** 000, 001

   The following figure depicts the diagram of the circuit. The output from the majority detector is **1** if at least 2 of its inputs are 1, and **0** otherwise.



Solution:

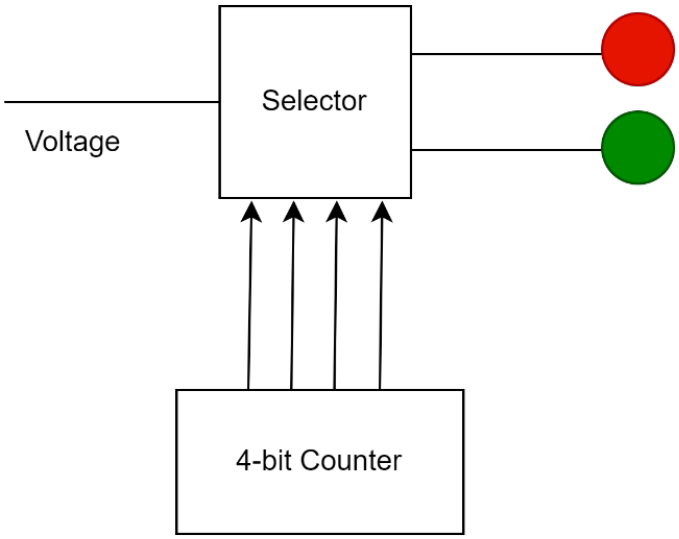


3. Assume that the traffic lights system is designed to include Red and Green lights. The lights are activated by the voltage input. The Selector component connects voltage input to one of the traffic lights based on the value of a counter. The 4-bit counter is used to determine which light should be active. **(15 points)**

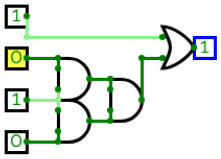
   The system includes a 4-bit counter that determines which light should be active:

   - If the value of the counter is less than or equal to 5, the **Red** light will turn on.
   - If the value of the counter is greater than 5, the **Green** light will turn on.

   Design Task: Design the circuit for the *Selector* component using logic gates. Assume the counter is provided. You only need to design the *Selector* box, as shown below.



Solution:



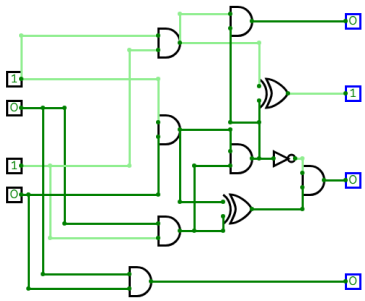
1 is green 0 is red

4. The addressability of the memory system of a computer is two bytes. You need 18 bits to access a location in memory. What is the total size of the memory in Bytes? **(10 points)**

Solution: $2^{18} = 262,144$

5. Design a circuit to multiply two 2-bit binary numbers. You may use logic gates or adders. **(15 points)**

Solution:



6. In the following shift register, select bits of the multiplexers determine the operation.

   The register can: **(10 points)**

   - Preserve the current value.
   - Shift left with serial input from the least significant bit.
   - Shift right with serial input from the most significant bit.
   - Accept parallel input.

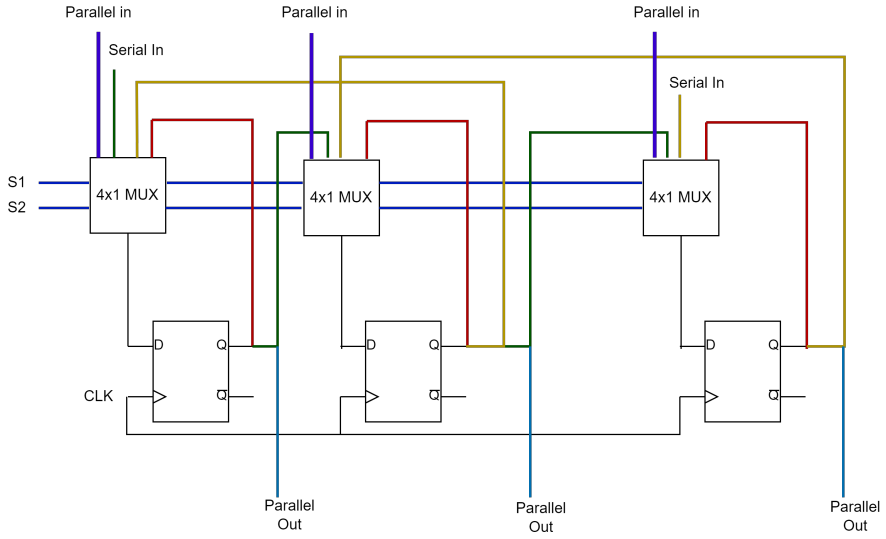
   Design Task: Modify the circuit to perform circular shifts instead of serial input shifts.

   - In a **left circular shift**, the most significant bit is placed at the least significant bit position.
   - In a **right circular shift**, the least significant bit is placed at the most significant bit position.

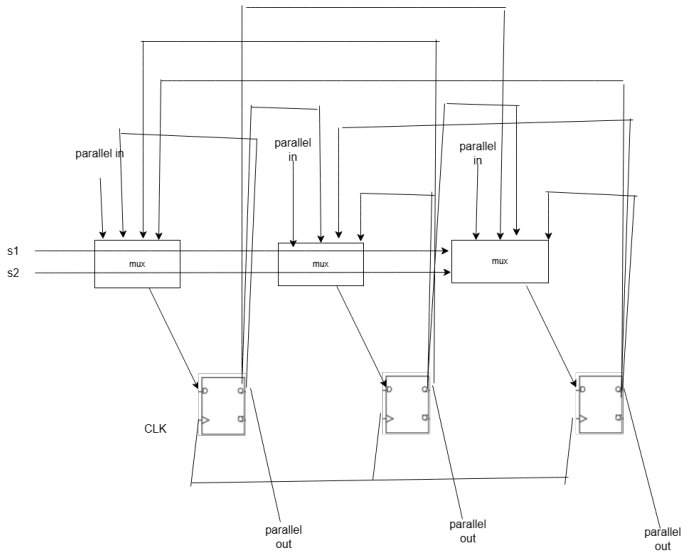
   Examples:

   - Current value: 0011

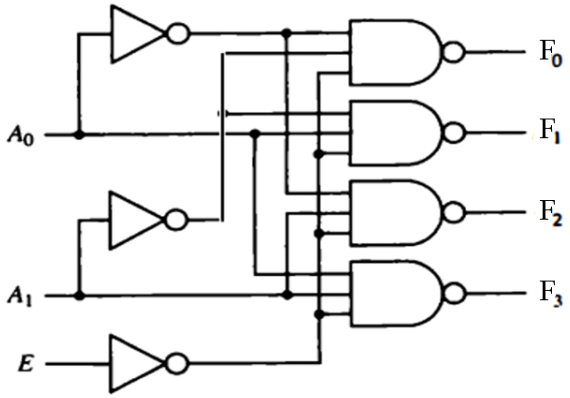
- After left circular shift: 0110
- After right circular shift: 1001



Solution:



7. The following figure depicts a combinational logic circuit of a 2-to-4 decoder (two inputs A_1 and A_0 and 2^2 outputs: F_3, F_2, F_1, F_0) with an enable input signal E. **(10 points)**



a) Fill all of the missing values in the following truth table and provide the steps you followed to obtain your answers. Please note that symbol X in the table can represent both 0 or 1 (the so-called "don't care").

Solution:

E	A_1	A_0	F_3	F_2	F_1	F_0
1	X	X	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

Case 1

- $E = 1$, $A_1 = X$, $A_0 = X$
- When $E = 1$, $\overline{E} = 0$, disabling all outputs.
- All $F_i = 1$ (don't care about A_1 and A_0).

Case 2

- $E = 0$, $A_1 = 0$, $A_0 = 0$
- $\overline{E} = 1$, circuit enabled.
- Decoder activates $F_0 = 0$, leaving $F_1, F_2, F_3 = 1$.

Case 3

- $E = 0$, $A_1 = 0$, $A_0 = 1$
- $\overline{E} = 1$, circuit enabled.
- Decoder activates $F_1 = 0$, leaving $F_0, F_2, F_3 = 1$.

Case 4

- $E = 0$, $A_1 = 1$, $A_0 = 0$
- $\overline{E} = 1$, circuit enabled.
- Decoder activates $F_2 = 0$, leaving $F_0, F_1, F_3 = 1$.

Case 5

- $E = 0$, $A_1 = 1$, $A_0 = 1$
- $\overline{E} = 1$, circuit enabled.
- Decoder activates $F_3 = 0$, leaving $F_0, F_1, F_2 = 1$.

b) How many 2-to-4 decoders are needed to design a 4-to-16 decoder? Explain your answer.

Solution: 5 decoders: 1 main 2-to-4 decoder which will enable the first 2 bits of the input, and 4 2-to-4 decoders which each will connect to each output of the first decoder and they will respresent the remaining 2 bits.

8. Design a logic unit capable of performing **AND**, **OR**, **XOR**, **NAND**, **NOR**, and **XNOR** operations on two 1-bit inputs.

   Use a 4x1 multiplexer to select the desired operation and a 3x8 decoder to generate control signals. **(15 points)**

   The desired operation is given as a 3-bit value, as shown below:

Operation	Code
AND	000
OR	001
XOR	010
NAND	011
NOR	100
XNOR	101

Solution: