Summary - ZCU111 Platform

This is a preliminary release of this document

Name	zcu111
Worker Type	Platform
Latest Supported OpenCPI Version	release_1.4_zynq_ultra custom version
Supported Vendor Toolset/Version	Vivado 2018.2 + SDK
Component Library	com.geontech.bsp.zcu1xx
Workers	zcu111

Revision History

Revision	Description of Change	Date
release_1.4_zynq_ultra (Geontech custom release)	Initial Release of Zynq UltraScale+ Support in branch off of OpenCPI's release_1.4	1/2019

1 Block Diagrams

1.1 Top level

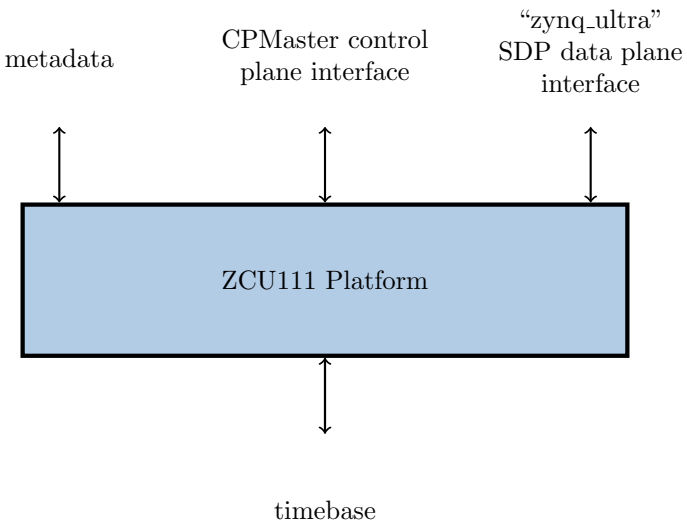

Table of Contents

List of Figures

List of Tables

2 Functionality

The zcu111 platform worker exposes the OpenCPI control plane, data plane, and timebase interface on the Xilinx Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit [4]. The control and data planes interface with the zeroth Zynq UltrsaScale+ High-performance AXI4 interface port (HP0). The worker uses the zeroth Zynq PS FCLK clock as the control plane, data plane, and timebase port clocks.

3 Worker Implementation Details

The zcu111 platform worker instantiates version 3.2 of the Xilinx Zynq UltraScale+ Processing System LogiCORE IP core [3].

> IMPORTANT: This worker's references to AXI GP refer to the GP ports of the generated IP core. The UltraScale+ Device Technical Reference Manual (TRM) refers to the IP core's GP ports as High Performance (HP) ports. Note that the useGP1 property is disabled for this worker because software does not yet recognize this property change for the ZynqMP.

4 Source Dependencies

- bsp_zcu111/hdl/platforms/zcu111/zcu111.vhd
- bsp_zcu111/hdl/primitives/zynq_ultra/vivado_zynq_ultra/zynq_ultra_ps_e_0.vhd
- bsp_zcu111/hdl/primitives/zynq_ultra/vivado_zynq_ultra/zynq_ultra_ps_e_v3_2_1.v
- bsp_zcu111/hdl/primitives/zynq_ultra/vivado_zynq_ultra/zynq_ultra_ps_e_pkg.vhd
- bsp_zcu111/hdl/primitives/zynq_ultra/zynq_ultra_pkg.vhd
- bsp_zcu111/hdl/primitives/zynq_ultra/zynq_ultra_ps_e.vhd
- opencpi/projects/core/hdl/primitives/bsv/bsv_pkg.vhd
- opencpi/projects/core/hdl/primitives/bsv/imports/SyncResetA.v
- opencpi/projects/core/hdl/primitives/axi/axi2cp.vhd
- opencpi/projects/core/hdl/primitives/axi/axi_pkg.vhd
- opencpi/projects/core/hdl/primitives/axi/m_axi_gp2hp.vhd
- opencpi/projects/core/hdl/primitives/sdp/sdp2axi_rd.vhd
- opencpi/projects/core/hdl/primitives/sdp/sdp2axi_wd.vhd
- opencpi/projects/core/hdl/primitives/sdp/sdp_body.vhd
- opencpi/projects/core/hdl/primitives/sdp/sdp_pkg.vhd
- opencpi/projects/core/hdl/primitives/sdp/sdp2axi.vhd
- opencpi/projects/core/hdl/primitives/sdp/sdp2axi_addr36_ent.vhd
- opencpi/projects/core/hdl/primitives/sdp/sdp_axi_addr36_pkg.vhd

5 Worker Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
platform	String	31	-	Parameter	Standard	zcu111	Name of this platform
sdp_width	UChar	-	-	Parameter	Standard	1	Width of data plane in DWORDS
UUID	ULong	-	16	Readable	Standard	-	UUID of this platform
oldtime	ULongLong	-	-	Padding	Standard	-	N/A
romAddr	UShort	-	-	Writable	Standard	-	
romData	ULong	-	-	Volatile	Standard	-	
nSwitches	ULong	-	-	Readable	Standard	-	Number of switches
nLEDs	ULong	-	-	Readable	Standard	-	Number of LEDs
memories_length	ULong	-	-	Readable	Standard	-	
memories	ULong	-	4	Readable	Standard	-	The memory regions that may be used by various other elements, which indicates aliasing etc. The values describing each region are: Bit 31:28 - External bus/BAR connected to this memory (0 is none) Bit 27:14 - Offset in bus/BAR of this memory (4KB units) Bit 13:0 - Size of this memory (4KB units) units)
dna	ULongLong	-	-	Readable	Standard	-	DNA (unique chip serial number) of this platform
switches	ULong	-	-	Volatile	Standard	-	Current value of any switches in the platform
led	ULong	-	-	Writable, Readable	Standard	-	Setting of LEDs in the platform, with readback. A value of true illuminates the given LED. The indices and their corresponding LEDs are index 12: LED DS17, 11: DS18, 10: DS20, 9: DS19, 8: DS16, 7: unused, 6: DS22, 5: DS15, 4: DS13, 3: DS10, 2: DS9, 1: DS11, 0: unused. For example, writing a value of 0x1002 will illuminate only LEDs DS17 and DS11.
nSlots	ULong	-	-	Parameter	Standard	0	Number of slots available for cards, which indicates the usable length of the slotCardIsPresent array property.
slotNames	String	32	-	Parameter	Standard	""	A string which is intended to include comma-separated names of the slots available for cards. The inter-comma position of each name corresponds to the same index of the slotCardIsPresent array property.
slotCardIsPresent	Bool	-	64	Volatile	Standard	-	An array of booleans, where each index contains an indication whether a card is physically present in the given index's slot. For a description of a given index's slot, see the corresponding comma-separated string contents in the slotName property. Note that only the first min(nSlots,64) of the 64 indices contain pertinent information.
axi_error	Bool	-	4	Volatile	Standard	-	-
sdpDropCount	UChar	-	-	Volatile	Standard	-	-
debug_state	ULongLong	-	4	Volatile	Standard	-	-
debug_state1	ULongLong	-	4	Volatile	Standard	-	-
debug_state2	ULongLong	-	4	Volatile	Standard	-	-

6 Worker Ports

No ports are included in the component specification.

7 Worker Interfaces

Type	Name	Master	Count	Usage
metadata	-	true	-	Access to container metadata via the platform worker. All platform workers must provide this port.
timebase	-	true	-	Providing a timebase for the time service. All platform workers must provide this port.
cpmaster	-	true	-	This platform worker provides a control plane.
sdp	`zynq_ultra`	true	4	-

8 Platform Devices

The following is a table which enumerates which device workers are allowed in platform configurations and in assembly containers. The parameter values specified restrict allowed implementations. Note that the worker signals listed are only those who are unconnected on the platform or whose platform signal name differ from the worker signal name. Note that device workers allowed by cards are not included in this list.

Name	Property Name	Property Value	Worker Signal	Platform Signal
time_server	frequency	$100*10^6$		

9 Signals

Note that this signal table does not include signals that may be provided by slots.

Name	Type	Differential	Width	Description
led	Output	false	8	-

10 Slots

Note that slots exist on the ZCU111 board but that have not yet been interfaced with the platform worker.

11 Platform Configurations

Name	Platform Configuration Workers	Card	Slot
base	zcu111	-	-
	time_server	-	-

12 Control Timing and Signals

13 Performance and Resource Utilization

14 Troubleshooting

The UltraScale+ AXI HP registers [1] can be inspected by running the following command on the ZCU111.

```
ocpizynq axi_hp
```

15 Test and Verification

All of the application worker unit tests in the core and assets projects have been run succesfully on the ZCU111 platform. This effectively tests both the control and data planes in various scenarios.

References

[1] Zynq UltraScale+ MPSoC Register Reference
https://www.xilinx.com/html_docs/registers/ug1087/ug1087-zynq-ultrascale-registers.html

[2] Zynq UltraScale+ Device Technical Reference Manual
https://www.xilinx.com/support/documentation/user_guides/ug1085-zynq-ultrascale-trm.pdf

[3] Zynq UltraScale+ MPSoC Processing System v3.2 Product Guide (PG201)
https://www.xilinx.com/support/documentation/ip_documentation/zynq_ultra_ps_e/v3_2/pg201-zynq-ultrascale-plus-processing-system.pdf

[4] Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit
https://www.xilinx.com/products/boards-and-kits/zcu111.html