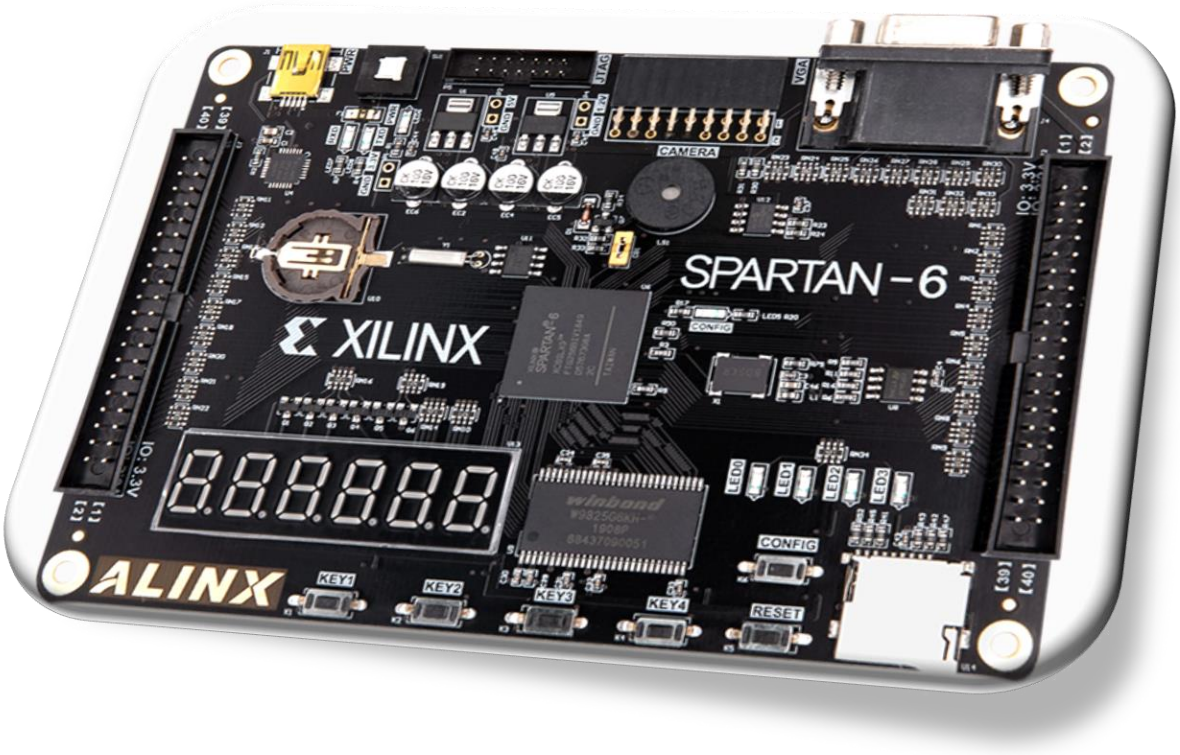
Spartan6 - DSP48A1-Project

Digital Designer: George Safwat Wasfy

Presented for:

Digital Design Using Verilog &FPGA Flow Using VIVADO Diploma

Under supervision of: Eng. Kareem Waseem



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1-RTL code

First: Instantiation Modules

```
module Mux_Reg(in,clk,out,rst,CE,sel);
parameter input_size=18,RSTTYPE="SYNC";
input [input_size-1:0]in;
input clk,rst,CE,sel;
output [input_size-1:0] out;
reg [input_size-1:0]regs;

assign out= (sel==1)?  regs:in;

generate
    if(RSTTYPE=="SYNC")begin
always @(posedge clk) begin
     if(rst)
regs<=0;
else begin
    if(CE)
regs<=in;
end
end
    end
else begin
if(RSTTYPE=="ASYNC")begin
always @(posedge clk or posedge rst) begin
    if(rst)
regs<=0;
else begin
    if(CE)
regs<=in;
end
    end
end
end

endgenerate
endmodule
```

```
module Muxb(in0,in1,b0);
parameter sel="Direct";
input [17:0]in0;
input [17:0]in1;
output [17:0]b0;                        //Input B
assign b0= (sel=="Direct")?  in0:(sel=="CASCADE")? in1:0;
endmodule


module mux2(sel,in0,in1,out);
input [17:0] in0,in1;  //in0=pre   in1=b0_out
input sel;
output [17:0] out;              //opmode[4]
assign out=(sel==0)? in1:in0;
endmodule

module mux_cin(in0,in1,out);
parameter sel="OPMODE5";
input in0,in1;
output out;             //opmode[5]
assign out=(sel=="OPMODE5")? in0:in1;
endmodule

module mux4(in0,in1,in2,in3,out,sel);
input [47:0]in0,in1,in2;
input [1:0]sel;      //for Mux Z
output [47:0]out;
input in3;
assign out=(sel==0)? in3:(sel==1)? in2:(sel==2)? in1:in0;
endmodule
```

```
module mux4_x(in0,in1,in2,in3,out,sel);
input [47:0]in0,in1;
input [35:0]in2;
input [1:0]sel;                 //for Mux X
output [47:0]out;
input in3;
assign out=(sel==0)? in3:(sel==1)? in2:(sel==2)? in1:in0;
endmodule
```

Second: Spartan6 - DSP48A1-Design

Inputs, Outputs &Parameters:

```
module  DSP(A,B,C,D,CARRYIN,M,P,CARRYOUT,
CARRYOUTF,clk,opmode,cea,ceb,cec,cecarryin,
ced,cem,ceopmode,cep,rsta,rstb,rstc,rstcarryin,
rstd,rstm,rstopmode,rstp,BCOUT,PCIN,PCOUT,BCIN);
parameter A0REG=0,B0REG=0,A1REG=1,B1REG=1,CREG=1, DREG=1, MREG=1,
PREG=1, CARRYINREG=1,CARRYOUTREG=1,OPMODEREG=1,
CARRYINSEL="OPMODE5",B_INPUT="DIRECT",RSTTYPE="SYNC";


input CARRYIN,clk,cea,ceb,cec,cecarryin,
ced,cem,ceopmode,cep,rsta,rstb,rstc,rstcarryin,
rstd,rstm,rstopmode,rstp;
input [7:0]opmode;
input [17:0]A,B,D,BCIN;
input [47:0]C,PCIN;
output [47:0]P,PCOUT;
output [35:0]M;
output reg CARRYOUT;
output CARRYOUTF;
output [17:0]BCOUT;
```

```
wire [17:0]a,a1_out,d,b0,b0_out,b1,b1_out;
reg [17:0]pre_add_sub;
reg [48:0]post_add_sub;
wire [35:0]M_out;
reg [35:0]M_in;
wire [47:0]c,z,x;
wire [7:0]opmode_out;
wire cyi,cyi_out,cyo_out;
```

Blue signals are Internal Wires.

Red signals are Internal Registers.

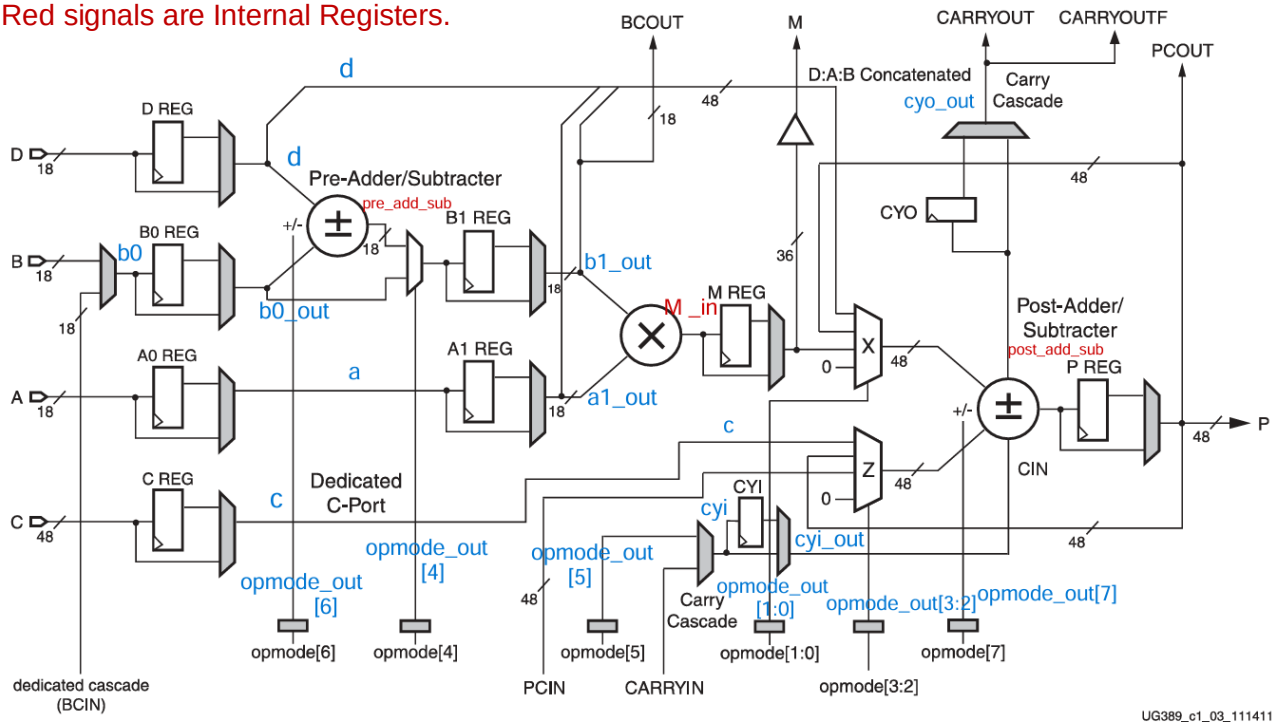


Figure 1-3: **DSP48A1 Slice**

Instantiations

```
//Input A
Mux_Reg a0(.in(A),.clk(clk),.out(a),.rst(rsta),.CE(cea),.sel(A0REG));
Mux_Reg a1(.in(a),.clk(clk),.out(a1_out),.rst(rsta),.CE(cea),.sel(A1REG));
//Input B
Muxb B_in(.in0(B),.b0(b0),.in1(BCIN));
Mux_Reg B0(.in(b0),.clk(clk),.out(b0_out),.rst(rstb),.CE(ceb),.sel(B0REG));
mux2 b_in(.sel(opmode_out[4]),.in0(pre_add_sub),.in1(b0_out),.out(b1));
Mux_Reg B1(.in(b1),.clk(clk),.out(b1_out),.rst(rstb),.CE(ceb),.sel(B1REG));
//Input C
Mux_Reg #(.input_size(48))c_in(.in(C),.clk(clk),.out(c),.rst(rstc),.CE(cec),.sel(CREG));
//Input D
Mux_Reg d_in(.in(D),.clk(clk),.out(d),.rst(rstd),.CE(ced),.sel(DREG));
//Output P
Mux_Reg #(.input_size(48))p(.in(post_add_sub),.clk(clk),.out(P),.rst(rstp),.CE(cep),.sel(PREG));
//M
Mux_Reg #(.input_size(36))m(.in(M_in),.clk(clk),.out(M_out),.rst(rstm),.CE(cem),.sel(MREG));
//Opmodes
Mux_Reg #(.input_size(2)) op1(.in(opmode[1:0]),.clk(clk),.out(opmode_out[1:0]),.rst(rstopmode),.CE(ceopmode),.sel(OPMODEREG));
Mux_Reg #(.input_size(2)) op2(.in(opmode[3:2]),.clk(clk),.out(opmode_out[3:2]),.rst(rstopmode),.CE(ceopmode),.sel(OPMODEREG));
Mux_Reg #(.input_size(1)) op4(.in(opmode[4]),.clk(clk),.out(opmode_out[4]),.rst(rstopmode),.CE(ceopmode),.sel(OPMODEREG));
Mux_Reg #(.input_size(1)) op5(.in(opmode[5]),.clk(clk),.out(opmode_out[5]),.rst(rstopmode),.CE(ceopmode),.sel(OPMODEREG));
Mux_Reg #(.input_size(1)) op6(.in(opmode[6]),.clk(clk),.out(opmode_out[6]),.rst(rstopmode),.CE(ceopmode),.sel(OPMODEREG));
Mux_Reg #(.input_size(1)) op7(.in(opmode[7]),.clk(clk),.out(opmode_out[7]),.rst(rstopmode),.CE(ceopmode),.sel(OPMODEREG));
//CARRYIN
mux_cin cin(.in0(opmode[5]),.in1(CARRYIN),.out(cyi));
Mux_Reg #(.input_size(1)) CYI(.in(cyi),.clk(clk),.out(cyi_out),.rst(rstcarryin),.CE(ceopmode),.sel(CARRYINREG));
//CARRYOUT
Mux_Reg #(.input_size(1)) CYO(.in(post_add_sub[48]),.clk(clk),.out(cyo_out),.rst(rstcarryin),.CE(ceopmode),.sel(CARRYOUTREG));
//MUX_z
mux4 MUXz(.in0(c),.in1(PCIN),.in2(P),.in3(0),.out(z),.sel(opmode[3:2]));
//MUX_x
mux4_x MUXx(.in0({d[11:0],a1_out,b1_out}),.in1(P),.in2(M_out),.in3(0),.out(x),.sel(opmode[1:0]));
```

```
always @(posedge clk) begin
case({opmode[7],opmode[6]})
2'b00:begin
pre_add_sub= d + b0_out;
M_in= b1_out*a1_out ;
post_add_sub=x+z;
CARRYOUT=cyo_out;
end

2'b01:begin
pre_add_sub=d-b0_out;
M_in=b1_out*a1_out;
post_add_sub=z+x;
CARRYOUT=cyo_out;
end

2'b10:begin
pre_add_sub=d+b0_out;
M_in=b1_out*a1_out;
post_add_sub=z-(x+cyi_out);
CARRYOUT=cyo_out;
end

2'b11:begin
pre_add_sub=d-b0_out;
M_in=b1_out*a1_out;
post_add_sub=z-(x+cyi_out);
CARRYOUT=cyo_out;
end
endcase

end
assign BCOUT=b1_out;
assign M=~(~M_out);
assign CARRYOUTF=CARRYOUT;
assign PCOUT=P;

endmodule
```

2-Testbench-code

```
module DSP_tb();
parameter A0REG=0,B0REG=0,A1REG=1,B1REG=1,CREG=1, DREG=1, MREG=1,
PREG=1, CARRYINREG=1,CARRYOUTREG=1,OPMODEREG=1,
CARRYINSEL="OPMODE5",B_INPUT="DIRECT",RSTTYPE="SYNC";

reg CARRYIN,clk,cea,ceb,cec,cecarryin,
ced,cem,ceopmode,cep,rsta,rstb,rstc,rstcarryin,
rstd,rstm,rstopmode,rstp;

reg [7:0]opmode;
reg [17:0]A,B,D;
reg [47:0]C,PCIN;
reg [17:0]BCIN;

wire [47:0]P,PCOUT;
wire [35:0]M;
wire CARRYOUT;
wire CARRYOUTF;
wire [17:0]BCOUT;


DSP DSP_test(.A(A),.B(B),.C(C),.D(D),.CARRYIN(CARRYIN),.M(M),.P(P),.CARRYOUT(CARRYOUT),
.CARRYOUTF(CARRYOUTF),.clk(clk),.opmode(opmode),.cea(cea),.ceb(ceb),.cec(cec),.cecarryin(cecarryin),
.ced(ced),.cem(cem),.ceopmode(ceopmode),.cep(cep),.rsta(rsta),.rstb(rstb),.rstc(rstc),.rstcarryin(rstcarryin),
.rstd(rstd),.rstm(rstm),.rstopmode(rstopmode),.rstp(rstp),.BCOUT(BCOUT),.PCIN(PCIN),.PCOUT(PCOUT));

initial begin
clk=1;
forever #1 clk=~clk;
end
```

```
integer i;
initial begin
//Test reset
rsta=1;
rstb=1;
rstc=1;
rstcarryin=1;
rstd=1;
rstm=1;
rstopmode=1;
rstp=1;

cea=0;
ceb=0;
cec=0;
cecarryin=0;
ced=0;
cem=0;
ceopmode=0;
cep=0;


A=$random;
B=$random;
C=$random;
D=$random;
opmode=$random;
CARRYIN=$random;
BCIN=$random;
PCIN=$random;
repeat (7) @(negedge clk);

if(P!=0)begin
$display("Error in Design");
$stop;
end
```

```
rsta=0;
rstb=0;
rstc=0;
rstcarryin=0;
rstd=0;
rstm=0;
rstopmode=0;
rstp=0;

cea=1;
ceb=1;
cec=1;
cecarryin=1;
ced=1;
cem=1;
ceopmode=1;
cep=1;

for(i=0;i<10;i=i+1)begin
//test addition
A=$urandom_range(0,1000);
B=$urandom_range(0,1000);
C=$urandom_range(0,1000);
D=$urandom_range(0,1000);
opmode=8'b00111101;
CARRYIN=$random;
BCIN=$random;
PCIN=$random;
repeat (7) @(negedge clk);
```

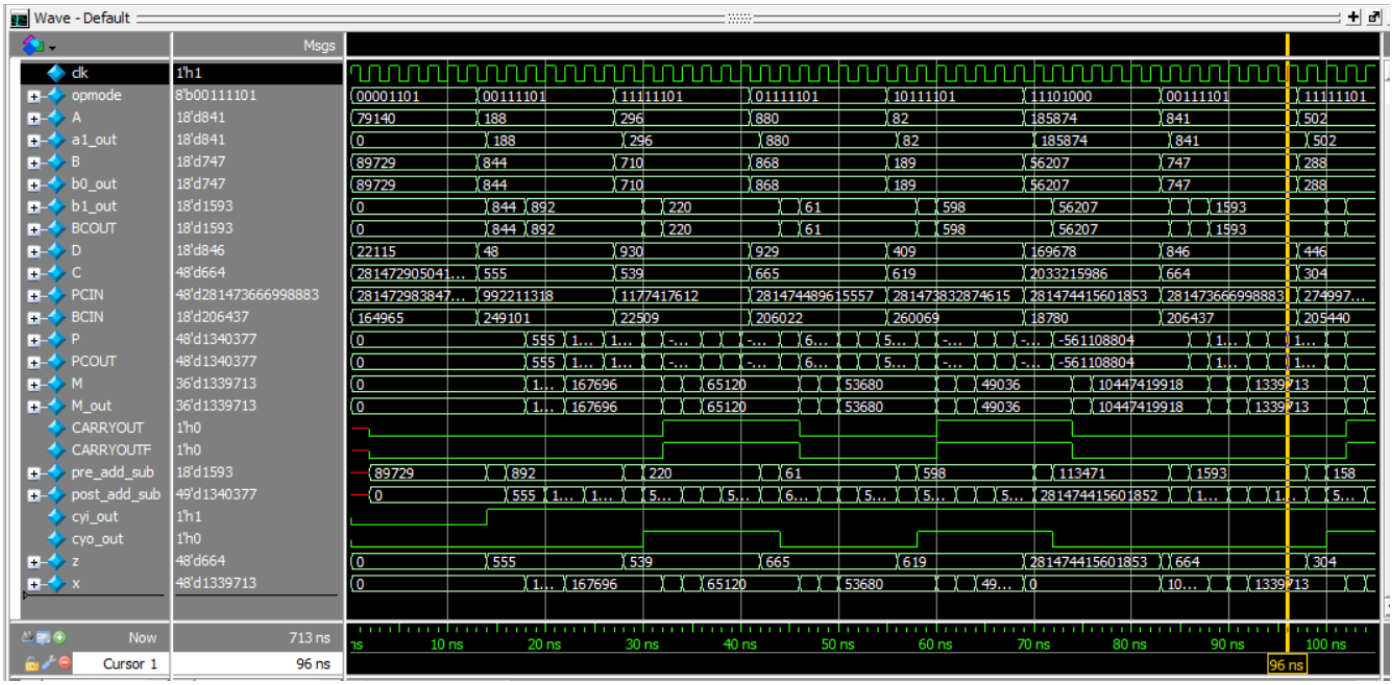
```
//test subtraction
A=$urandom_range(0,1000);
B=$urandom_range(0,1000);
C=$urandom_range(0,1000);
D=$urandom_range(0,1000);
opmode=8'b11111101;
CARRYIN=$random;
BCIN=$random;
PCIN=$random;
repeat (7) @(negedge clk);

//test subtraction then addition

A=$urandom_range(0,1000);
B=$urandom_range(0,1000);
C=$urandom_range(0,1000);
D=$urandom_range(0,1000);
opmode=8'b01111101;
CARRYIN=$random;
BCIN=$random;
PCIN=$random;
repeat (7) @(negedge clk);

//test addition then subtraction
A=$urandom_range(0,1000);
B=$urandom_range(0,1000);
C=$urandom_range(0,1000);
D=$urandom_range(0,1000);
opmode=8'b10111101;
CARRYIN=$random;
BCIN=$random;
PCIN=$random;
repeat (7) @(negedge clk);
```

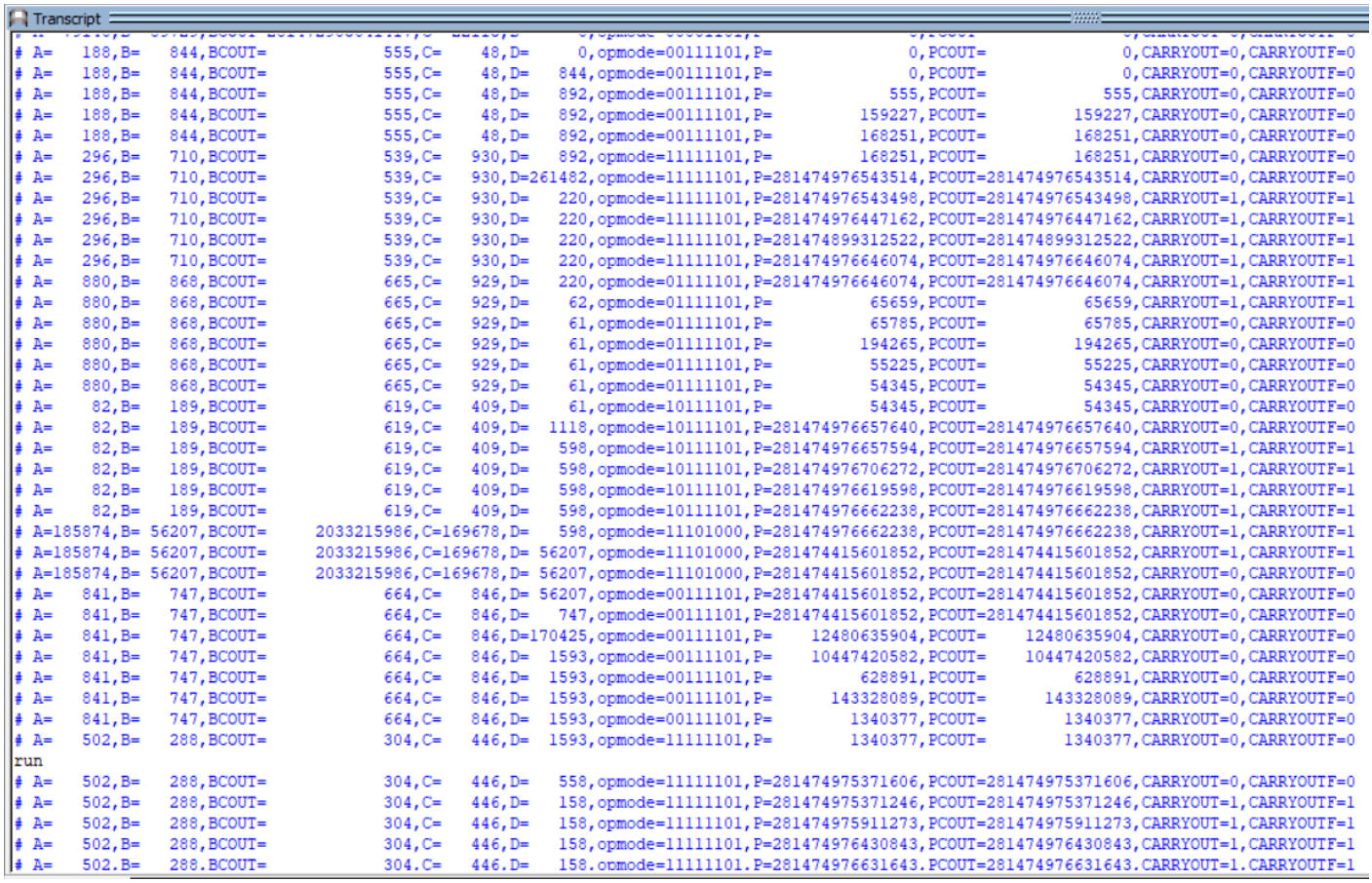
```
//Test all cases
A=$random;
B=$random;
C=$random;
D=$random;
opmode=$random;
CARRYIN=$random;
BCIN=$random;
PCIN=$random;
repeat (7) @(negedge clk);


end
$stop;

end
initial begin
    $monitor("A=%d,B=%d,BCOUT=%d,C=%d,D=%d,opmode=%b,P=%d,PCOUT=%d,CARRYOUT=%d,CARRYOUTF=%d",A,B,C,D,BCOUT,opmode,P,PCOUT,CARRYOUT,CARRYOUTF,);
end
endmodule
```

3-Do file

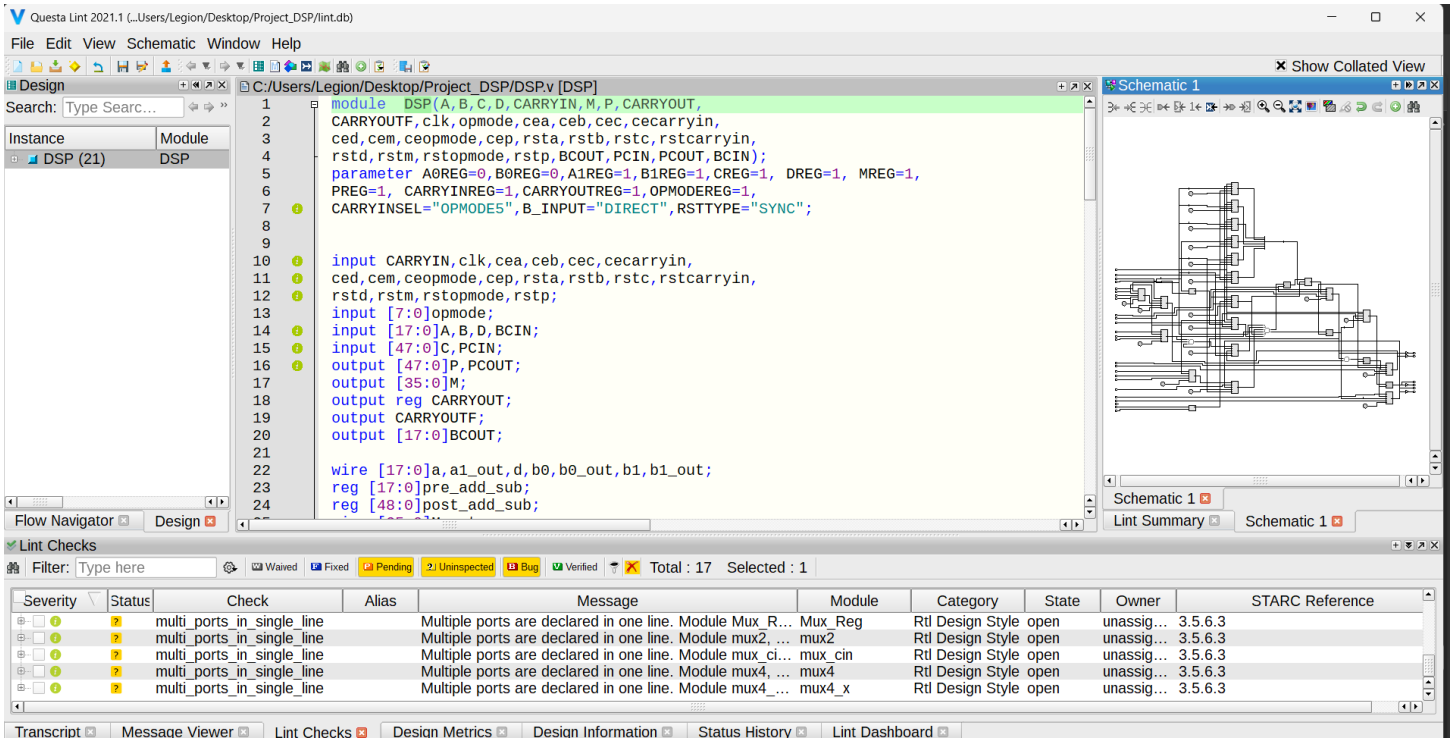
```
vlib work
vlog DSP.v DSP_tb.v MUX_REG.v
vsim -voptargs=+acc work.DSP_tb
add wave *
run -all
```

4-QuestaSim


Wave - Default
Msgs
clk
opmode
A
a1_out
B
b0_out
b1_out
BCOUT
D
C
PCIN
BCIN
P
PCOUT
M
M_out
CARRYOUT
CARRYOUTF
pre_add_sub
post_add_sub
cyi_out
cyo_out
z
x
Now
713 ns
Cursor 1
96 ns

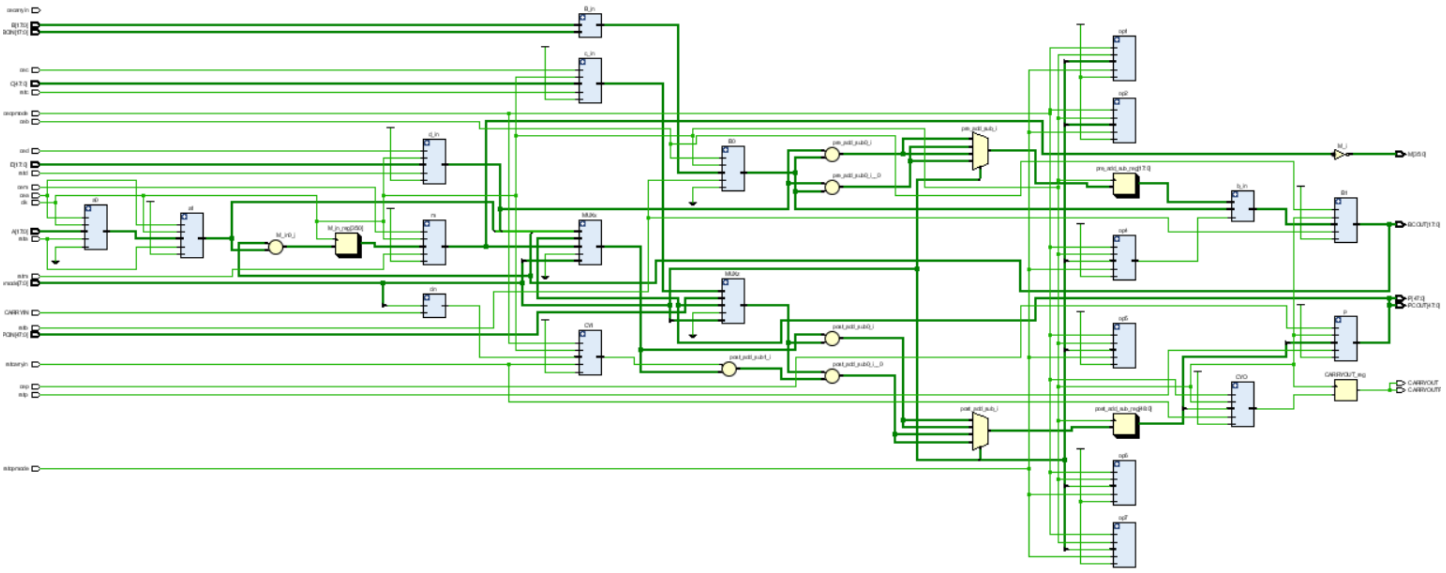

Transcript
A= 188,B= 844,BCOUT= 555,C= 48,D= 0,opmode=00111101,P= 0,PCOUT= 0,CARRYOUT=0,CARRYOUTF=0
A= 188,B= 844,BCOUT= 555,C= 48,D= 844,opmode=00111101,P= 0,PCOUT= 0,CARRYOUT=0,CARRYOUTF=0
A= 188,B= 844,BCOUT= 555,C= 48,D= 892,opmode=00111101,P= 555,PCOUT= 555,CARRYOUT=0,CARRYOUTF=0
A= 188,B= 844,BCOUT= 555,C= 48,D= 892,opmode=00111101,P= 159227,PCOUT= 159227,CARRYOUT=0,CARRYOUTF=0
A= 188,B= 844,BCOUT= 555,C= 48,D= 892,opmode=00111101,P= 168251,PCOUT= 168251,CARRYOUT=0,CARRYOUTF=0
A= 296,B= 710,BCOUT= 539,C= 930,D= 892,opmode=11111101,P= 168251,PCOUT= 168251,CARRYOUT=0,CARRYOUTF=0
A= 296,B= 710,BCOUT= 539,C= 930,D=261482,opmode=11111101,P=281474976543514,PCOUT=281474976543514,CARRYOUT=0,CARRYOUTF=0
A= 296,B= 710,BCOUT= 539,C= 930,D= 220,opmode=11111101,P=281474976543498,PCOUT=281474976543498,CARRYOUT=1,CARRYOUTF=1
A= 296,B= 710,BCOUT= 539,C= 930,D= 220,opmode=11111101,P=281474976447162,PCOUT=281474976447162,CARRYOUT=1,CARRYOUTF=1
A= 296,B= 710,BCOUT= 539,C= 930,D= 220,opmode=11111101,P=281474899312522,PCOUT=281474899312522,CARRYOUT=1,CARRYOUTF=1
A= 296,B= 710,BCOUT= 539,C= 930,D= 220,opmode=11111101,P=281474976646074,PCOUT=281474976646074,CARRYOUT=1,CARRYOUTF=1
A= 880,B= 868,BCOUT= 665,C= 929,D= 220,opmode=01111101,P=281474976646074,PCOUT=281474976646074,CARRYOUT=1,CARRYOUTF=1
A= 880,B= 868,BCOUT= 665,C= 929,D= 62,opmode=01111101,P= 65659,PCOUT= 65659,CARRYOUT=1,CARRYOUTF=1
A= 880,B= 868,BCOUT= 665,C= 929,D= 61,opmode=01111101,P= 65785,PCOUT= 65785,CARRYOUT=0,CARRYOUTF=0
A= 880,B= 868,BCOUT= 665,C= 929,D= 61,opmode=01111101,P= 194265,PCOUT= 194265,CARRYOUT=0,CARRYOUTF=0
A= 880,B= 868,BCOUT= 665,C= 929,D= 61,opmode=01111101,P= 55225,PCOUT= 55225,CARRYOUT=0,CARRYOUTF=0
A= 880,B= 868,BCOUT= 665,C= 929,D= 61,opmode=01111101,P= 54345,PCOUT= 54345,CARRYOUT=0,CARRYOUTF=0
A= 82,B= 189,BCOUT= 619,C= 409,D= 61,opmode=10111101,P= 54345,PCOUT= 54345,CARRYOUT=0,CARRYOUTF=0
A= 82,B= 189,BCOUT= 619,C= 409,D= 1118,opmode=10111101,P=281474976657640,PCOUT=281474976657640,CARRYOUT=0,CARRYOUTF=0
A= 82,B= 189,BCOUT= 619,C= 409,D= 598,opmode=10111101,P=281474976657594,PCOUT=281474976657594,CARRYOUT=1,CARRYOUTF=1
A= 82,B= 189,BCOUT= 619,C= 409,D= 598,opmode=10111101,P=281474976706272,PCOUT=281474976706272,CARRYOUT=1,CARRYOUTF=1
A= 82,B= 189,BCOUT= 619,C= 409,D= 598,opmode=10111101,P=281474976619598,PCOUT=281474976619598,CARRYOUT=1,CARRYOUTF=1
A= 82,B= 189,BCOUT= 619,C= 409,D= 598,opmode=10111101,P=281474976662238,PCOUT=281474976662238,CARRYOUT=1,CARRYOUTF=1
A=185874,B= 56207,BCOUT= 2033215986,C=169678,D= 598,opmode=11101000,P=281474976662238,PCOUT=281474976662238,CARRYOUT=1,CARRYOUTF=1
A=185874,B= 56207,BCOUT= 2033215986,C=169678,D= 56207,opmode=11101000,P=281474415601852,PCOUT=281474415601852,CARRYOUT=1,CARRYOUTF=1
A=185874,B= 56207,BCOUT= 2033215986,C=169678,D= 56207,opmode=11101000,P=281474415601852,PCOUT=281474415601852,CARRYOUT=0,CARRYOUTF=0
A= 841,B= 747,BCOUT= 664,C= 846,D= 56207,opmode=00111101,P=281474415601852,PCOUT=281474415601852,CARRYOUT=0,CARRYOUTF=0
A= 841,B= 747,BCOUT= 664,C= 846,D= 747,opmode=00111101,P=281474415601852,PCOUT=281474415601852,CARRYOUT=0,CARRYOUTF=0
A= 841,B= 747,BCOUT= 664,C= 846,D=170425,opmode=00111101,P= 12480635904,PCOUT= 12480635904,CARRYOUT=0,CARRYOUTF=0
A= 841,B= 747,BCOUT= 664,C= 846,D= 1593,opmode=00111101,P= 10447420582,PCOUT= 10447420582,CARRYOUT=0,CARRYOUTF=0
A= 841,B= 747,BCOUT= 664,C= 846,D= 1593,opmode=00111101,P= 628891,PCOUT= 628891,CARRYOUT=0,CARRYOUTF=0
A= 841,B= 747,BCOUT= 664,C= 846,D= 1593,opmode=00111101,P= 143328089,PCOUT= 143328089,CARRYOUT=0,CARRYOUTF=0
A= 841,B= 747,BCOUT= 664,C= 846,D= 1593,opmode=00111101,P= 1340377,PCOUT= 1340377,CARRYOUT=0,CARRYOUTF=0
A= 502,B= 288,BCOUT= 304,C= 446,D= 1593,opmode=11111101,P= 1340377,PCOUT= 1340377,CARRYOUT=0,CARRYOUTF=0
run
A= 502,B= 288,BCOUT= 304,C= 446,D= 558,opmode=11111101,P=281474975371606,PCOUT=281474975371606,CARRYOUT=0,CARRYOUTF=0
A= 502,B= 288,BCOUT= 304,C= 446,D= 158,opmode=11111101,P=281474975371246,PCOUT=281474975371246,CARRYOUT=1,CARRYOUTF=1
A= 502,B= 288,BCOUT= 304,C= 446,D= 158,opmode=11111101,P=281474975911273,PCOUT=281474975911273,CARRYOUT=1,CARRYOUTF=1
A= 502,B= 288,BCOUT= 304,C= 446,D= 158,opmode=11111101,P=281474976430843,PCOUT=281474976430843,CARRYOUT=1,CARRYOUTF=1
A= 502,B= 288,BCOUT= 304,C= 446,D= 158,opmode=11111101,P=281474976631643,PCOUT=281474976631643,CARRYOUT=1,CARRYOUTF=1

5-QuestaLint

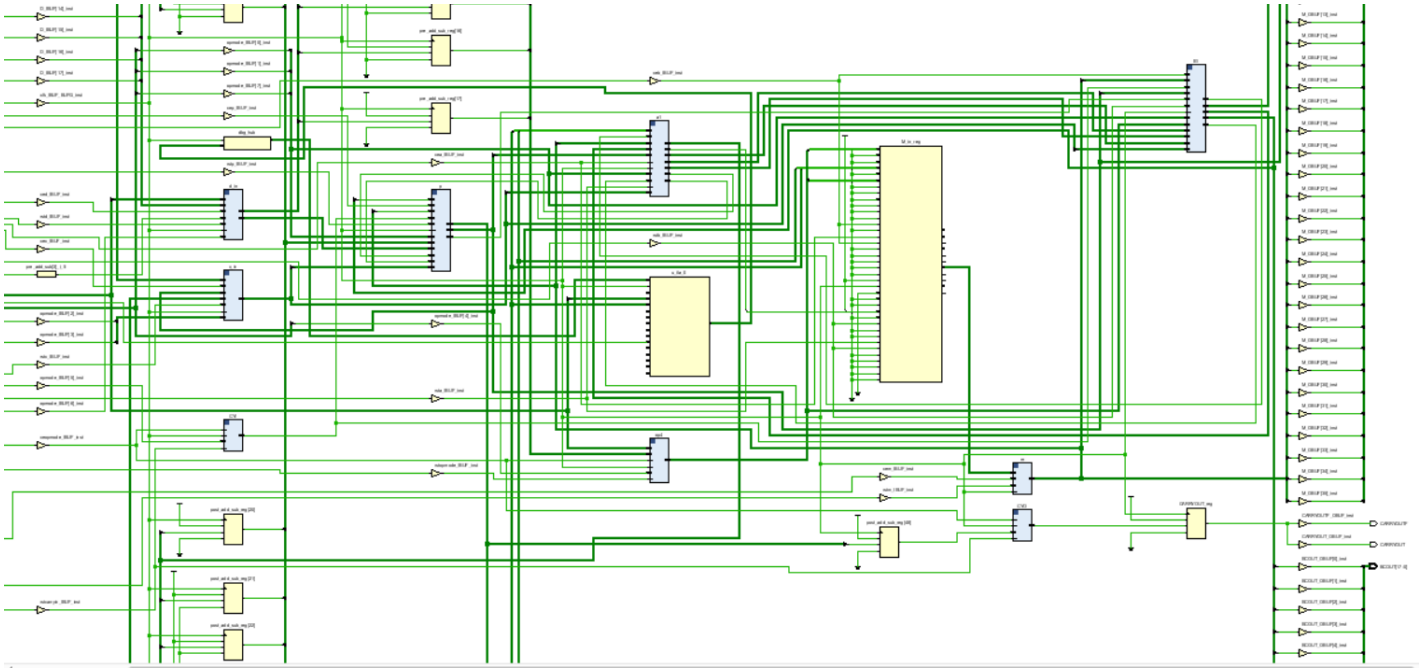


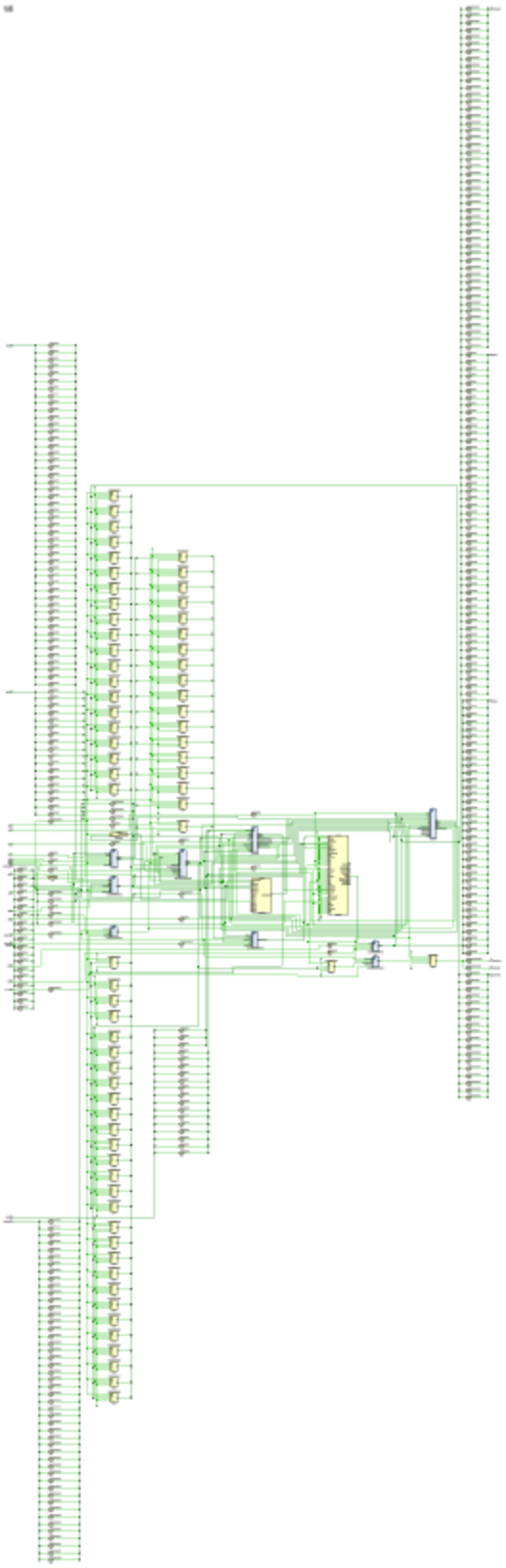
6-Synthesize

Elaborated Design:



Synthesized design:





Report timing summary:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.609 ns	Worst Hold Slack (WHS):	0.140 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	209	Total Number of Endpoints:	209	Total Number of Endpoints:	259

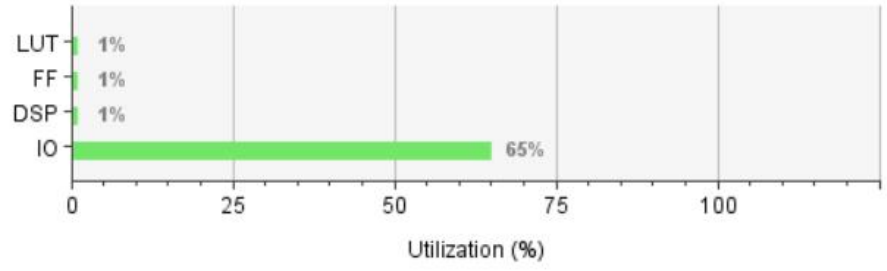
All user specified timing constraints are met.

Utilization summary:

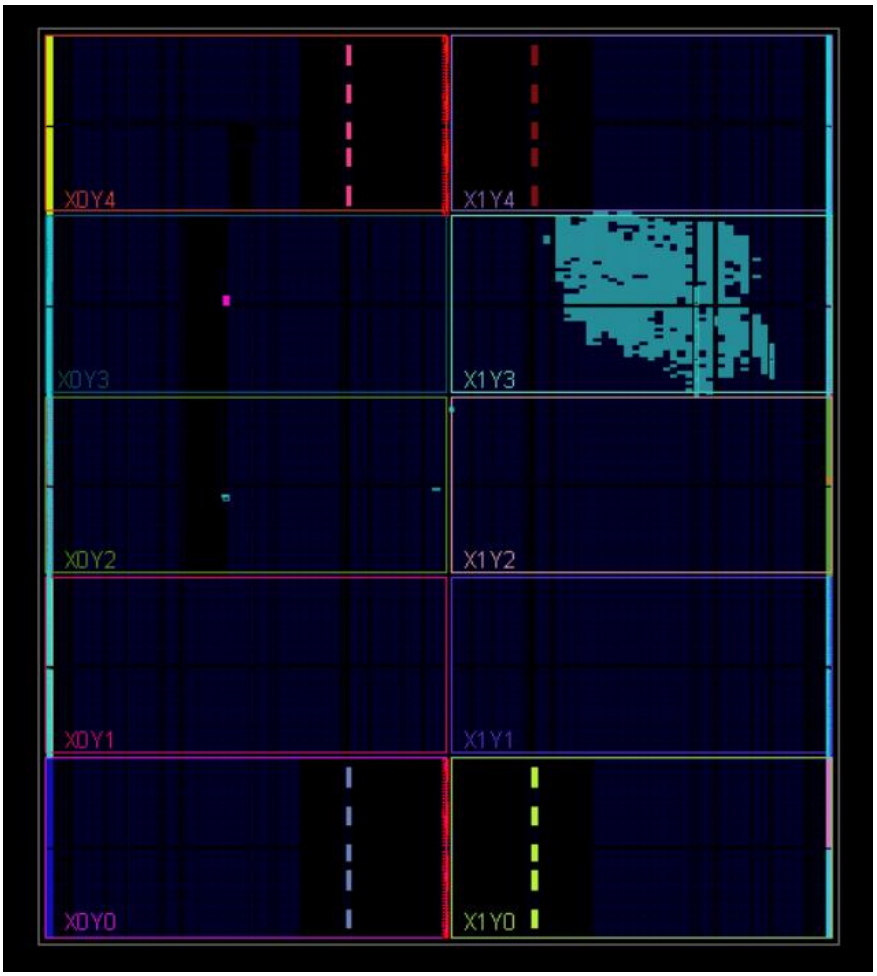
Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP	242	257	1	326	1
a1 (Mux_Reg_1)	54	18	0	0	0
B1 (Mux_Reg)	55	18	0	0	0
c_in (Mux_Reg__para...	48	48	0	0	0
CYI (Mux_Reg__para...	0	1	0	0	0
CYO (Mux_Reg__para...	1	1	0	0	0
d_in (Mux_Reg_2)	17	18	0	0	0
dbg_hub (dbg_hub_CV)	0	0	0	0	0
m (Mux_Reg__parame...	0	36	0	0	0
op4 (Mux_Reg__para...	18	1	0	0	0
p (Mux_Reg__paramet...	50	48	0	0	0
u_ila_0 (u_ila_0_CV)	0	0	0	0	0

Summary

Resource	Utilization	Available	Utilization %
LUT	242	134600	0.18
FF	257	269200	0.10
DSP	1	740	0.14
IO	326	500	65.20



7-Implementation



Report timing summary:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.920 ns	Worst Hold Slack (WHS):	0.058 ns	Worst Pulse Width Slack (WPWS):	3.950 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8088	Total Number of Endpoints:	8072	Total Number of Endpoints:	5173

All user specified timing constraints are met.

Utilization summary:

Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	BSCANE2 (4)
N DSP	2671	4272	96	11	1452	2202	469	1555	8	1	326	2	1
a1 (Mux_Reg_1)	54	18	0	0	24	54	0	0	0	0	0	0	0
B1 (Mux_Reg)	55	18	0	0	20	55	0	0	0	0	0	0	0
c_in (Mux_Reg__para...	48	48	0	0	35	48	0	0	0	0	0	0	0
CYI (Mux_Reg__para...	0	1	0	0	1	0	0	0	0	0	0	0	0
CYO (Mux_Reg__para...	1	1	0	0	1	1	0	1	0	0	0	0	0
d_in (Mux_Reg_2)	17	18	0	0	12	17	0	0	0	0	0	0	0
dbg_hub (dbg_hub)	475	727	0	0	243	451	24	298	0	0	0	1	1
m (Mux_Reg__parame...	0	36	0	0	6	0	0	0	0	0	0	0	0
op4 (Mux_Reg__para...	18	1	0	0	6	18	0	0	0	0	0	0	0
p (Mux_Reg__paramet...	50	48	0	0	26	50	0	0	0	0	0	0	0
u_ila_0 (u_ila_0)	1954	3288	96	11	1122	1509	445	1181	8	0	0	0	0

Resource	Utilization	Available	Utilization %
LUT	2671	133800	2.00
LUTRAM	469	46200	1.02
FF	4272	267600	1.60
BRAM	8	365	2.19
DSP	1	740	0.14
IO	326	500	65.20