DSP48A1 Slice in Detail

Figure 1-3 shows a DSP48A1 slice and its associated datapaths. The inputs to the shaded multiplexers are selected by configuration control signals. These attributes are set in the HDL source code or by the User Constraint File (UCF).

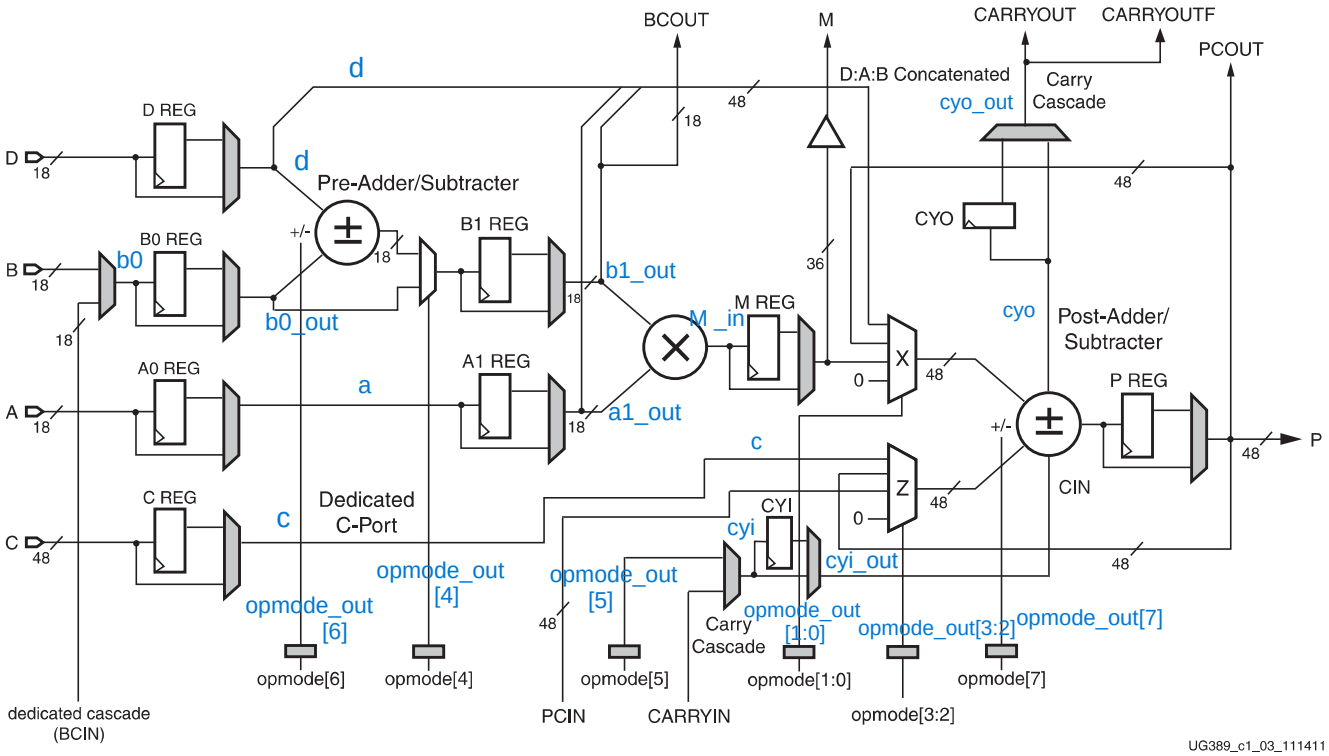

Figure 1-3: **DSP48A1 Slice**

Notes relevant to Figure 1-3:

1. The 18-bit A, B, and D buses are concatenated in the following order: D[11:0], A[17:0], B[17:0].
2. The X and Z multiplexers are 48-bit designs. Selecting any of the 36-bit inputs provides a 48-bit sign-extended output.
3. The multiplier outputs a 36-bit result that can be optionally registered to the M register.
4. The multiply-accumulate path for P is through the Z multiplexer. The P feedback through the X multiplexer enables accumulation of P cascade when the multiplier is not used.
5. The gray-colored multiplexers are programmed at configuration time. The clear multiplexers are controlled by OPMODE inputs, allowing dynamic changes to functionality.
6. The C register supports multiply-add or wide addition operations.
7. Enabling SUBTRACT implements Z – (X + CIN) at the output of the post-adder/subtracter.
8. B input can be added or subtracted from the D input using the pre-adder/subtracter. Enabling SUBTRACT implements D – B at the output of the pre-adder/subtracter.