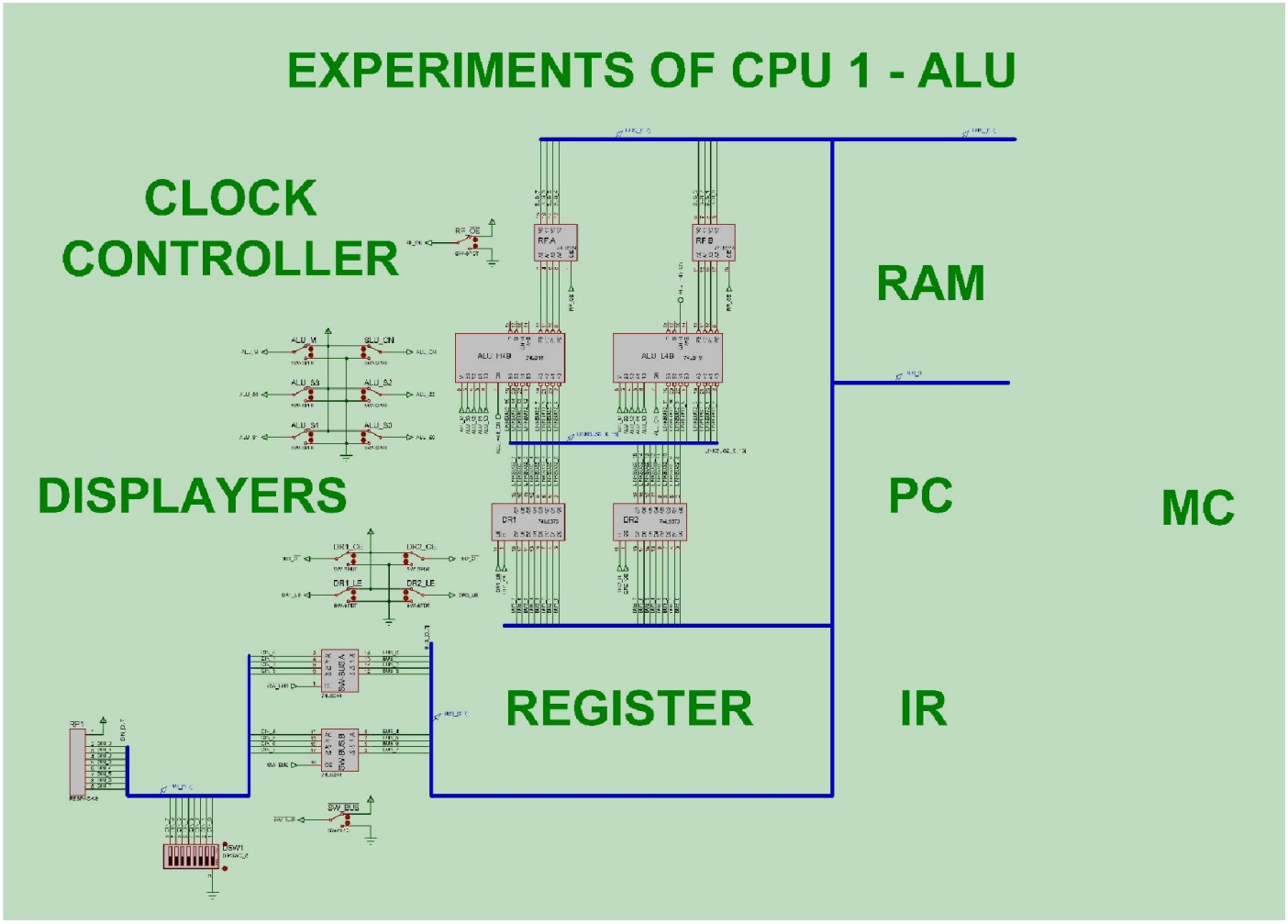
Laboratory Manual of Computer Organization and Architecture

EXPERIMENTS 1 – ALU

Circuit Diagram



New Concept

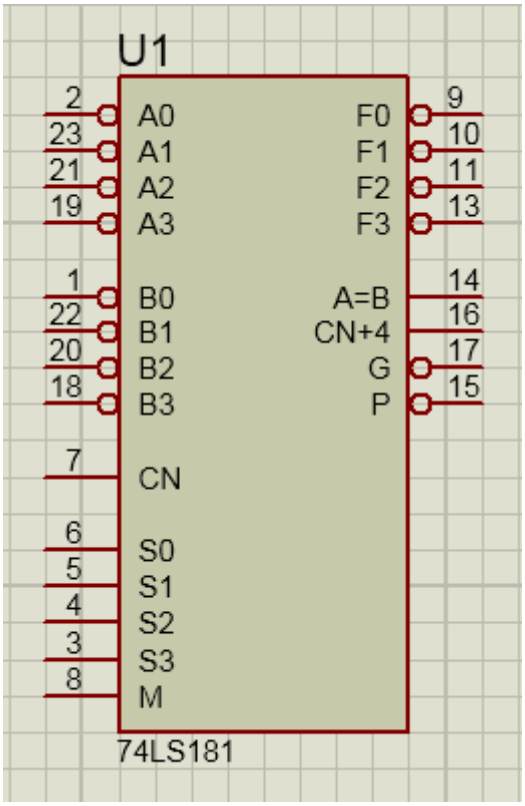
Pin: The single wire connector between the device or the component and the peripheral circuit.

Port: A set of pins with the same function of the device.

Enabling Pin: The pin to control the device.

Device List

74LS181: Arithmetic Logic Unit



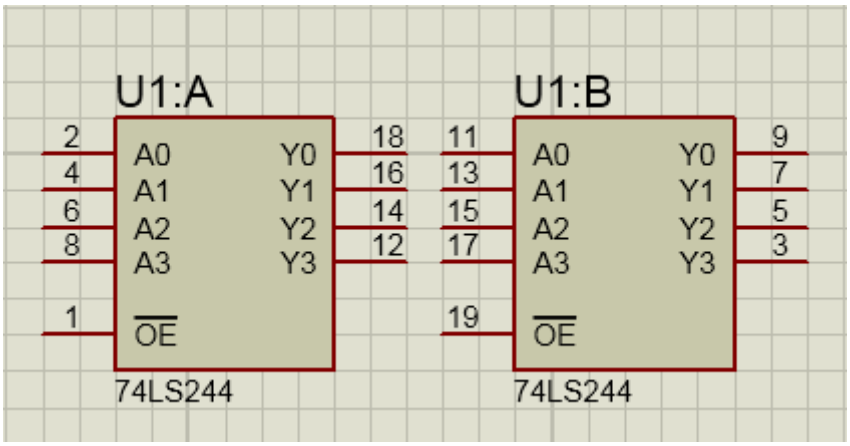
Function Table

Mode Select Inputs				Active LOW Operands & F_n Outputs		Active HIGH Operands & F_n Outputs	
S3	S2	S1	S0	Logic (M = H)	Arithmetic** (M = L) (C_n = L)	Logic (M = H)	Arithmetic** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A + B}$	A$\overline{B}$ minus 1	$\overline{AB}$	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{AB}$	A plus (A + B)	$\overline{A}$ + B	A plus AB
H	L	L	H	A ⊕ B	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	A$\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

*Each bit is shifted to the next most significant position.

**Arithmetic operations expressed in 2s complement notation.

74LS244: Octal Buffers/Line Drivers with Tristate Outputs

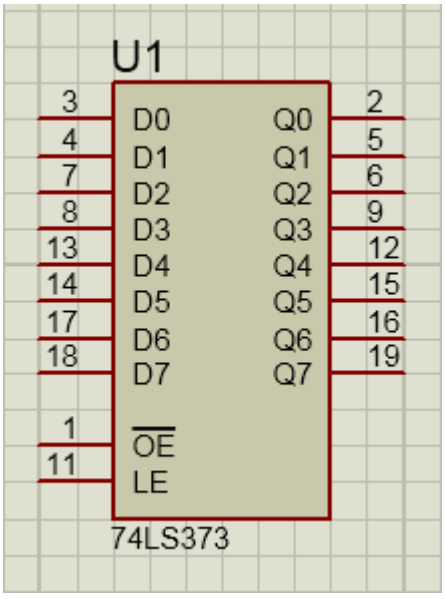


Function Table

Inputs		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = LOW Logic Level
H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
Z = High Impedance

74LS373: Octal D-Type Transparent Latches with Tristate Outputs



SN54/74LS373 • SN54/74LS374

TRUTH TABLE

LS373

D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z*

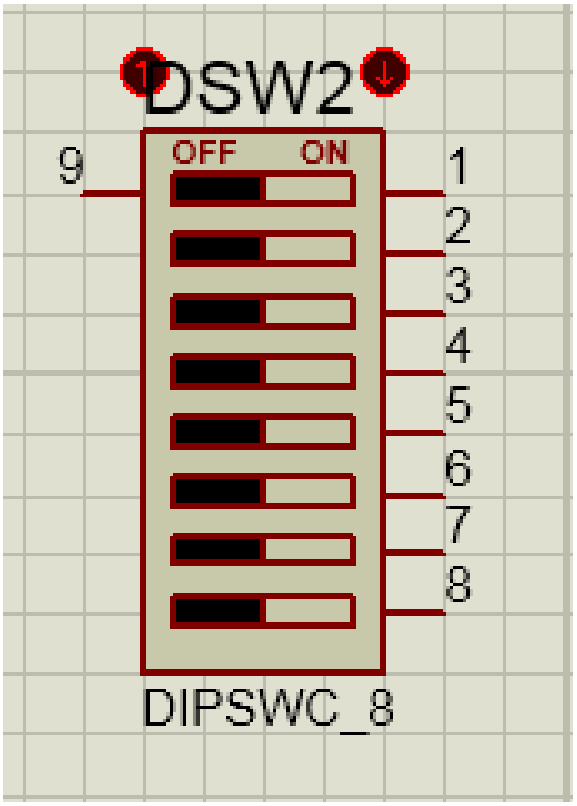
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

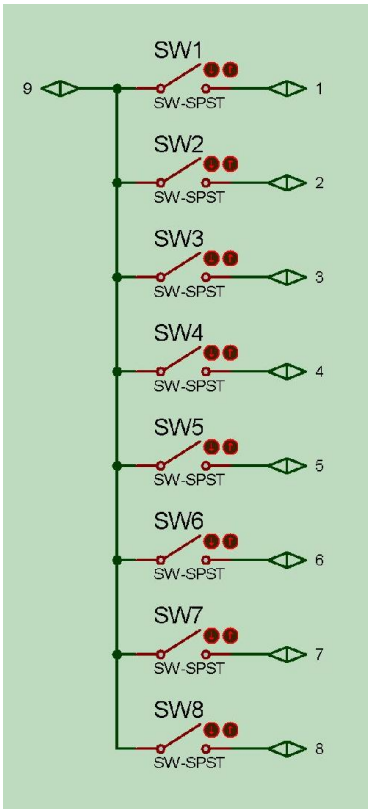
LS374

D_n	LE	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z*

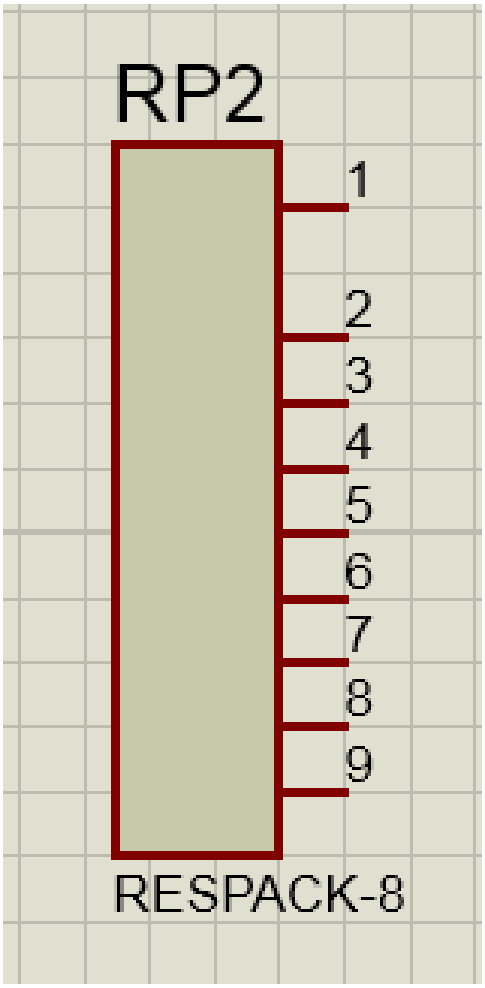
* Note: Contents of flip-flops unaffected by the state of the Output Enable input ($\overline{OE}$).

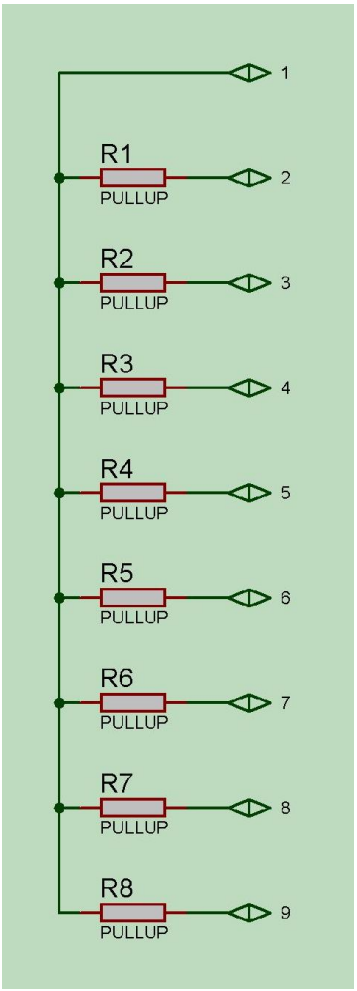
DIPSWC_8: Interactive DIP Switch 8 Common elements





RESPACK-8: 8 way resistor pack witn common





SW-SPDT: Interactive SPDT(Single-Pole Double-Throw) Switch

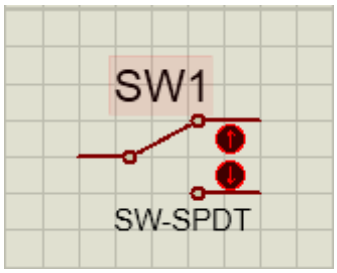


Table of Experiment Data Record

S3 S2 S1 S0	Data1	Data2	Arithmetic Operation (M = 0)		Logic Operation (M = 1)
			CN = 1 (No Carry)	CN = 0 (Carry)	
0 0 0 0	0AAH	55H			
0 0 0 1	0AAH	55H			
0 0 1 0	0AAH	55H			
0 0 1 1	0AAH	55H			
0 1 0 0	0FFH	01H			
0 1 0 1	0FFH	01H			
0 1 1 0	0FFH	01H			
0 1 1 1	0FFH	01H			
1 0 0 0	0FFH	0FFH			
1 0 0 1	0FFH	0FFH			
1 0 1 0	0FFH	0FFH			
1 0 1 1	0FFH	0FFH			
1 1 0 0	55H	01H			
1 1 0 1	55H	01H			
1 1 1 0	55H	01H			
1 1 1 1	55H	01H			

Steps of the Experiment

(1) Reset all the enabling pins of 74LS181. Set all the enabling pins of other devices;

(2) Lock data 0AAH to DR1 and data 55H to DR2. Disable the output of SW-BUS;

(3) Set the enabling pins $S_3S_2S_1S_0$ into 0000. Reset the enabling pin M and set the enabling pin CN. Record the output data of 74LS181;

(4) Keep the state of enabling pins $S_3S_2S_1S_0$ and the enabling pin M. Reset the enabling pin CN. Record the output data of 74LS181;

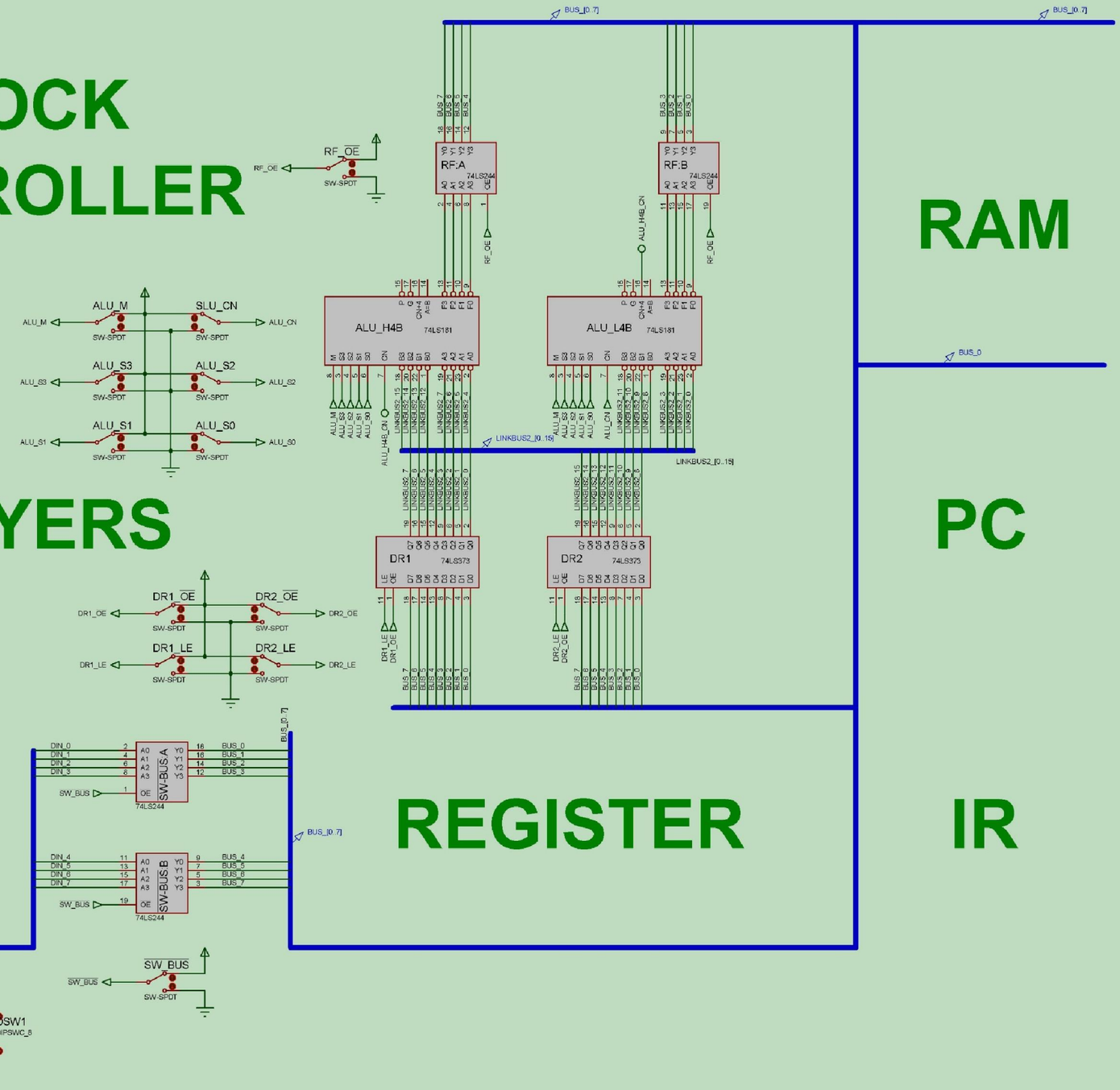
(5) Keep the state of enabling pins $S_3S_2S_1S_0$. Set the enabling pin M. Record the output data of 74LS181;

(6) Set the enabling pins $S_3S_2S_1S_0$ into the next state and redo the step (2) to (5).

EXPERIMENTS OF CPU 1 - ALU

CLOCK

CONTROLLER



RAM

DISPLAYERS

PC

MC

REGISTER

IR