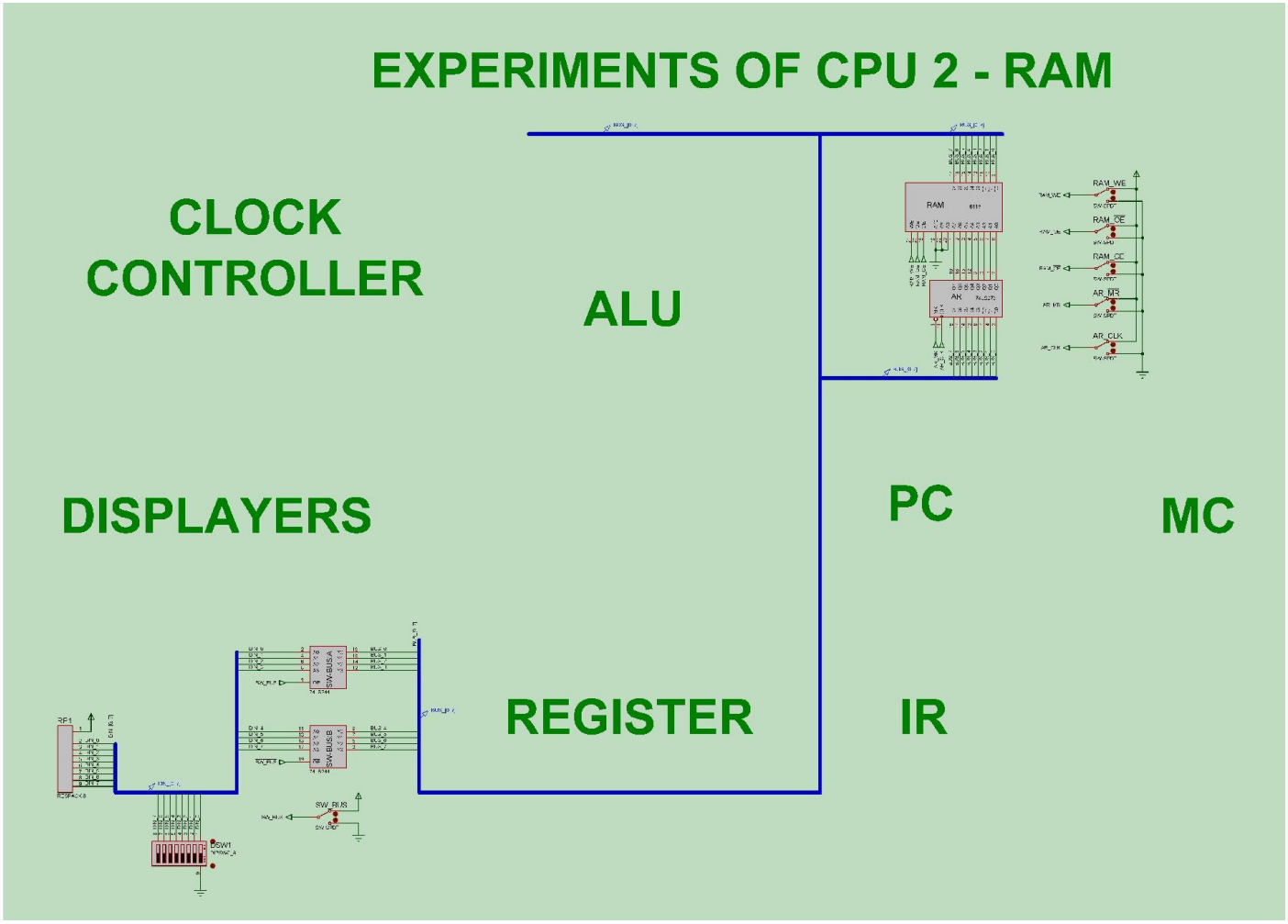
Laboratory Manual of Computer Organization and Architecture

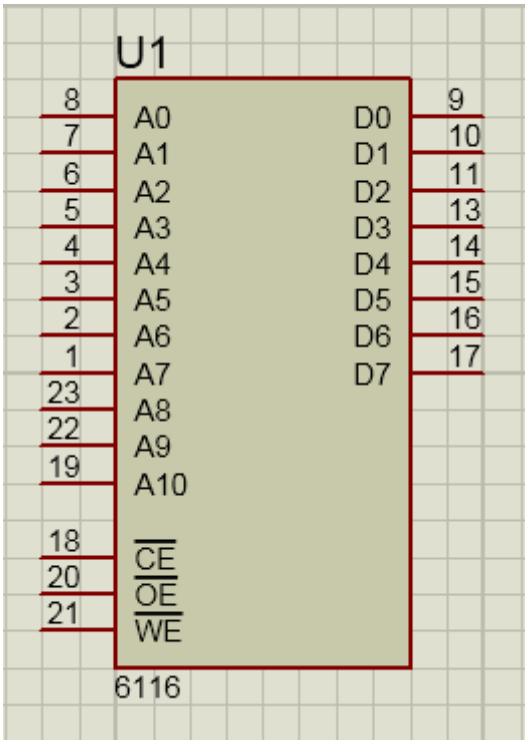
EXPERIMENTS 2 – RAM

Circuit Diagram



Device List

6116: 16K (2K X 8) Static RAM



PIN DESCRIPTIONS

A_0–A_{13}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

3089 tbl 01

TRUTH TABLE(1)

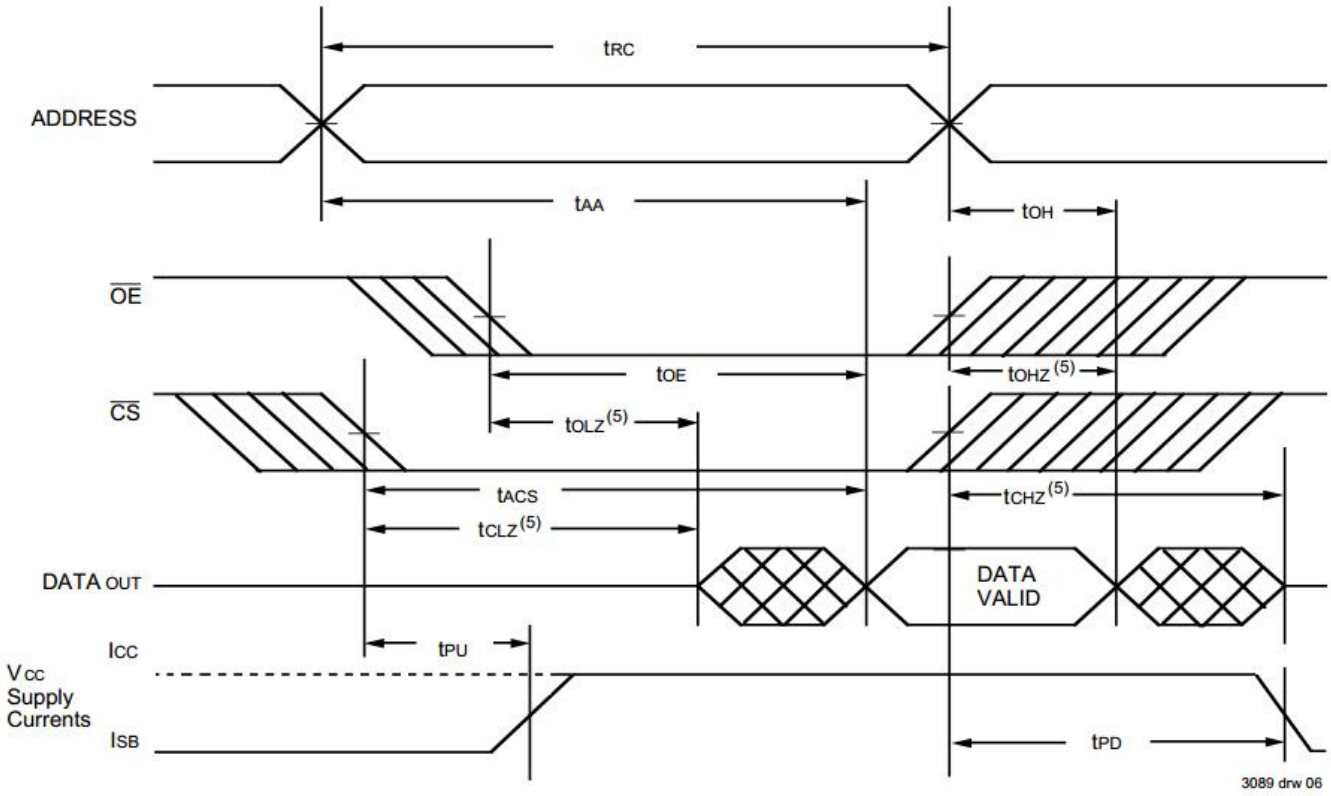
Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High-Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High-Z
Write	L	X	L	$DATA_{IN}$

NOTE:

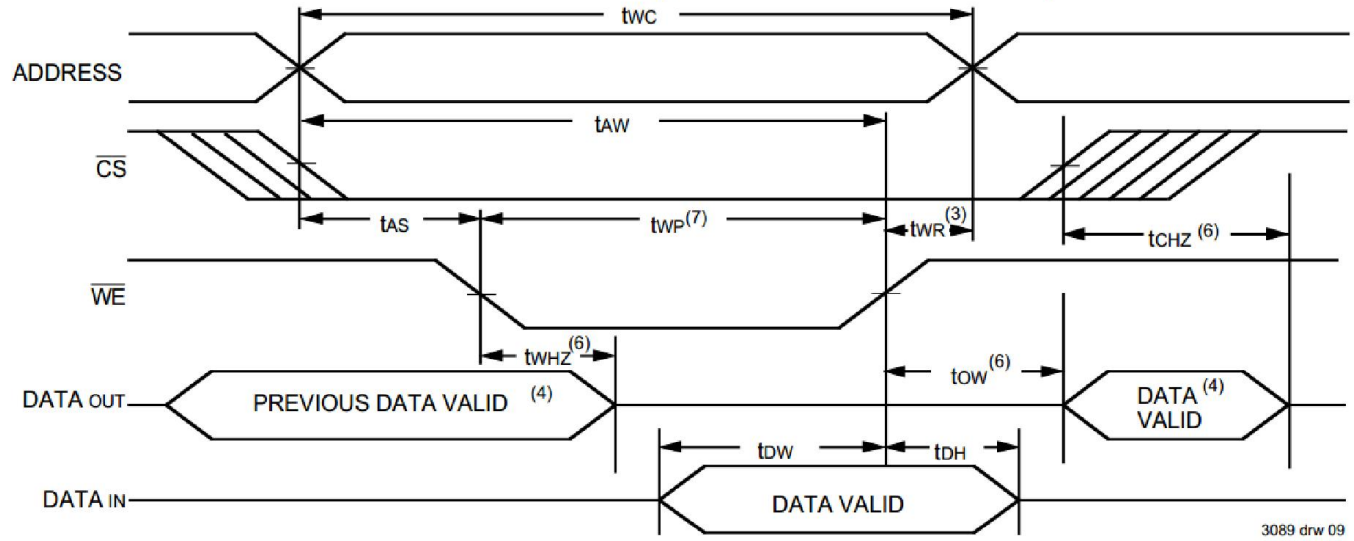
3089 tbl 02

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

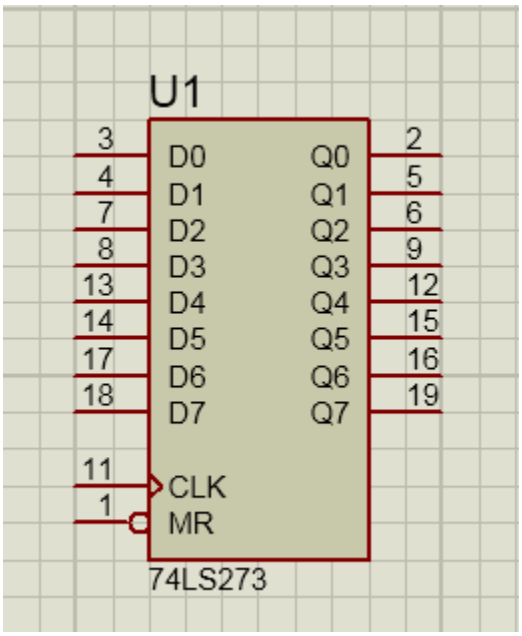
TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 1, (WE CONTROLLED TIMING) (1, 2, 5, 7)



74LS273: Octal D-Type Positive-Edge-Triggered Flip-Flops With Clear



Pin Descriptions

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D0–D7	Data Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
Q0–Q7	Flip-Flop Outputs

Truth Table

Inputs			Outputs
MR	CP	D_n	Q_n
L	X	X	L
H	⌐	H	H
H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Table of Experiment Data Record

DSW1	74LS244 $\overline{OE}$[1]	74LS273 CLK[2]	6116[1]			74LS273 Q_7-Q_0	6116 D_7-D_0	Steps
			$\overline{CE}$	$\overline{OE}$	$\overline{WE}$			
								Write address 00H to AR
								Write data 01H to RAM
								Write address 10H to AR
								Write data 02H to RAM
								Read data from address 00H
								Read data from address 10H

Remark:

1. For the enabling pins in the table above, please use 'H' for High Level State and 'L' for Low Level State.
2. For the pin CLK in 74LS273 in the table above, please use ' ↑ ' for the rising-edge and '-' for non-rising-edge.

Steps of the Experiment

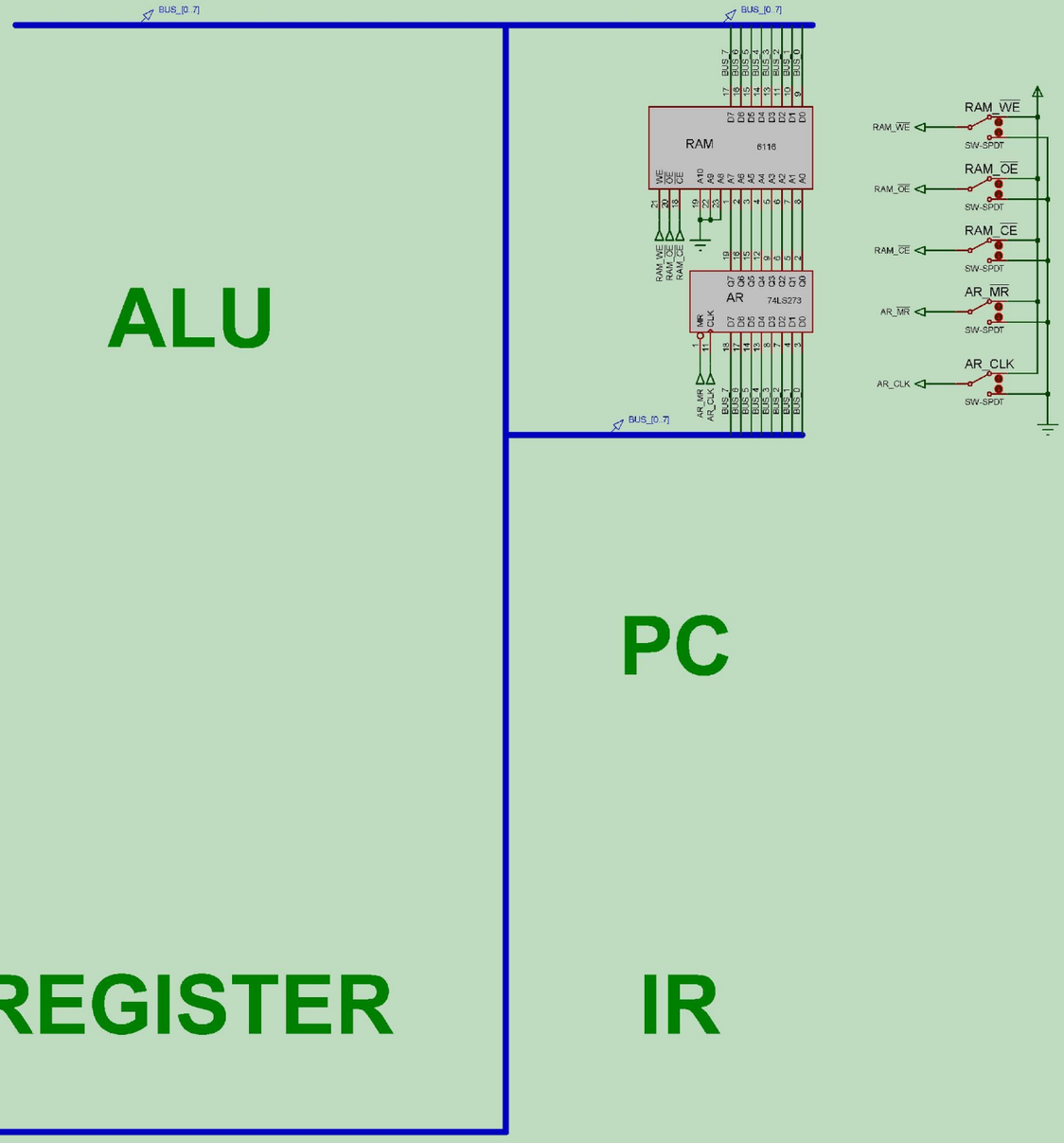
(1) Set all the enabling pins except for enabling pin AR_CLK. Then start the simulation.
(2) Enable the SW-BUS. Write address 00H on the BUS. Give a single positive pulse to AR_CLK. (Lock Address for purpose)
(3) Write data 01H on the BUS. Enable the pin RAM_CE. Give a single negative pulse to RAM_WE. (Write data for purpose)
(4) Lock Address 10H to AR using the same way mentioned in step (2).
(5) Write data 02H using the same way mentioned in step (3).
(6) Lock Address 00H to AR using the same way mentioned in step (2). Disable the SW-BUS. Enable RAM_CE and RAM_OE. (Read data for purpose)
(7) Read data from address 10H using the same way mentioned in step (6).
(8) Pause the simulation. Click the menu 'Debug' and then 'Memory Contents-RAM' to see data written in RAM.

EXPERIMENTS OF CPU 2 - RAM

CLOCK

CONTROLLER

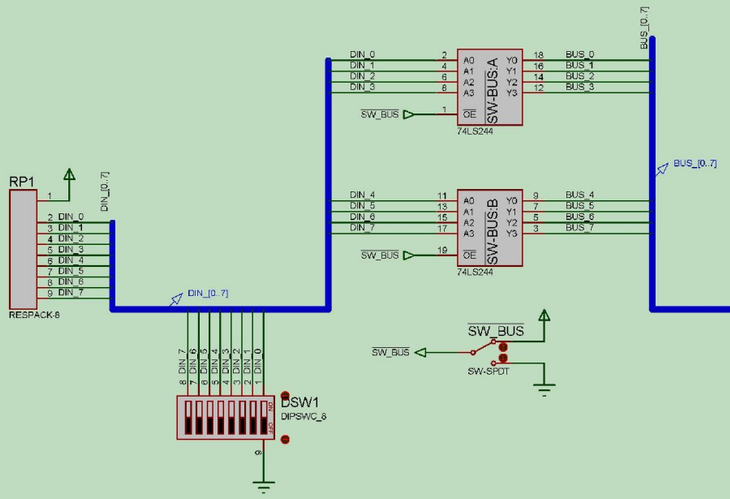
ALU



DISPLAYERS

PC

MC



REGISTER

IR