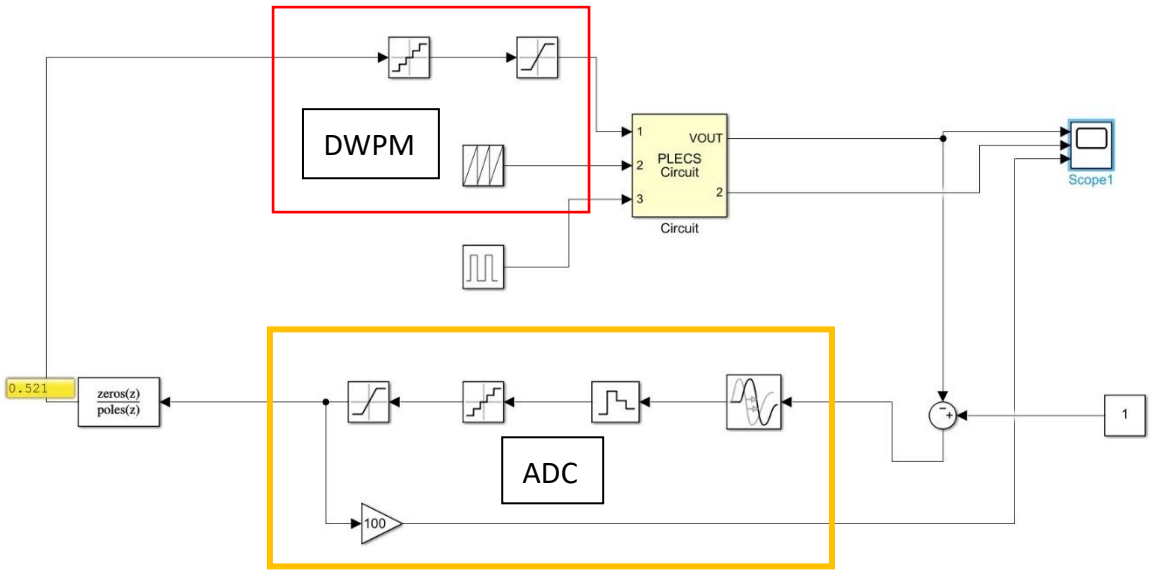
Digitally Controlled Voltage Mode Buck Converter Report

1. Implementation Report:

A. Digital buck converter system design

The Digital buck converter includes DWPM and ADC parts, the following is the overall architecture diagram of the circuit, and the design considerations for each design module will be explained below.



i. ADC:

The design of ADC is mainly divided into Transport Delay, Zero-Order Hold, Quantizer, Saturation and other parts.

The transport delay part is mainly to adjust the parameters of time delay, the algorithm of time delay is: t = tconv + tcal + tg, according to the required parameters substituted into the formula, you can get loop delay = 420ns + 65ns + 10ns = 495ns.

The Zero-Order Hold module mainly adjusts the sample time(switching period) with the algorithm of 1/(switching frequency) = 2*10^-6.

I take 7 bits after calculating the ADC bits, and the algorithm of the quantization interval is (VFS/ADC bits), and after calculation, I take 15.625*10^-3V.

The Saturation module determines its upper limit and lower limit, which ranges from (-4*Vq)~(+4Vq), and is calculated to be -62.5mV to 62.5mV.

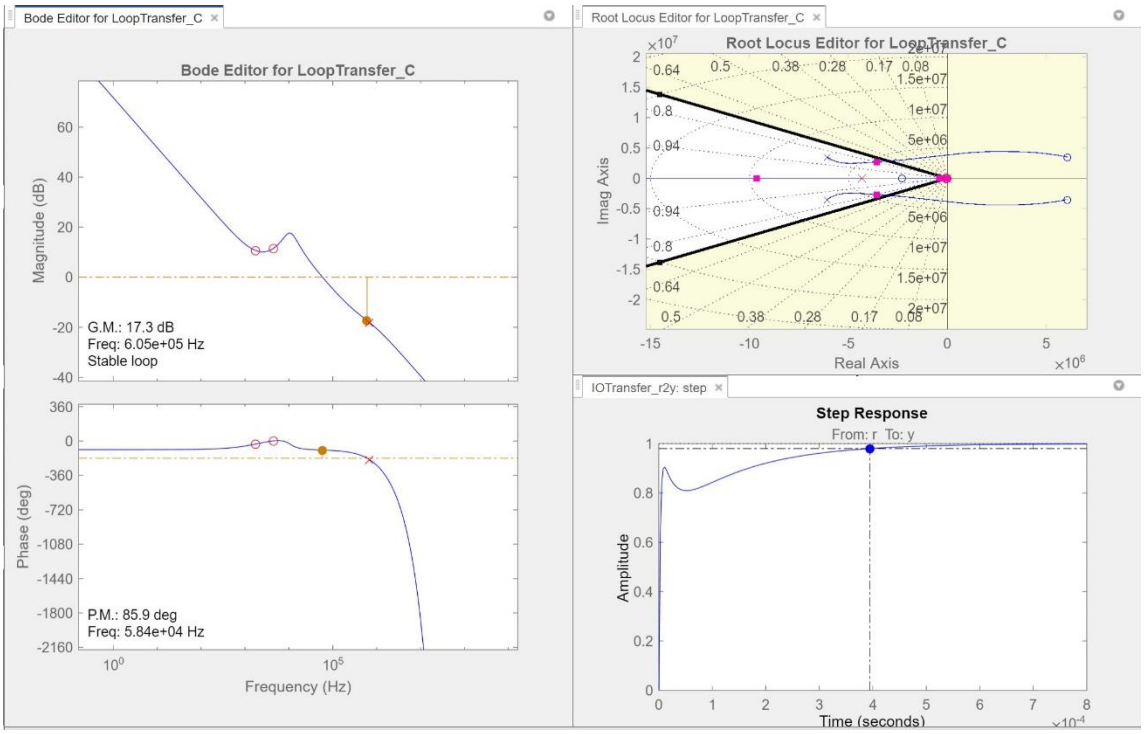
ii. DWPM:

DWPM design, DWPM has a number of bits of 9bits, and the quantization interval is designed.

B. Digital compensator design

i. Design by Emulation

In this step, the compensator meets the specifications, firstly, place the pole and zero point in the original converter considering loop delay and adjust it to meet the system specificationsonsttraints.



Then, send the designed compensator data back to MATLAB for s-to-z conversion, and add the prewarp instruction to the MATLAB code to get the form of the z-domain transfer functionp rewarp directive used by atlab:

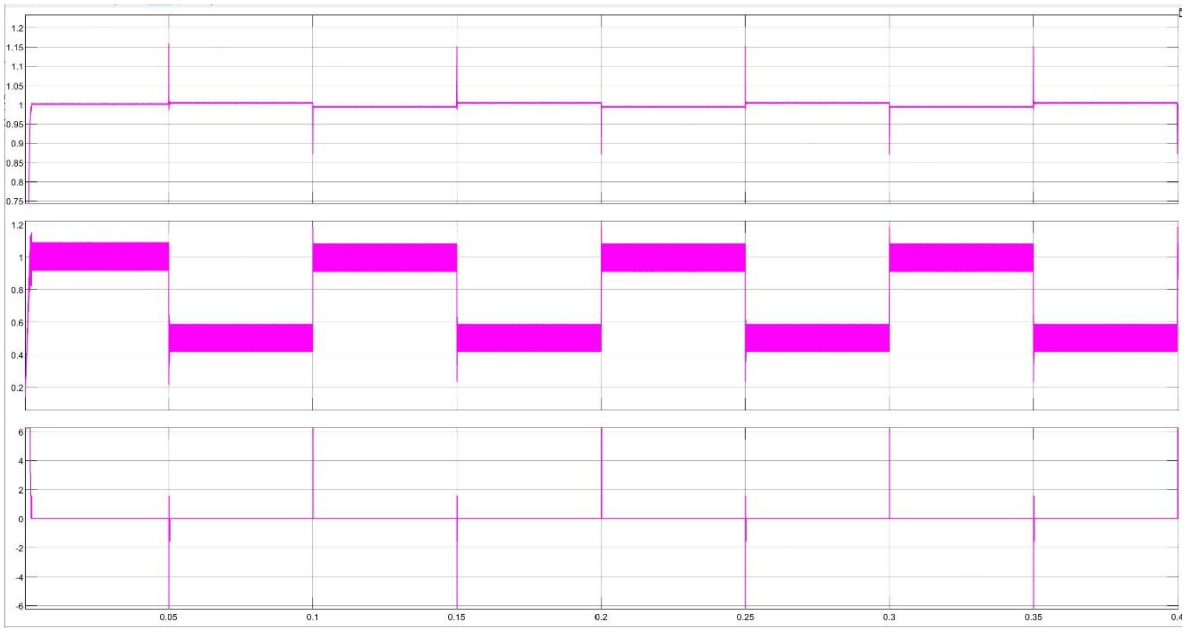
```
>> c2d(C,2e-6,'prewarp',360026)

ans =

  10.566 (z-0.9425) (z-0.9771)
  ----------------------------
        (z+0.6367) (z-1)

Sample time: 2e-06 seconds
Discrete-time zero/pole/gain model.
```

C. Digital buck converter closed-loop simulation (including power stage, ADC, PWM and compensator).

i. Design by Emulation

The following are the time-domain results for the overall waveform, steady-state, and instantaneous after closed-loop simulation:

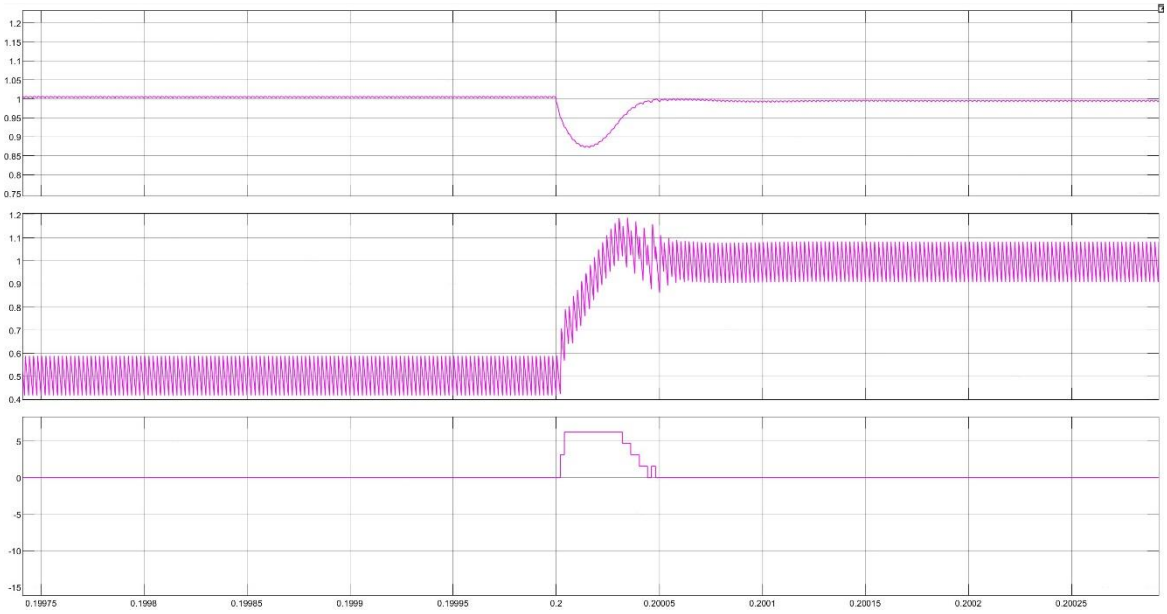
- Overall waveform:



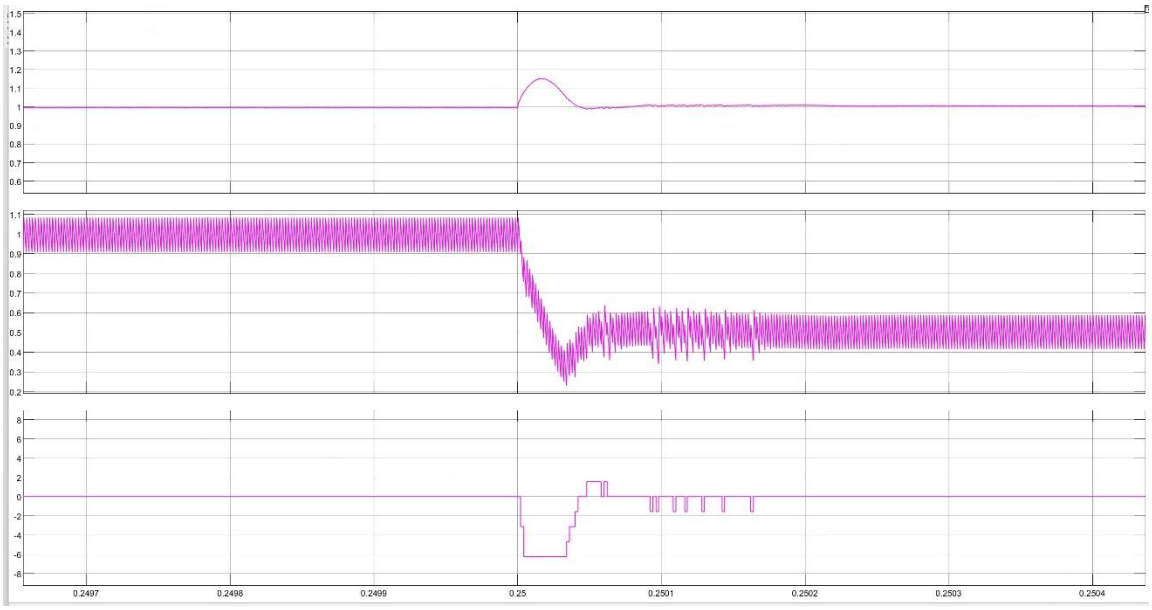
Overall waveform

The figure above shows the overall waveform, and it can be seen that the current is between 0.5A and 1A.

- Instantaneous waveform :

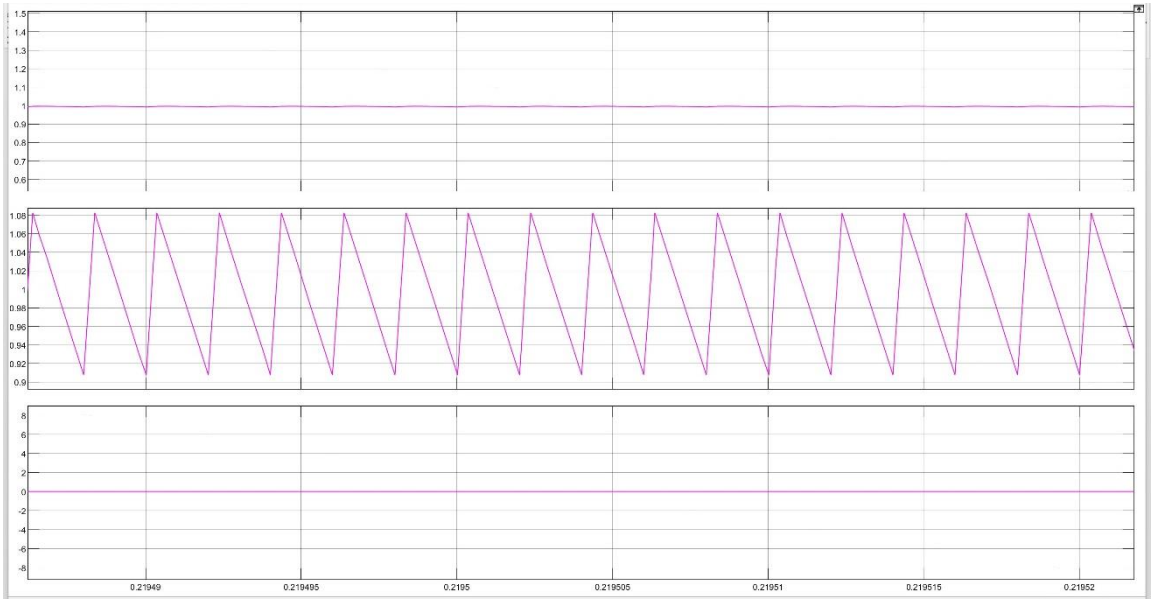


Transfer from Light load to heavy load

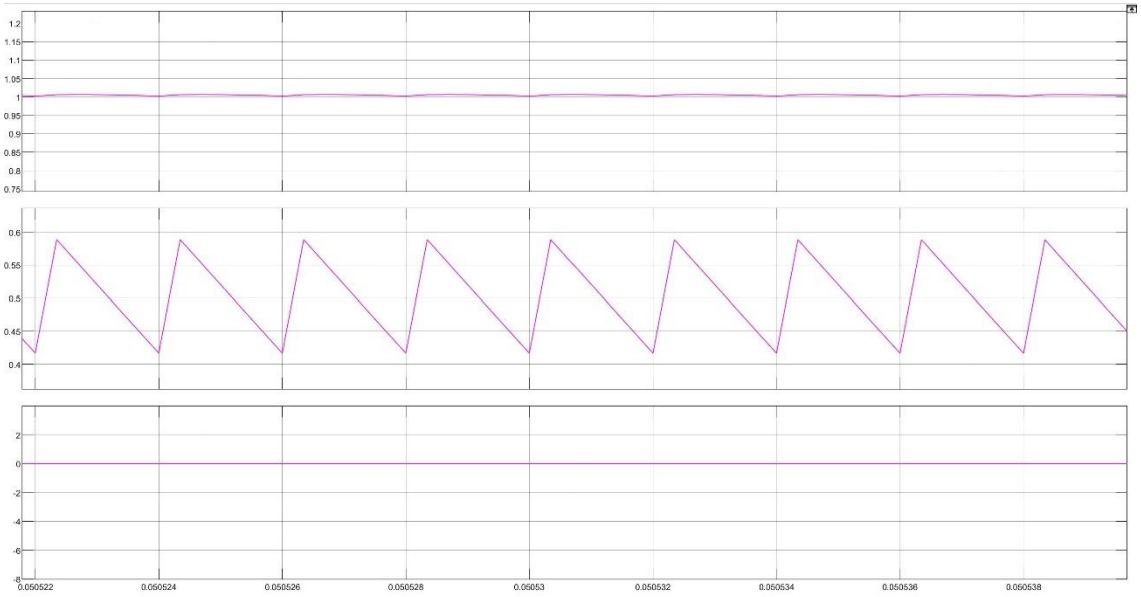


Transfer from Light load to heavy load

The above figures are the results of transferring the light load to heavy load and heavy load to light load, respectively, and it can be seen that the change of waveform is in line with expectations.



Steady-state: 1A

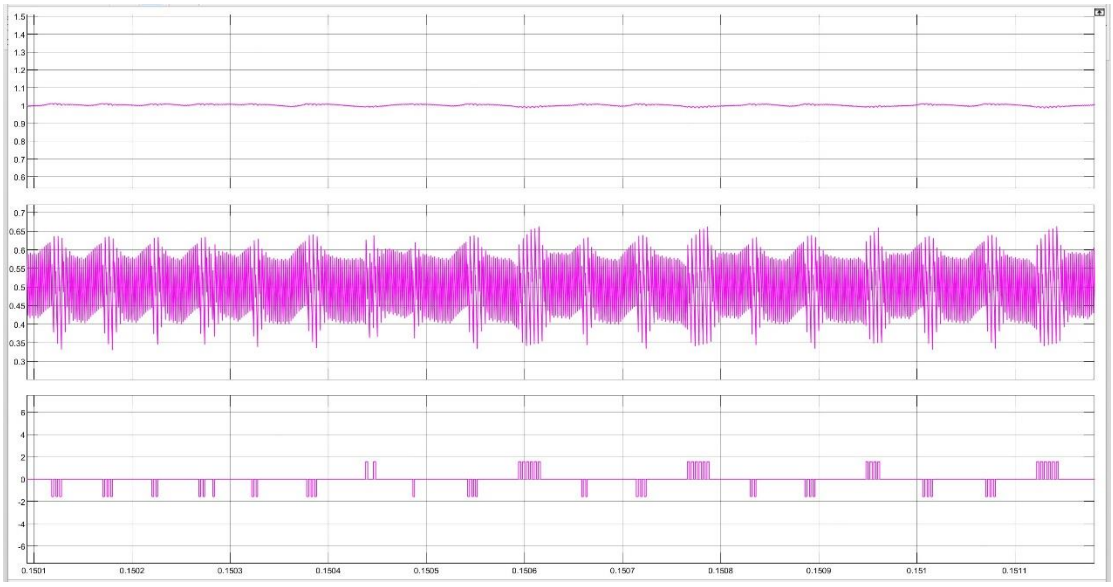


Steady-state: 0.5A

The diagram above shows the steady-state waveform with currents at 1A and 0.5 A, respectively.

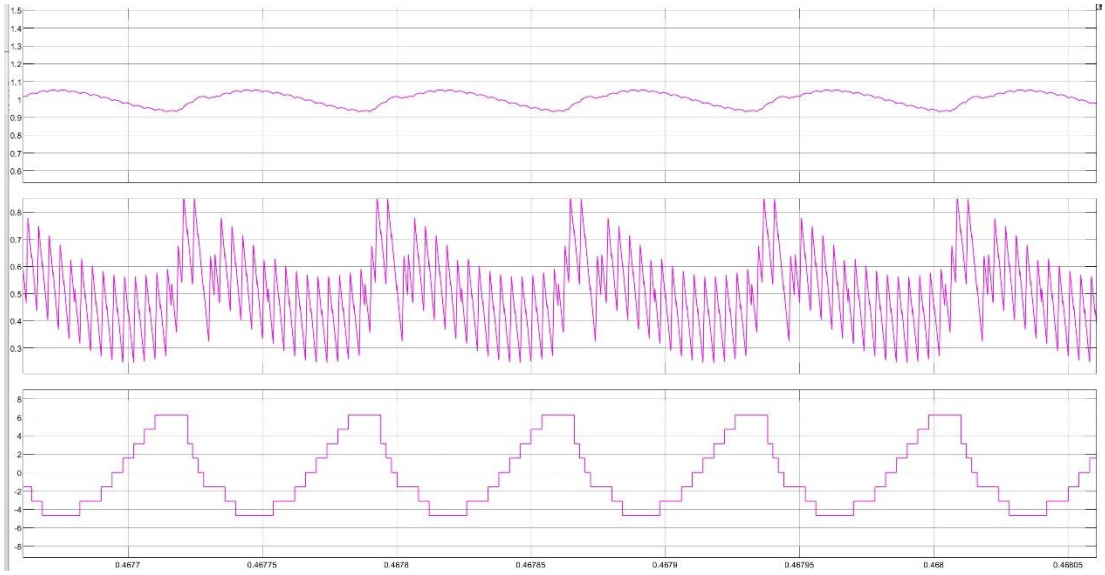
D. Violation of LCO simulation

i. A1



To simulate the LCO A1 situation, you only need to reduce the number of bits of DWPM, and I adjusted the original calculation of 9 bits to 5 bits to generate the above waveform diagram.

ii. A2



The above figure shows the waveform of the LCO A2 violation case, A2 case is that the compensator has no effective limit, resulting in the instability of the control system, so to simulate the LCO A2 case, it is necessary to increase the gain, I adjusted the gain to twice the original design to produce the above waveform.

2. Submission information

A. Implementation report document (Report.docx).

B. Power stage and compensator transfer function Matlab file (.m).
DBE.m

C. Simulink file (.mdl).
Model.mdl