FPGA Verifiaction

One. Brief introduction

In this practice, the previous practice content is burned to the FPGA board, and the practice specifications are the same as before, with an input voltage of 6V and an output voltage of 1 V. The FPGA analog digital compensator part is used with the actual external circuit board to represent the power stage and ADC.

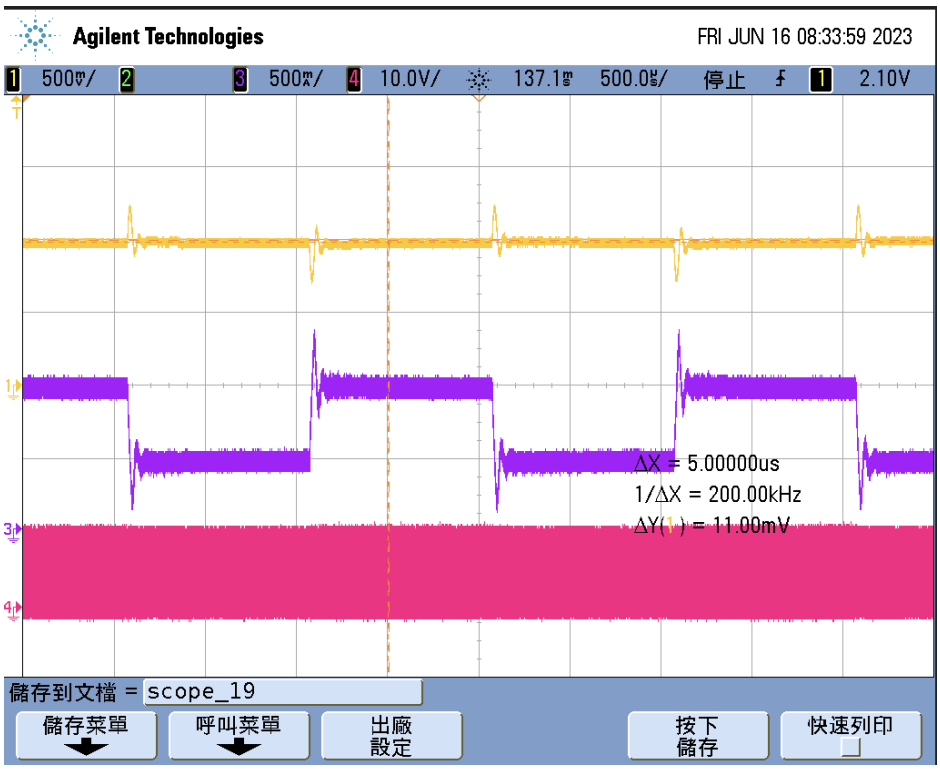
Two. Implementation steps

Before pouring into the FPGA board. First of all, we need to use the Quartus software to convert the previously completed Verilog code into a .sof file, and the following is the detailed practical process:

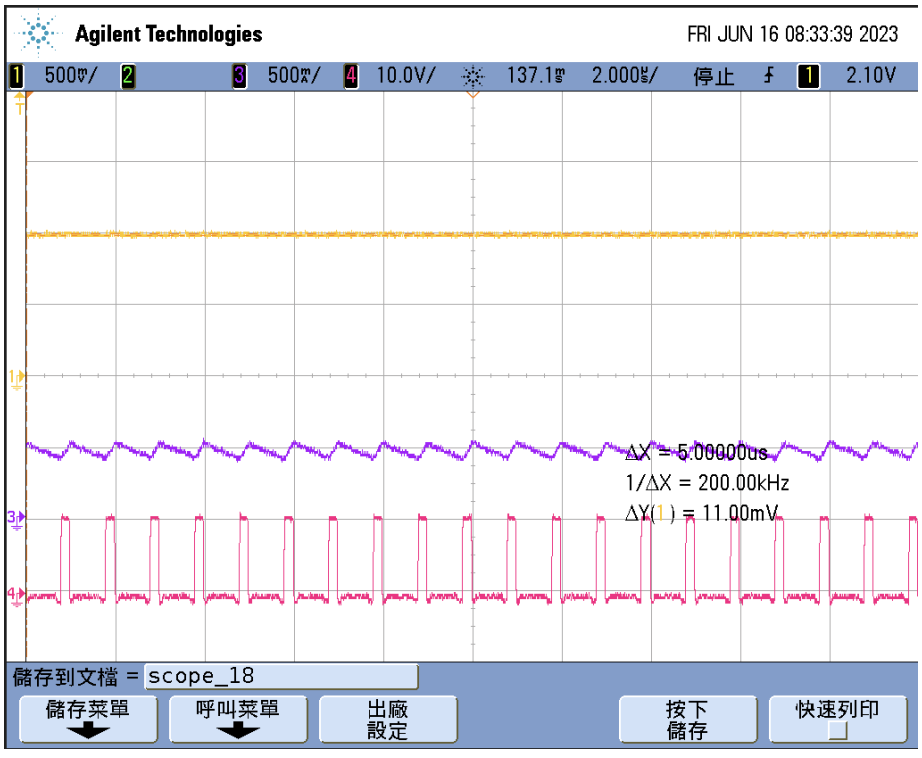
1. Build a new project first and put it all ...V gear added
2. Complete the settings for Family and Devices
3. Set the built-in PLL: Set the clock frequency and add it to the project.
4. Change the top c lk of the top module to the i nclk generated by the PLL module
5. Start compiling and review the results. The relationship between the modules can be confirmed through the RTL Viewer
6. Pin pin as assign action, this step is performed in the pin planner in Assignments, and the datasheet is compared.
7. Finally, the generated .sof file is poured into the FPGA through the settings of Add Hardware and Auto detect
8. Finally, after turning on the instrument in the correct switching sequence, the measurement is started, and the result section diagram is saved to the flash drive

Three. Measurement results

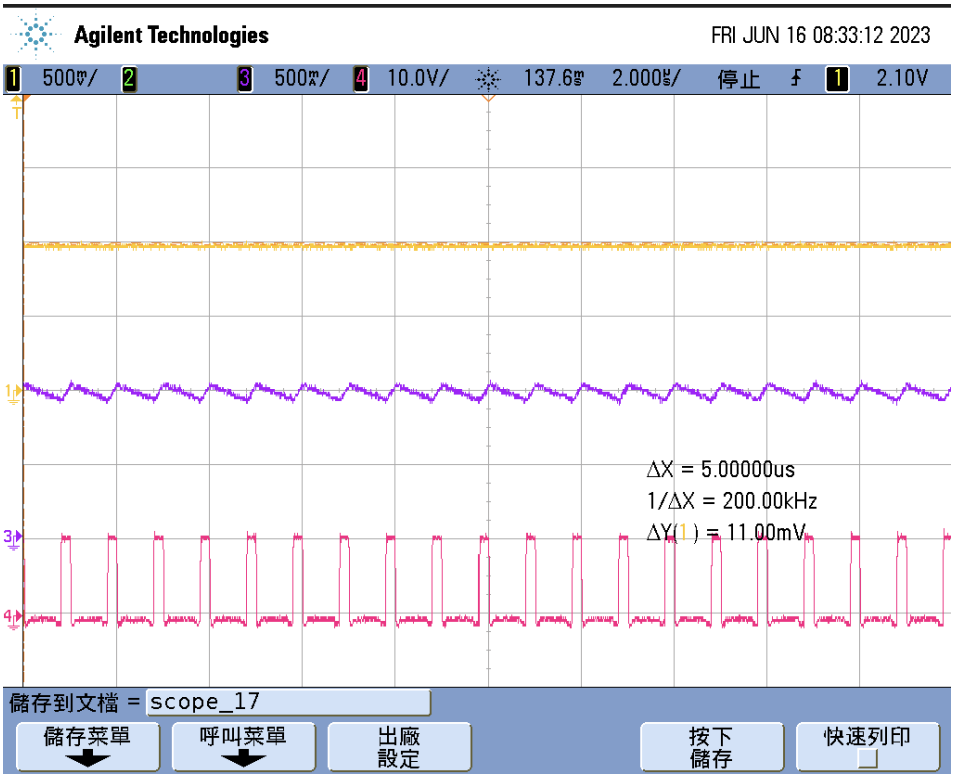
The following is a waveform diagram of the measurement results, which is divided into the overall waveform, steady-state and instantaneous parts.



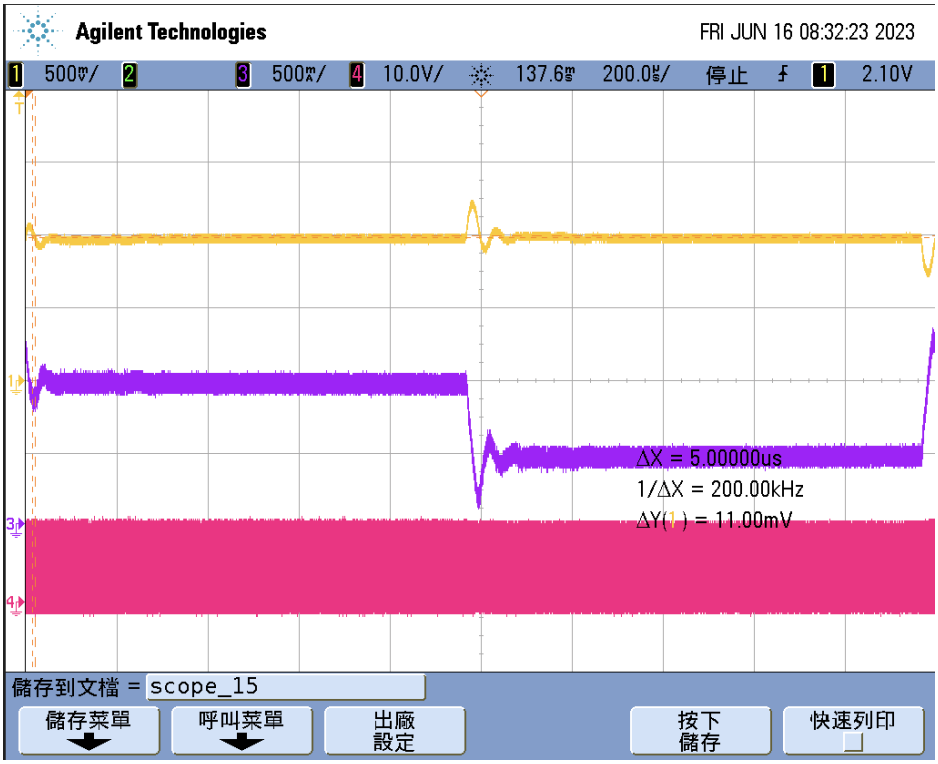
Overall waveform



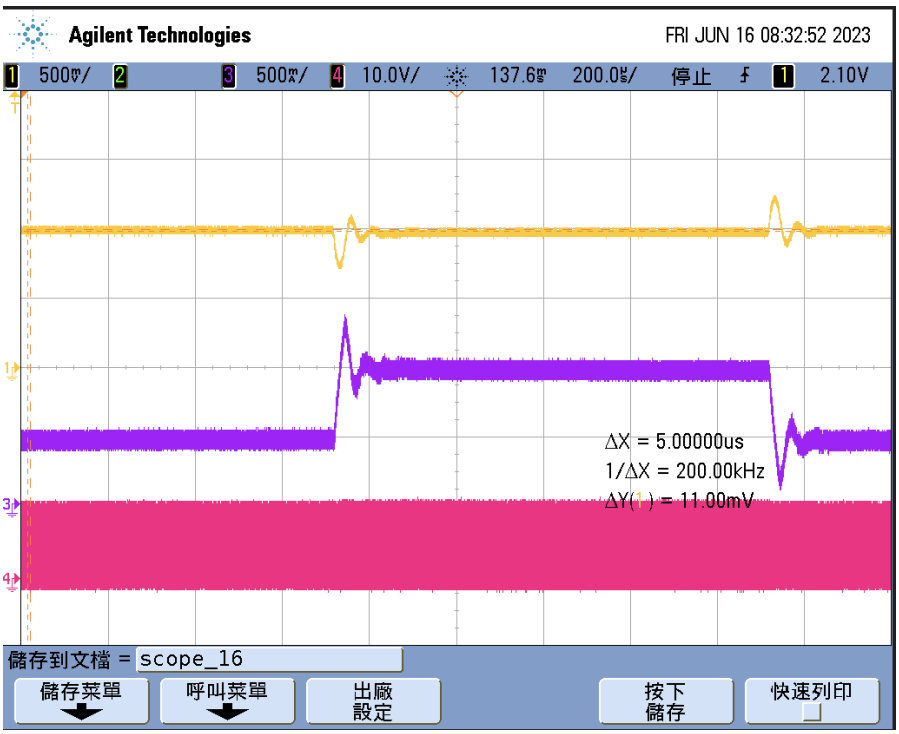
Steady-state 500mA



Steady-state 1A



Transfer from heavy load to light load



Transfer from light load to heavy load

From the above waveform diagram, it can be seen that the steady-state waveform part is verystable and correct at 5 00 mA and 1 A. The instantaneous waveform pattern shows that it is very stable in switching between heavy and light loads, which meets the design specifications.