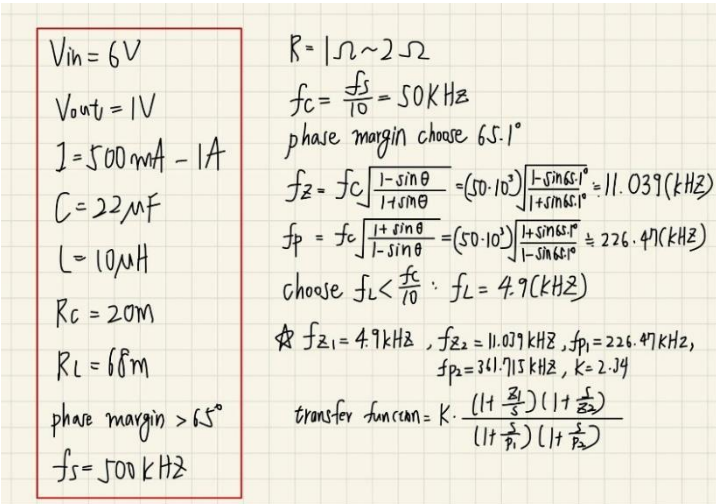
Analog Voltage Mode Buck DC-DC Converter Report

1. Analog compensator design

   i. A hand-calculated compensator

   A. Description of design considerations

      Set values such as L, C, RL, Rload, and R c according to the specifications to obtain the original uncompensated curves, and then obtain pole and zero through the formula, and the following is the calculation process



$V_{in} = 6V$

$V_{out} = 1V$

$I = 500mA - 1A$

$C = 22\mu F$

$L = 10\mu H$

$R_C = 20m$

$R_L = 68m$

phase margin > 65°

$f_s = 500kHz$

$R = 1\Omega \sim 2\Omega$

$f_c = \frac{f_s}{10} = 50KHz$

phase margin choose 65.1°

$f_z = f_c\sqrt{\frac{1-\sin\theta}{1+\sin\theta}} = (50\cdot10^3)\sqrt{\frac{1-\sin65.1^\circ}{1+\sin65.1^\circ}} = 11.039(kHz)$

$f_p = f_c\sqrt{\frac{1+\sin\theta}{1-\sin\theta}} = (50\cdot10^3)\sqrt{\frac{1+\sin65.1^\circ}{1-\sin65.1^\circ}} \doteqdot 226.47(kHz)$

choose $f_L < \frac{f_c}{10}$ ∴ $f_L = 4.9(kHz)$

☆ $f_{z1} = 4.9kHz$, $f_{z2} = 11.039kHz$, $f_{p1} = 226.47kHz$, $f_{p2} = 361.715kHz$, $K = 2.34$

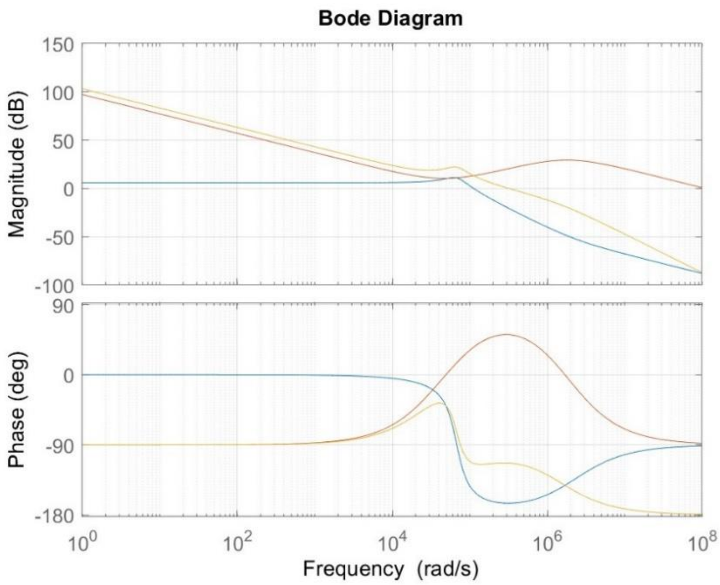
transfer function $= K\cdot\frac{(1+\frac{z_1}{s})(1+\frac{s}{z_2})}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})}$

   B. Simulation Description

      When you are done, you can click run to generate a waveform

   C. outcome

      As shown in the figure below, the dark blue line is the waveform before compensation, the red line is the compensator waveform, and the yellow line is the waveform after compensation



ii. Compensator Obtained Using SISOTool

A. Description of design considerations

Import the original uncompensated curve into SISOTool, adjust the position of pole and zero, and adjust the gain by pulling it up and down to meet the following requirements

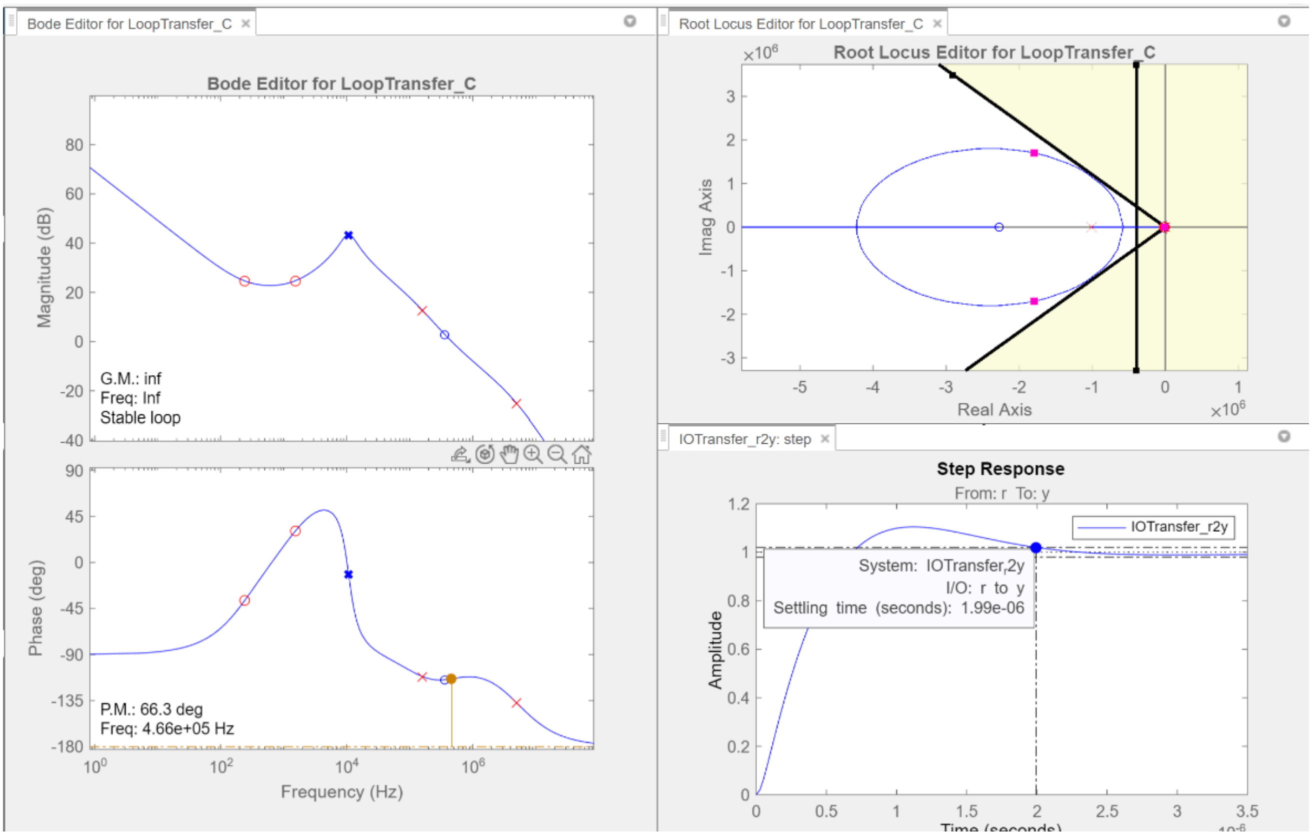
1. Meets the limit of phase margin>65 degrees
2. Meets the limits of damping ratio >0.7 and settling time <10us (Root locus and step response)

B. Simulation Description

Right-click in the root locus diagram and select design requirement-edit to adjust the damping ratio and settling time limits, set the step response by right-click characteristic-check settling time to view the current settling time, and view the current phase margin in the lower left corner and fc. Finally click C in the controller and fixed blocks in the upper left corner to view the transfer function of the complete compensator.

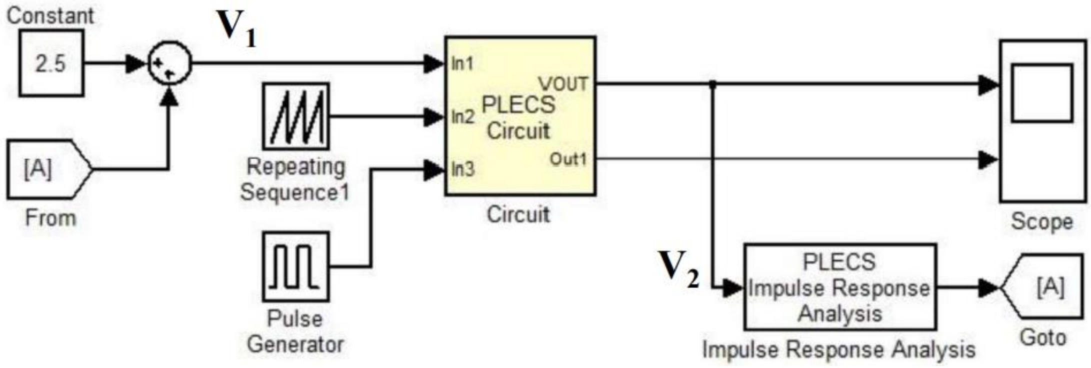
C. Outcome

As shown in the figure below, you can see that the upper left and lower left images are the adjusted magnitude waveform and phase waveform, while the upper right is the root locus and its limitations (need to be designed in the white area)and the step response graph in the lower right corner (you can see whether it is converging or not and the settling time)



2. Buck converter open loop simulation (power stage, PWM only).

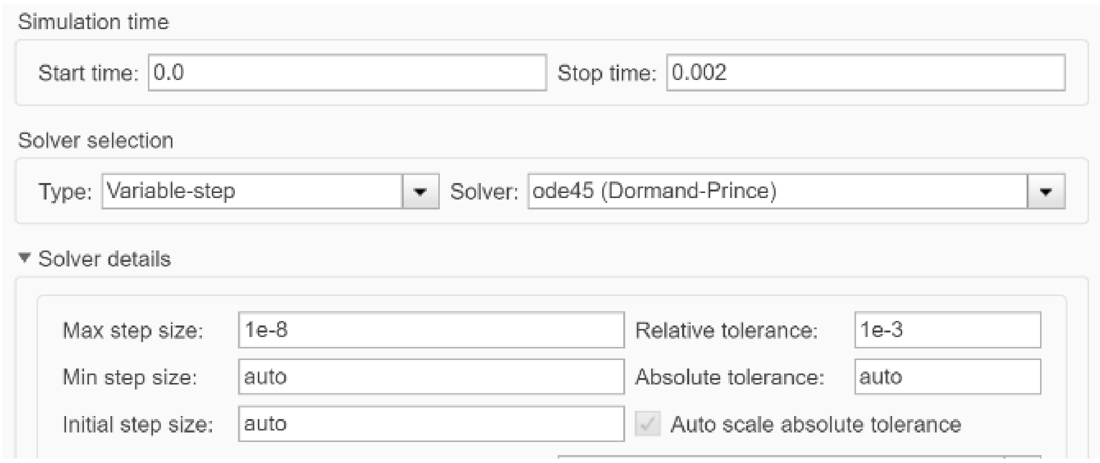
A. Description of design considerations



According to this figure as the benchmark design, the ideal compensation value is 0.5, but the graph is not very accurate, the adjusted compensation value is set to 0.534, set the model setting, triangle wave and square wave parameters, the following is explained

1. Model setting

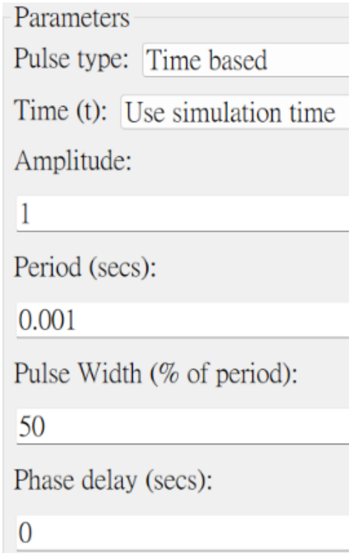
   The Stop time is set to 0.002



2. Triangle waves

   The period is set to 2*10^-6, and the amplitude is set to 3

3. square wave



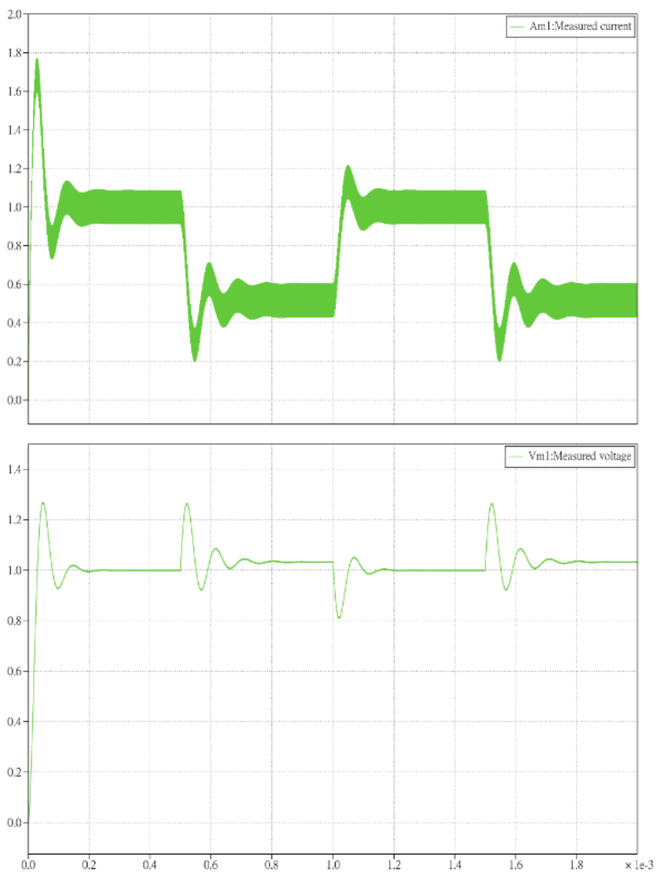
The period is half the time of the simulation

B. Simulation Description

After clicking run, click on the scope in the PLECS circuit to view the voltage and current waveform graphs

C. Outcome

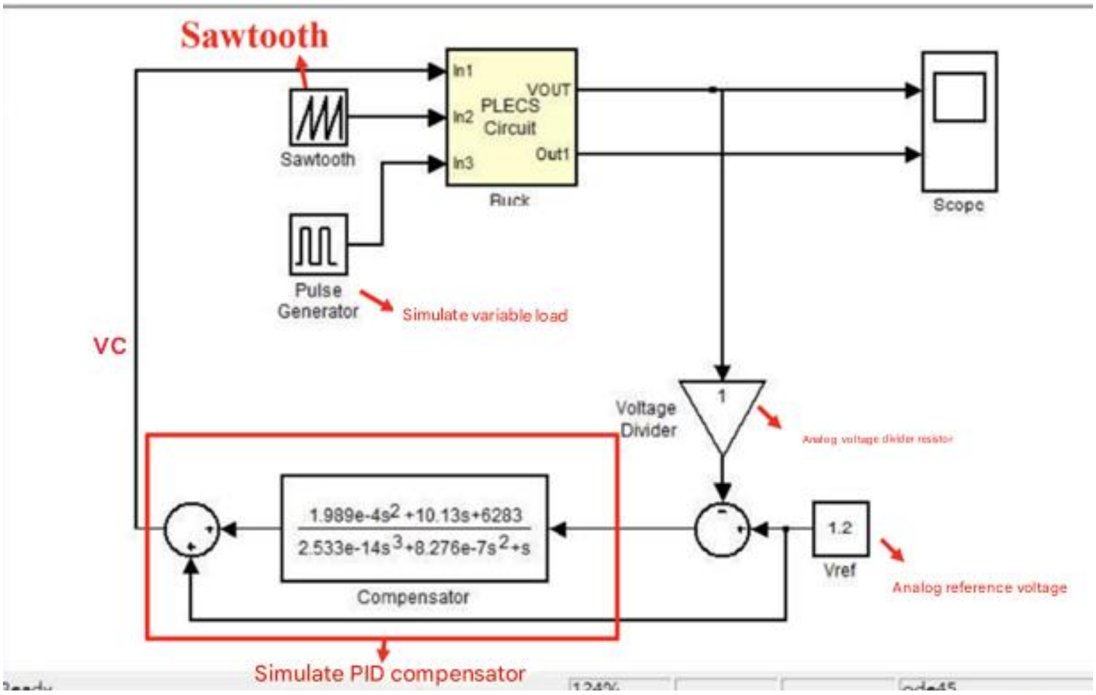
As can be seen in the figure below, the output voltage is 1 and the output current is between 500mA and 1A, which meets the specifications



3. Buck converter closed-loop simulation (including power stage, PWM, compensator).

i. Steady-state

A. Description of design considerations



Based on this diagram, the model setting, triangle wave, and square wave parameters are set in the same way as the open loop

The Compensator part is to input the transfer function into the module of the simulated PID compensator according to the sisotool simulation results, and the following is the transfer function I derived in sisotool

Compensator

$$C = 9025 \times \frac{(1 + 0.0001s)\,(1 + 0.00066s)}{s\,(1 + 1e\text{-}06s)\,(1 + 3.2e\text{-}08s)}$$

After multiplying, click on the PID compensator module to enter the numerator and denominator coefficients in a deciding way as follows

Numerator coefficients:

[5.9565e-04 6.859 9025]

Denominator coefficients:

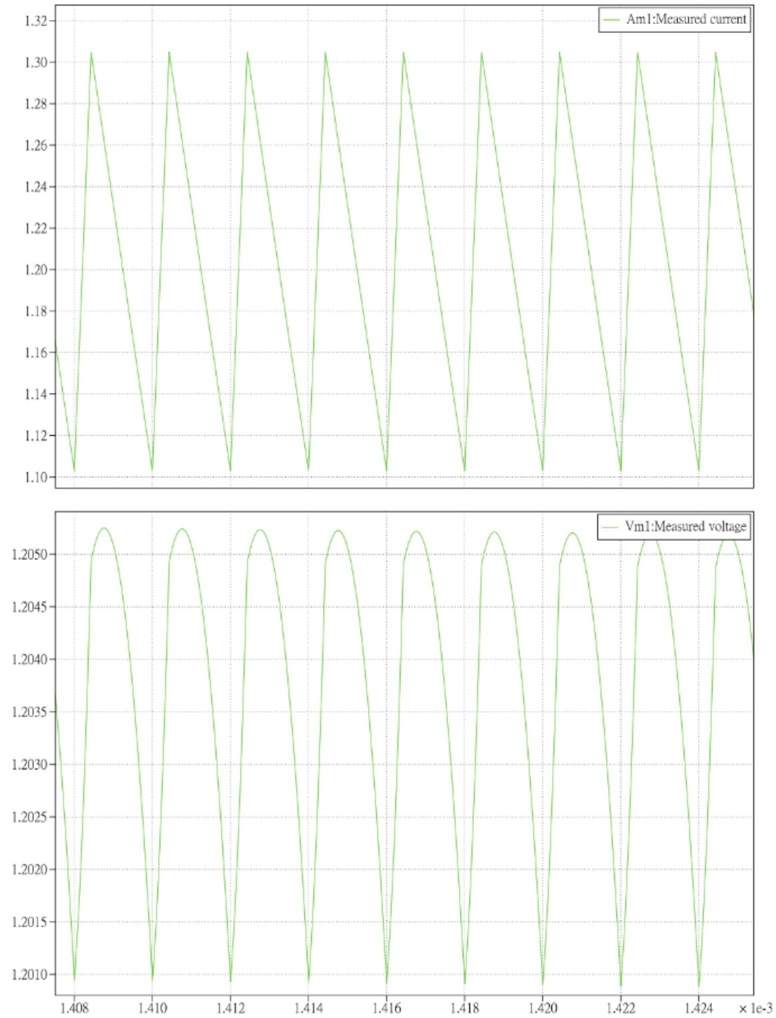
[3.2e-014 1.032e-06 1 0]

B. Simulation Description

After clicking run, click on the scope in the PLECS circuit to view the voltage and current waveform graphs

C. Outcome

As shown in the figure below, the normal convergence of the wave line shows the accuracy of the steady-state result



ii. Transient-switching

A. Description of design considerations

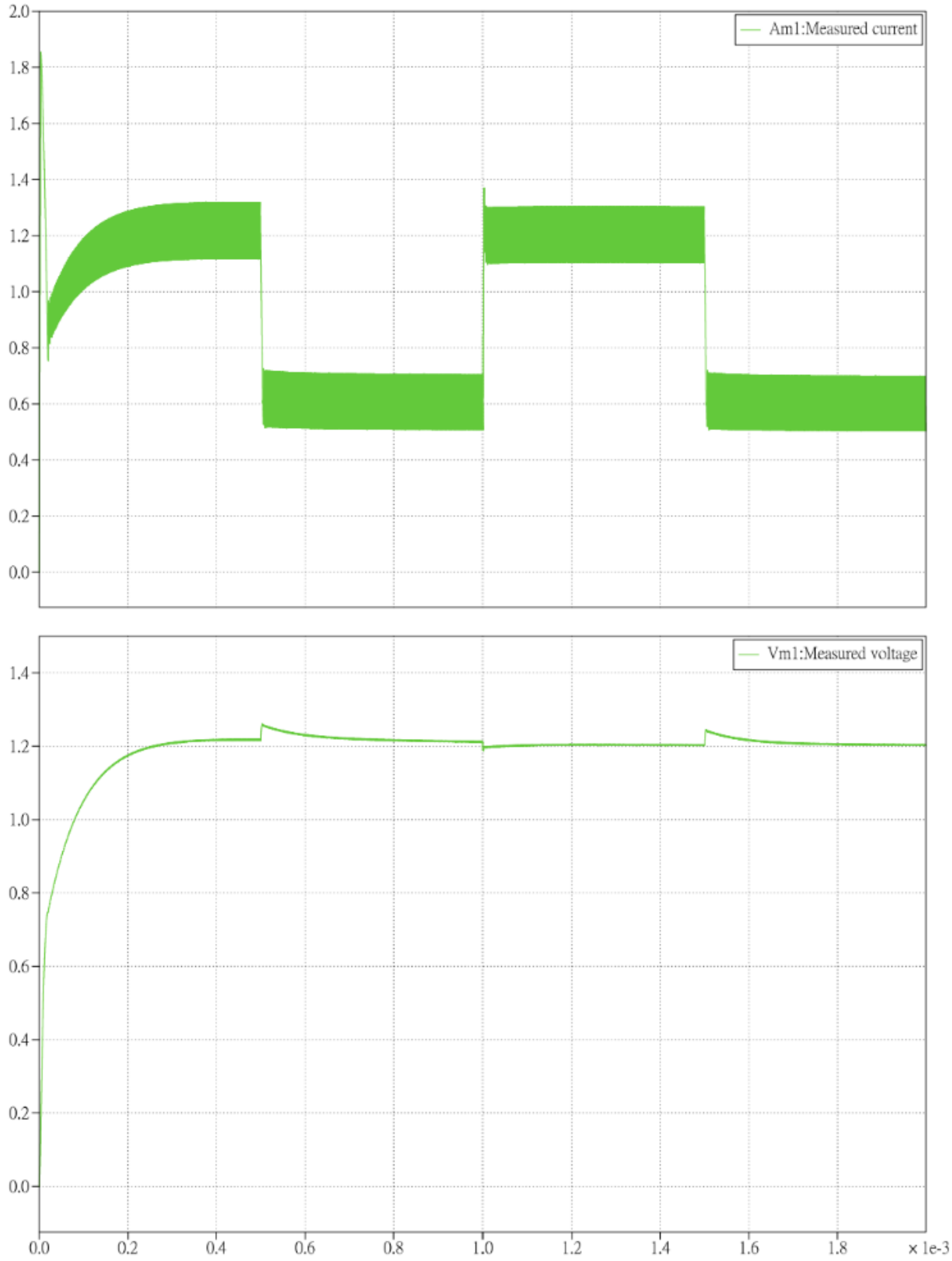
In fact, it was originally set to see the instantaneous need to adjust In3 (square wave), because its period is preset to 1. If there is no adjustment, it can only show a steady-state result, and after adjustment, you can see the change of voltage and current between the switch ON-OFF. But because the parameters of I n3 (square wave) have been adjusted during the steady state, there is no need to adjust the model The settings, triangle waves, and parameters are the same as in the previous experiment)

B. Simulation Description

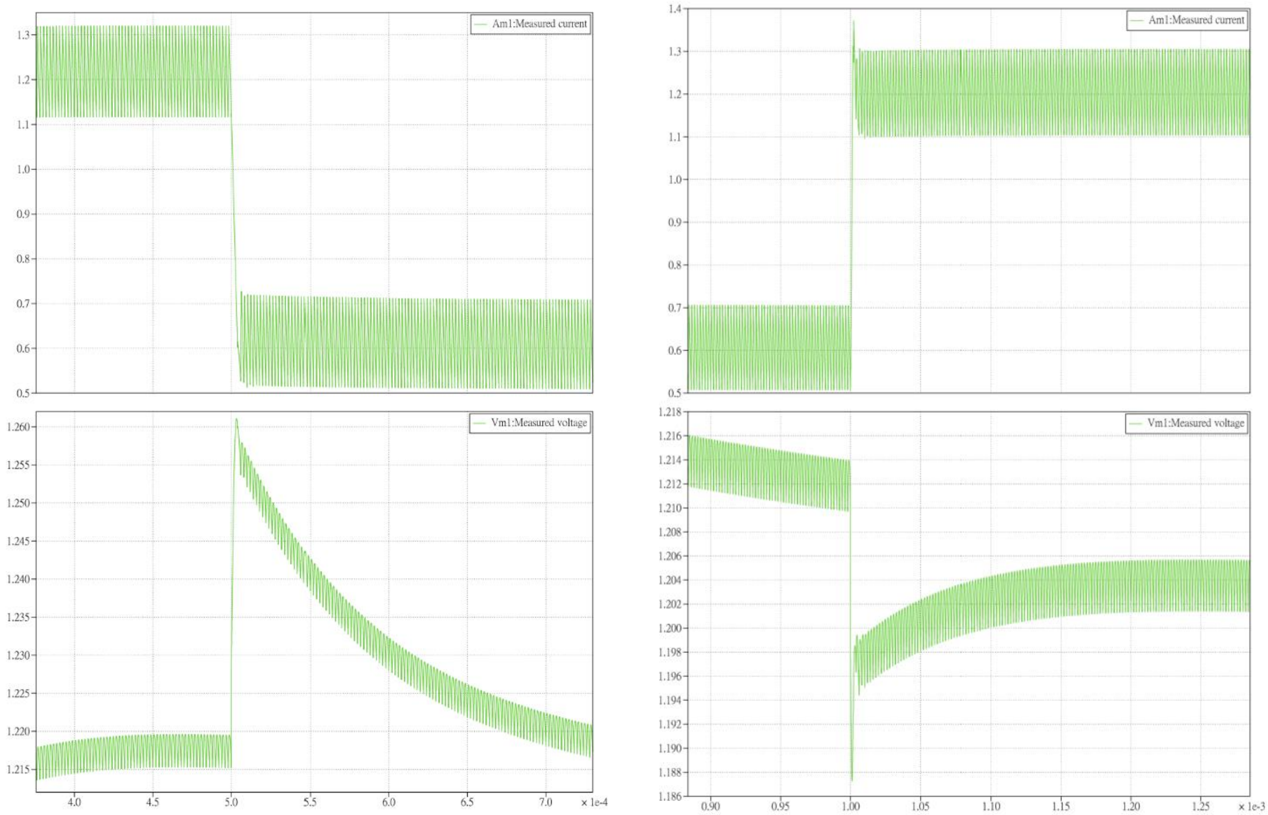
After clicking run, click on the scope in the PLECS circuit to view the voltage and current waveform graphs

C. Outcome

As shown in the figure below, you can see the changes in voltage and current when switching ON-OFF



These two graphs show the change in waveform when switching on and switching off is magnified



4. Submission of information

1. Report Document (Report.docx).
2. Power stage and compensator transfer function Matlab file (. m)
   compensator.m
3. Simulink file (.mdl)
   close_circuit.mdl
   open_circuit_mdl