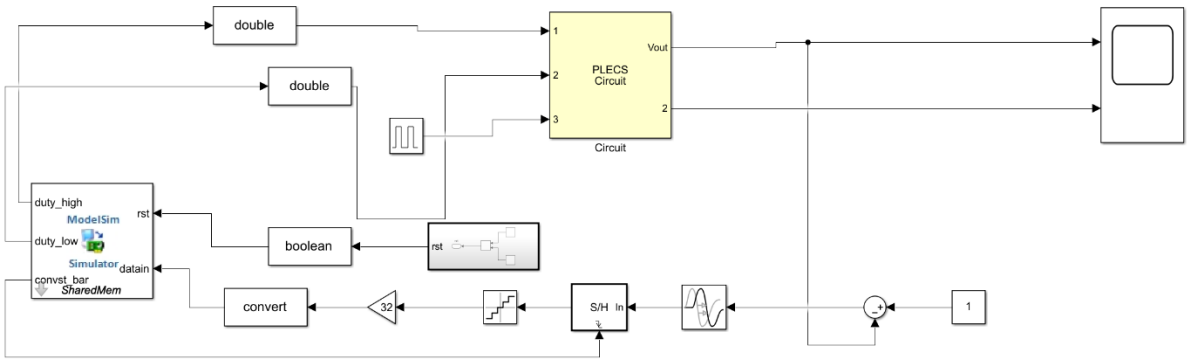
ADC Encoder Report

1. Implementation Report

A. ADC encode considerations

The function of ADC encoder is to replace the module of the original ADC limits. First, calculate the ADC output when the input voltage is 1V. The ADC range is between 0 and 255, it is found that the position of 1V corresponds to the ADC input of 128 after proportional calculation. Take the position where the ADC input is 130 as zero, and the deduce +4~-4 by adding or subtracting four

B. Digital buck converter closed-loop simulation

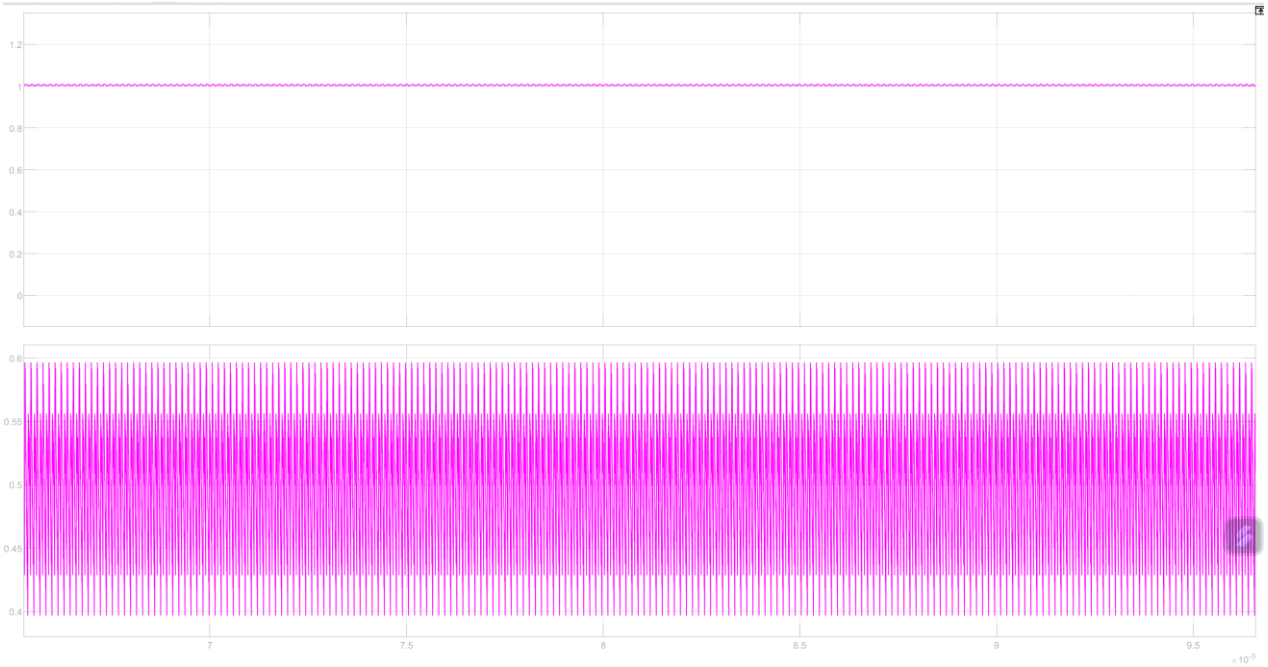


This lab is mainly to combine the design results of previous labs with top, and add ADC encoder, the above is my wiring diagram, and then explain the considerations of my modules in the design:

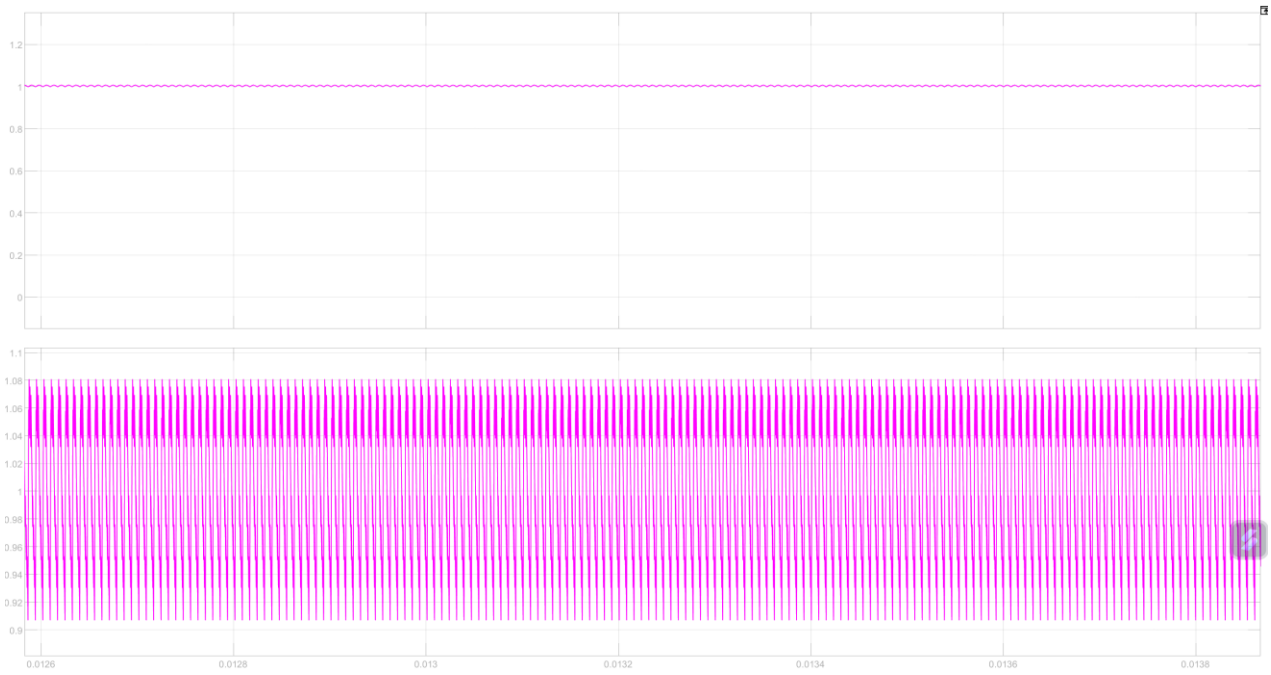
1. ADC: Mainly to change the sample control module type (Sample and Hold) designed before, and change the trigger type to falling edge.
2. Data type conversion: Change the output data type of the convert to 8bits
3. HDL Co-simulation: This module is equivalent to PID compensator, Dither DPWM, Encoder and Clk divider After the signal autofill is in, the sample time of output is set to 4e-9, the same as the previous lab, and considering that the counter is 6bits, The frequency is 64MHz, so after calculating its reciprocal, 15e-9 is chosen as the period of clock
4. Quantizer : Since the specification is 8 bits, the quantization interval needs to be changed to 7.8125e-3
5. Power stage: Remove the comparator and not gate from the PLECS circuit, and leave the rest of the components unchanged.
6. Constant : If not adding constant, the value of the voltage will be doubled, so constant must be added.

7. The design of the other modules has not changed much from previous experiments

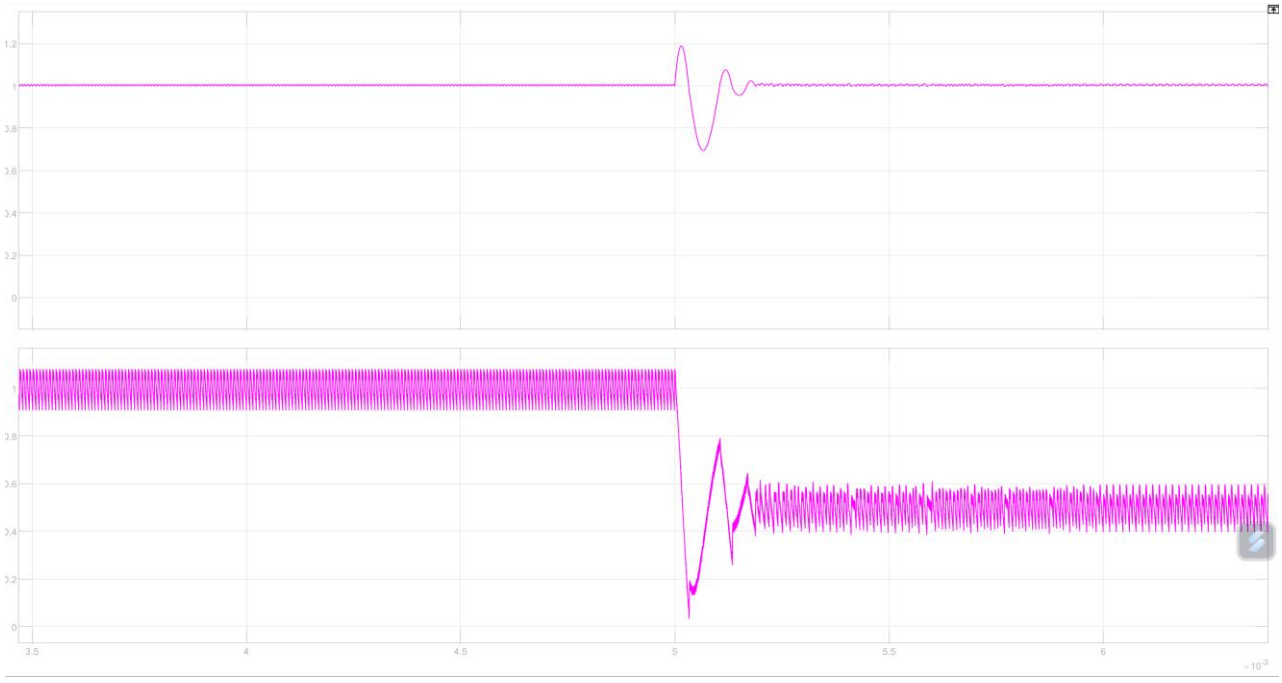
The results are presented, which are divided into four parts: steady state (1A), steady state (0.5A), transfer from heavy load to light load and light load to heavy load.
The result shows that the voltage waveform oscillates around 1V, and the current ripple wave is 1 for heavy load and light load respectively switching between 1A and 0.5A, which meets the specifications.



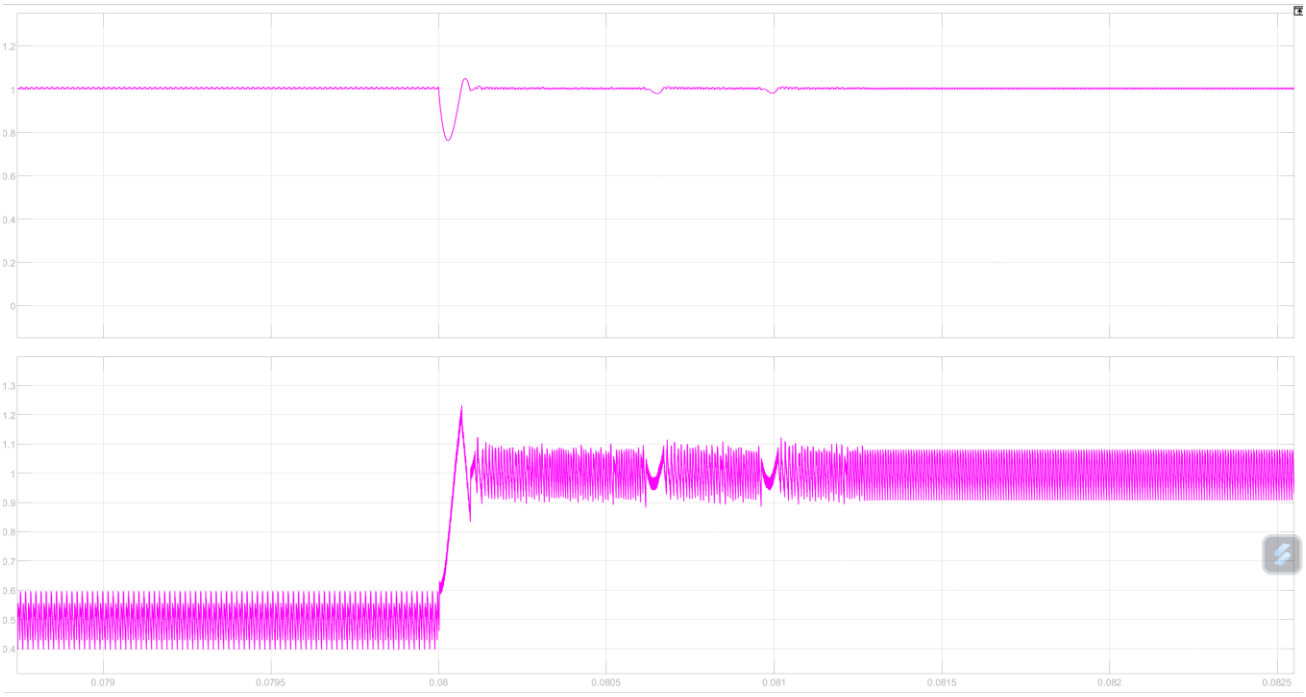
Steady-state (0.5A)



Steady-state (1A).



Transfer from heavy load to light load



Transfer from light to heavy load

2. Submission of information

A. Implementation report document

B. Verilog (.v) file

top.v

clk_divider.v

compensator.v

deadtime.v

dither.v

encoder.v