Digital PID Compensator Implement

1. Implementation Report:

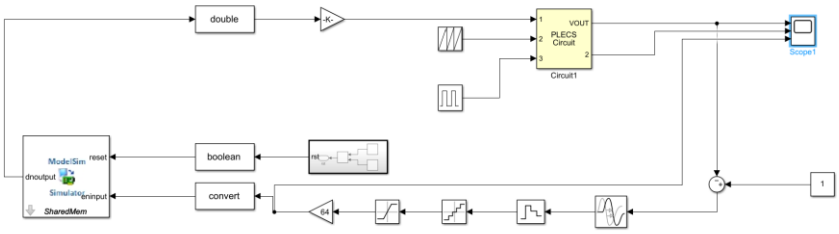
A. Digital compensator quantization

The quantization step is to first convert the compensator coefficients into binary form, and multiply the coefficients with the input results to determinethe number of bits and the internal value of L UT. According to the results of my Matlab execution, when the LUT is 16bits, the specification requirements can be met and the conversion can be successfully completed.

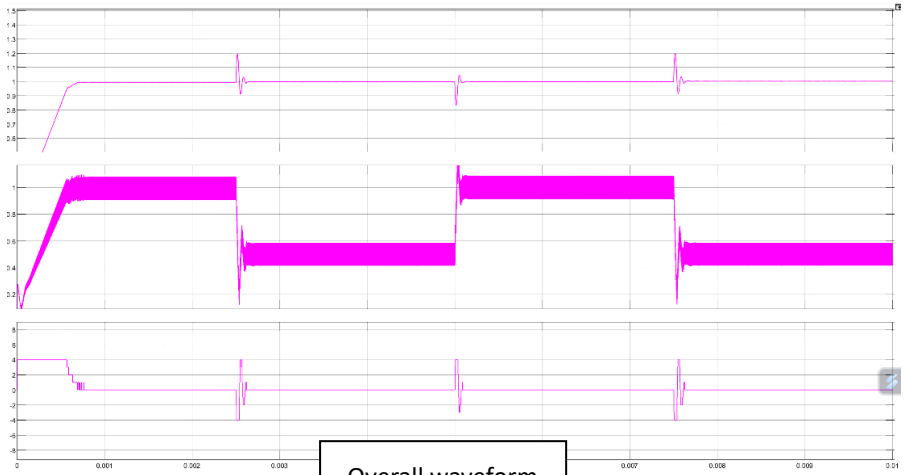
B. Digital compensator hardware description language implementation

According to the results of the matlab execution, build the Verilog code and modulate the integer number to be consistent with the LUT results, and fill in the results in the Look-up-table. Through truncation, the next 6 bits are discarded, so that the output meets the required 9 bits.

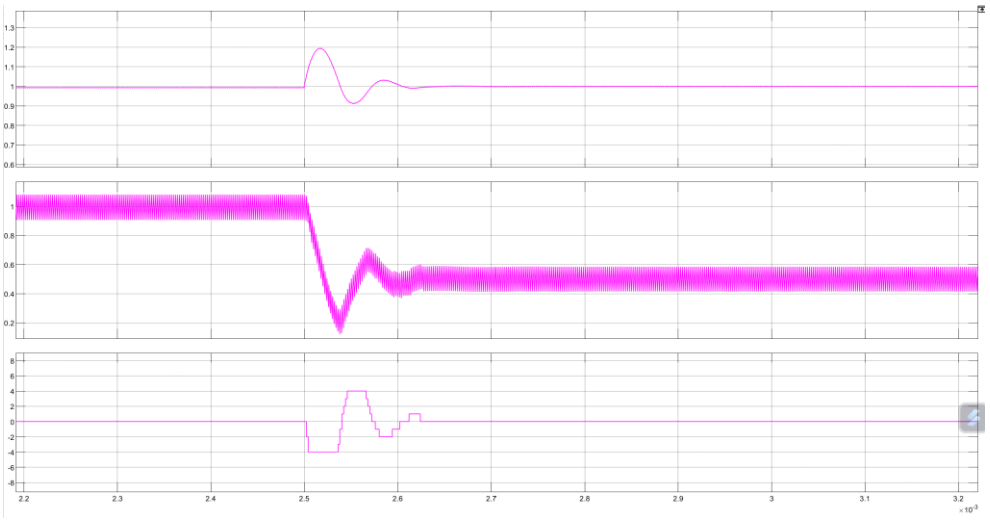
C. Buck converter closed-loop simulation (including power stage, PWM, compensator)



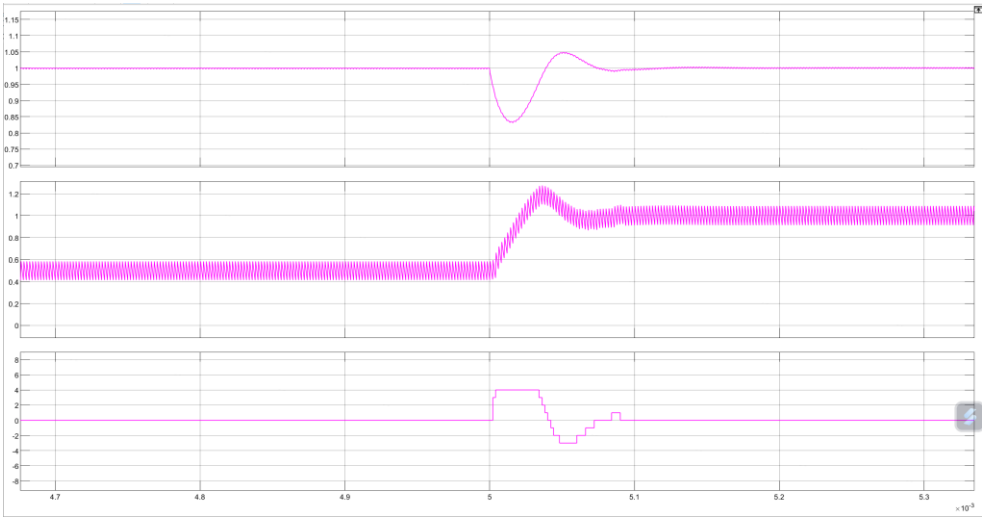
The above figure is the architecture diagram, the implementation method is to autofill the signal into the circuit through co-simulation, and set the sample time to 2*10^-6, and adjust the gain part through the number of bits, and the resulting waveform diagram is as follows



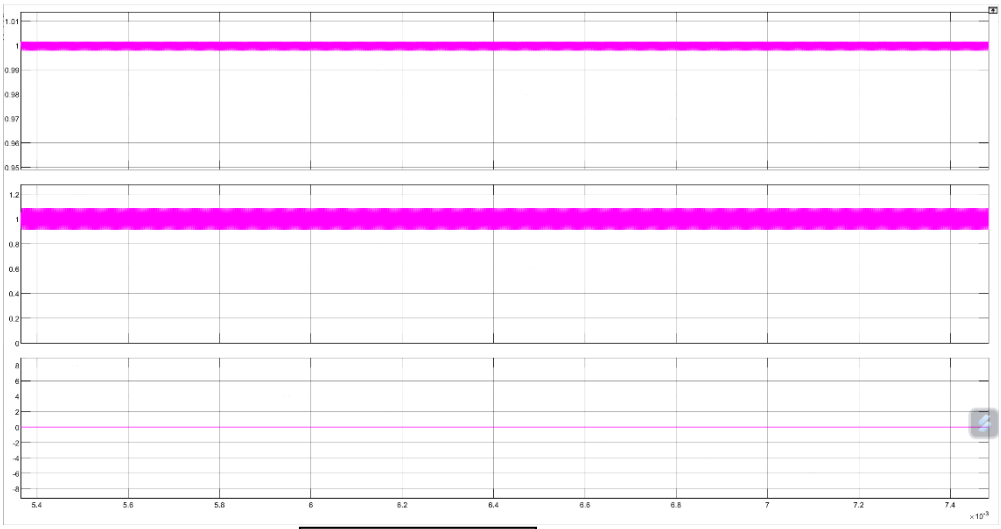
Overall waveform



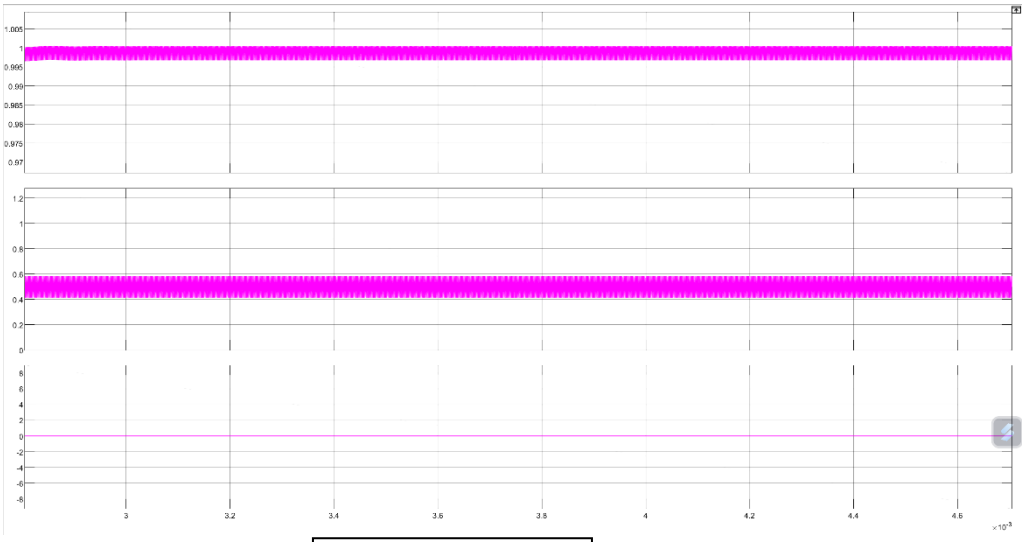
Transfer from heavy load to light load



Transfer from light load to heavy load



Steady-state (1A).



Steady-state (0.5A).

From the above simulation graphs, it can be seen that all the graphs are very similar to the Lab2 graphs. The voltage waveform is stable at around 1V, and the currentswitches between 1 A and 0.5A for heavy and light loads, respectively, all of which meet the system specifications.

2. Submission of information

A. Implementation Report Documentation (Report.docx)

B. Compensator quantization calculation Matlab file (.m).
quantization.m

C. Compensator verilog file (.v).
compensator.v