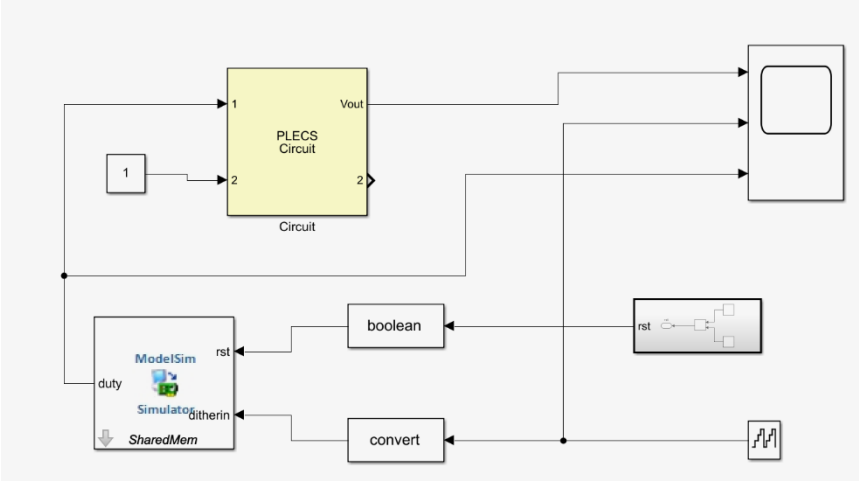
Realization of DPWM Report

A. Counter DPWM

This is the open-loop simulation of 9bits Counter DPWM. The following is my PLECS architecture diagram, I removed the pulse generator, not pump the load first but inputed a constant. When constant is set to 1, it means that the state is heavy-load, and when it is set to 0, it means that the state is light-load. The goal of this implementation is to observe the change of the voltage of each counter, so it is easier to observe without pump the load.



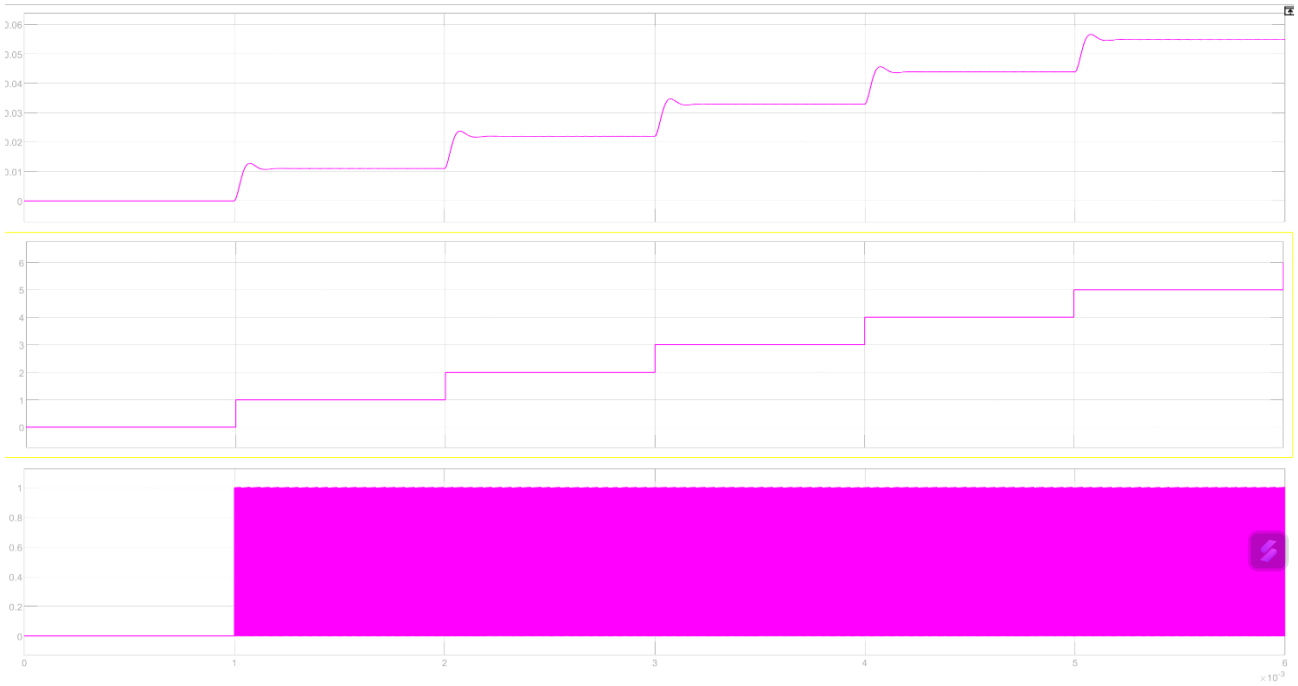
Set up each block:

i. Counter free-running: bits is set to 9bits, and sample time is set to 1e-3

ii. Data type conversion: Change the output data type to fixdt(1,9,0) to meet the requirements of the 9bits specification

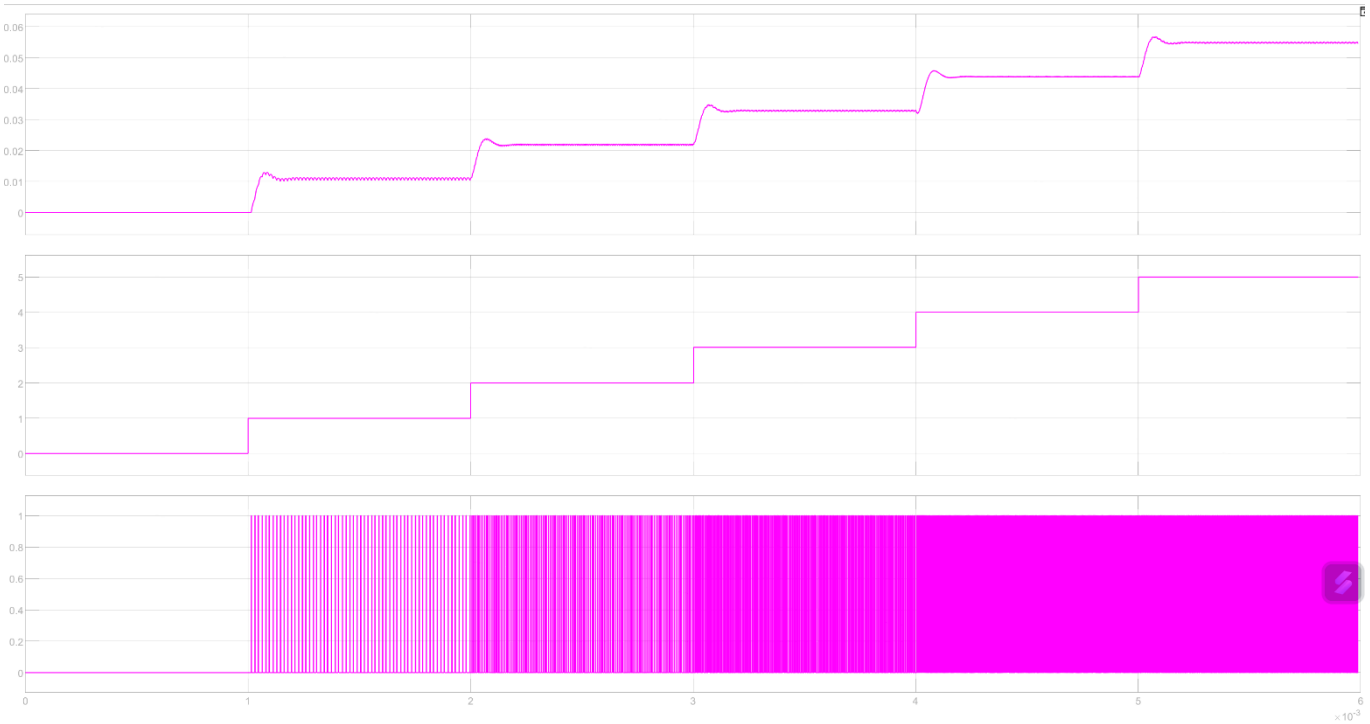
iii. HDL Co-simulation: Add each signal autofill, and adjust the duty sample time and clock period to 4e-9, the algorithm is 1/(2^9*500k), 9 represents the actual 9bits, and 500k is the switching frequency.

The following is a presentation of the analog results, and it can be seen that V rises as the voltage of the digital circuit rises, which is in line with the expected results.



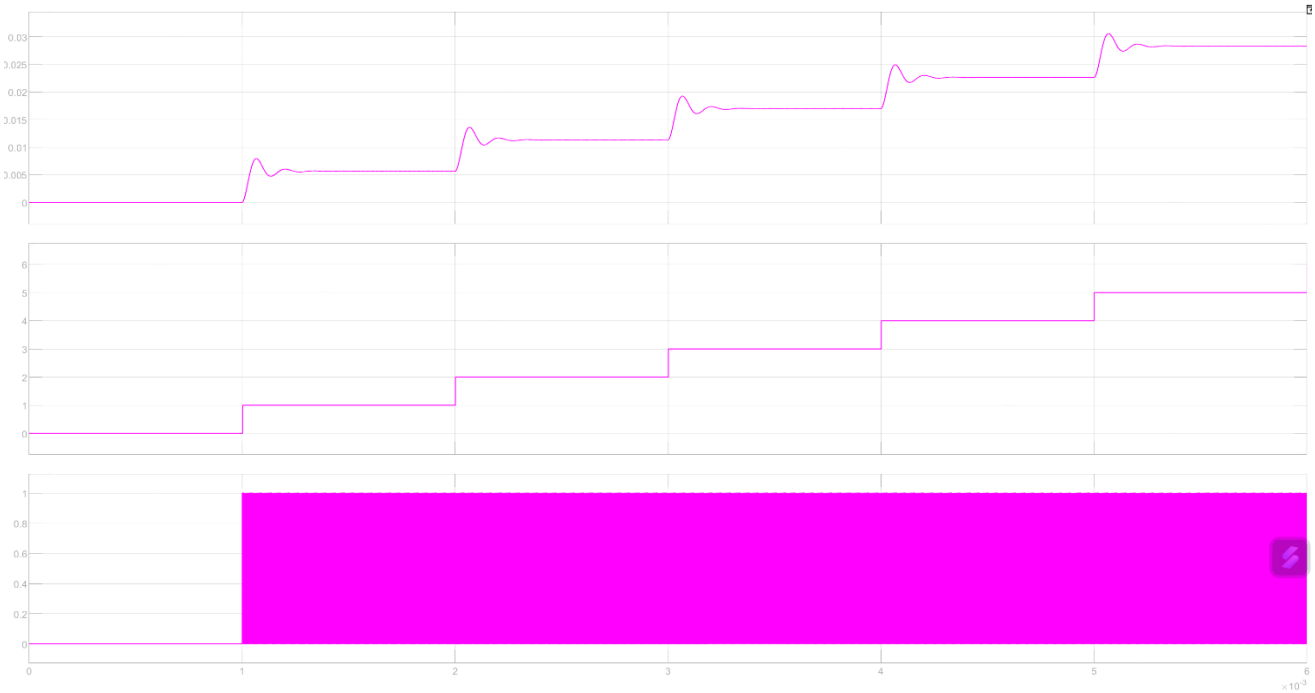
B. Hybrid DPWM

This is a 9bits Hybrid DPWM, which is a mixture of a 6bits DPWM and a 3bits delay line, most of the designs are the same as the previous Counter DPWM, but the clock frequency algorithm is 2^6*500k (because DWPM is 6bits), so the clock period is 32e-9. The part of the Duty sample time was originally set to 4e-9, but later it was found that the rising voltage of every two step waves only rises once, considering that the sample time may betoo long to take samples when each step wave rises, so I used the sample for this part Change time to 2e-9 to work normally. The following are the simulation results, and the waveform plot is also as expected



C. Dither DPWM

This implementation requires the addition of two other modules, dither, and top files. The result is as expected, and the co-simulation is the same as the previous setup. The following is the simulation result, which can be seen, the change in voltage was also as expected.



D. Dither DPWM with dead-time

This module needs to make some changes to the original dither DPWM. First of all, I need to set the output of the top file to the form of duty_high and duty_low, and no need to add counter.v when doing co-simulation, and removed NOT from PLECS circuit and add a new input, change the external cable to divide the output waveform into duty_high and duty_low. The periods of duty_high and duty_low are all 2e-9. The following is the wiring diagram and the simulation results