Bio-signal Noise Reduction Using Switched-Capacitor Filters

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Development Tools: Hspice, MATLAB

I. ABSTRACT

This project develops a switched-capacitor filter system for effective noise suppression in bio-signals, integrating a 4th-order Chebyshev I low-pass filter and targeted notch filters. The design process begins with FFT analysis to identify noise frequencies, guiding precise tuning of Q factors and cutoff frequencies to achieve optimal signal fidelity.

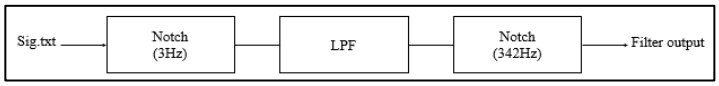


Fig 1. Filter circuit structure

The system incorporates a telescopic operational amplifier designed for high efficiency, featuring a unity-gain bandwidth of 119 kHz and low power consumption through subthreshold operation. Switched-capacitor circuits replace high-resistance components, minimizing circuit area while ensuring performance, with support from a custom non-overlapping clock circuit.

Simulation results demonstrate the system's ability to suppress noise effectively while maintaining high signal integrity and low power usage, showcasing its suitability for bio-signal processing.

II. INTRODUCTION

My goal focuses on designing a low-power switched-capacitor filter tailored for noise reduction in bio-signals. The primary goal is to restore the original signal's integrity while minimizing power consumption and maintaining high accuracy. The design is implemented using a 0.18 µm CMOS process, conforming to strict specifications for capacitance, resistance, and operational amplifier performance. The filter is evaluated using given bio-signal data files, including clean signals, noise-contaminated signals, and signals with DC bias, under a 10 kHz sampling rate.

A. Objectives

1. **Error Minimization:** The error metric is calculated using an error calculation file, which compares the normalized output signal of the filter to the original clean signal. This involves processing only the second half of the signal data, aligning the output signal, and calculating the least square error over a defined range.
2. **Power Efficiency:** The design leverages switched-capacitor circuits to reduce power consumption while ensuring high performance.
3. **Figure of Merit (FoM):** The FoM is derived from error, total capacitance and resistance, and average power consumption, providing a comprehensive measure of design efficiency and performance. It is calculated using the formula:

$$FoM = Error \times log\left(\frac{Power}{1\ nW}\right)$$

B. Design Constraints

1. **Power Consumption:** Minimized through efficient SC circuit design.
2. **Component Limits:** The total capacitance and resistance are restricted to 1 nF and 100 MΩ, respectively.

Before designing the filter, an FFT analysis was performed on the HSPICE-generated signal and the ideal input signal. By comparing the frequency spectra of both signals, the approximate noise frequencies were identified, providing a basis for the filter design.

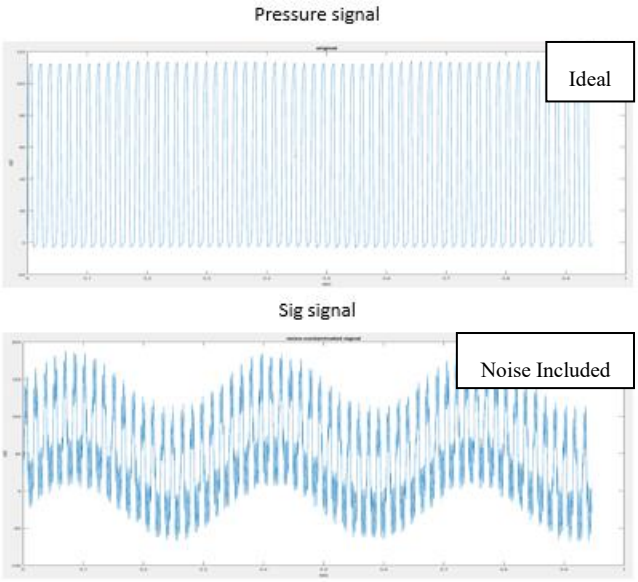


Fig 2. Time domain of the ideal signal and the signal with noise

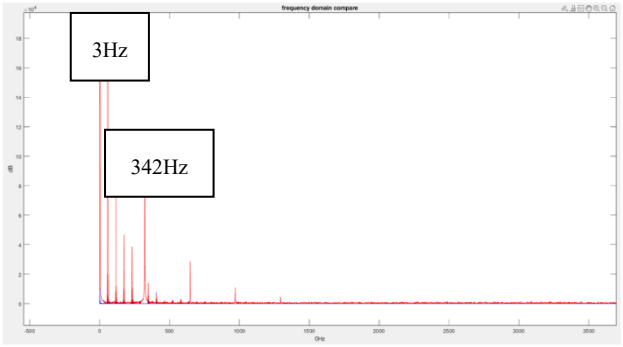


Fig 3 Frequency Spectrum of the Ideal Signal and the Noisy Input Signal

III. ANALYSIS OF CIRCUIT LEVEL

A. Design Process

After identifying the noise frequency at 342 Hz through time domain analysis, I designed a filter to achieve significant attenuation at this frequency. By using MATLAB to evaluate various filter configurations, I determined that the Chebyshev I filter produced the lowest error. I attribute this to its superior attenuation characteristics in the transition region compared to Butterworth and Bessel filters. Based on these findings, I chose the Chebyshev I filter for my design.

	PASSBAND	TRANSITION REGION	STEP RESPONSE
BUTTERWORTH	Maximally flat magnitude response in pass-band.	Steeper than Bessel, not as steep as Chebyshev filter.	Some overshoot and ringing but less than the Chebyshev filter.
CHEBYSHEV	Ripple in the pass-band.	Steeper than Butterworth and Bessel filters.	Fair degree of overshoot and ringing.
BESSEL	Flat magnitude response in pass-band.	Slower than the Butterworth, Chebyshev filters.	Very little overshoot or ringing as compared to the Butterworth and Chebyshev.

Fig 4. Comparison table of different types of filters

In the first version of the filter design, I adopted a Chebyshev I bandpass filter with a low-frequency corner at approximately 35 Hz and a high-frequency corner at 250 Hz. The simulation results showed that the error could be reduced to around 14.78. However, the Chebyshev I bandpass filter proved challenging to implement due to circuit complexity. As a result, I decided to revise the design strategy for the next version.

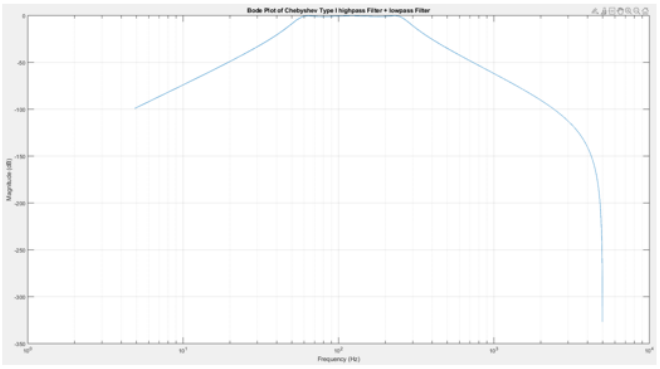
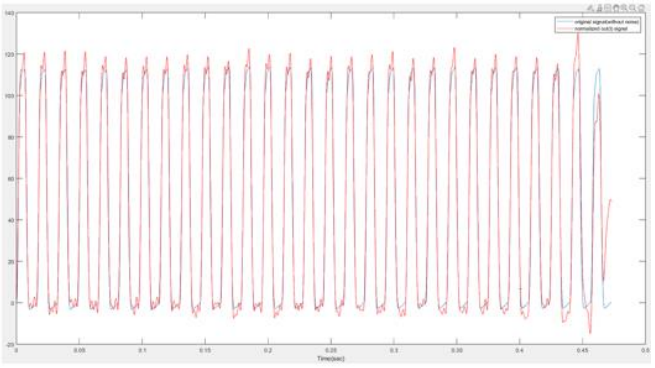


Fig 5. Chebyshev I Bandpass Filter



```
error_min= 14.799318
```

Fig 6. Chebyshev I Bandpass Filter error result

For the second version of the design, I revised the strategy by replacing the Chebyshev I bandpass filter with a combination of Chebyshev I high-pass and low-pass filters in series to achieve a bandpass effect. The low corner frequency was set at approximately 35 Hz, and the high corner frequency at 240 Hz. This approach yielded a performance comparable to the first version of the bandpass filter but significantly simplified circuit implementation. Simulation results showed that the error could be reduced to around 13.5. However, during the implementation of the Chebyshev I high-pass filter, it became apparent that the attenuation at lower frequencies (approximately 3 Hz) was insufficient. This limitation caused the overall error to increase significantly, highlighting a trade-off in performance for easier circuit realization.

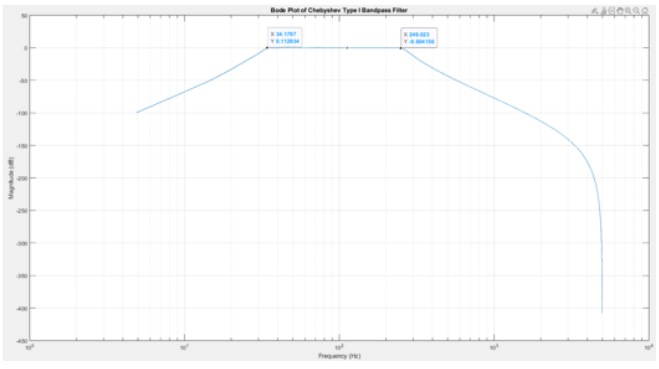
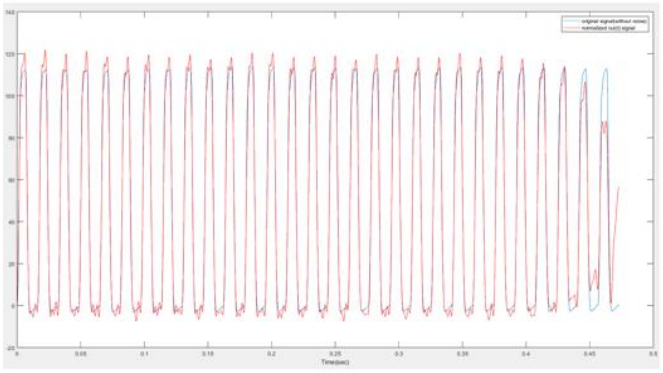


Fig 7. Chebyshev I High pass + Low pass Filter



```
error_min= 13.417391
```

Fig 8. Chebyshev I High pass + Low pass error 結果

The final filter design consists of a low-frequency notch filter to attenuate the tone at 3 Hz, a 4th-order Chebyshev I low-pass filter with a corner frequency of 210 Hz to suppress higher-frequency noise, and a high-frequency notch filter around 342 Hz to further reduce the tone at this frequency. This architecture effectively targets key noise components while maintaining signal fidelity.

B. Low Pass Filter

The 4th-order Low Pass Filter employs a Unity-Gain KRC Circuit, a configuration that combines an operational amplifier with resistor-capacitor networks to ensure stable gain and precise filtering. This structure is well-suited for high-precision signal processing applications. The filter is implemented as two cascaded KRC stages. Based on the design principles of Chebyshev 1.00-dB ripple, it is optimized for low-frequency noise rejection and signal passband response. The following is the design formula and the estimated RC results.

Resistor：R1 = mR, R2 = R

Capacitor：C1 = nC, C2 = C

Quality Factor :$Q = \frac{\sqrt{mn}}{m+1}$

Angular frequency:$w_0 = \frac{1}{\sqrt{mn}RC}$

1.00-dB ripple Chebyshev low-pass Filter

f01	Q1	f02	Q2
0.993	3.559	0.529	0.785

R1	R2	R3	R4
0.04G	2.13G	0.27G	0.34G
C1	C2	C3	C4
0.97pf	0.67pf	6.21pf	0.97pf

Fig 9. RC result

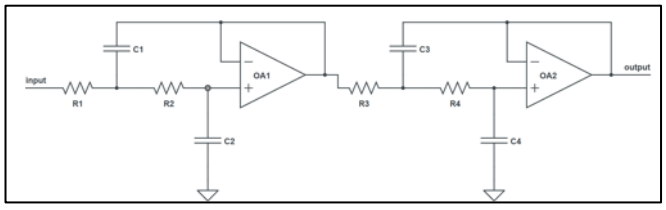


Fig 10. 4 order Low pass Filter

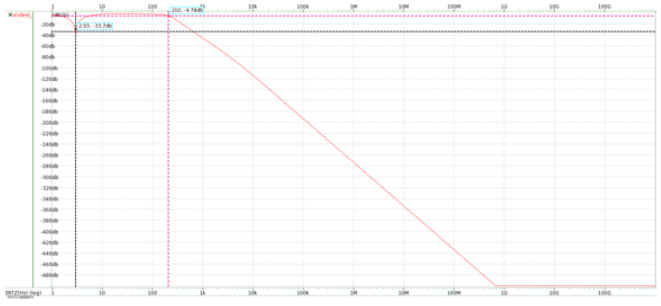


Fig 11. Frequency response diagram of the overall circuit

C. Low Pass Notch Filter

Our design features a Single Op-amp Twin-T Notch Filter to suppress noise at a specific frequency. The formula for calculating the center frequency fN is:

$$fN = \frac{1}{4\pi RC}$$

The calculated parameters are as follows:

$$R = 2.7G\Omega$$

$$C = 9.82pF$$

$$k = \frac{RB}{RA+RB} = 1 - \frac{1}{4Q}$$

$$RA = 0.11G\Omega$$

$$RB = 0.12G\Omega$$

The design incorporates a high resistance value RRR, chosen to enable a corresponding small capacitance value when converted to a switched-capacitor (SC) circuit in future implementations. Simulation results demonstrate a nearly 33 dB attenuation at the target frequency of 3 Hz, effectively suppressing noise while maintaining excellent stability and low power consumption.

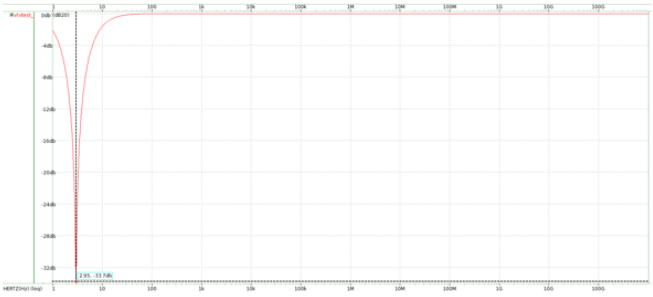
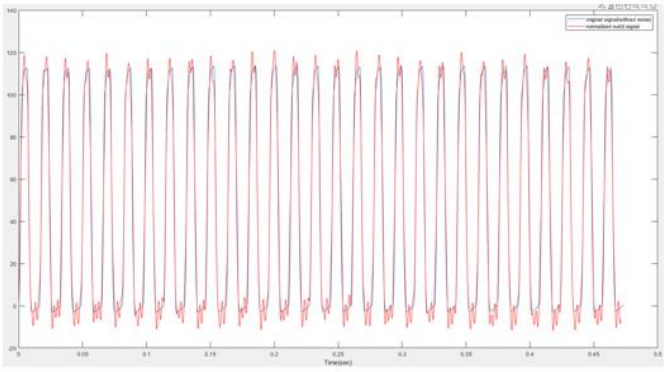


Fig 12. Passive notch frequency response

D. Operational Amplifier

The initial simulation was conducted using an ideal operational amplifier (OP), yielding an error of approximately 35.22. Following this, the strategy was to replace the ideal OP with a custom-designed non-ideal OP to evaluate its performance in the system.



error_min= 35.216805

Fig 13. Ideal Operational Amplifier error result

For the operational amplifier (OP) design, several architectures were considered, and the Telescope Opamp was selected due to its capability for achieving the lowest power consumption. Although its DC gain and bandwidth are lower compared to other amplifier options, it meets the requirements for the low-pass filter and notch filter to function properly.

To further minimize power consumption, the bias point of the OP was carefully set so that all transistors operate in the subthreshold region, with the bias circuit designed specifically to support this configuration. The resulting OP design features a unity-gain bandwidth of 119 kHz, a DC gain of 77 dB, and a phase margin of 90 degrees, providing a balance between performance and power efficiency. These specifications ensure the amplifier's stable operation within the designed system.

Structure	Advantage	Disadvantage
2-Stage OP	(1)High gain (2)Superior precision	(1)Higher power (2)Complex
Telescope OP	(1)Low power (2)Easy design	(1)Limit gain (2)Variations
Folded cascode OP	(1)Good bandwidth (2)Good CMRR	(1)Higher power (2)Complex

Fig 14. Operational Amplifier comparison table

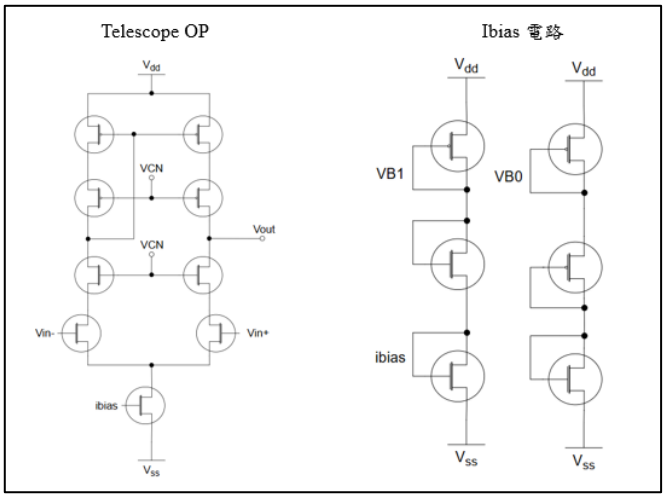


Fig 15. Telescope structure & Ibias Circuit

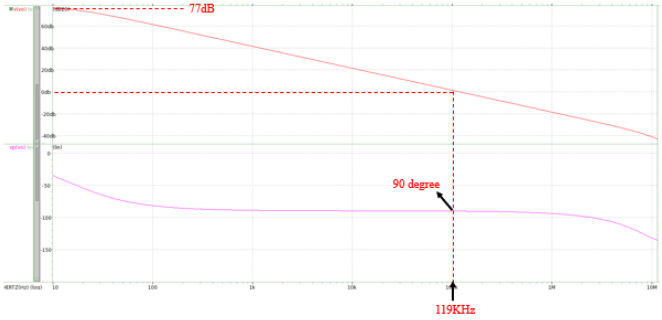
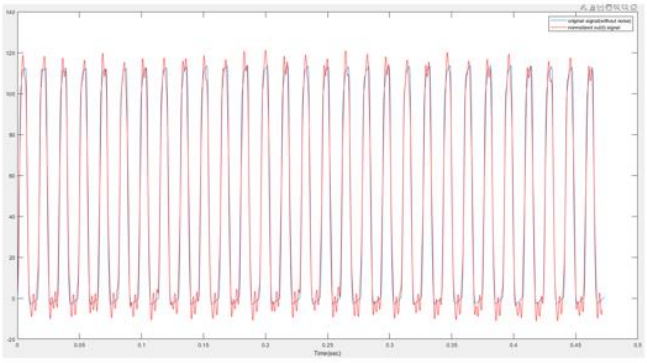


Fig 16. Operational Amplifier Performance

Operational Amplifiler performance	
Region	Subthreshold
DC gain	77dB
Phase Margin	90 degree
UGB	119kHz
DC power consumption	0.6893 uW

Fig 17. Operational Amplifier performance table



error_min= 35.372680

Fig 18. Non-ideal Operational Amplifier error result

The simulation results indicate that the error value with the non-ideal operational amplifier is approximately 35.37, only slightly higher than that of the ideal op amp. This demonstrates that the circuit

performance remains stable even with the non-ideal component. Following this, the resistive elements in the circuit were replaced with equivalent switched-capacitor (SC) circuits. This conversion reduces the circuit area and power dissipation while preserving the accuracy and performance of the original design.

E. Switch Capacitor (SC) & Non-overlapped circuit

In my design, I replaced high-value resistors in the notch and low-pass filters with switched-capacitor (SC) circuits. While SC circuits introduce noise at the switching frequency, the benefit of significantly reducing the resistor area outweighs this drawback.

I designed the SC circuit (Fig. 19) to work with a non-overlapped circuit (Fig. 20) that generates the SC control signals. These non-overlapping control signals help reduce current noise, minimize instantaneous power consumption during switching, and mitigate additional errors caused by signal coupling.

The operation of the SC circuit is based on the principle of charge conservation, described by the equation:

$$\frac{vin - vout}{R} = \frac{Cs(Vin - Vout)}{T}$$

From this, I derived the equivalent resistance R as:

$$R = \frac{T}{C}$$

To ensure reliable operation, I set the frequency of the external control signal to 20 kHz.

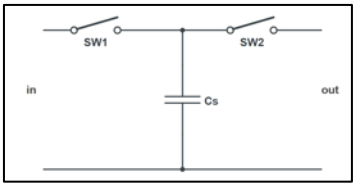


Fig 19. Switch Capacitor circuit

I designed the Non-overlapped Circuit to generate two clock signals, ϕ1 and ϕ2, with an appropriate non-overlapping interval. This prevents short circuits from simultaneous switching, ensuring stable and efficient operation of the switched-capacitor filters.

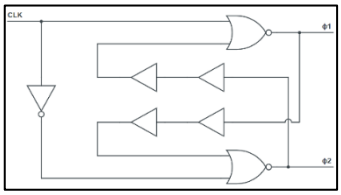


Fig 20. Non-overlapped circuit

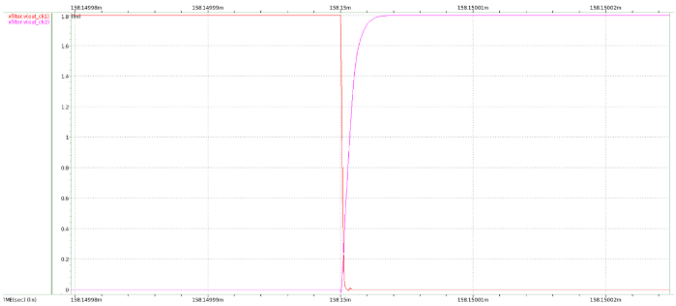


Fig 21. Non-overlapped circuit waveview

IV. SIMULATION RESULTS AND PERFORMANCE

A. Error

Fig. 22 shows the overlay of the original and filtered signals, with a minimum error value of error_min=42.04, demonstrates the filter's effectiveness in noise suppression while preserving signal fidelity.

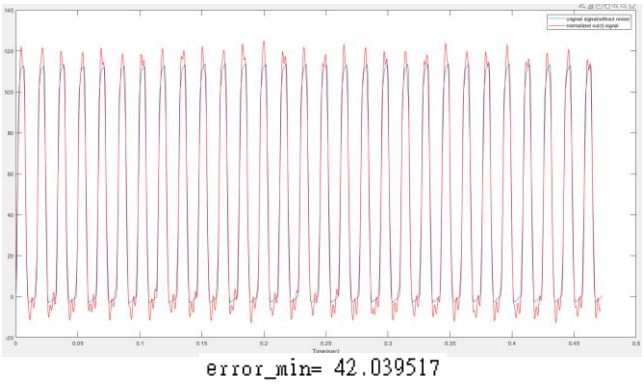


Fig 22. Minimum Error and Overlay of Original and Filtered Signals

B. Performance Summary

The performance summary table (Fig. 23) presents key results of my design. The power consumption pie chart (Fig. 24) shows most power is used by the SC circuit. While the design is efficient, future improvements could focus on optimizing the SC circuit to further reduce power consumption.

Performance	Usage	Limitation
Resistors(MΩ)	0	100
Capacitor(pf)	59.5	1000
Power(nW)	126500	
Error	42.04	
FoM	217.16	

Fig 23. Performance Summary Table

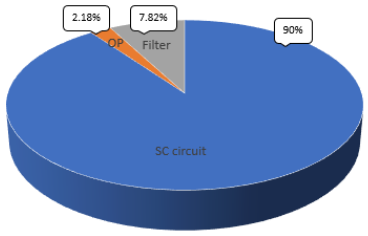


Fig 24. Power consumption pie chart

V. CONCLUSION

My design effectively suppresses noise at 3 Hz and 342 Hz using a 4th-order Chebyshev I low-pass filter and notch filters. My design that incorporating a telescopic operational amplifier and SC circuits achieved low power consumption. Simulation results confirmed its stability and efficiency, with an error of 42.04, and identified SC circuit power consumption as a focus for future optimization.

VI. Future Work

1. Replace the 3 Hz notch filter with a high-pass filter to further minimize low-frequency errors.
2. Optimize the delay of the non-overlapped clock circuit to enhance overall performance.
3. Improved operational amplifier (OP) design to reduce power consumption and improve circuit stability.

Through these adjustments, we hope to further improve the efficiency and efficiency of the circuit while maintaining the accuracy of the original design.

VII. Reference

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