

National Cheng Kung University

Department of Electrical Engineering

Introduction to VLSI CAD (Spring 2024)

Lab Session 5

FSM&Synthesis of Sequential Logic

Name	Student ID	
游宗謀	E94106151	
Practical Sections	Points	Marks
Lab in class	15	
Prob A	20	
Prob B	10	
Prob C	15	
Report	35	
File hierarchy, naming...etc.	5	
Notes:		

Due Date: 14:59, April 4, 2024 @ moodle

Deliverables

- 1) All Verilog codes including testbenches for each problem should be uploaded.
NOTE: Please **DO NOT** include source code in the paper report!
- 2) All homework requirements should follow the naming rule in this file hierarchy or you will not get the full credit.
NOTE: Please **DO NOT** upload waveforms!
- 3) **Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.**
- 4) If you upload a dead body, which we cannot even compile, you will get **NO** credit!
- 5) All Verilog file before synthesizing should get at least **95%** Superlint Coverage.
- 6) Lab5_Student_ID.tar (English alphabet of Student_ID should be **capital**.)

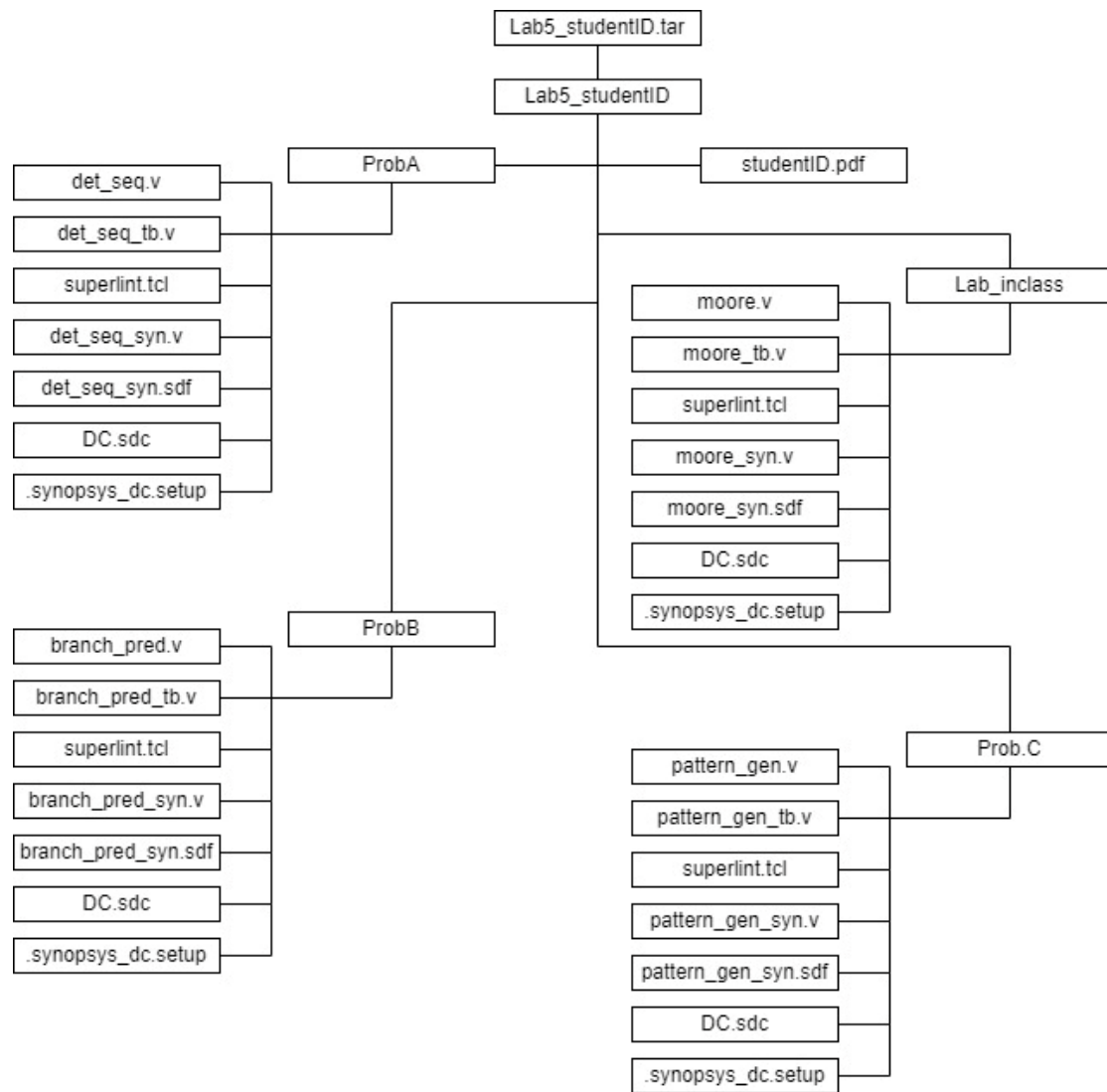
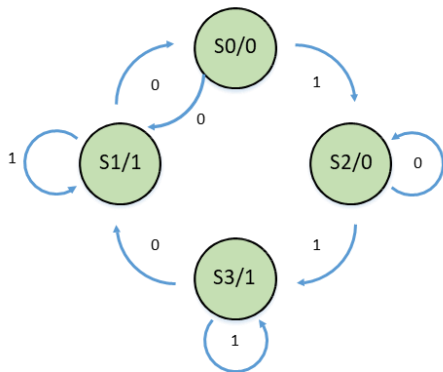


Fig.1 File hierarchy for Homework submission

- 1) Design a Moore machine circuit that can be synthesized. The following is Moore machine module's specification. (Do **NOT** add or delete I/O ports, but you can change their behavior.)



Current State	Next State		qout
	din=0	din=1	
S0=00	S1	S2	0
S1=01	S0	S1	0
S2=10	S2	S3	1
S3=11	S1	S3	1

Signal	Type	Bits	Description
clk	input	1	Clock pin.
rst	input	1	Reset pin. Reset all of the flip flops to zeros.
din	input	1	Control signal for fsm.
qout	output	1	1:when current state==S1 or current state==S3 0: when current state==S0 or current state==S2

- 2) Please describe your FSM in detail

Explanation about your FSM
<p>This is a Moore machine that will decide its output based on its current state, and the changes of its next state will be depends on its input. So, as the plot and form above, there are four different cases below. First, if the current state is s0, it will output(qout) 0, and the next state will become s1 if the input(din) is 0 or s2 if din is 1. Second, if the current state is s1, it will output 0, and the next state will become s0 if din is 0 or s1 if din is 1. Third, if the current state is s2, it will output 1, and the next state will become s2 if din is 0 or s3 if din is 1. Last, if the current state is s3, it will output 1, and the next state will become s1 if din is 0 or s3 if din is 1.</p>

- 3) After synthesizing your design, you may have some information about the circuit. Please fill in the following form.

Timing (slack)	Area (total cell area)	Power (total)
0.32	4.147200 um ²	6.7439e-03 mW

4) Please attach your design waveforms.

Your simulation result on the terminal.

RTL:

```
1401161566-PJTV
FDSB Dumper for VCS, Release Verdi_E-2023.03-892, Linux x86_64/64bit, 08/28/2023
(C) 1996 - 2023 by Synopsys, Inc.
*Verdi* - Create FDSB file "memore.fdsb"
*Verdi* - Begin traversing the scopes, layer (0).
*Verdi* - End of traversing.
time 25 output is correct
time 35 output is correct
time 45 output is correct
time 55 output is correct
time 65 output is correct
time 75 output is correct
time 85 output is correct
time 95 output is correct
time 105 output is correct
time 115 output is correct
time 125 output is correct
time 135 output is correct
time 145 output is correct
time 155 output is correct
time 165 output is correct
time 175 output is correct
time 185 output is correct
time 195 output is correct

*****
**                               |__|
** Congratulations !!          / 0.0 |
**                               |      |
** Simulation PASS!!           /---\ |
**                               |_____|
*****

$finish called from file "memore.tb.v", line 88.
$finish at simulation time 23000
V C S   S i m u l a t i o n   R e p o r t
Time: 230000 ps
CPU Time: 0.530 seconds Data structure size: 0.00Mb
Sun Mar 30 21:21:48 2024
CPU time: .366 seconds to compile + .450 seconds to elab + .239 seconds to link
+.164 seconds in simulation
vlsicadb:/home/user2/vlsi24/vlsi2415/Lab5/E94106151/Lab_inclass x
```

Gate:

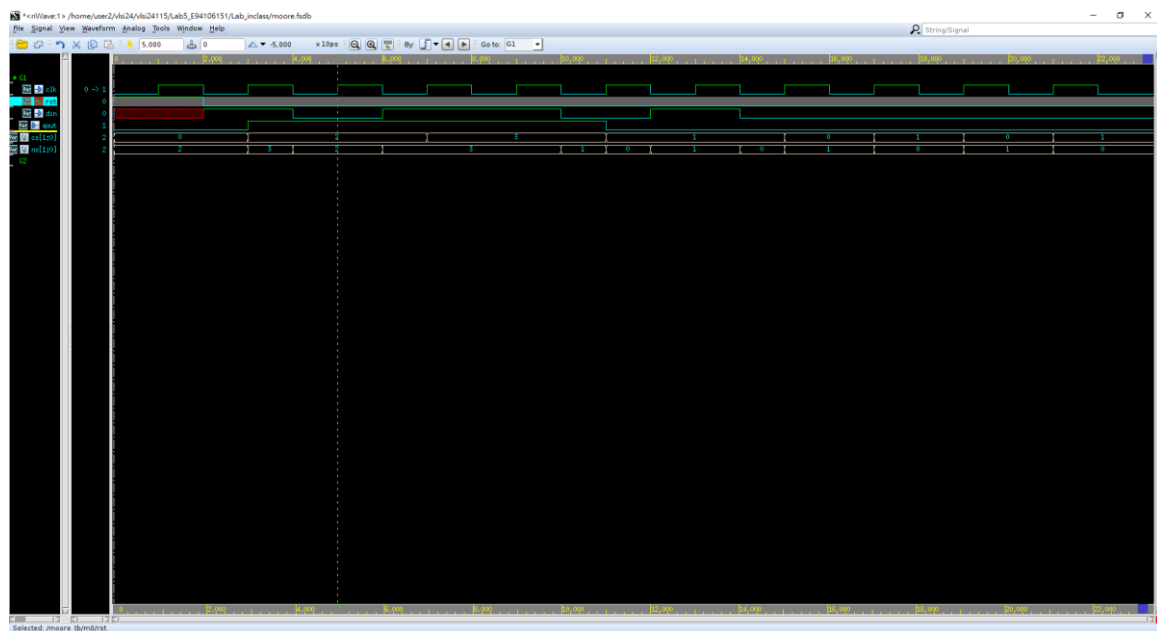
```
Gate
(C) 1996 - 2023 by Synopsys, Inc.
*Verdi* FDSB WARNING: The FDSB file already exists. Overwriting the FDSB file may crash the programs that are using this file.
*Verdi* - Create FDSB file "det_seq_tb.fdsb"
*Verdi* - Begin traversing the scopes, layer (0).
*Verdi* - End of traversing.
Result No 1 is correct
Result No 2 is correct
Result No 3 is correct
Result No 4 is correct
Result No 5 is correct
Result No 6 is correct
Result No 7 is correct
Result No 8 is correct
Result No 9 is correct
Result No 10 is correct
Result No 11 is correct
Result No 12 is correct
Result No 13 is correct
Result No 14 is correct
Result No 15 is correct
Result No 16 is correct
Result No 17 is correct
Result No 18 is correct
Result No 19 is correct
Result No 20 is correct
Result No 21 is correct
Result No 22 is correct
Result No 23 is correct
Result No 24 is correct
Result No 25 is correct
Result No 26 is correct
Result No 27 is correct
Result No 28 is correct
Result No 29 is correct
Result No 30 is correct
The total number of pattern 101011 is 4. Correct!

*****
**                               |__|
** Congratulations !!          / 0.0 |
**                               |      |
** Simulation PASS!!           /---\ |
**                               |_____|
*****

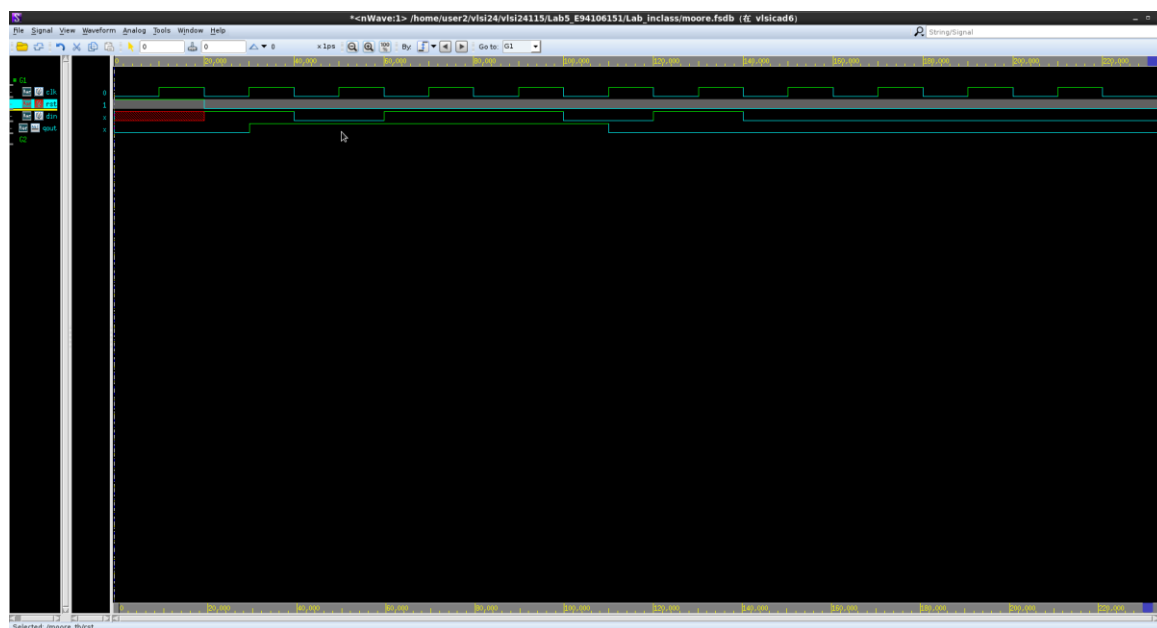
$finish called from file "det_seq_tb.v", line 142.
$finish at simulation time 65000
V C S   S i m u l a t i o n   R e p o r t
Time: 65000 ps
CPU Time: 0.720 seconds Data structure size: 0.59Mb
Sun Mar 31 02:18:14 2024
CPU time: .787 seconds in simulation
vlsicadb:/home/user2/vlsi24/vlsi2415/Lab5/E94106151/ProbA x
```

Your waveform :

RTL:



Gate:

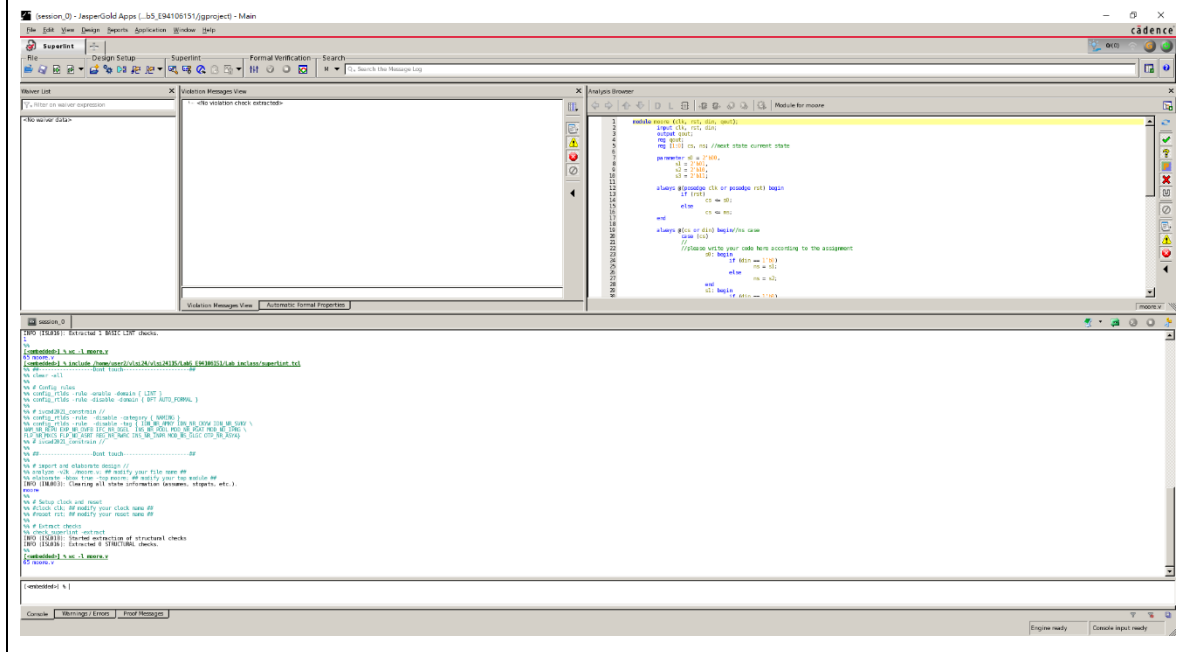


Explanation of your waveform :

以黃色標記指到的位置為例，前一個 clock cycle 的 state 為 $s2(cs=2)$ ，所以輸出 $qout$ 為 1，而因為輸入 din 為 0，所以下一個 state 仍然是 $s2(cs=2)$ ，同理其他 clk 正緣也是跟這樣可以用狀態機的圖表解釋。

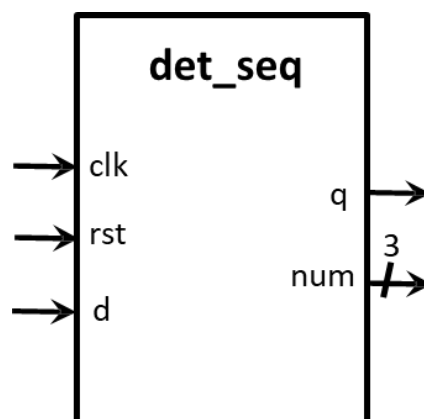
Superlint Coverage

$$\text{Coverage} = (1 - (0/65)) * 100\% = 100\%$$



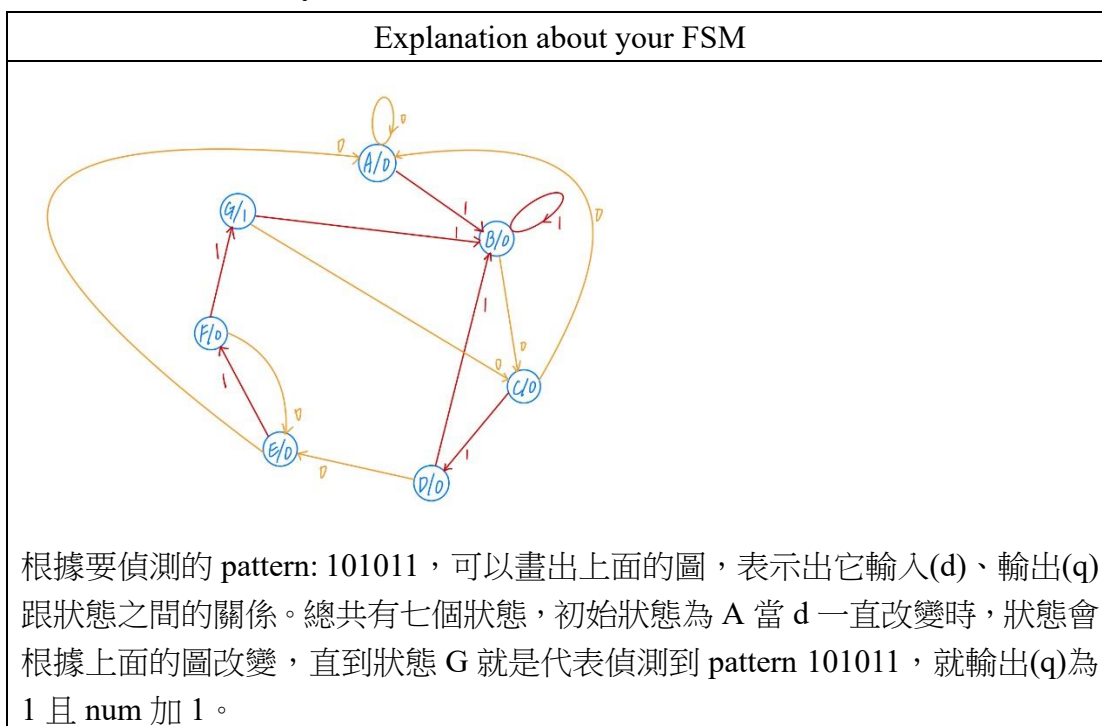
ProbA: Design a circuit “detecting pattern 101011”

- 1) Design a pattern seq-detecting circuit that can be synthesized with **moore machine**. The following is det_seq module’s specification. (Do **NOT** add or delete I/O ports, but you can change their behavior.)



Signal	Type	Bits	Description
clk	input	1	clock
rst	input	1	reset, active high
d	input	1	pattern bit
q	output	1	When detect pattern 101011, q pulls to high at next clock posedge. Otherwise, q is low.
num	output	3	Count the number of pattern 101011

2) Please describe your FSM in detail

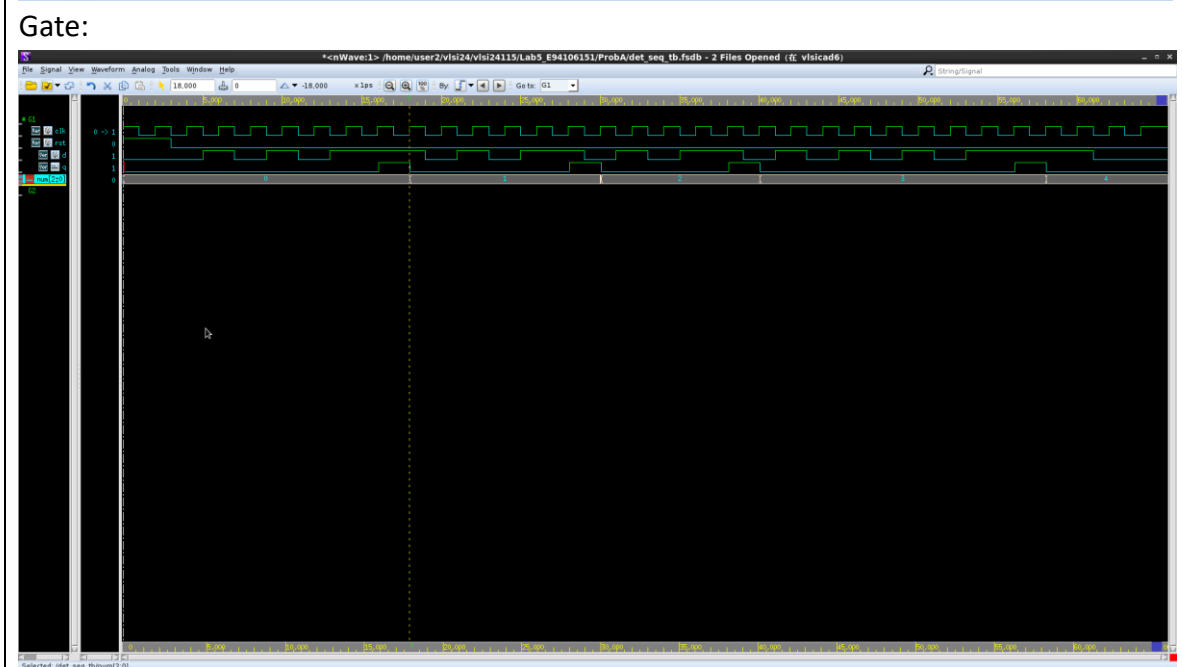


3) After synthesizing your design, you may have some information about the circuit. Please fill in the following form.

Timing (slack)	Area (total cell area)	Power (total)
0.30	12.286080 um ²	1.4213e-02 mW

4) Please attach your design waveforms.

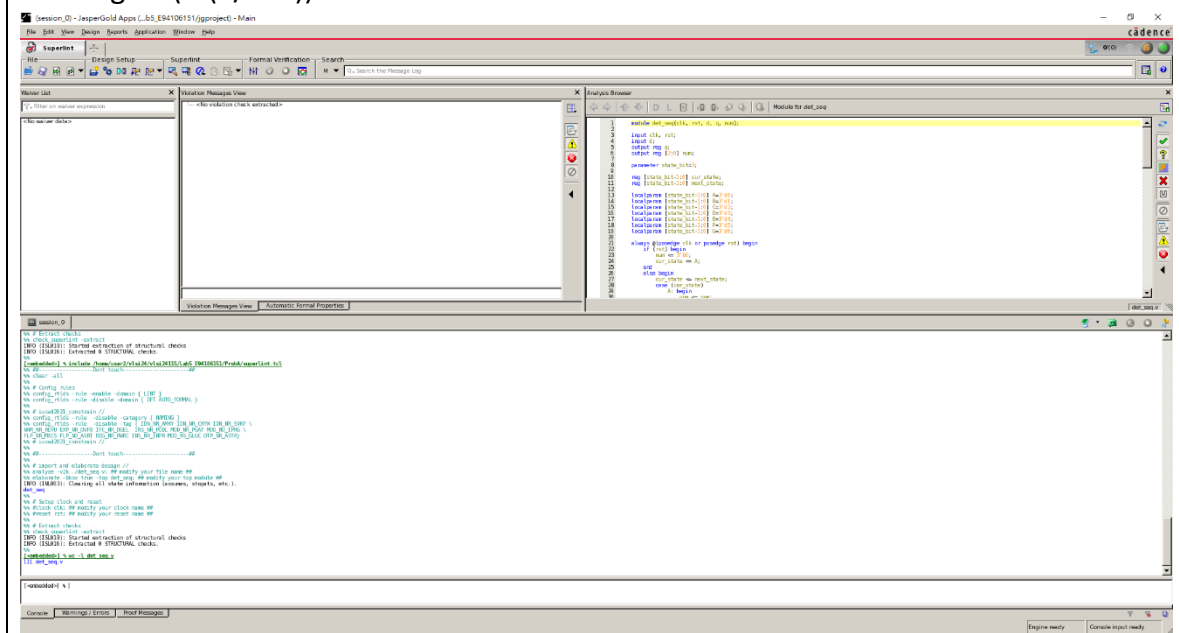
Your simulation result on the terminal.



以黃色標記指到的位置(RTL)為例，前一個 clock cycle 的 state 為 E(cur_state=4)，所以輸出 q 為 0、num 沒增加，而因為輸入 d 為 1，所以下一個 state 變成 F(cur_state=5)，同理其他 clk 正緣也是跟這一樣可以用狀態機的圖表解釋。

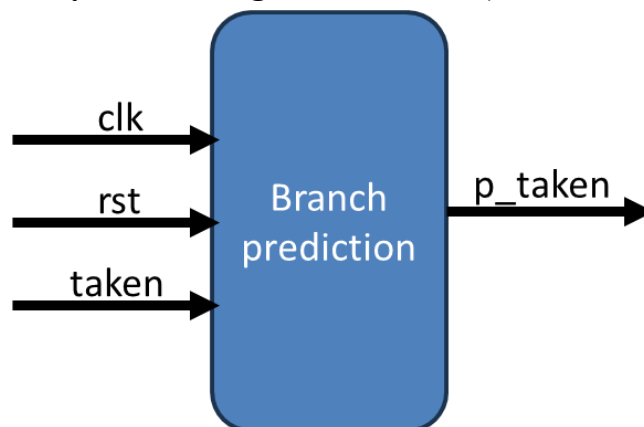
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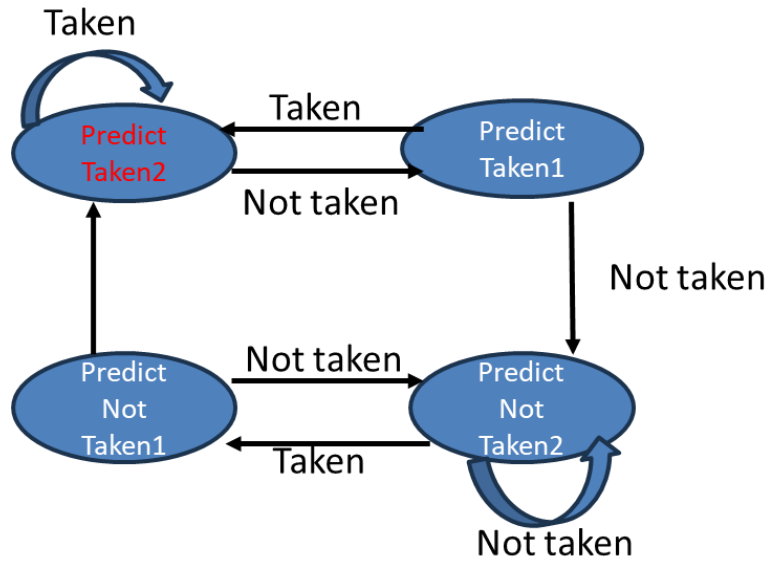
$$\text{Coverage} = (1 - (0/111)) * 100\% = 100\%$$



ProbB: Design a 2-bit branch prediction

- 1) Design a 2-bit branch prediction with **moore machine**. The following is 2-bit branch prediction module's specification. (Do **NOT** add or delete any I/O ports, but you can change their behavior.)





2) Please describe your FSM in detail.

Explanation about your FSM
<p>根據上圖我們可以設計四個 state 的 Moore machine。在 Predict Taken1 時，p_taken 為 1，若 taken 為 1 則下個 state 為 Predict Taken2、為 0 則下個 state 為 Predict Not Taken2。在 Predict Taken2 時，p_taken 為 1，若 taken 為 1 則下個 state 為 Predict Taken2、為 0 則下個 state 為 Predict Not Taken1。在 Predict Not Taken1 時，p_taken 為 0，若 taken 為 1 則下個 state 為 Predict Taken2、為 0 則下個 state 為 Predict Not Taken2。在 Predict Not Taken2 時，p_taken 為 0，若 taken 為 1 則下個 state 為 Predict Not Taken1、為 0 則下個 state 為 Predict Not Taken2。</p>

3) After synthesizing your design, you may have some information about the circuit. Please fill in the following form.

Timing (slack)	Area (total cell area)	Power (total)
0.33	3.265920 μm^2	5.4371e-03 mW

4) Please attach your design waveforms.

Your simulation result on the terminal.

RTL:

```
140.116.156.6 - PuTTY
time      11 output is correct
time      12 output is correct
time      13 output is correct
time      14 output is correct
time      15 output is correct
time      16 output is correct
time      17 output is correct
time      18 output is correct
time      19 output is correct
time      20 output is correct
time      21 output is correct
time      22 output is correct
time      23 output is correct
time      24 output is correct
time      25 output is correct
time      26 output is correct
time      27 output is correct
time      28 output is correct
time      29 output is correct
time      30 output is correct
time      31 output is correct

*****
**          **          (\_ _|)
** Congratulations !! **          / 0.0 |
**          **          |
** Simulation PASSED!! **          / ^ ^ ^ \ |
**          **          | ^ ^ ^ ^ |w|
**          **          \m _ _ _|_|
*****

$finish called from file "branch_gcd_tb.v", line 147.
$finish at simulation time 31500
VCS Simulation Report
Time: 31500 ps
CPU Time: 0.530 seconds; Data structure size: 0.08Mb
Sat Mar 30 22:12:10 2024
CPU time: .293 seconds to compile + .454 seconds to elab + .287 seconds to link + .552 seconds in simulation
vlsicad6:/home/user2/vlsi24/vlsi2415/Lab5_E94106151/ProbB %
```

Gate:

```
140.116.156.6 - PuTTY
time      12 output is correct
time      13 output is correct
time      14 output is correct
time      15 output is correct
time      16 output is correct
time      17 output is correct
time      18 output is correct
time      19 output is correct
time      20 output is correct
time      21 output is correct
time      22 output is correct
time      23 output is correct
time      24 output is correct
time      25 output is correct
time      26 output is correct
time      27 output is correct
time      28 output is correct
time      29 output is correct
time      30 output is correct
time      31 output is correct

*****
**          **          (\_ _|)
** Congratulations !! **          / 0.0 |
**          **          |
** Simulation PASSED!! **          / ^ ^ ^ \ |
**          **          | ^ ^ ^ ^ |w|
**          **          \m _ _ _|_|
*****

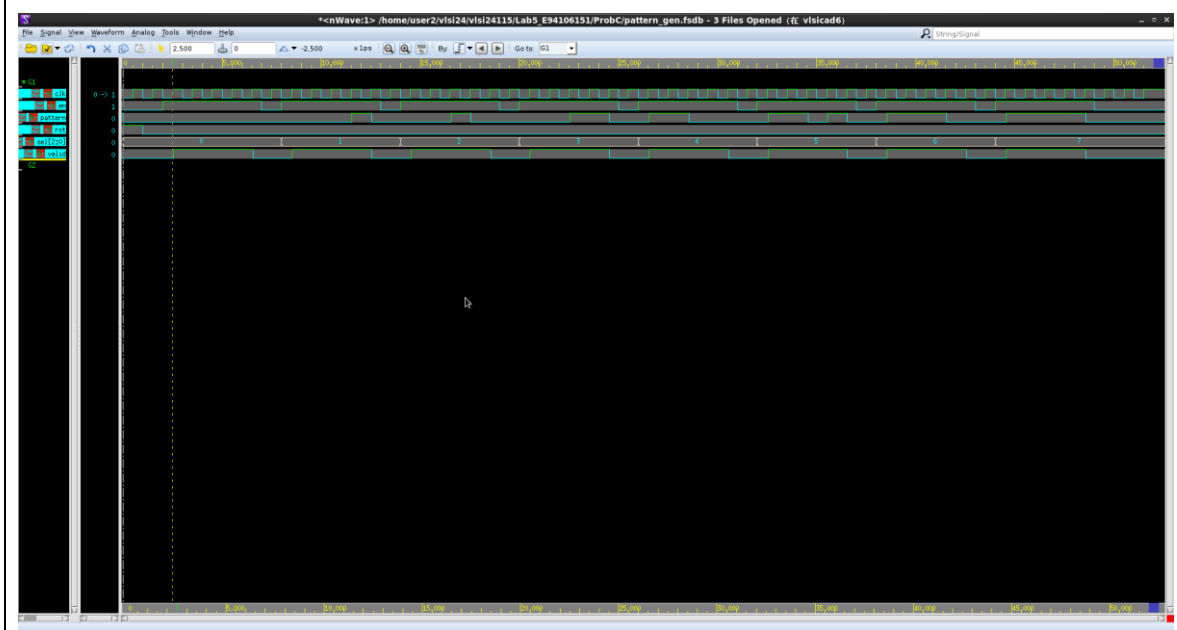
$finish called from file "branch_gcd_tb.v", line 147.
$finish at simulation time 31500
VCS Simulation Report
Time: 31500 ps
CPU Time: 0.720 seconds; Data structure size: 0.38Mb
Mon Apr 1 18:57:14 2024
CPU time: 10.840 seconds to compile + .544 seconds to elab + .719 seconds to link + 1.756 seconds in simulation
vlsicad6:/home/user2/vlsi24/vlsi2415/Lab5_E94106151/ProbB %
```

Your waveform :

RTL:



Gate:

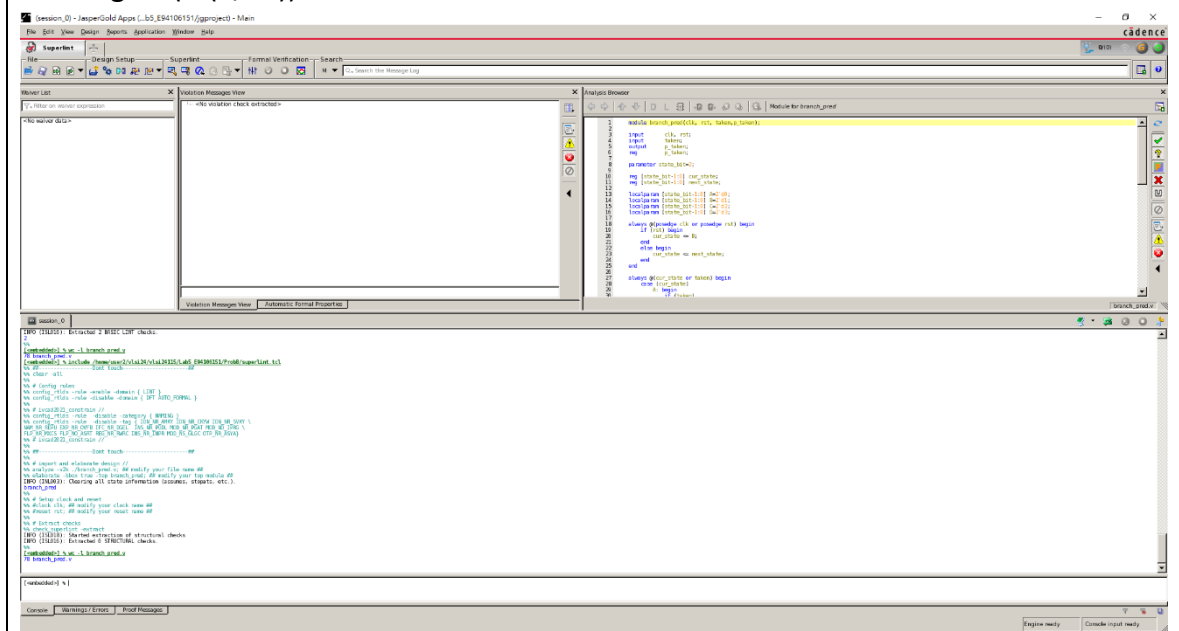


Explanation of your waveform :

以黃色標記指到的位置(RTL)為例，前一個 clock cycle 的 state 為 Predict Not Taken2(cur_state=3)，所以輸出 p_taken 為 0，而因為輸入 taken 為 1，所以下一個 state 變成 Predict Not Taken1(cur_state=2)，同理其他 clk 正緣也是跟這一樣可以用狀態機的圖表解釋。

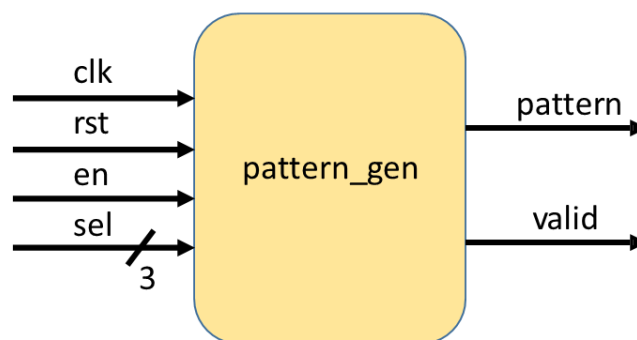
Superlint Coverage

Coverage = $(1-(0/78))*100\% = 100\%$



ProbC: Design a pattern generator

- 1) Design a pattern generator which can create the following pattern and use **mealy machine**. The following is pattern generator specification.



sel [2:0]	pattern
000	0000
001	0001
010	0010
011	0011
100	1100
101	1101
110	1110
111	1111

Signal	Bits	Type	Description
clk	1	input	clock
rst	1	input	reset, active high
en	1	input	When en is high, the system will start to make pattern. The pattern will be created once . If the host want to create the next pattern, it should pull down the en to 0, then restart en.
sel	3	input	According different sel signal to make different pattern
pattern	1	output	Pattern output
valid	1	output	When valid is 1, pattern's value is valid.

2) Please describe your FSM in detail.

Explanation about your FSM
<p>根據上面的表格我設計了一個 5 個 state 的 Mealy machine。state 為 R 時，valid 為 0 輸出無效，當 en 為 1 時下個 state 為 A。state 為 A 時，valid 為 1 輸出有效、pattern 根據上面藍色表格 sel 輸出 0 或 1，當 en 為 1 時下個 state 為 B。state 為 B 時，valid 為 1 輸出有效、pattern 根據上面藍色表格 sel 輸出 0 或 1，當 en 為 1 時下個 state 為 C。state 為 C 時，valid 為 1 輸出有效、pattern 根據上面藍色表格 sel 輸出 0 或 1，當 en 為 1 時下個 state 為 D。state 為 D 時，valid 為 1 輸出有效、pattern 根據上面藍色表格 sel 輸出 0 或 1，當 en 為 1 時下個 state 為 R。</p>

3) After synthesizing your design, you may have some information about the circuit. Please fill in the following form.

Timing (slack)	Area (total cell area)	Power (total)
0.30	10.264320 um ²	1.5215e-02 mW

4) Please attach your design waveforms.

Your simulation result on the terminal.

RTL:

```

Xilinx ISE 15.6 - BusTty

//////////////////////////////////////////////////////////////////sel is 010////////////////////////////////////////////////////////////////////
pattern is 0, pass!!
pattern is 0, pass!!
pattern is 1, pass!!
pattern is 0, pass!!

//////////////////////////////////////////////////////////////////sel is 011////////////////////////////////////////////////////////////////////
pattern is 0, pass!!
pattern is 0, pass!!
pattern is 1, pass!!
pattern is 0, pass!!

//////////////////////////////////////////////////////////////////sel is 100////////////////////////////////////////////////////////////////////
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 0, pass!!
pattern is 0, pass!!

//////////////////////////////////////////////////////////////////sel is 101////////////////////////////////////////////////////////////////////
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 0, pass!!
pattern is 1, pass!!

//////////////////////////////////////////////////////////////////sel is 110////////////////////////////////////////////////////////////////////
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 0, pass!!

//////////////////////////////////////////////////////////////////sel is 111////////////////////////////////////////////////////////////////////
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 1, pass!!

*****
**                                     |  |
** Congratulations!!                 / 0 0 \
**                                     |  |
** Simulation PASS!!                 |  |
**                                     |  |
*****

Finish called from file "pattern_gen_tb.v", line 332.
Finish at simulation time          3200
V C S  S i m u l a t i o n  R e p o r t
Time: 3200 ps
CPU Time: 0.022 seconds      Data structure size: 0.00B
Sat Mar 30 22:19:14 2024
CPU time: 16.96 seconds to compile + .062 seconds to elab + .282 seconds to link + .492 seconds in simulation
vlsicad:/home/user2/vlsi2/vlsi28125/Lab5_EB101919/Prob6
```

Gate:

```

RTL

pattern is 0, pass!!

//////////////////////////////////////////////////////////////////sel is 011////////////////////////////////////////////////////////////////////
pattern is 0, pass!!
pattern is 0, pass!!
pattern is 1, pass!!
pattern is 1, pass!!

//////////////////////////////////////////////////////////////////sel is 100////////////////////////////////////////////////////////////////////
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 0, pass!!
pattern is 0, pass!!

//////////////////////////////////////////////////////////////////sel is 101////////////////////////////////////////////////////////////////////
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 0, pass!!
pattern is 1, pass!!

//////////////////////////////////////////////////////////////////sel is 110////////////////////////////////////////////////////////////////////
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 0, pass!!

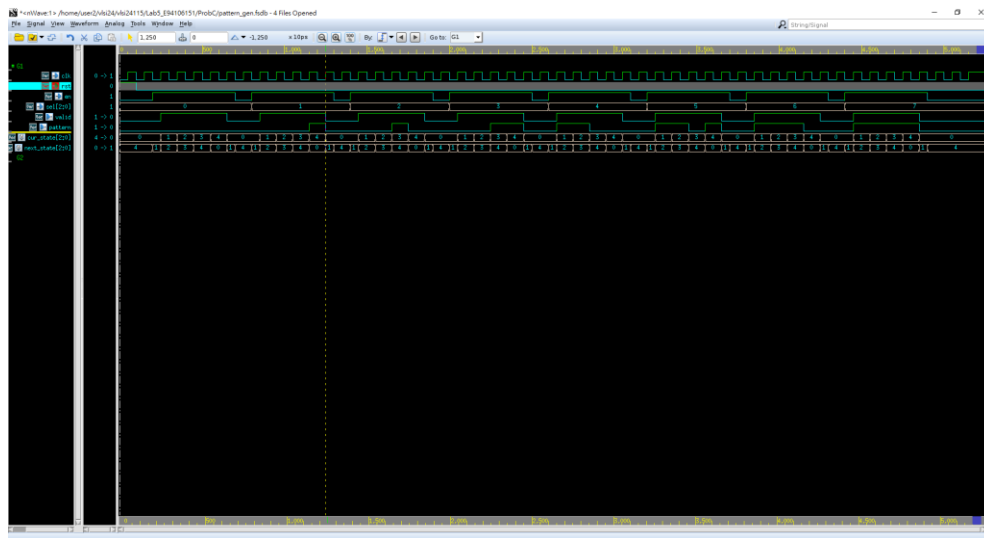
//////////////////////////////////////////////////////////////////sel is 111////////////////////////////////////////////////////////////////////
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 1, pass!!
pattern is 1, pass!!

*****
**                                     |  |
** Congratulations!!                 / 0 0 \
**                                     |  |
** Simulation PASS!!                 |  |
**                                     |  |
*****

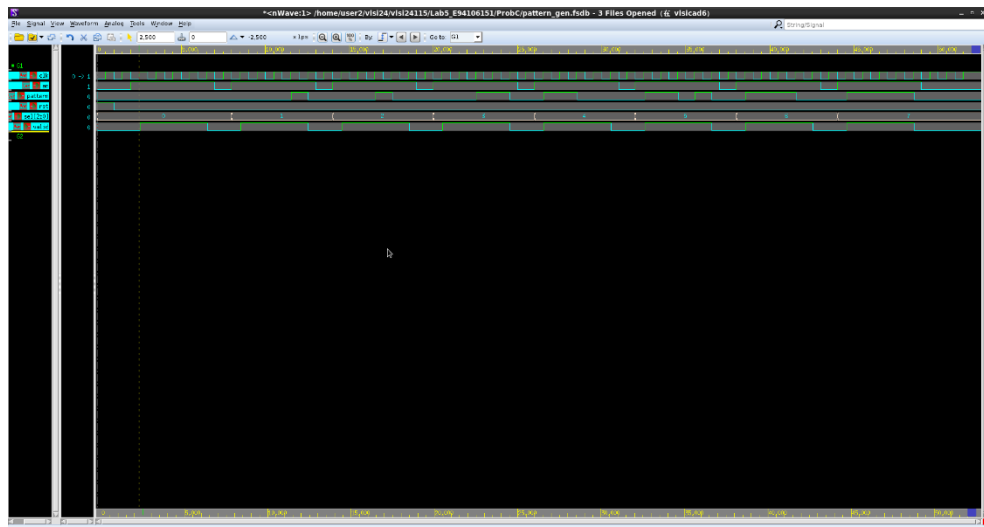
Finish called from file "pattern_gen_tb.v", line 332.
Finish at simulation time          3200
V C S  S i m u l a t i o n  R e p o r t
Time: 3200 ps
CPU Time: 0.720 seconds      Data structure size: 0.50B
Sat Mar 30 22:20:32 2024
CPU time: 10.639 seconds to compile + .369 seconds to elab + .706 seconds to link + .739 seconds in simulation
vlsicad:/home/user2/vlsi2/vlsi28125/Lab5_EB101919/Prob6
```

Your waveform :

RTL:



Gate:

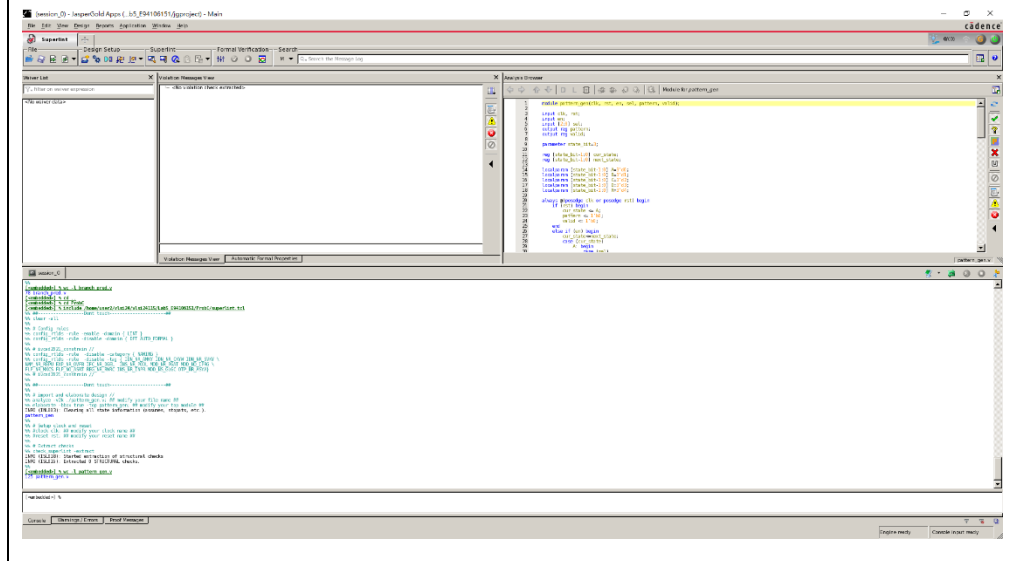


Explanation of your waveform :

以 1050ps 的位置(RTL)為例,前一個 clock cycle 的 state 為 C($cur_state=2$)、 sel 為 1, 所以輸出有效($valid=1$)、 $pattern$ 為 0、下一個 state 變成 D($cur_state=3$), 同理其他 clk 正緣也是跟這一樣可以用狀態機的圖表解釋。

Superlint Coverage

$$\text{Coverage} = (1 - (0/125)) * 100\% = 100\%$$



- 5) At last, please write the lessons learned from this lab session, or some suggestions for this lab session. Thank you.

在這次的實驗中，我學到兩種有限狀態機要如何用 verilog 實現，還有如何用 design version 這個 tool 做時序電路的合成，感謝助教每次都將步驟講解得很清楚，讓我們不容易在過程中做錯，還有最感謝黃浚喆同學的解答，解決了我 Gate-level simulation 無法 compile 的問題。希望之後的實驗課時，講到 clock specification 時，助教能稍微提一下 set time 和 hold time 是什麼？讓我能更加理解，什麼情況下需要用到 add buffer on clock path。

Appendix A : Commands we will use to check your homework

Problem		Command
Lab	Compile	% vcs -R moore.v -full64
	RTL-sim	% vcs -R moore_tb.v -debug_access+all -full64 +define+FSDB
	Gate-sim	% vcs -R moore_tb.v -debug_access+all -full64 +define+FSDB+syn

Problem		Command
ProbA	Compile	% vcs -R det_seq.v -full64
	RTL-sim	% vcs -R det_seq_tb.v -debug_access+all -full64 +define+FSDB
	Gate-sim	% vcs -R det_seq_tb.v -debug_access+all -full64 +define+FSDB+syn
ProbB	Compile	% vcs -R branch_pred.v -full64
	RTL-sim	% vcs -R branch_pred_tb.v -debug_access+all -full64 +define+FSDB
	Gate-sim	% vcs -R branch_pred_tb.v -debug_access+all -full64 +define+FSDB+syn
ProbC	Compile	% vcs -R pattern_gen.v -full64
	RTL-sim	% vcs -R pattern_gen_tb.v -debug_access+all -full64 +define+FSDB
	Gate-sim	% vcs -R pattern_gen_tb.v -debug_access+all -full64 +define+FSDB+syn