**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2024)***

**Lab Session 4**

**Register Files, Manhattan Distance and LFSR**

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| --- | --- | --- |
| Name | Student ID | |
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| **Practical Sections** | **Points** | **Marks** |
| Prob A | 30 |  |
| Prob B | 30 |  |
| Prob C | 20 |  |
| Report | 15 |  |
| File hierarchy, naming…etc. | 5 |  |
| Notes: | | |

**Due Date: 15:00, March 27, 2024 @ moodle**

**Deliverables**

1. All Verilog codes including testbenches for each problem should be uploaded.

NOTE: Please **DO NOT** include source code in the paper report!

1. All homework requirements should be uploaded in this file hierarchy or you will not get the full credit.

NOTE: Please **DO NOT** upload waveforms!

1. Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.
2. **If you upload a dead body which we can’t even compile you will get NO credit!**
3. **All Verilog file should get at least 90% superLint Coverage.**
4. **File hierarchy should not be changed; it may cause** your code can not be recompiled by TA successfully using the autograding commands

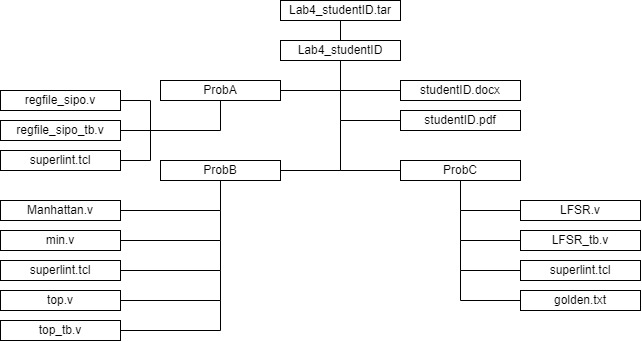


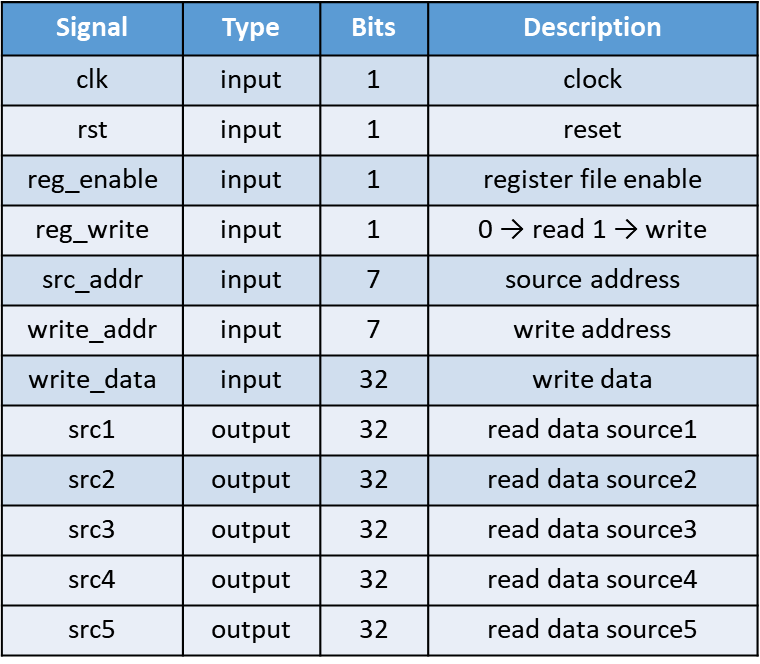
Fig.1 File hierarchy for Homework submission

Prob A: SIPO Register File

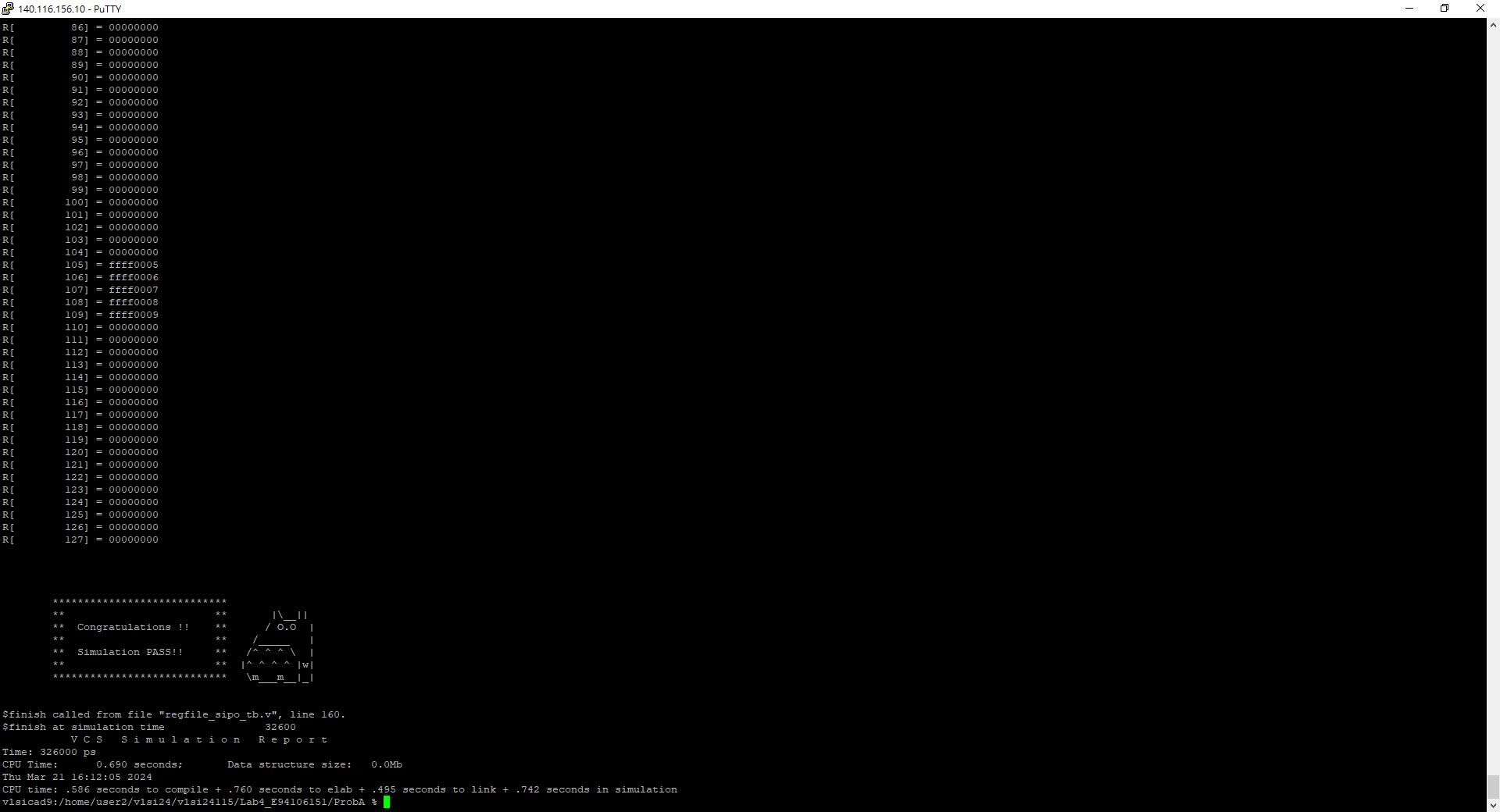
一張含有 文字, 圖表, 數字, 字型 的圖片

自動產生的描述

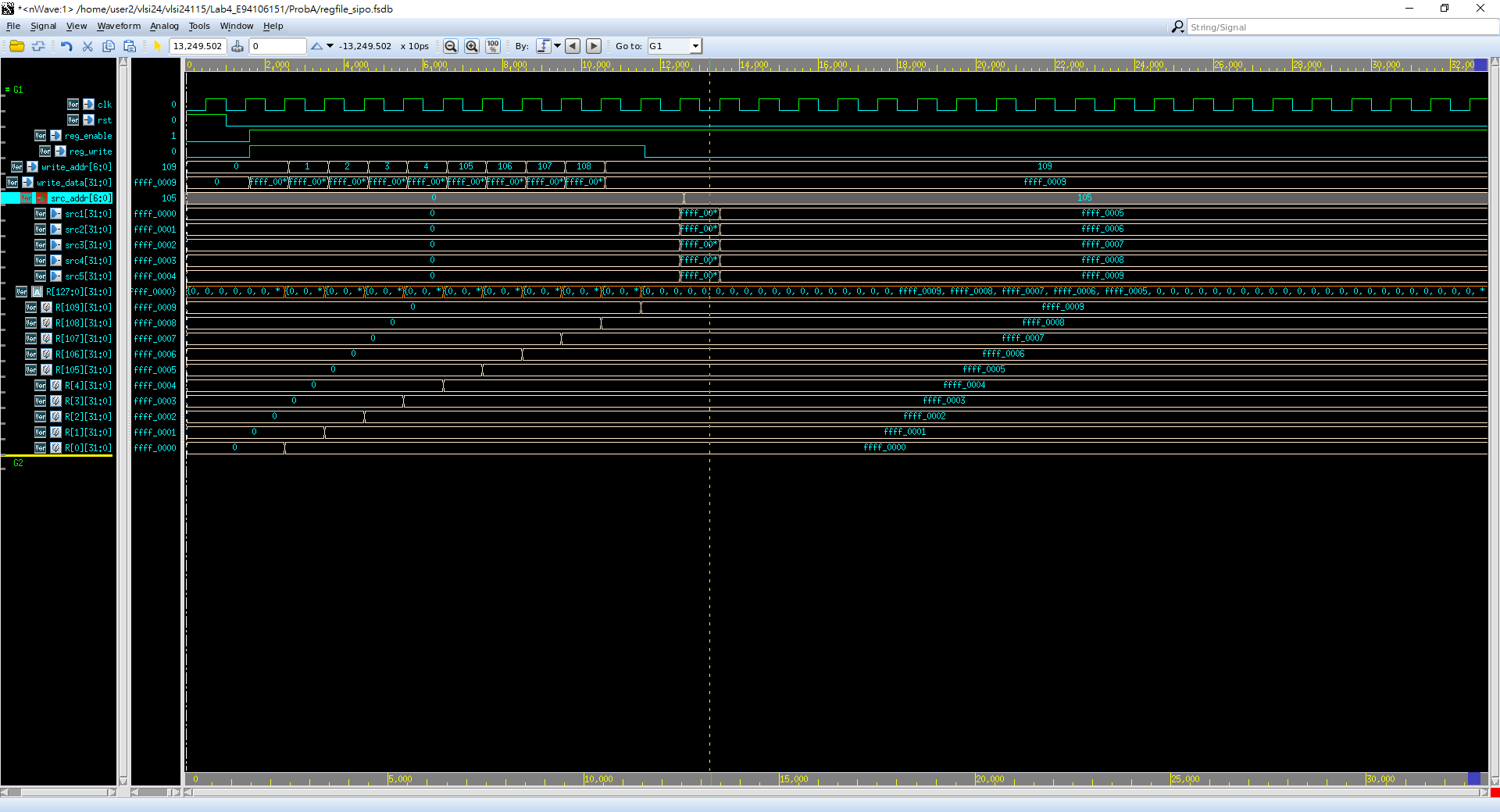
1. Based on the SIPO register file structure in LabA, please design a 128 x 32 SIPO register file with 5 output ports.
2. Port list



1. Show the simulation result on the terminal.



1. Show waveforms to explain that your register work correctly when read and write.



read

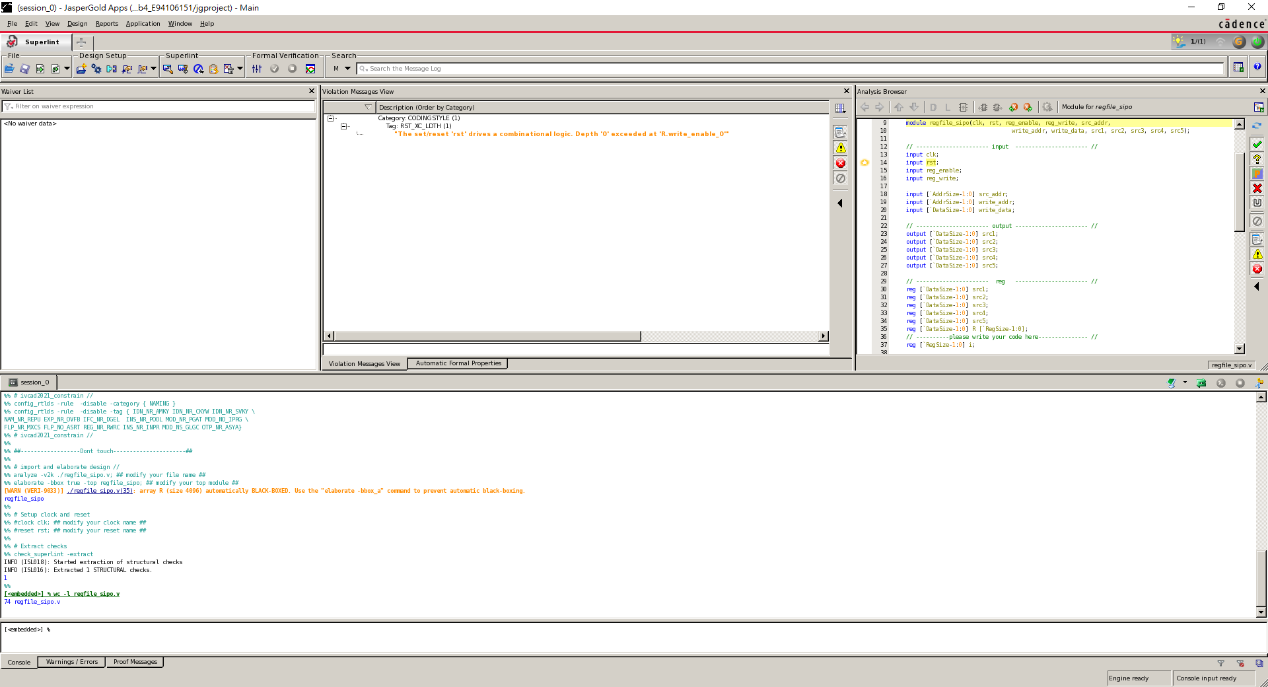
write

Read: 從標示出的位置可以看到要讀取的位址(src\_addr)為0到0+4=4，根據register(R)可以看出R[0] = 32’hffff0000, R[1] = 32’hffff0001, R[2] = 32’hffff0002, R[3] = 32’hffff0003, R[4] = 32’hffff0004，對應到輸出src1 = R[0] = 32’hffff0000, src2 = R[1] = 32’hffff0001, src3 = R[2] = 32’hffff0002, src4 = R[3] = 32’hffff0003, src5 = R[4] = 32’hffff0004。

Write: 從標示出的位置可以看到要寫入的位址(write\_addr)為0、要寫入的值(write\_data)為32’hffff0000，根據register(R)可以看出輸入後R[0] = 32’hffff0000。

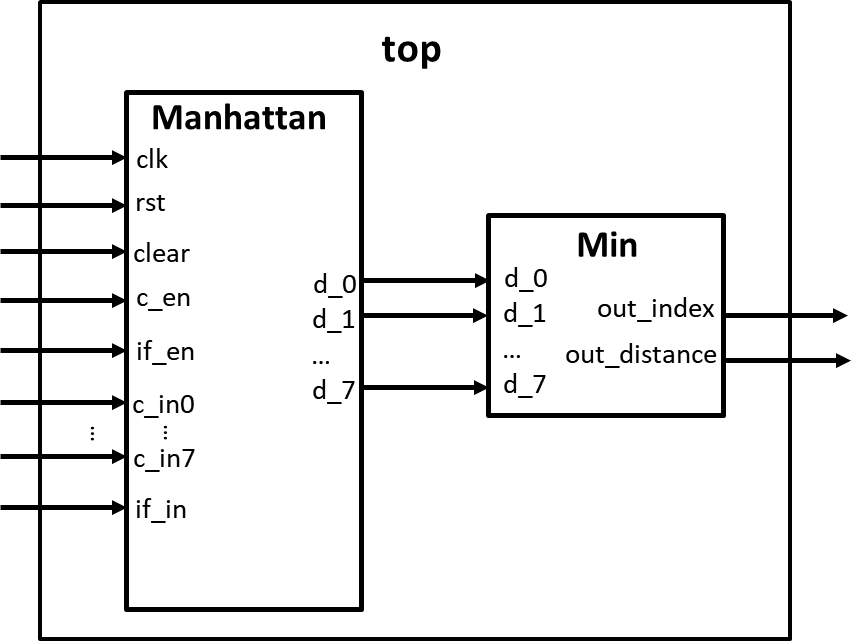
由此可知register有正常運作。

1. Show SuperLint coverage



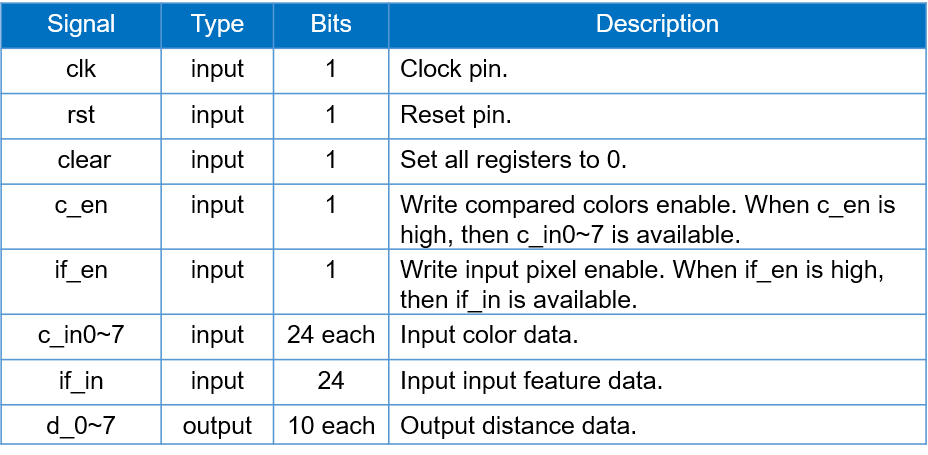
Coverage = (1-(1/74))\*100% = 98.65%

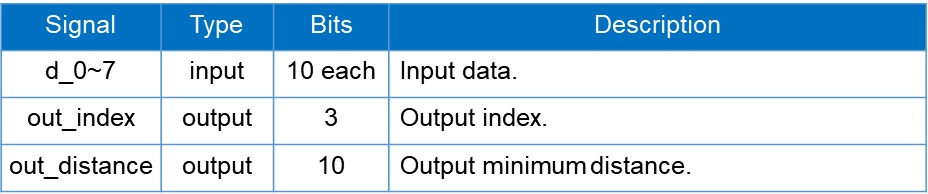
Prob B: Finding Smallest Distance



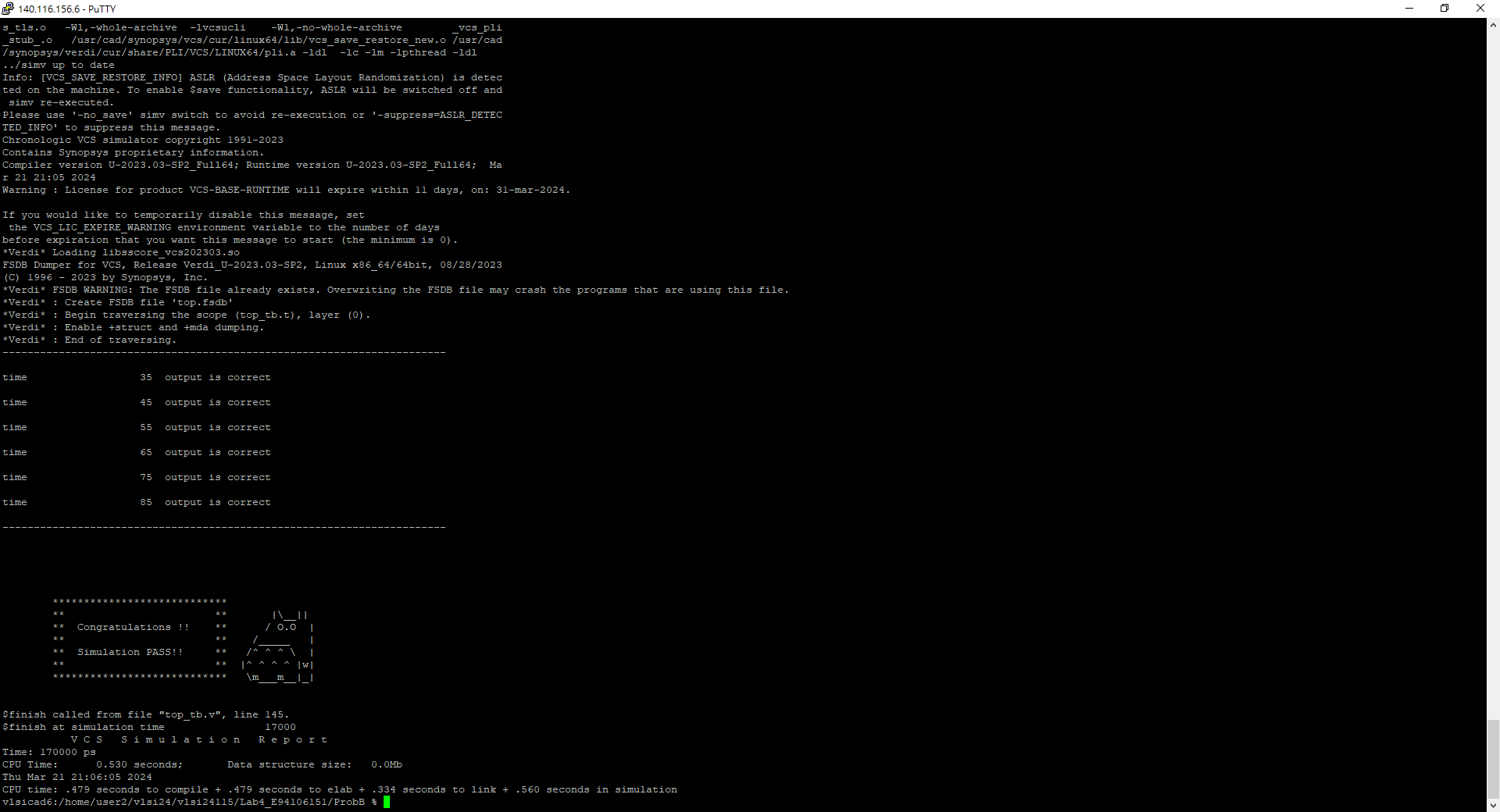
1. Please design a circuit that will find the smallest distance between the input feature and input colors, based on the structure given in the LAB4 slide.
2. Port list

Manhattan:

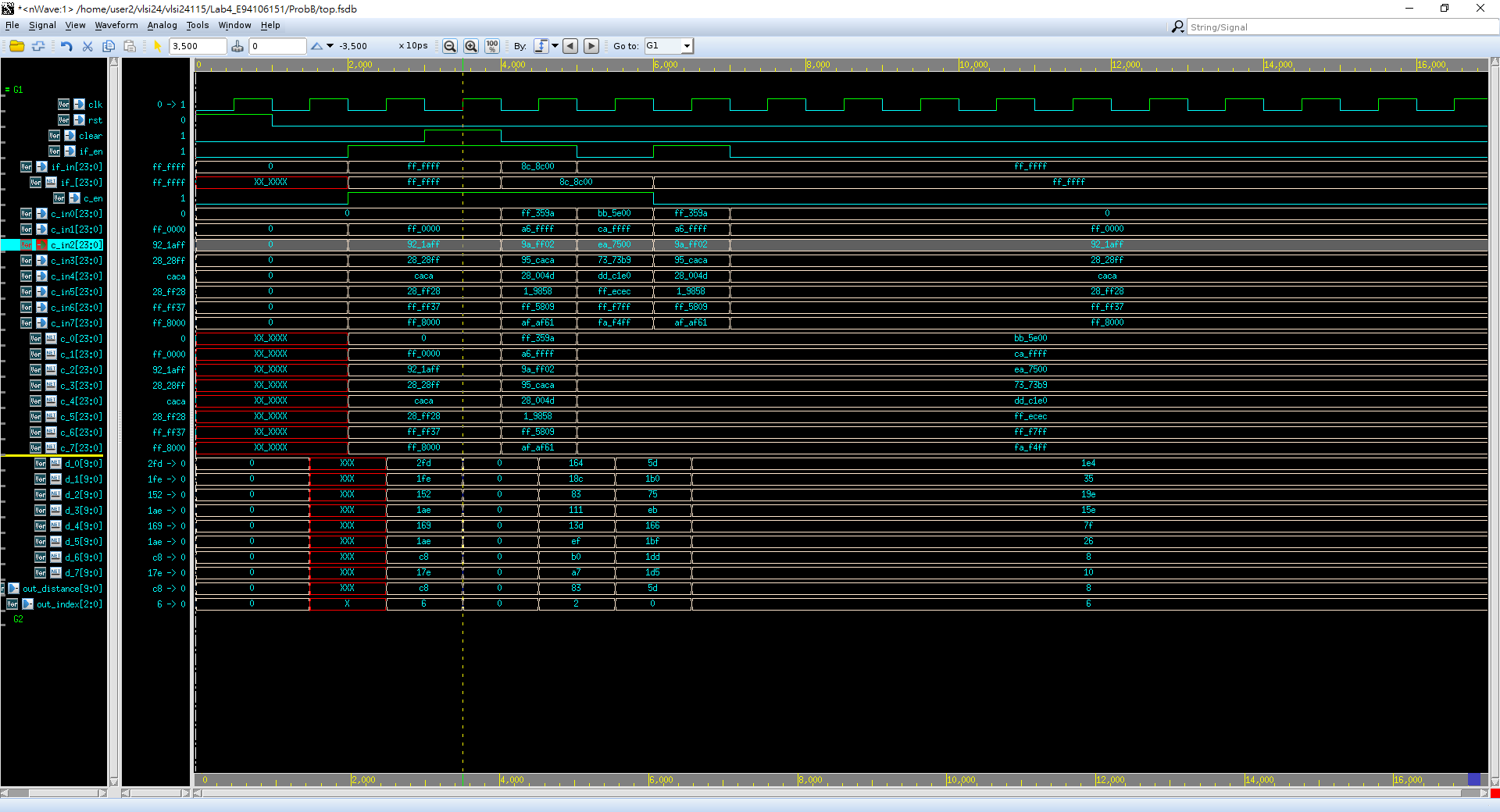
Min:



1. Show the simulation result on the terminal.

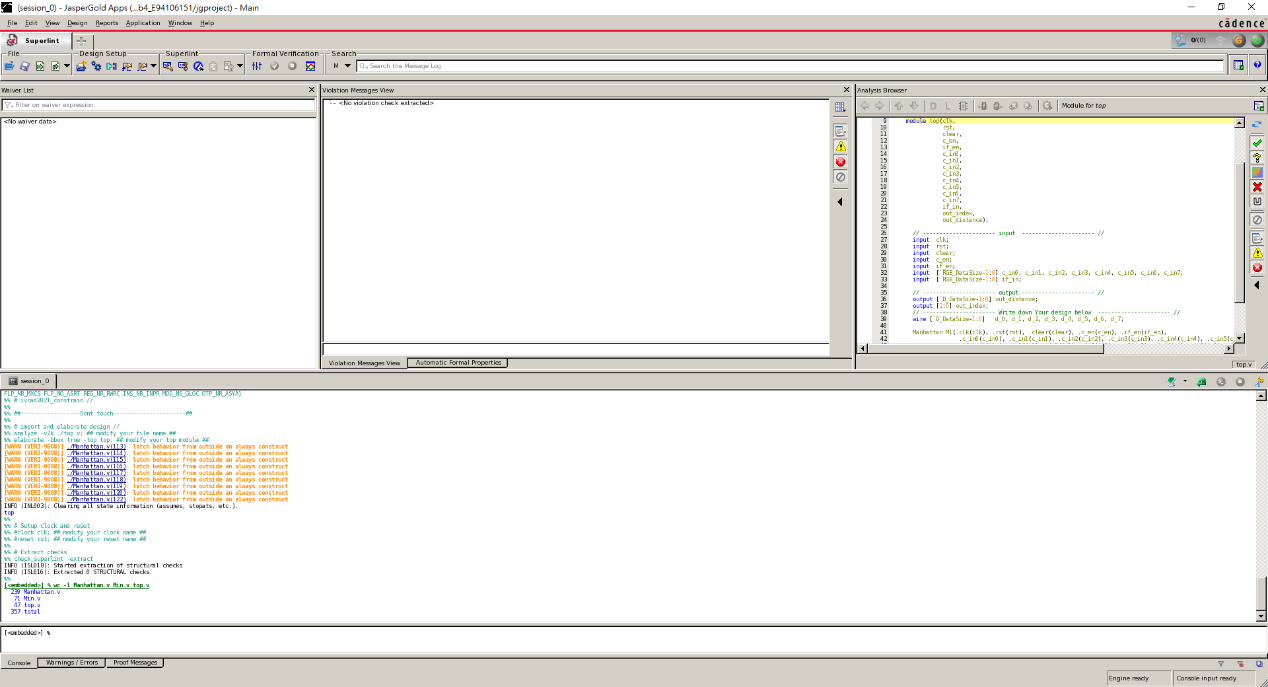


1. Show waveforms to explain that your design works correctly.



根據所標示的位置，Input feature data為if\_en = 24’hffffff(255, 255, 255)，Input color data 6為c\_in6 = 24’hffff37(255, 255, 55)，相差distance data為d\_6 = 10’h0c8(200)是相比其他輸入差最少的，所以output minimum distance為out\_distance = 10’h0c8，output index為out\_index = 3’h6。

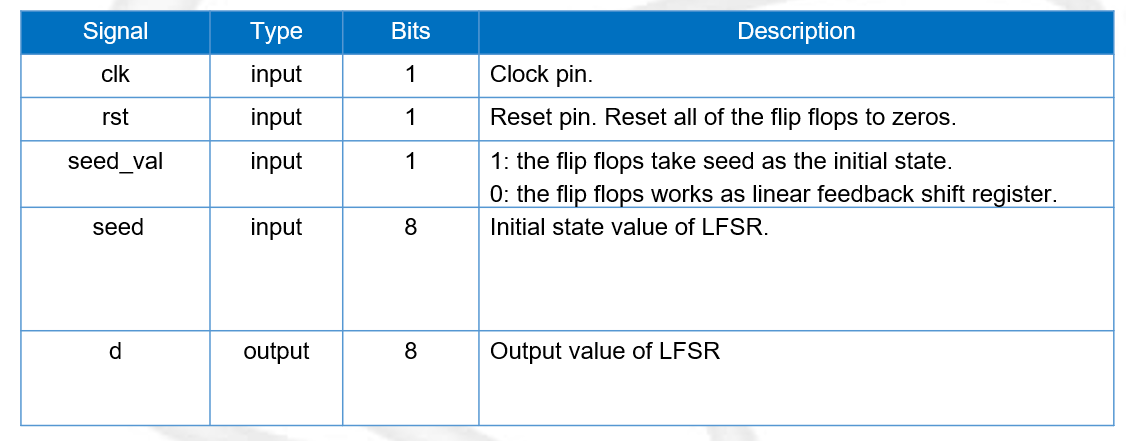
1. Show SuperLint coverage



Coverage = (1-(0/357))\*100% = 100%

Prob C: LFSR

1. Please design an 8-bit-LFSR, with the given feedback function in the LAB4 slide.
2. Port list



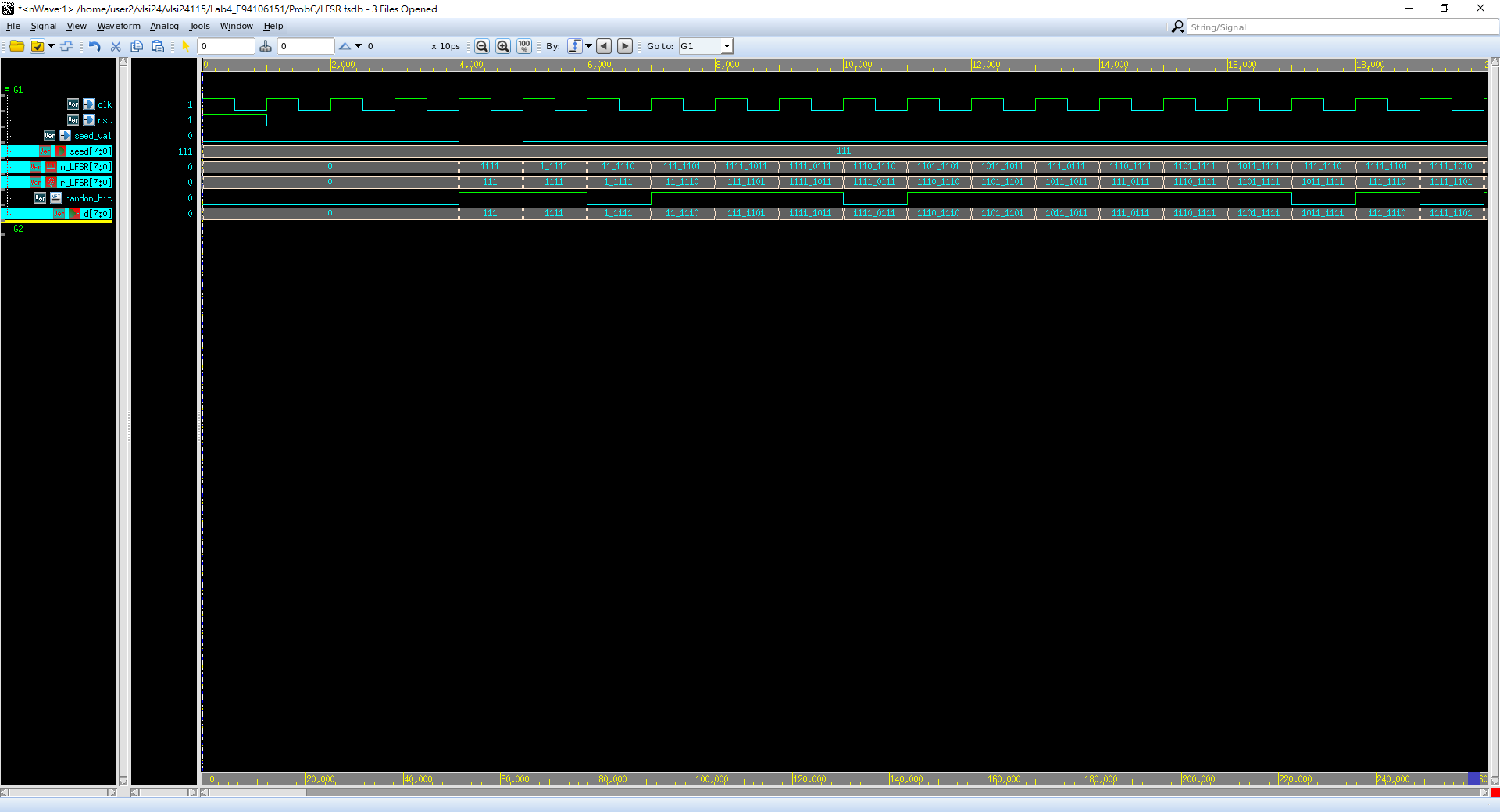
1. Feedback function

***d[0] = ( d[7] ^ d[5] ) ^ ( d[4] ^ d[2] )***

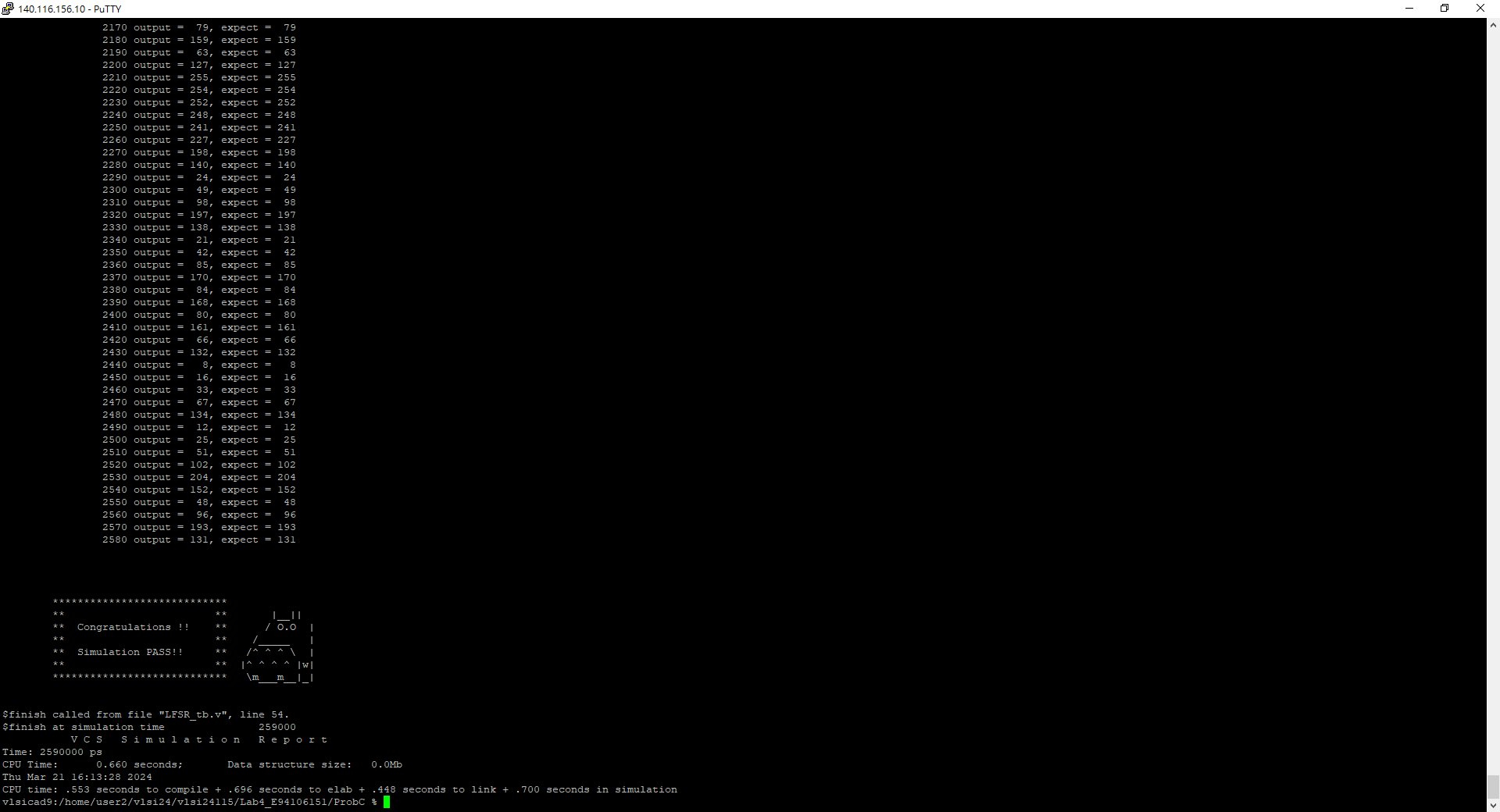
1. Show waveforms to explain that your LFSR module works correctly.

一張含有 螢幕擷取畫面, 文字, 電腦, 軟體 的圖片

自動產生的描述

從標示的位置可以看到在seed\_val為1時，seed = 8’b00000111有確實輸入進電路當中(d = 8’b00000111)，而在下一個clk posdege時，根據Feedback function對應d[0] = (d[7] ^ d[5]) ^ (d[4] ^ d[2]) = (0 ^ 0) ^ (0 ^ 1) = 0 ^ 1 = 1，可得d = 8’b00001111。

1. Show the simulation result on the terminal.



1. Show SuperLint coverage

一張含有 文字, 螢幕擷取畫面, 軟體, 陳列 的圖片

自動產生的描述

Coverage = (1-(0/32))\*100% = 100%

At last, please write the lesson you learned from Lab4

在這次的實驗課中我學到我們在計算機組織中上到的register file是是如何透過verilog實作出來的，讓我更了解計算機的架構。此外還學到了Manhattan和Euclidean兩種不同計算相對距離的方法，其中Manhattan是這次第二題所用到的方法，我想如果要用verilog實作出影像辨識，這應該會是其中一小部分吧？最後是我第一次接觸到的LFSR，我從來沒想過原來我們可以用這種方法用電路實作出接近隨機的數字產生器，沒想過原來D type Flip-Flop也有如此功用，讓我大開眼界。

Appendix A : Commands we will use to check your homework

