Русенски университет “Ангел Кънчев” Факултет
“Електротехника, електроника и автоматика” Дисциплина
“Цифрова Схемотехника”

Курсова работа Вариант 5

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Георги Чапъров,
Преслав Георгиев

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група: 26А
курс 2

/доц. д-р Адриана Бороджиева/

2024.19.04

1) кратки теоретични данни за броячите и синтез на синхронни броячи

Броячът е устройство, което регистрира броя на постъпилите на входа му импулси, като състоянието на брояча еднозначно се определя от броя на входните импулси. Най-простият брояч представлява един тригер, с който могат да се преброят два импулса.

Броячите могат да се разделят на:

I. В зависимост от системата на броене:
- кръгови
- двоични
- двоично-десетично

II. В зависимост от организацията на връзките между тригерите:
- асинхронни
- синхронни
- комбинирани

III. В зависимост от начина на броене:
- сумиращи
- изваждащи
- реверсивни
- с произволен ред на броене

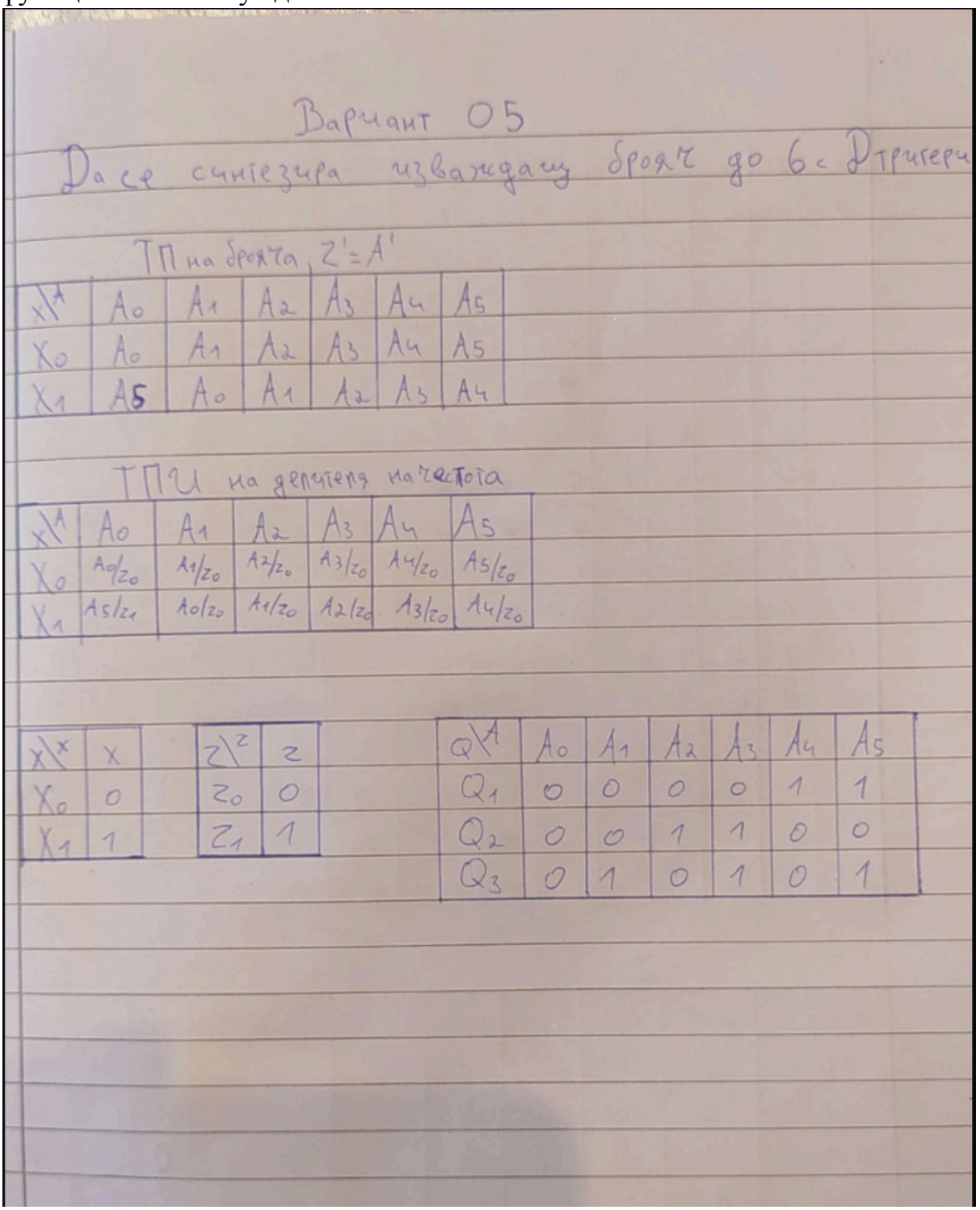
Синтез на синхронни броячи:

Синхронните броячи се създават чрез свързване на поредица от флип-флопи.

При всеки входящ импулс, стойността на брояча се увеличава с едно.

Общият брой на възможните състояния е равен на 2 на степен n, където n е броят на флип-флопите.

2) Таблици на преходите и изходите, кодиране на входните думи, изходните думи и вътрешните състояния, на преходите и изходите и функциите на възбуждане на елементите памет



Вариант 05

Да се синтезира изваждащ брояч до 6 с D тригери

ТП на броята, $Z' = A'$

$x \backslash A$	A_0	A_1	A_2	A_3	A_4	A_5
X_0	A_0	A_1	A_2	A_3	A_4	A_5
X_1	A_5	A_0	A_1	A_2	A_3	A_4

ТПИ на делителя на честота

$x \backslash A$	A_0	A_1	A_2	A_3	A_4	A_5
X_0	A_0/z_0	A_1/z_0	A_2/z_0	A_3/z_0	A_4/z_0	A_5/z_0
X_1	A_5/z_1	A_0/z_0	A_1/z_0	A_2/z_0	A_3/z_0	A_4/z_0

$x \backslash x$	x
X_0	0
X_1	1

$z \backslash z$	z
z_0	0
z_1	1

$Q \backslash A$	A_0	A_1	A_2	A_3	A_4	A_5
Q_1	0	0	0	0	1	1
Q_2	0	0	1	1	0	0
Q_3	0	1	0	1	0	1

№	x^t	A^t			A^{t+1}			z^t	y^t		
		Q_1^t	Q_2^t	Q_3^t	Q_1^{t+1}	Q_2^{t+1}	Q_3^{t+1}		D_1^t	D_2^t	D_3^t
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1	0	0	0	1
2	0	0	1	0	0	1	0	0	0	1	0
3	0	0	1	1	0	1	1	0	0	1	1
4	0	1	0	0	1	0	0	0	1	0	0
5	0	1	0	1	1	0	1	0	1	0	1
6	0	1	1	0	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ
7	0	1	1	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ
8	1	0	0	0	1	0	1	1	1	0	1
9	1	0	0	1	0	0	0	0	0	0	0
10	1	0	1	0	0	0	1	0	0	0	1
11	1	0	1	1	0	1	0	0	0	1	0
12	1	1	0	0	0	1	1	0	0	1	1
13	1	1	0	1	1	0	0	0	1	0	0
14	1	1	1	0	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ
15	1	1	1	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ

z

xQ_1 \ Q_2Q_3	00	01	11	10
00	0	0	0	0
01	0	0	ϕ	ϕ
11	0	0	ϕ	ϕ
10	1	0	0	0

D_1

xQ_1 \ Q_2Q_3	00	01	11	10
00	0	0	0	0
01	1	1	ϕ	ϕ
11	0	1	ϕ	ϕ
10	1	0	0	0

D_2

xQ_1 \ Q_2Q_3	00	01	11	10
00	0	0	1	1
01	0	0	ϕ	ϕ
11	1	0	ϕ	ϕ
10	0	0	1	0

D_3

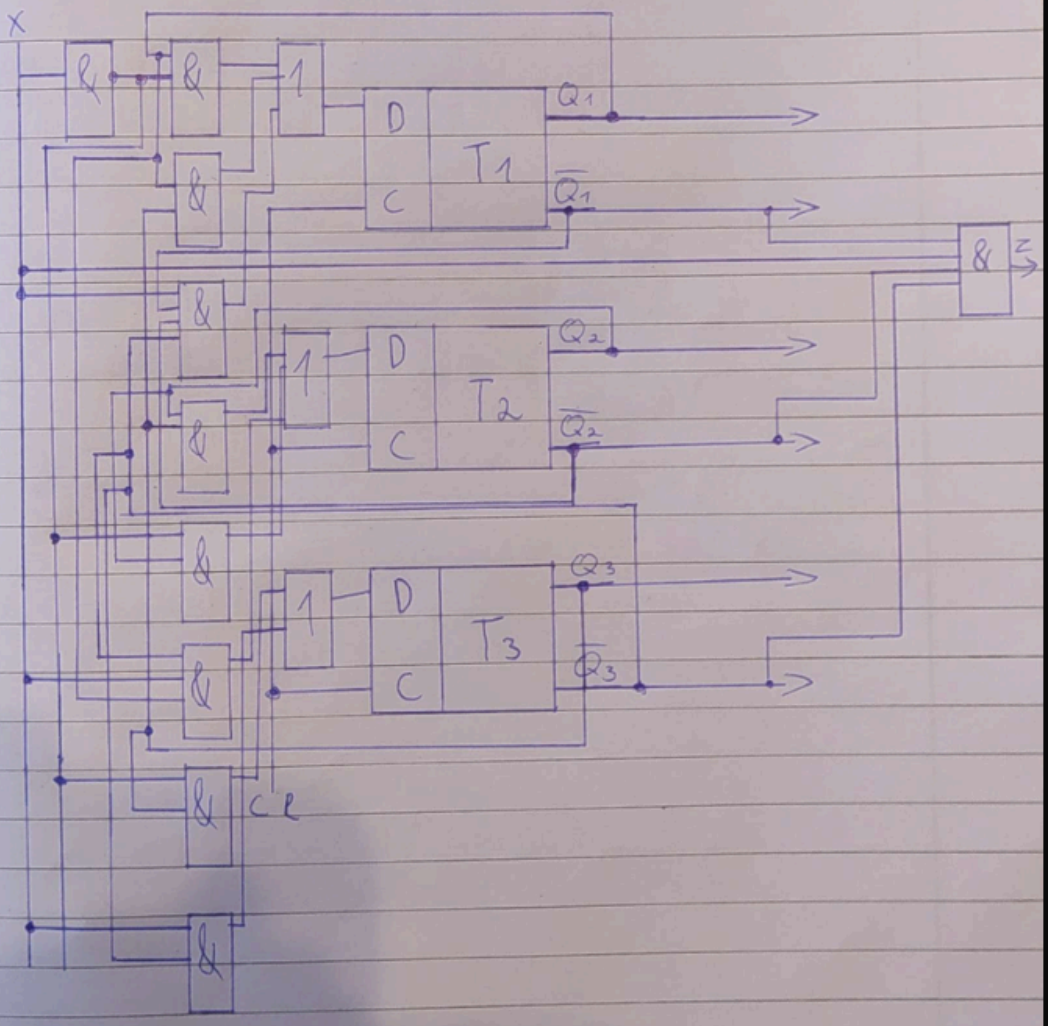
xQ_1 \ Q_2Q_3	00	01	11	10
00	0	1	1	0
01	0	1	ϕ	ϕ
11	1	0	ϕ	ϕ
10	1	0	0	1

$Z = x \cdot \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3$

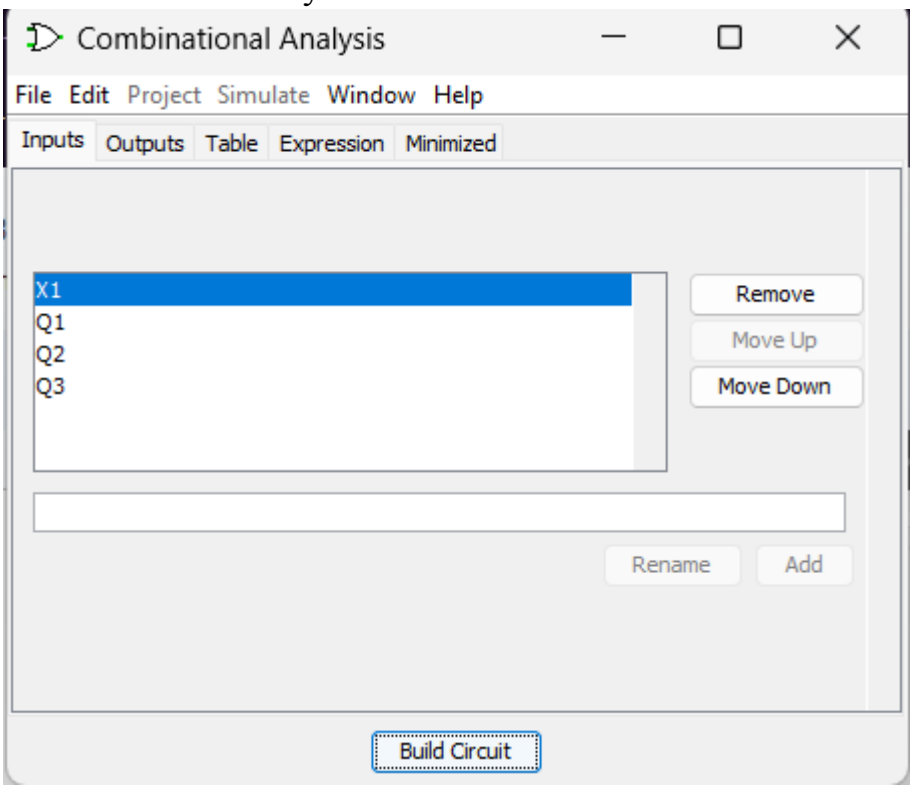
$D_1 = \bar{x} \cdot Q_1 \vee Q_1 \cdot Q_3 \vee x \cdot \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3$

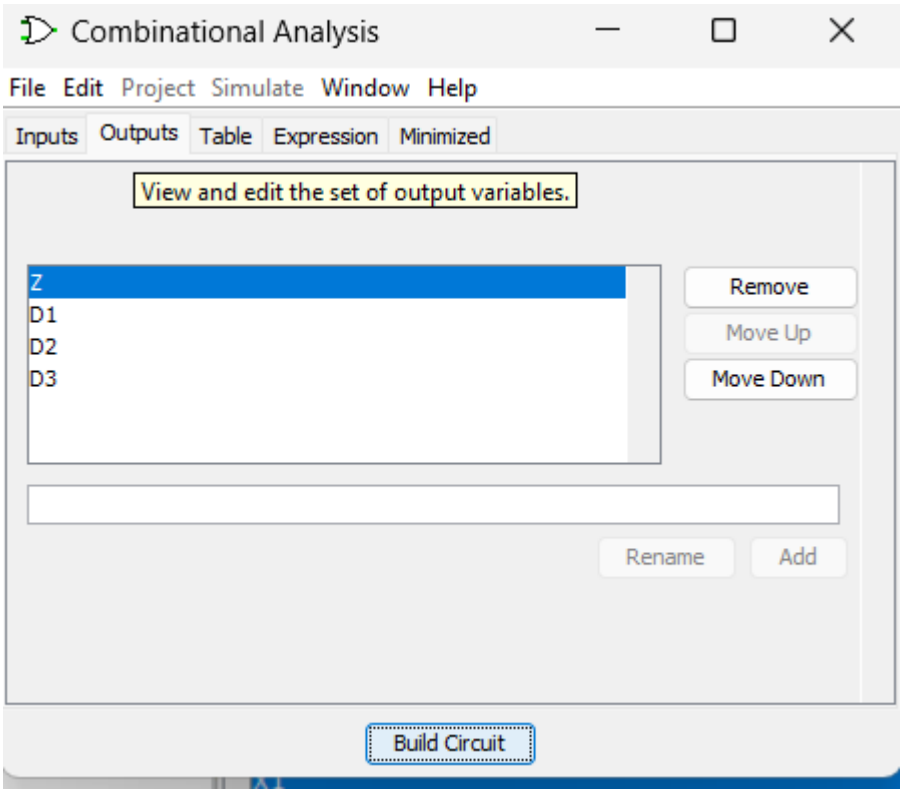
$D_2 = Q_2 \cdot Q_3 \vee \bar{x} \cdot Q_2 \vee \bar{Q}_3 \cdot x \cdot Q_1$

$D_3 = \bar{x} \cdot Q_3 \vee x \cdot \bar{Q}_3$

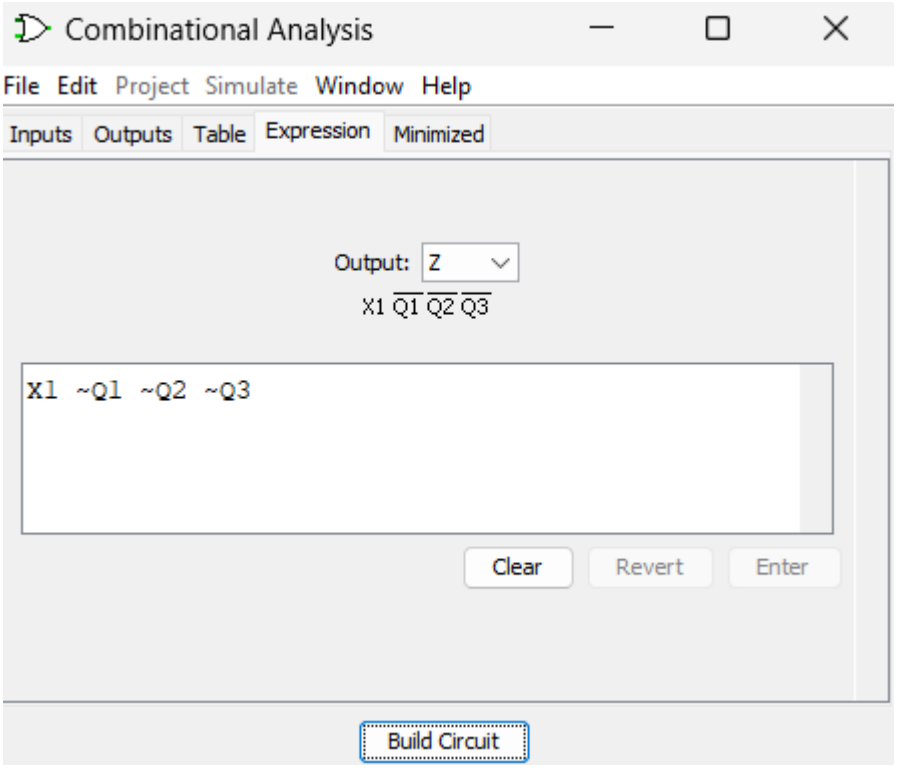


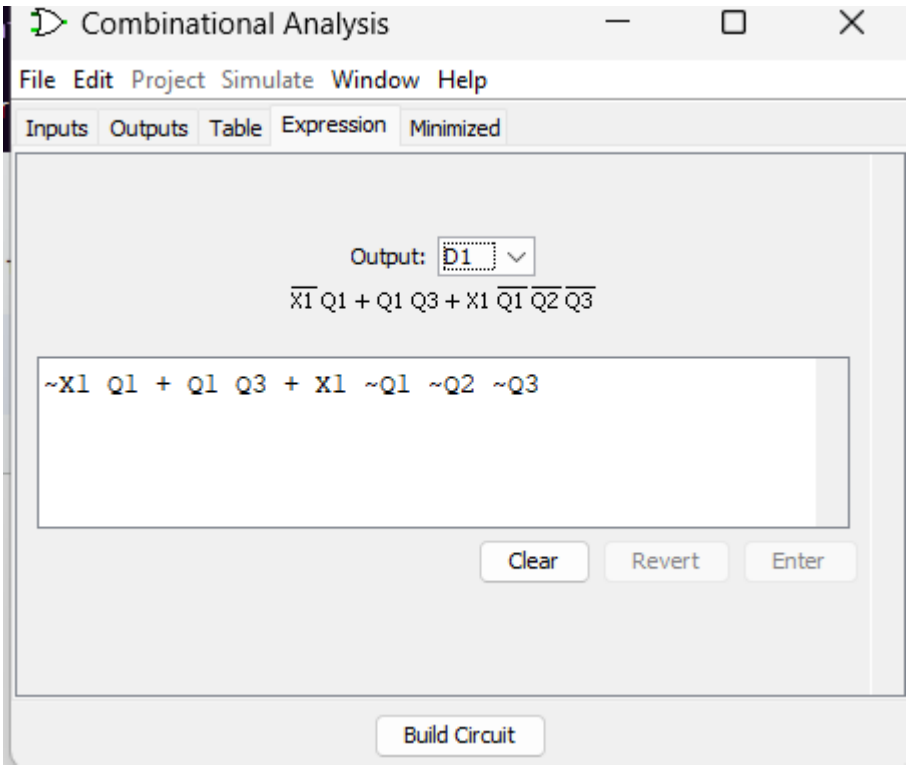
3) стъпките на самия синтез при използване на опцията Combinational Analysis

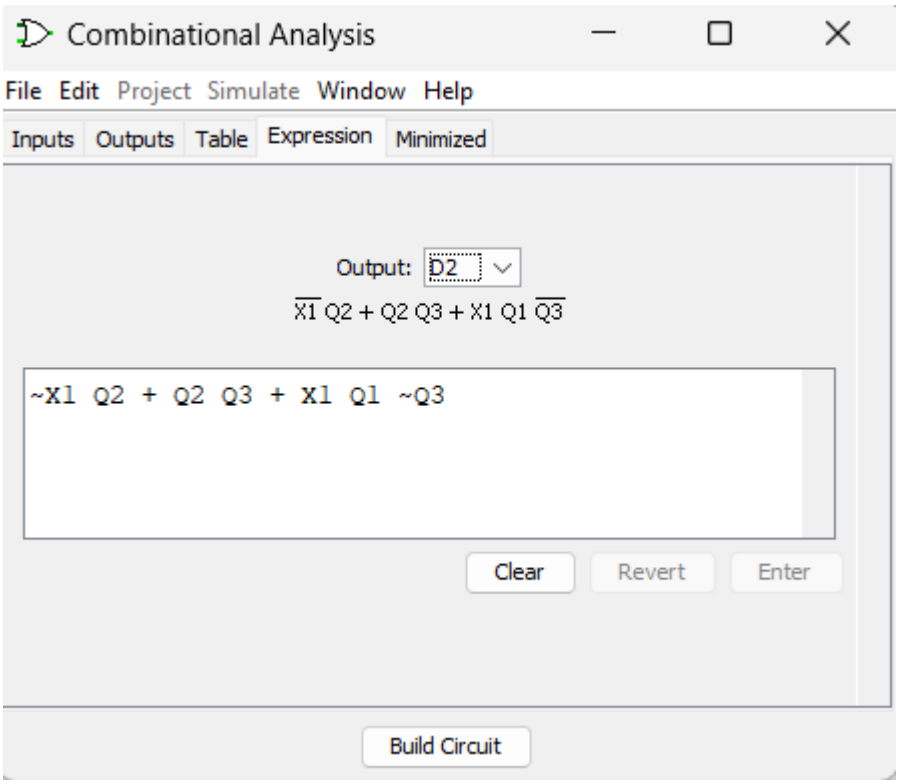


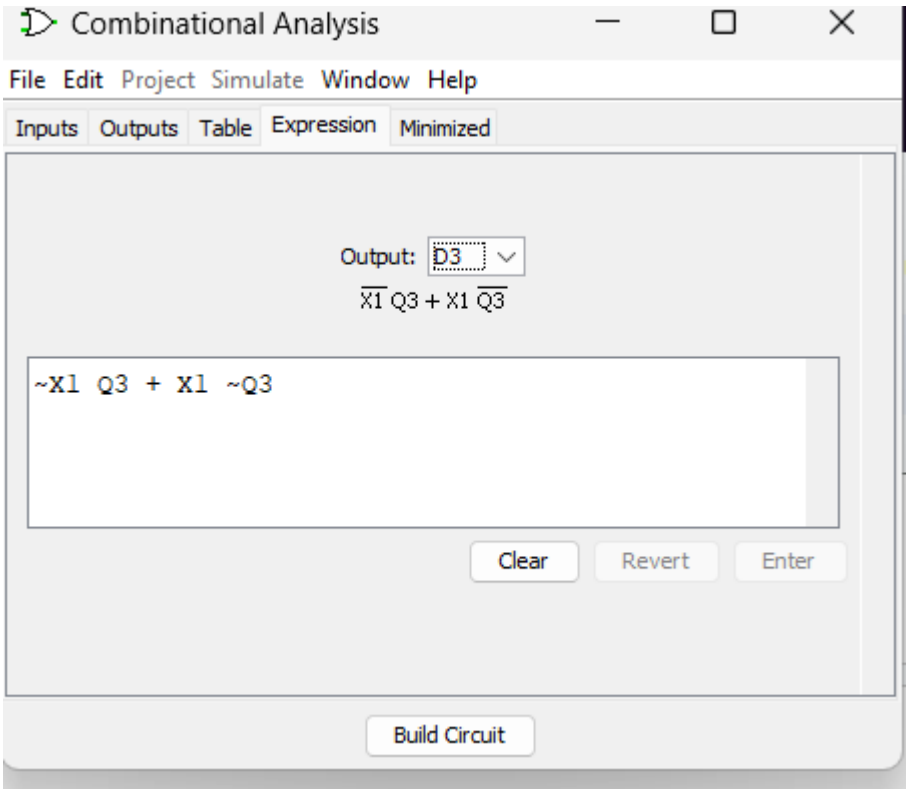


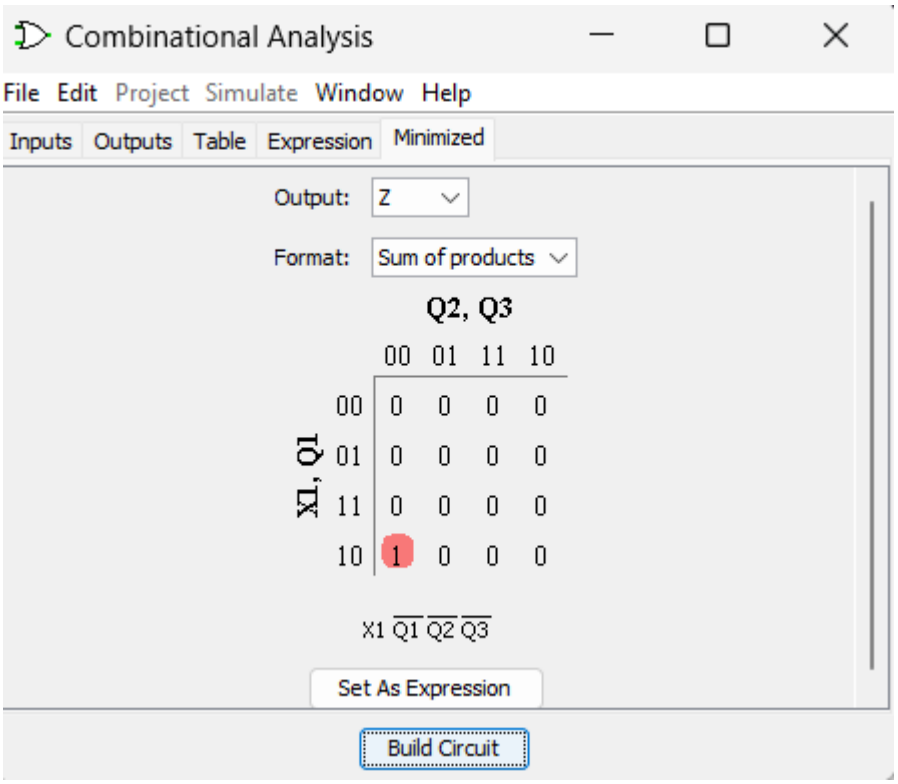
X1	Q1	Q2	Q3	Z	D1	D2	D3
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	1	1	1	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	1	1
1	1	0	1	0	1	0	0
1	1	1	0	1	0	1	1
1	1	1	1	1	1	1	0

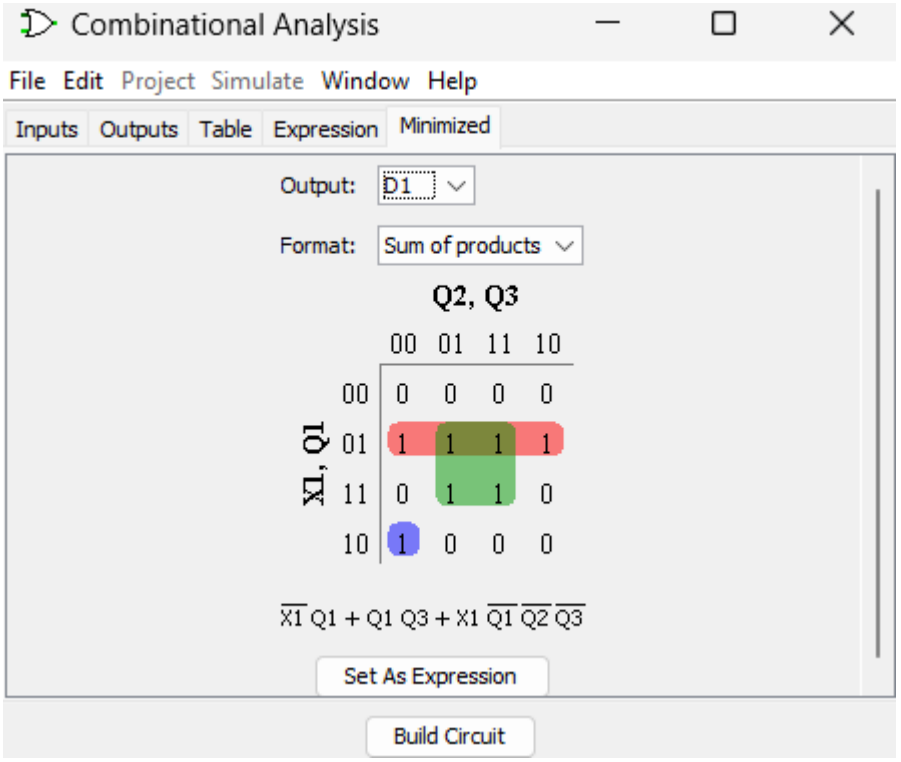


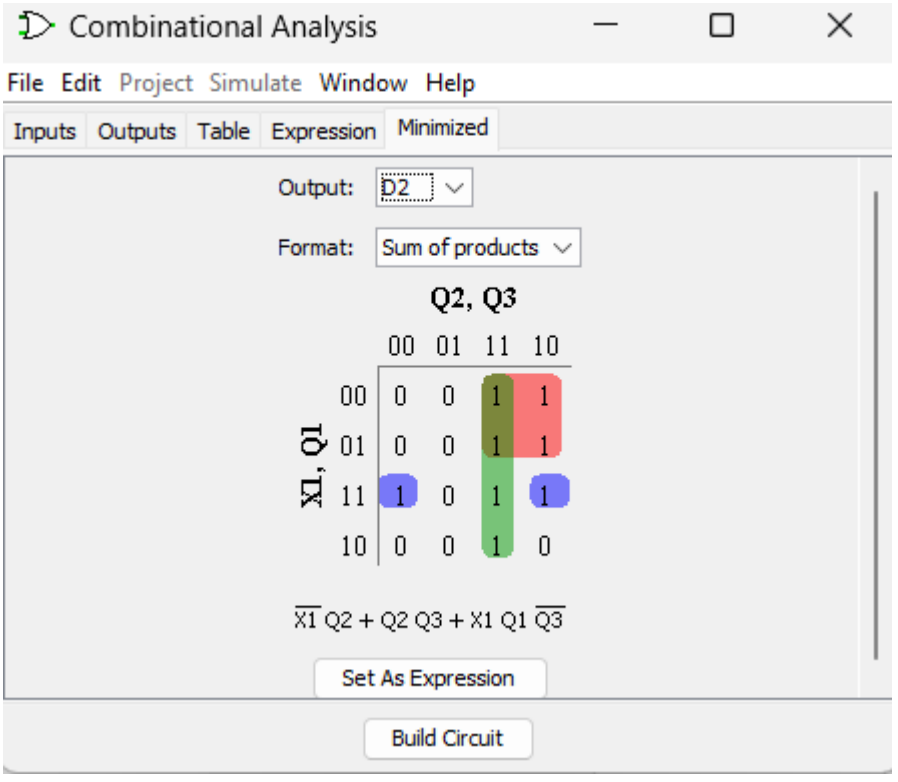

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: D1
$\overline{X1}\ Q1 + Q1\ Q3 + X1\ \overline{Q1}\ \overline{Q2}\ \overline{Q3}$
~X1 Q1 + Q1 Q3 + X1 ~Q1 ~Q2 ~Q3
Clear
Revert
Enter
Build Circuit

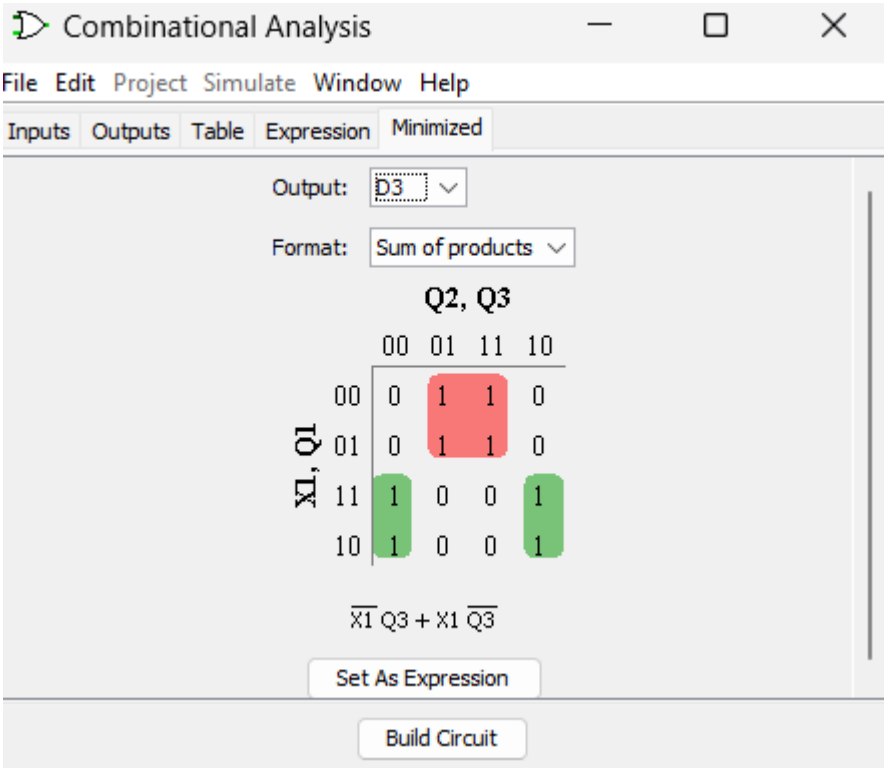

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: D2
$\overline{X1}\ Q2 + Q2\ Q3 + X1\ Q1\ \overline{Q3}$
~X1 Q2 + Q2 Q3 + X1 Q1 ~Q3
Clear
Revert
Enter
Build Circuit


Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: D3
$\overline{X1}\ Q3 + X1\ \overline{Q3}$
~X1 Q3 + X1 ~Q3
Clear
Revert
Enter
Build Circuit

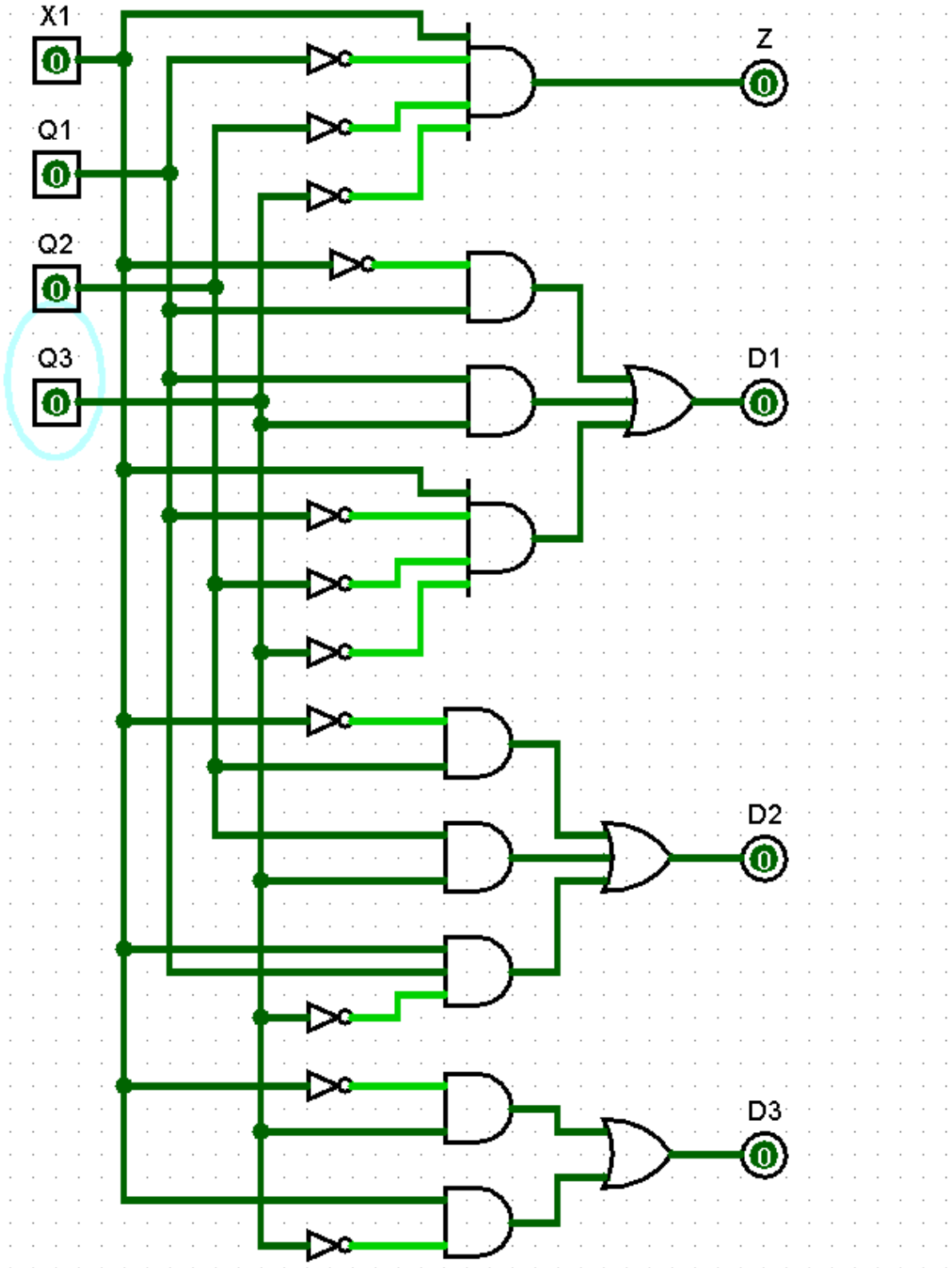

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: Z
Format: Sum of products
Q2, Q3
00 01 11 10
X1, Q1
00 0 0 0 0
01 0 0 0 0
11 0 0 0 0
10 1 0 0 0
$X1\ \overline{Q1}\ \overline{Q2}\ \overline{Q3}$
Set As Expression
Build Circuit

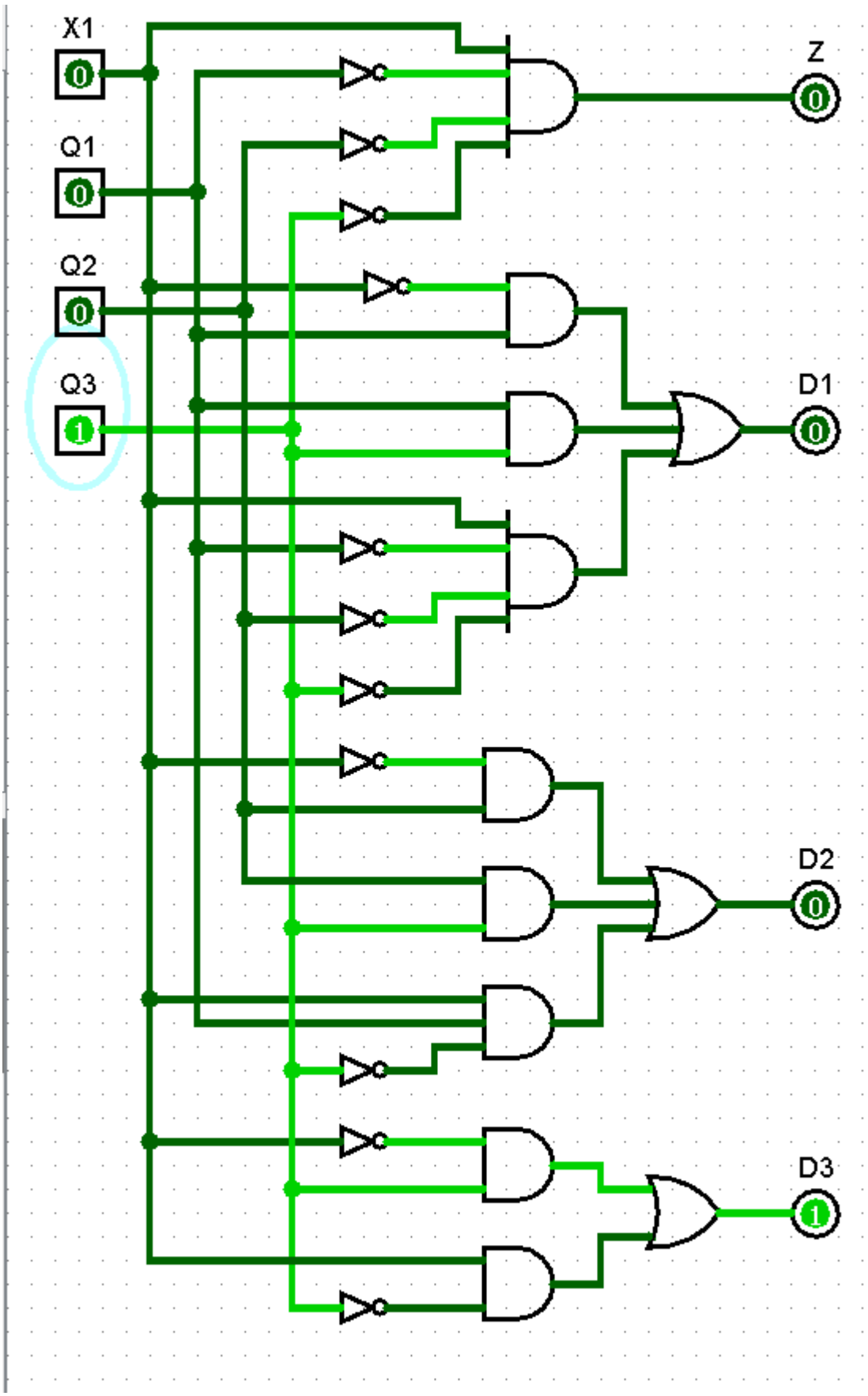

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: D1
Format: Sum of products
Q2, Q3
00 01 11 10
X1, Q1
00 0 0 0 0
01 1 1 1 1
11 0 1 1 0
10 1 0 0 0
X1 Q1 + Q1 Q3 + X1 Q1 Q2 Q3
Set As Expression
Build Circuit

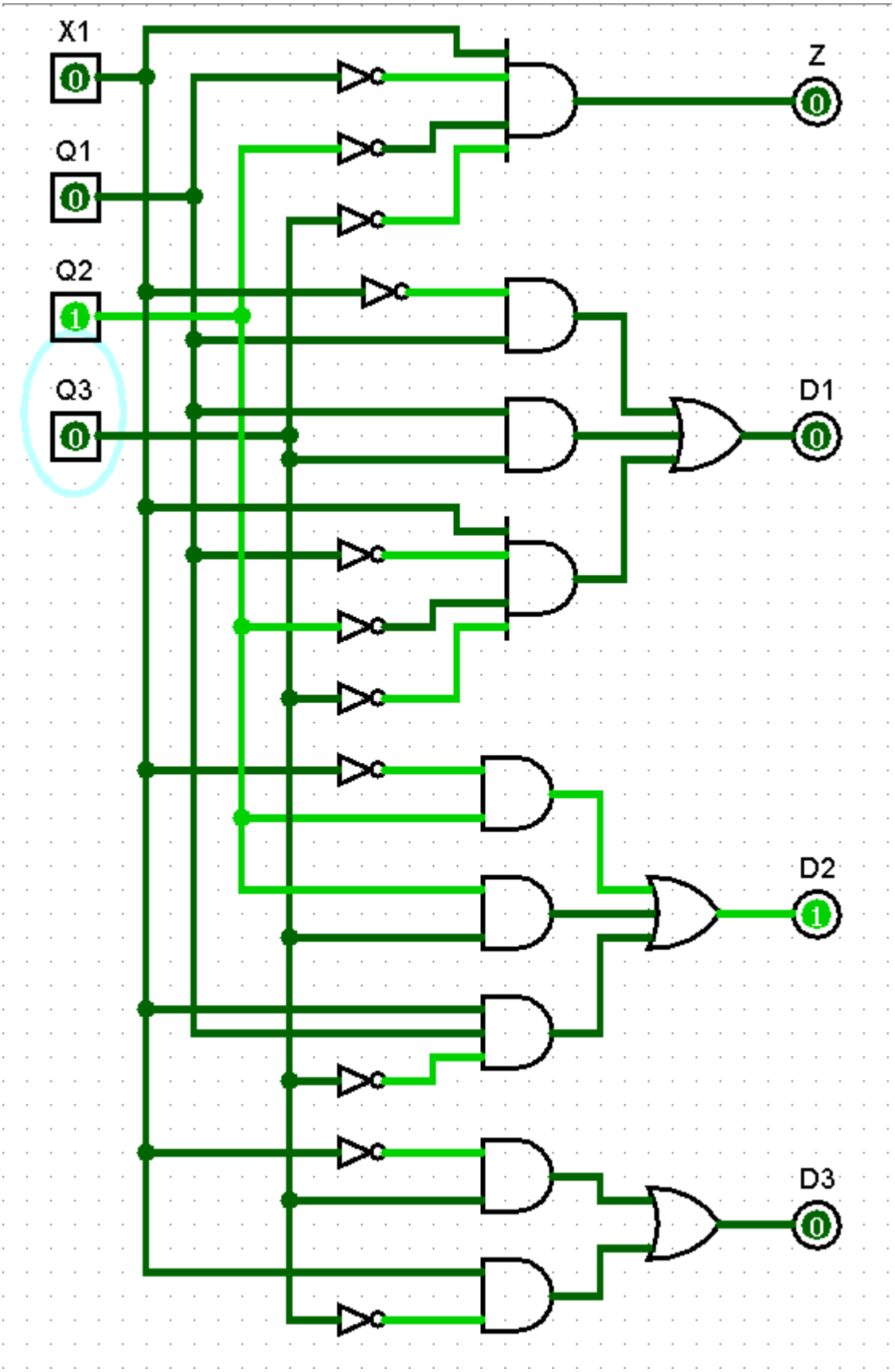

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: D2
Format: Sum of products
Q2, Q3
00 01 11 10
X1, Q1
00 0 0 1 1
01 0 0 1 1
11 1 0 1 1
10 0 0 1 0
X1 Q2 + Q2 Q3 + X1 Q1 Q3
Set As Expression
Build Circuit

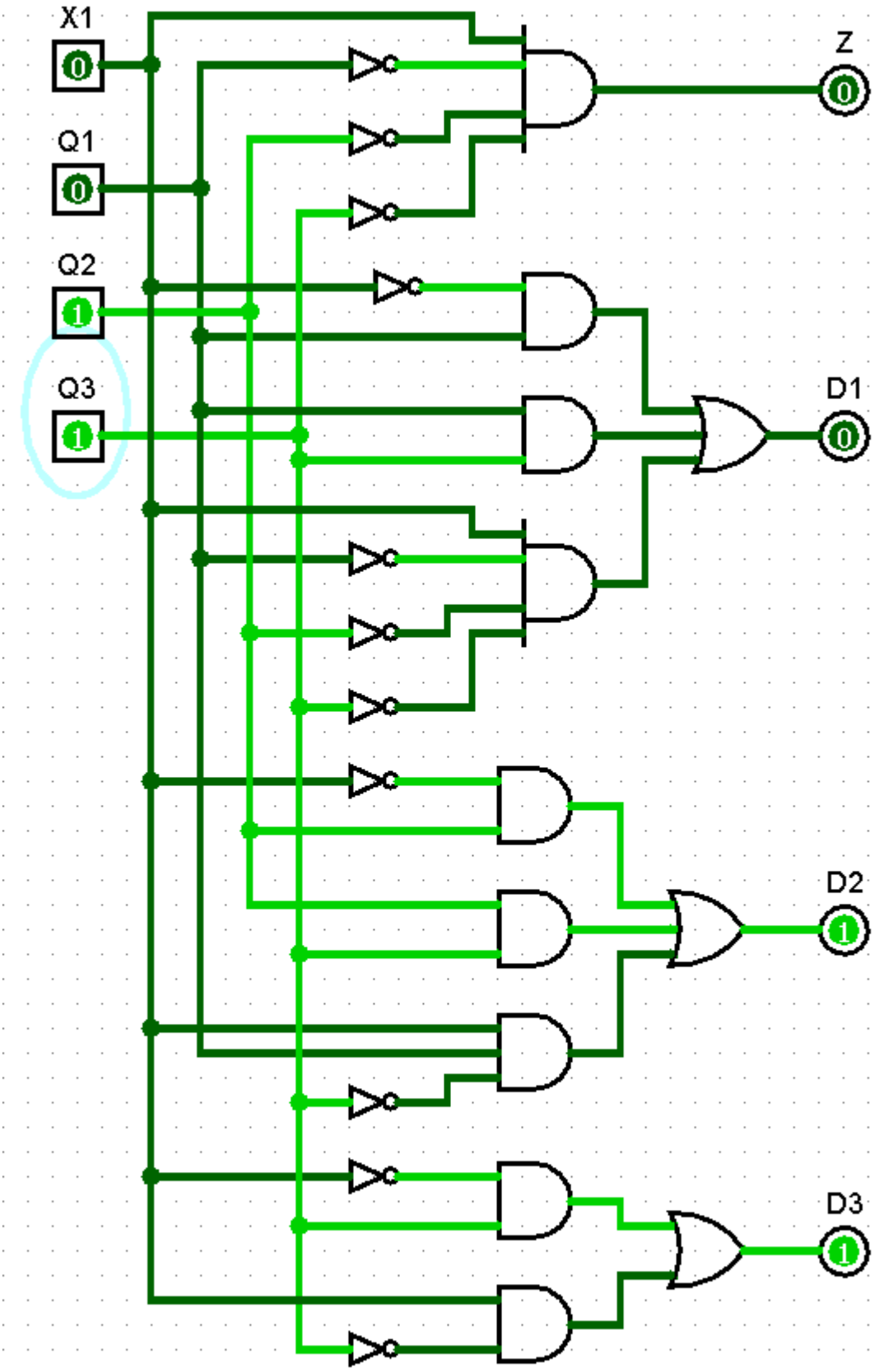

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: D3
Format: Sum of products
Q2, Q3
00 01 11 10
X1, Q1
00 0 1 1 0
01 0 1 1 0
11 1 0 0 1
10 1 0 0 1
X1 Q3 + X1 Q3
Set As Expression
Build Circuit

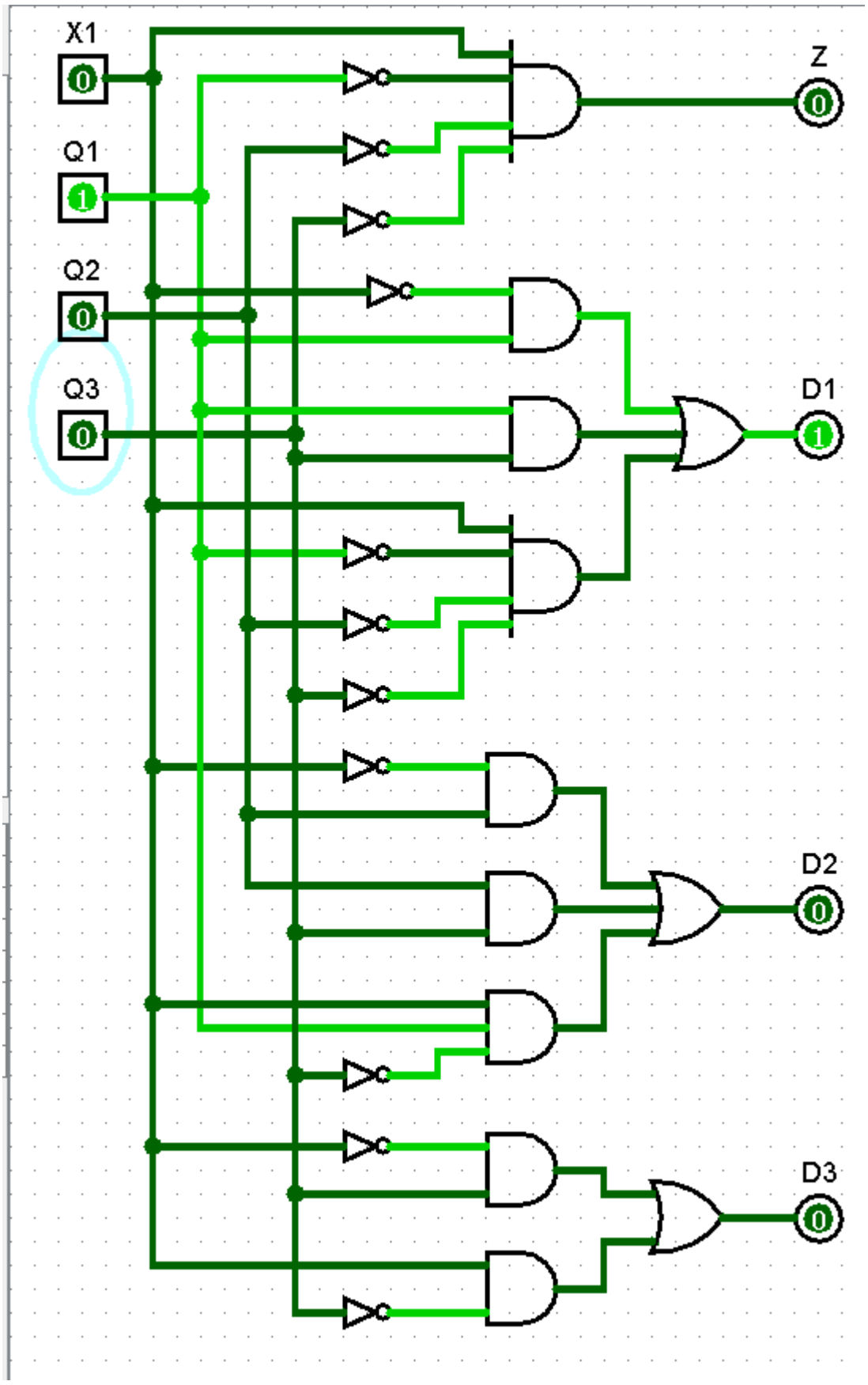
4) Автоматично генерирана схема

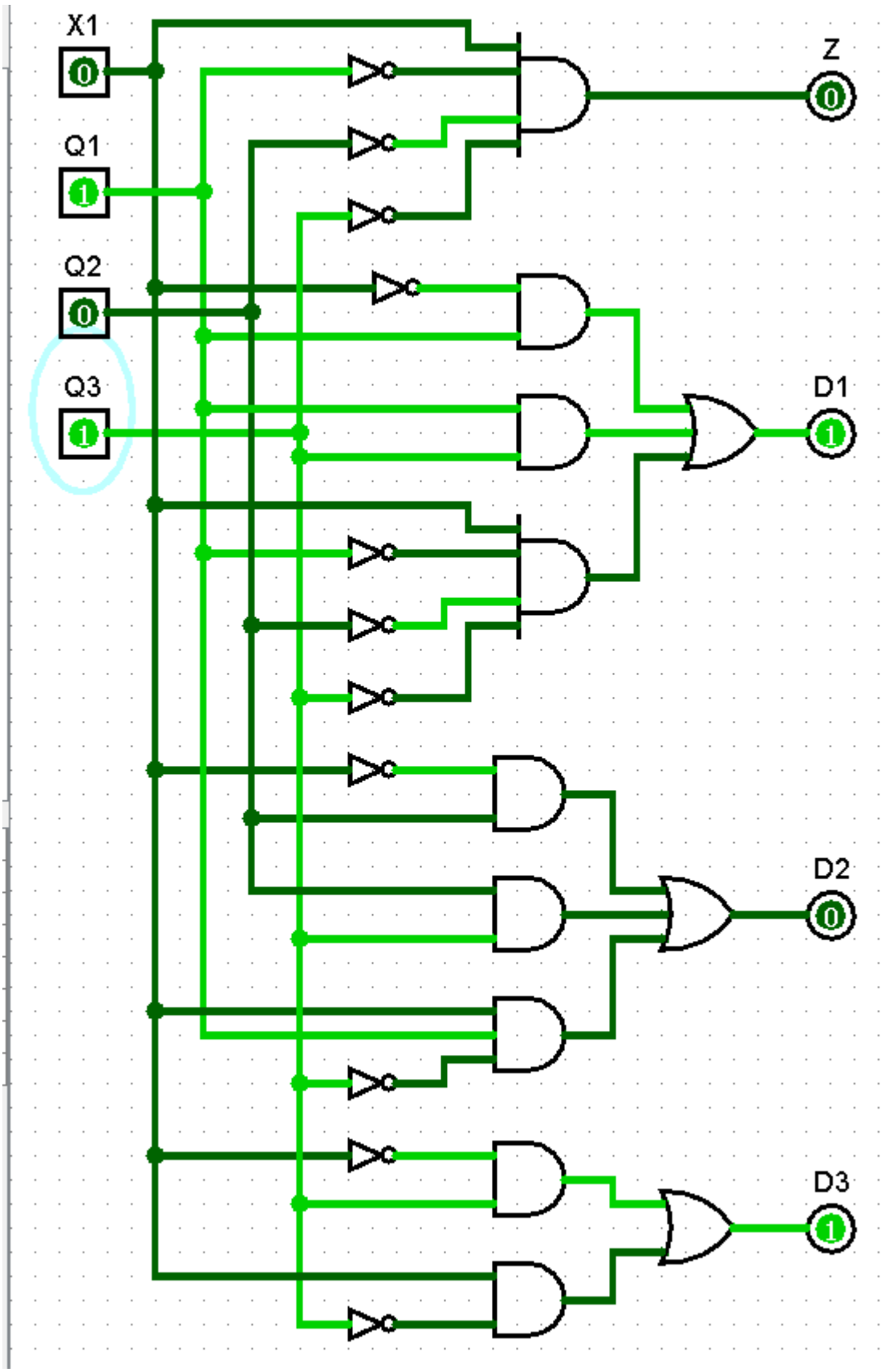


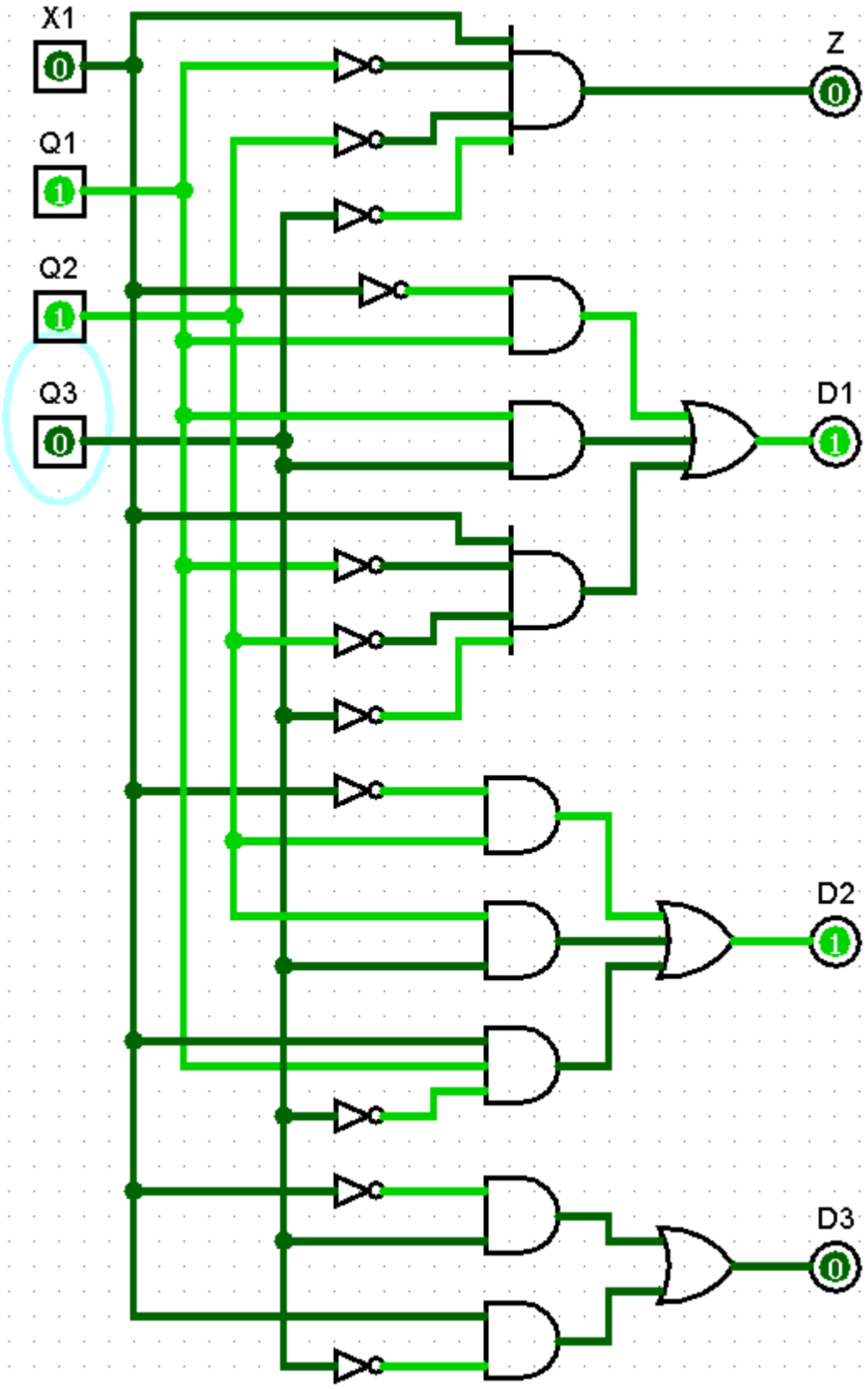

X1
0
Q1
0
Q2
0
Q3
1
Z
0
D1
0
D2
0
D3
1

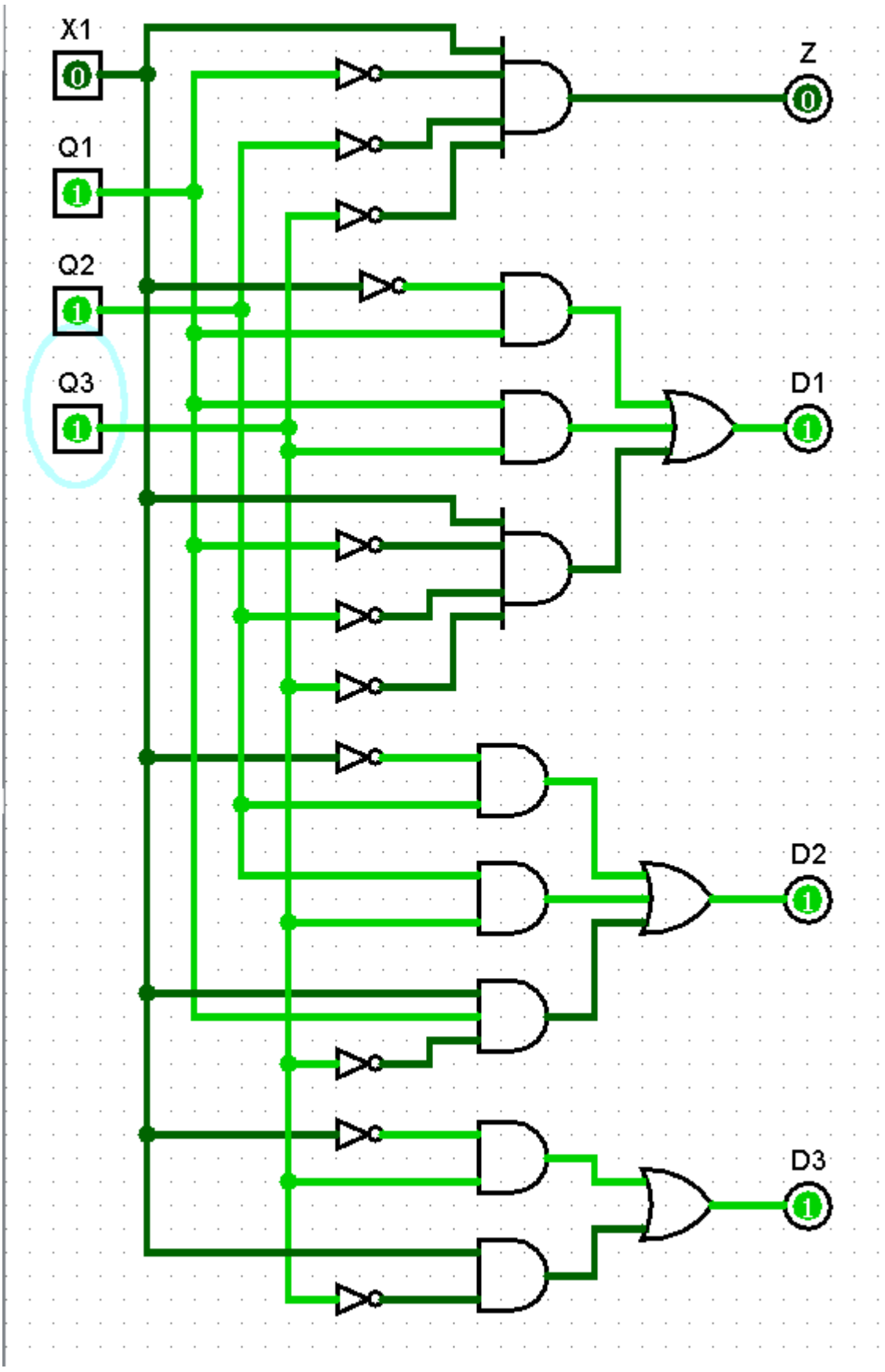

X1
0
Q1
0
Q2
1
Q3
0
Z
0
D1
0
D2
1
D3
0

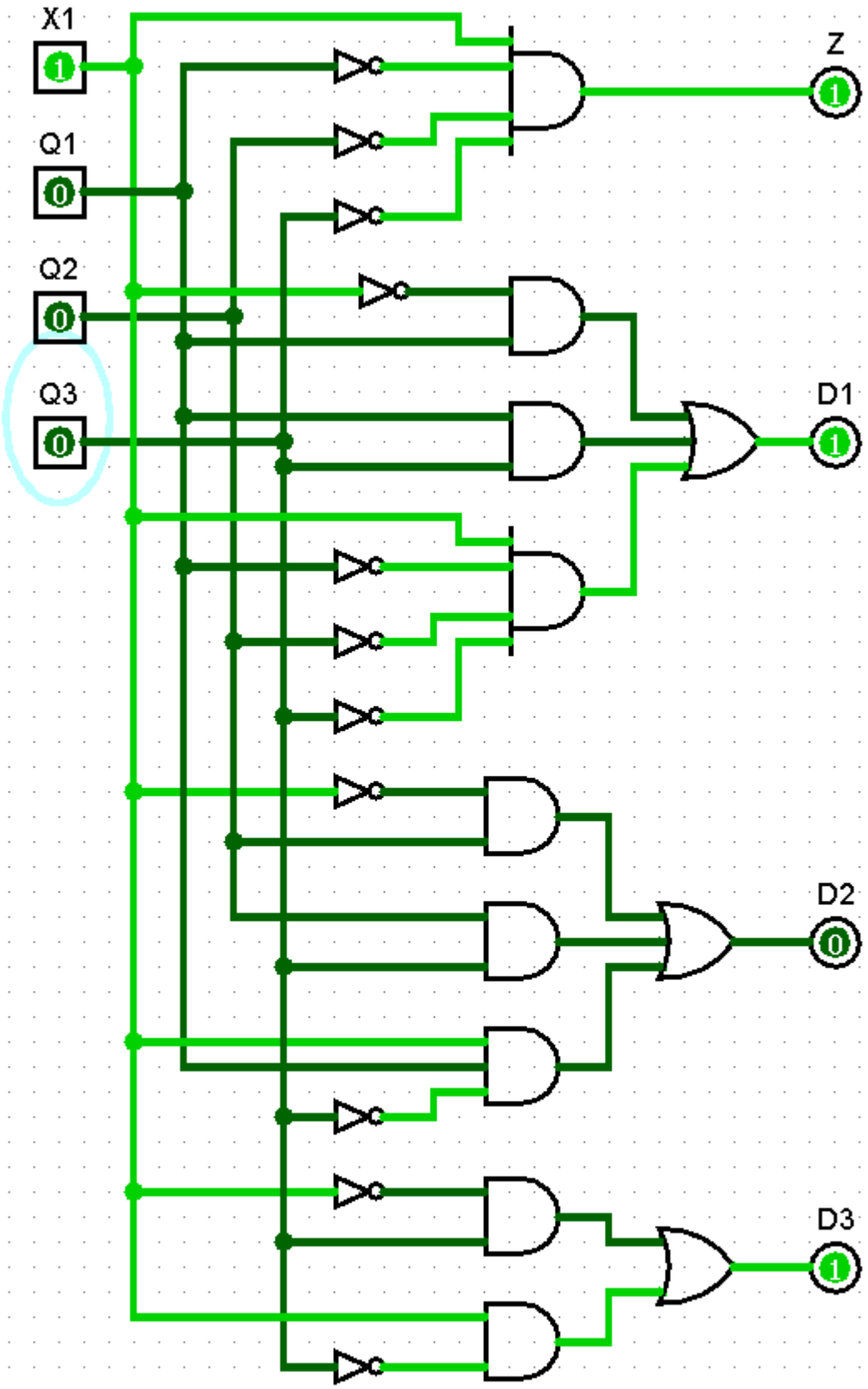

X1
0
Q1
0
Q2
1
Q3
1
Z
0
D1
0
D2
1
D3
1

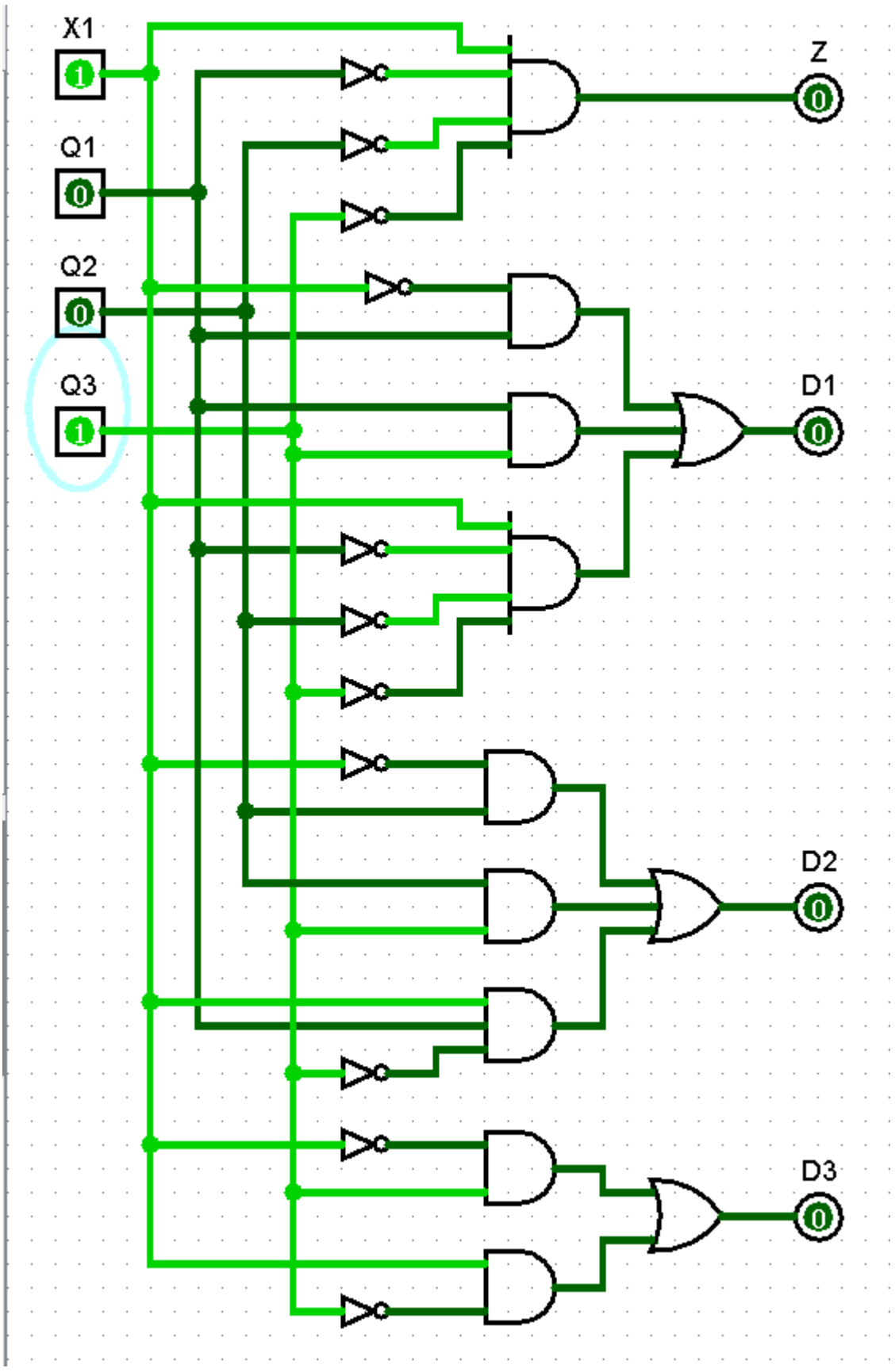

X1
0
Q1
1
Q2
0
Q3
0
Z
0
D1
1
D2
0
D3
0


X1
0
Q1
1
Q2
0
Q3
1
Z
0
D1
1
D2
0
D3
1


X1
0
Q1
1
Q2
1
Q3
0
Z
0
D1
1
D2
1
D3
0


X1
0
Q1
1
Q2
1
Q3
1
Z
0
D1
1
D2
1
D3
1


X1
1
Q1
0
Q2
0
Q3
0
Z
1
D1
1
D2
0
D3
1


X1
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Q1
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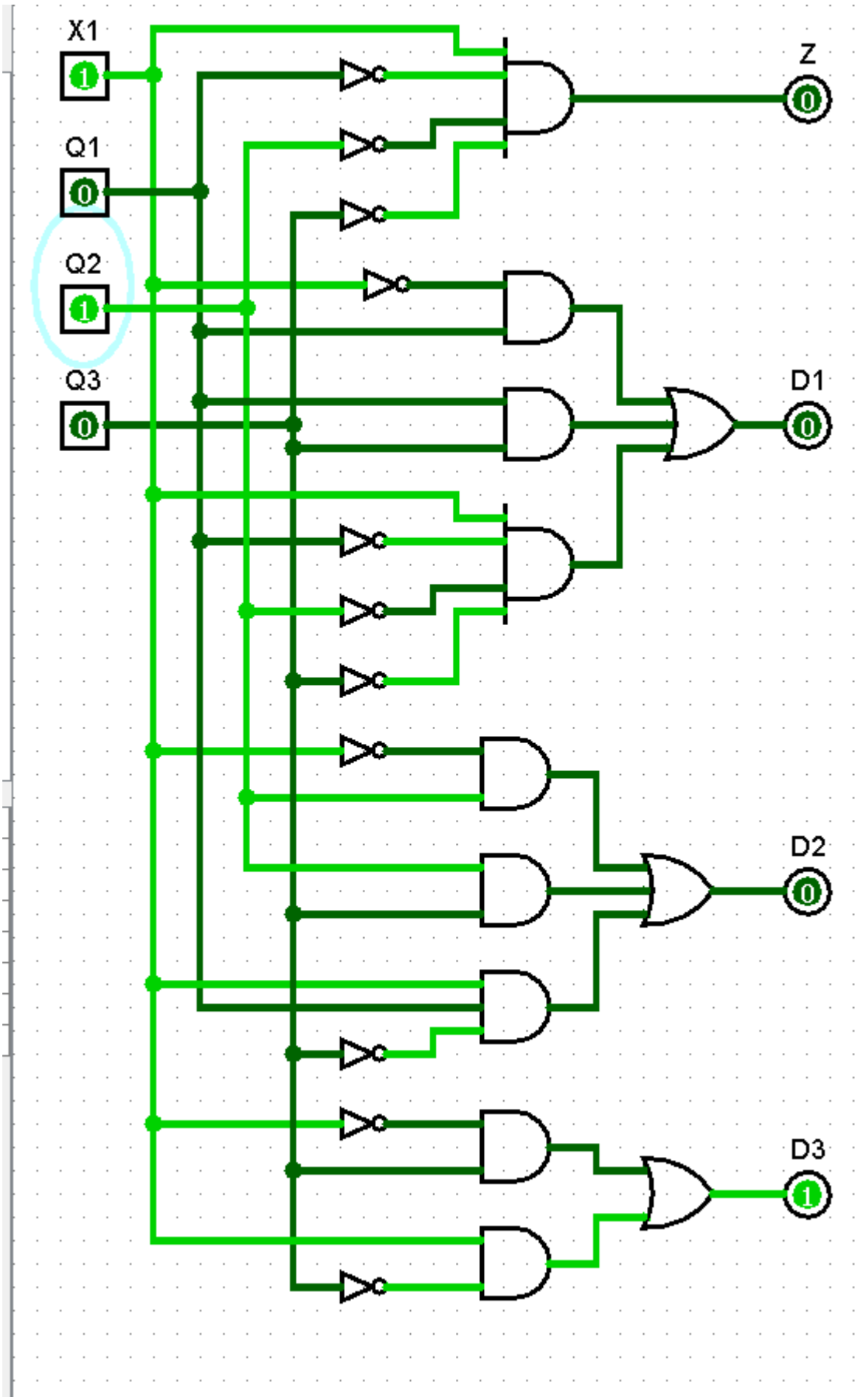
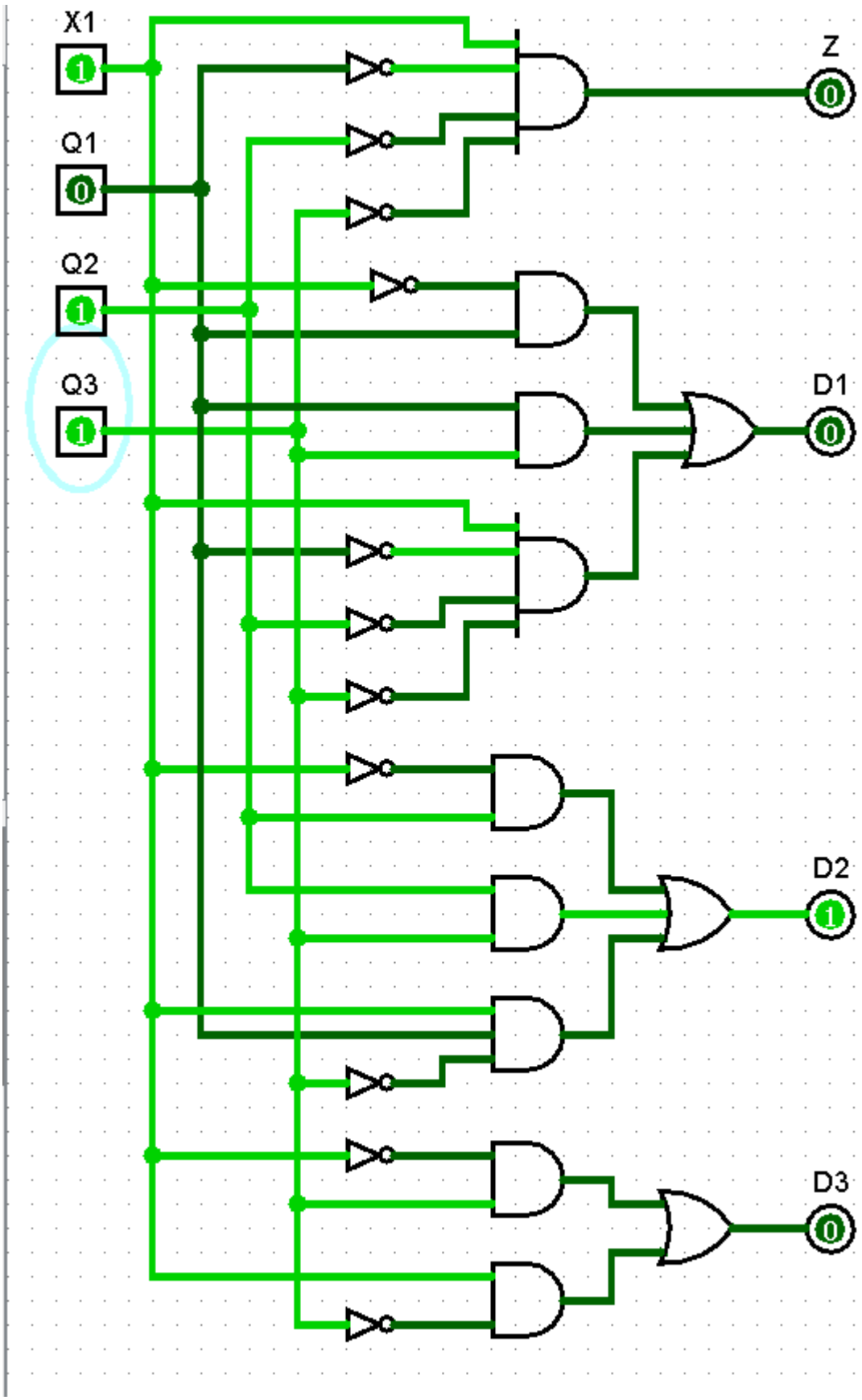
Q2
0
Q3
1
Z
0
D1
0
D2
0
D3
0


X1
1
Q1
0
Q2
1
Q3
0
Z
0
D1
0
D2
0
D3
1


X1
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Q1
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Q2
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Q3
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Z
0
D1
0
D2
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D3
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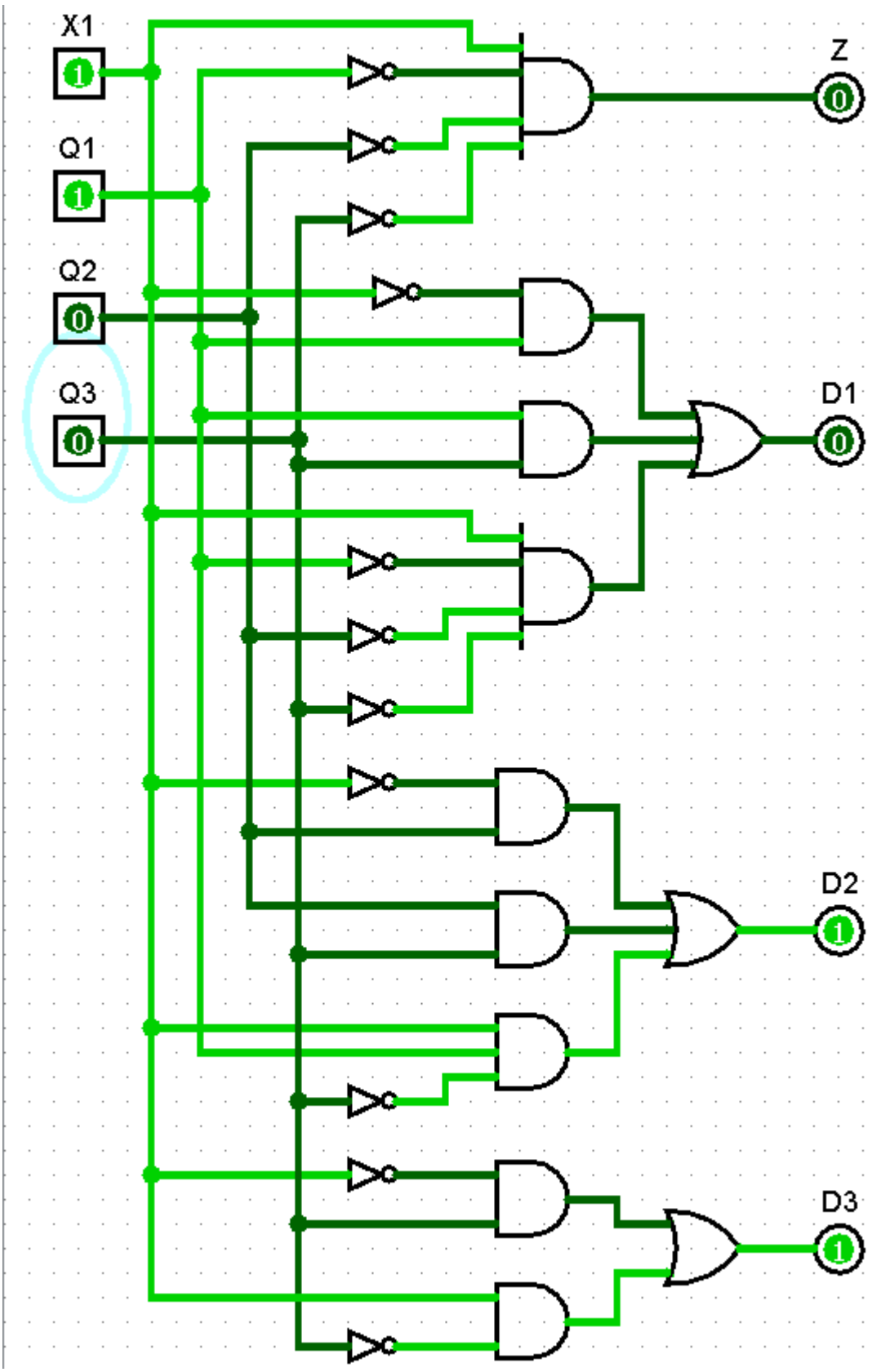
X1
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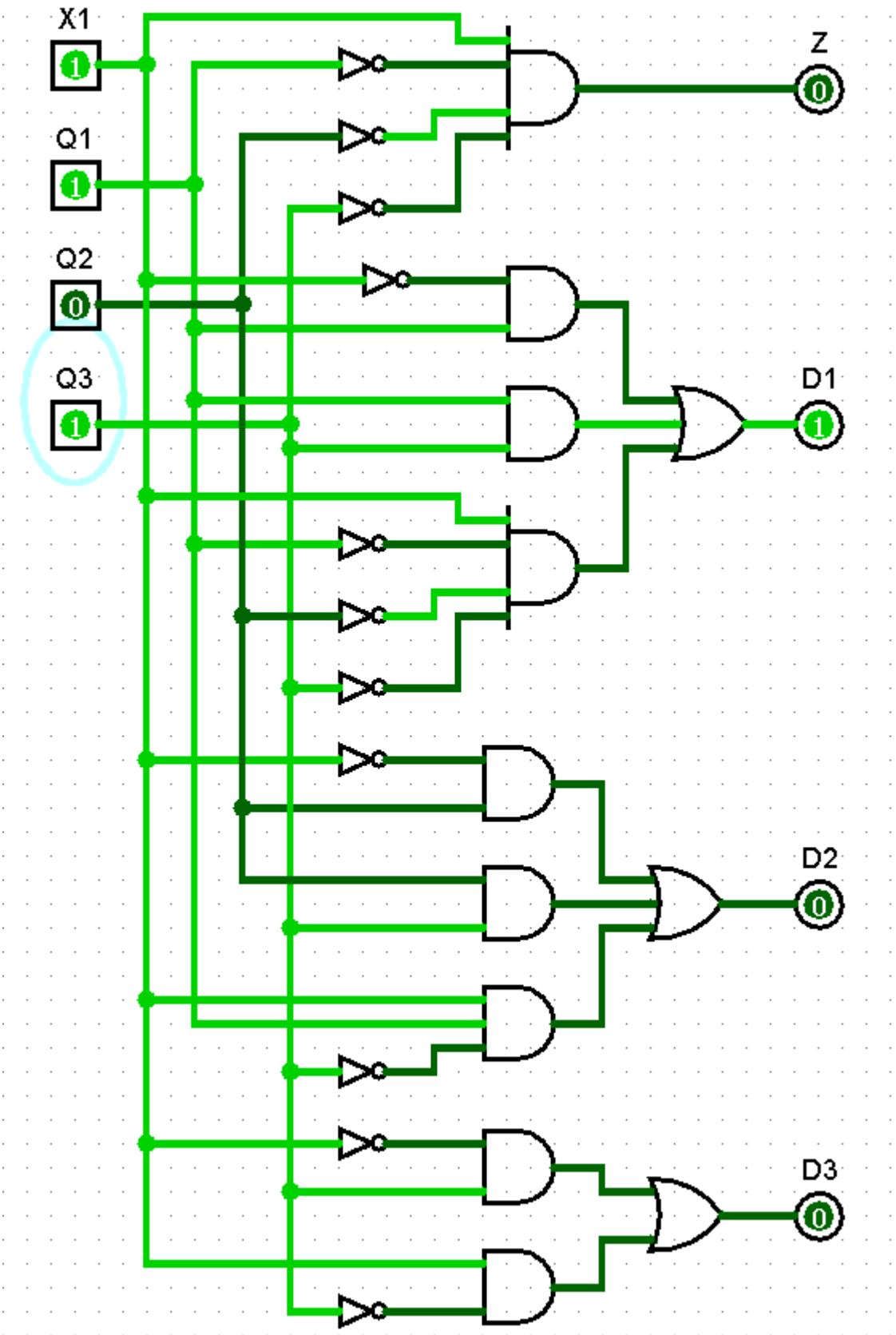
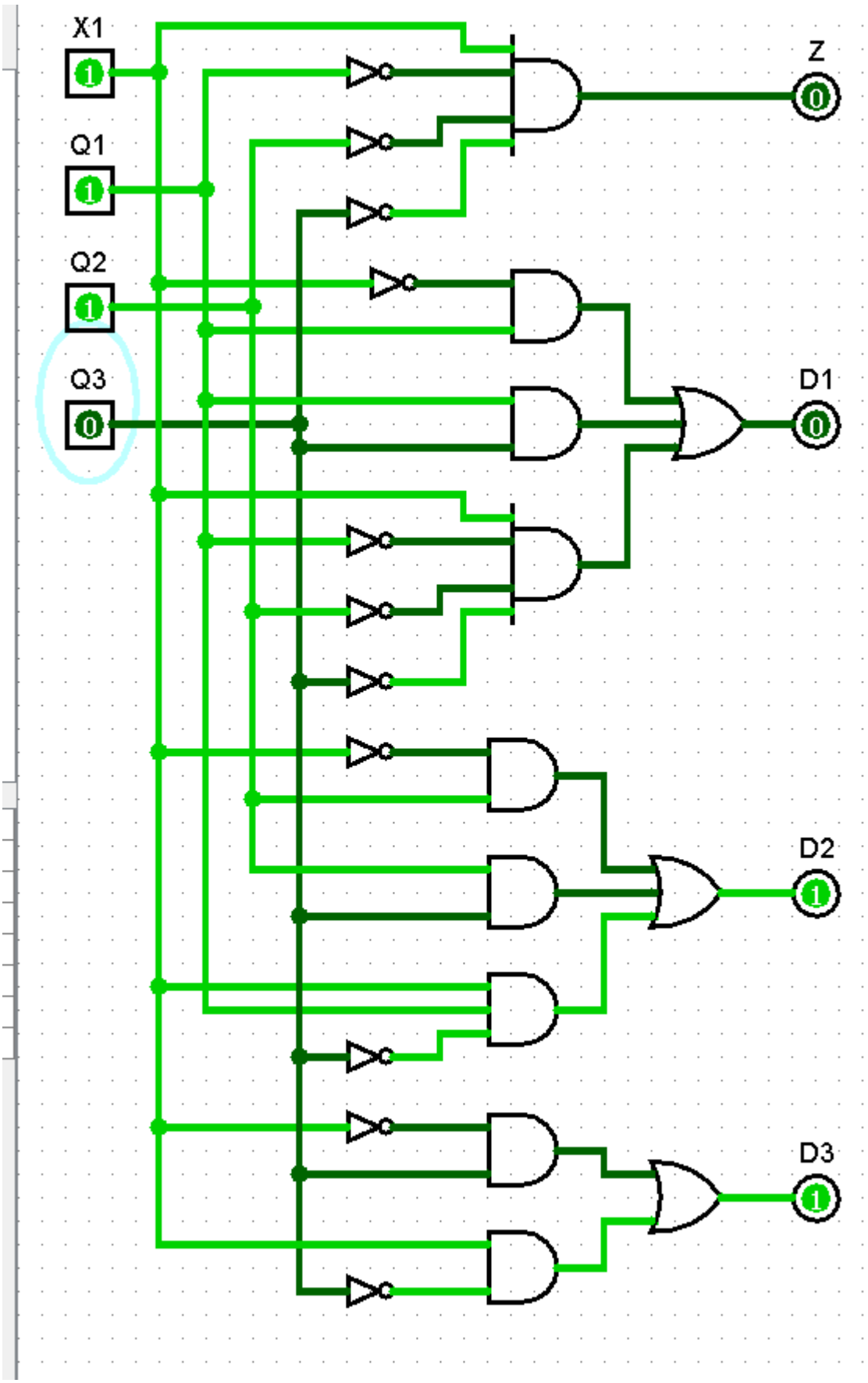
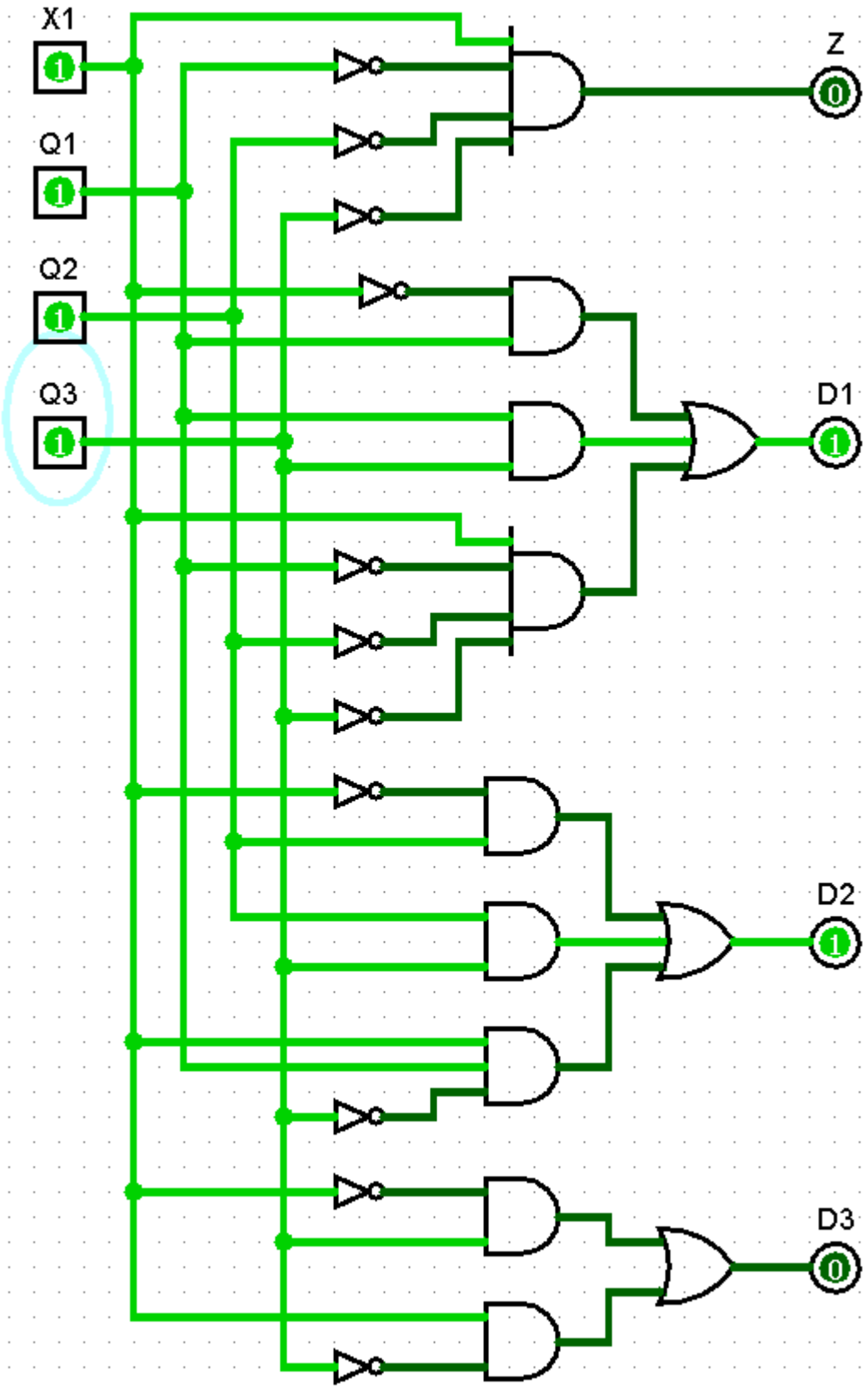
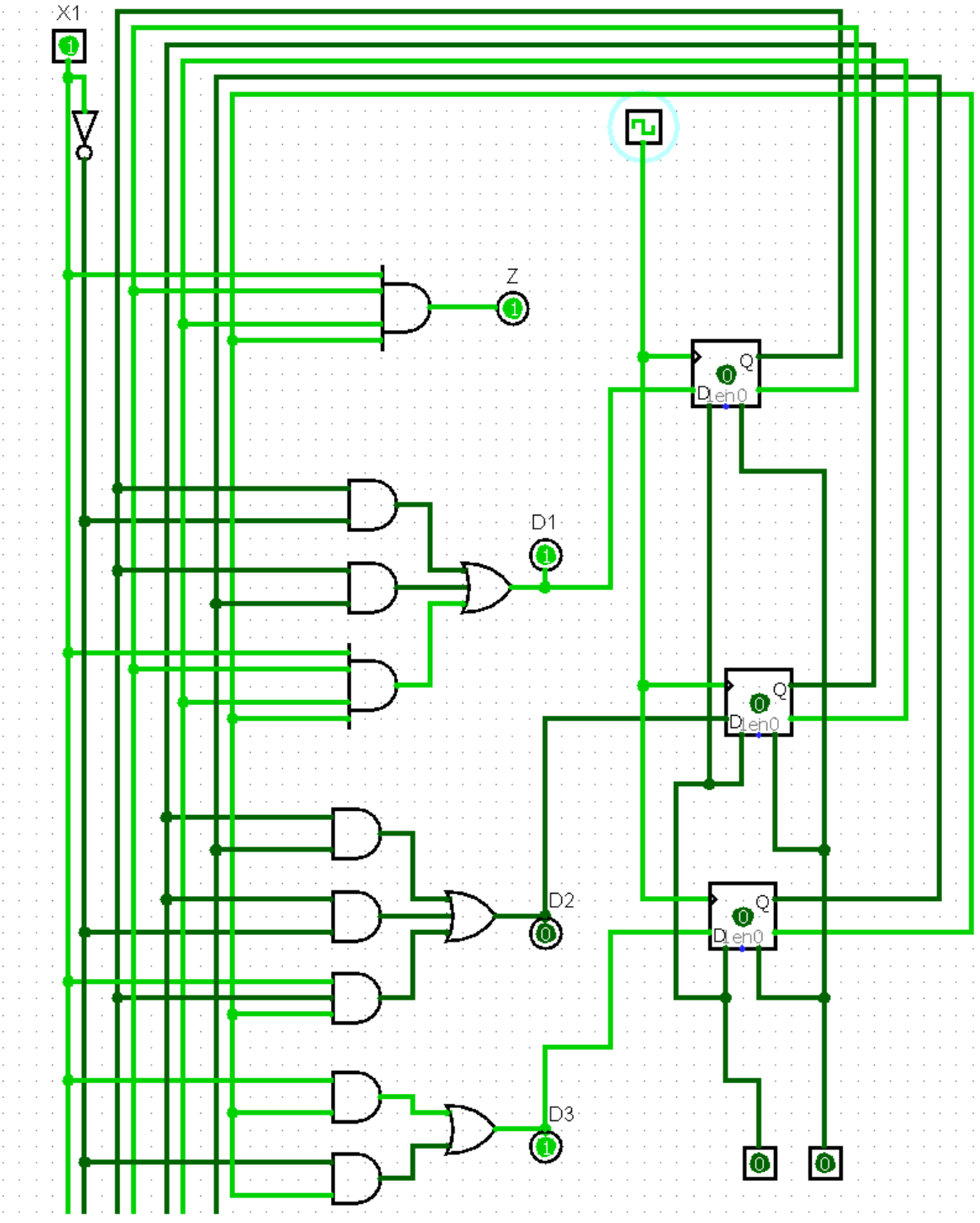
Q1
1
Q2
0
Q3
0
Z
0
D1
0
D2
1
D3
1

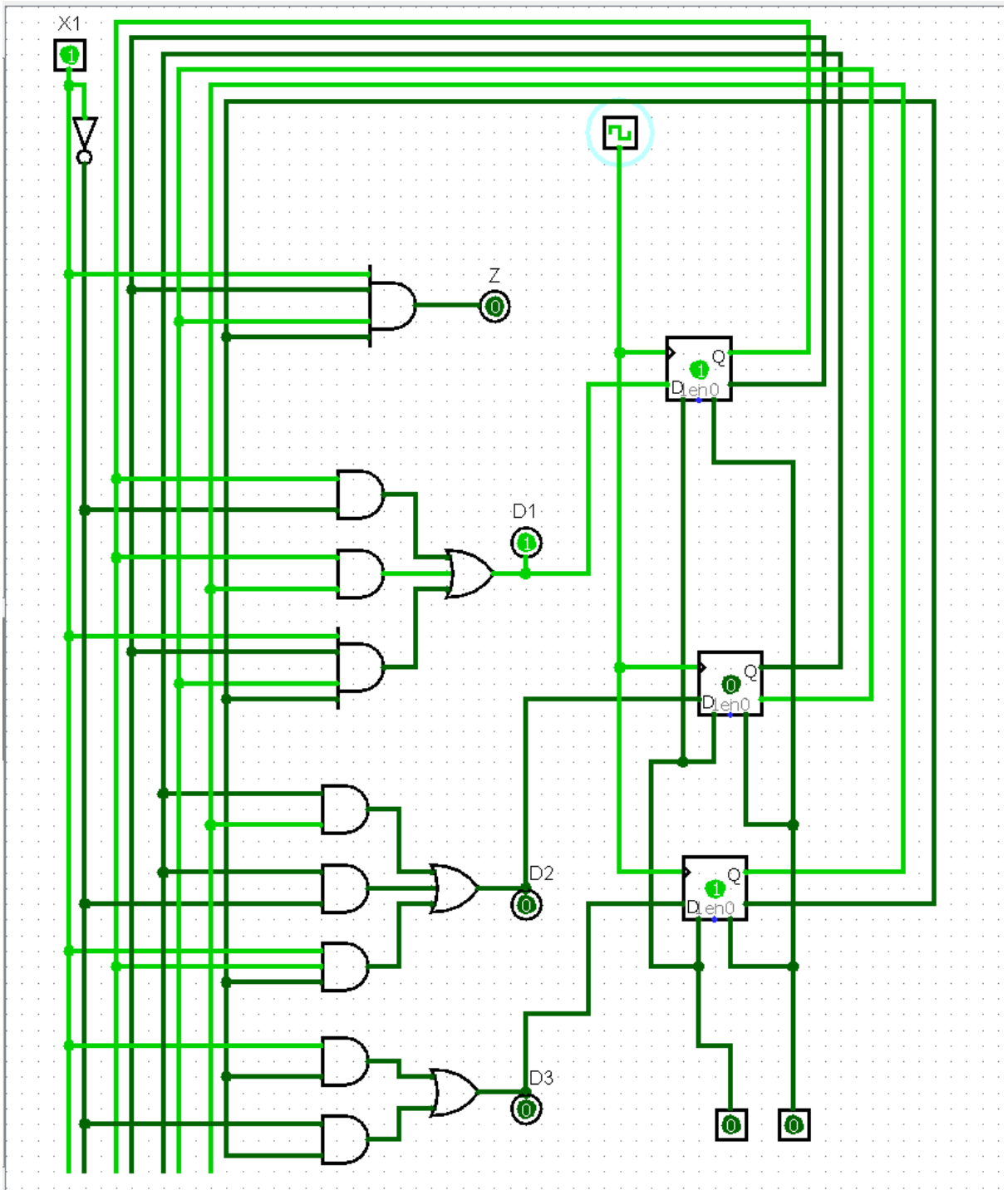

X1
1
Q1
1
Q2
0
Q3
1
Z
0
D1
1
D2
0
D3
0

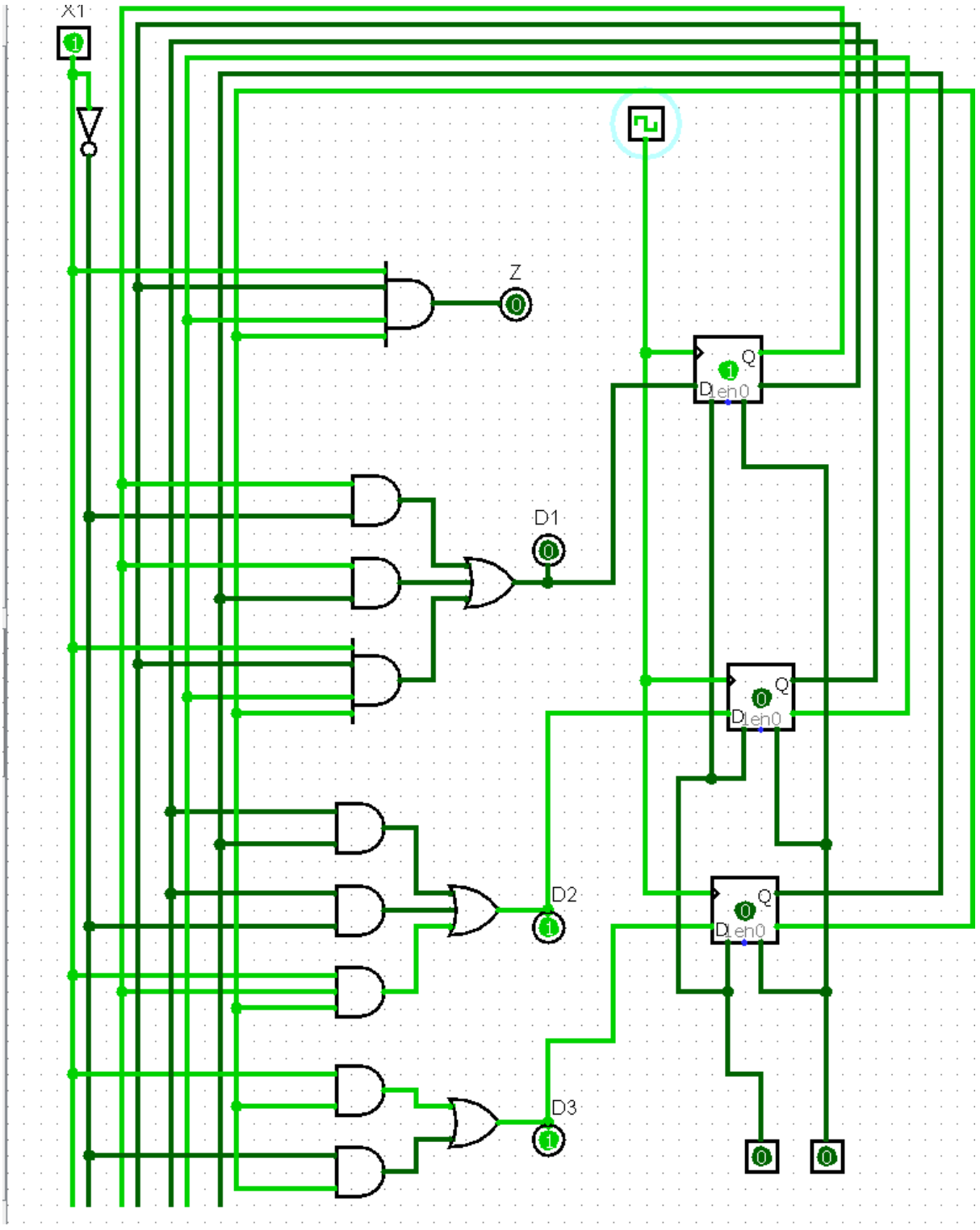

X1
1
Q1
1
Q2
1
Q3
0
Z
0
D1
0
D2
1
D3
1

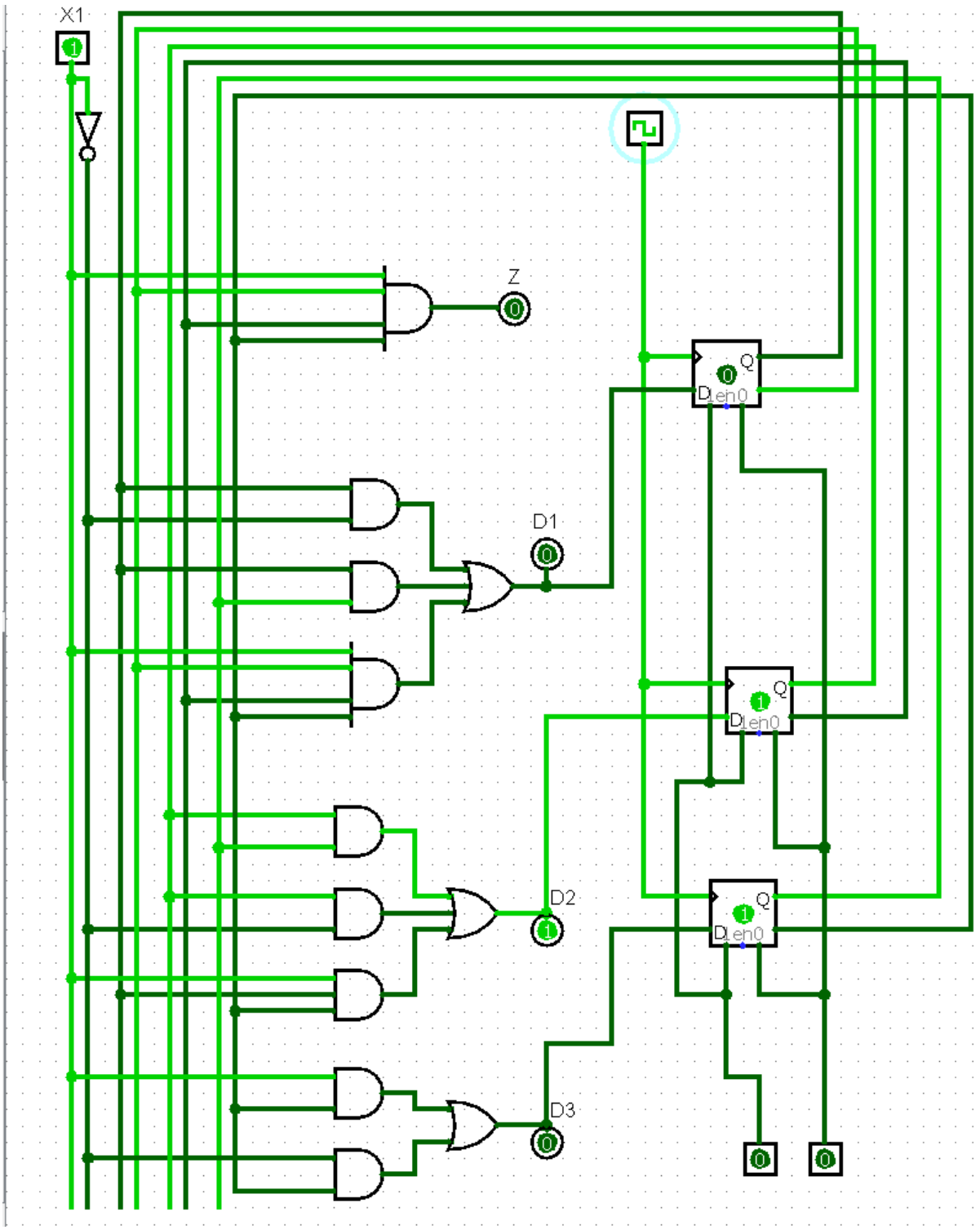

X1
1
Q1
1
Q2
1
Q3
1
Z
0
D1
1
D2
1
D3
0

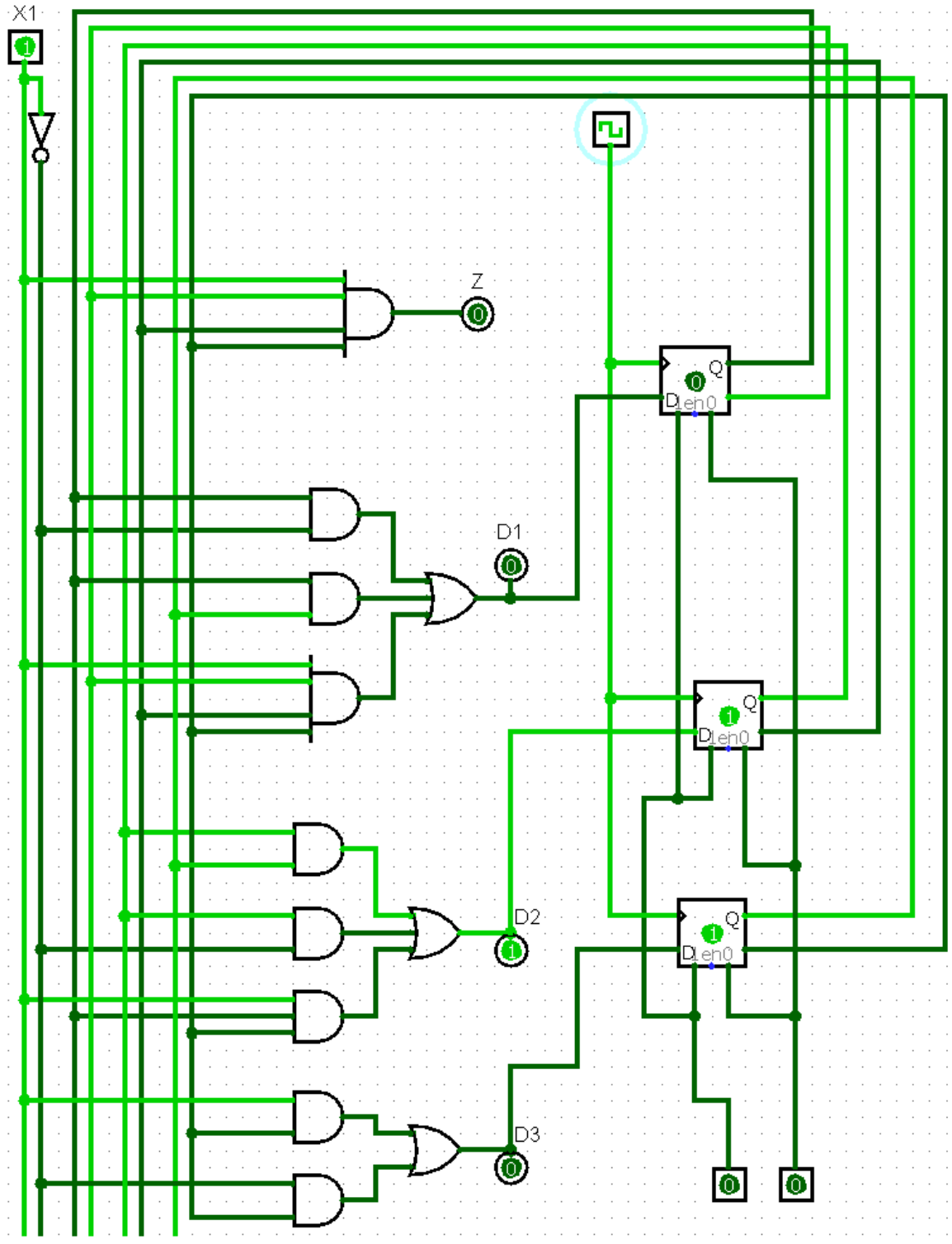
5) Модифицирана схема

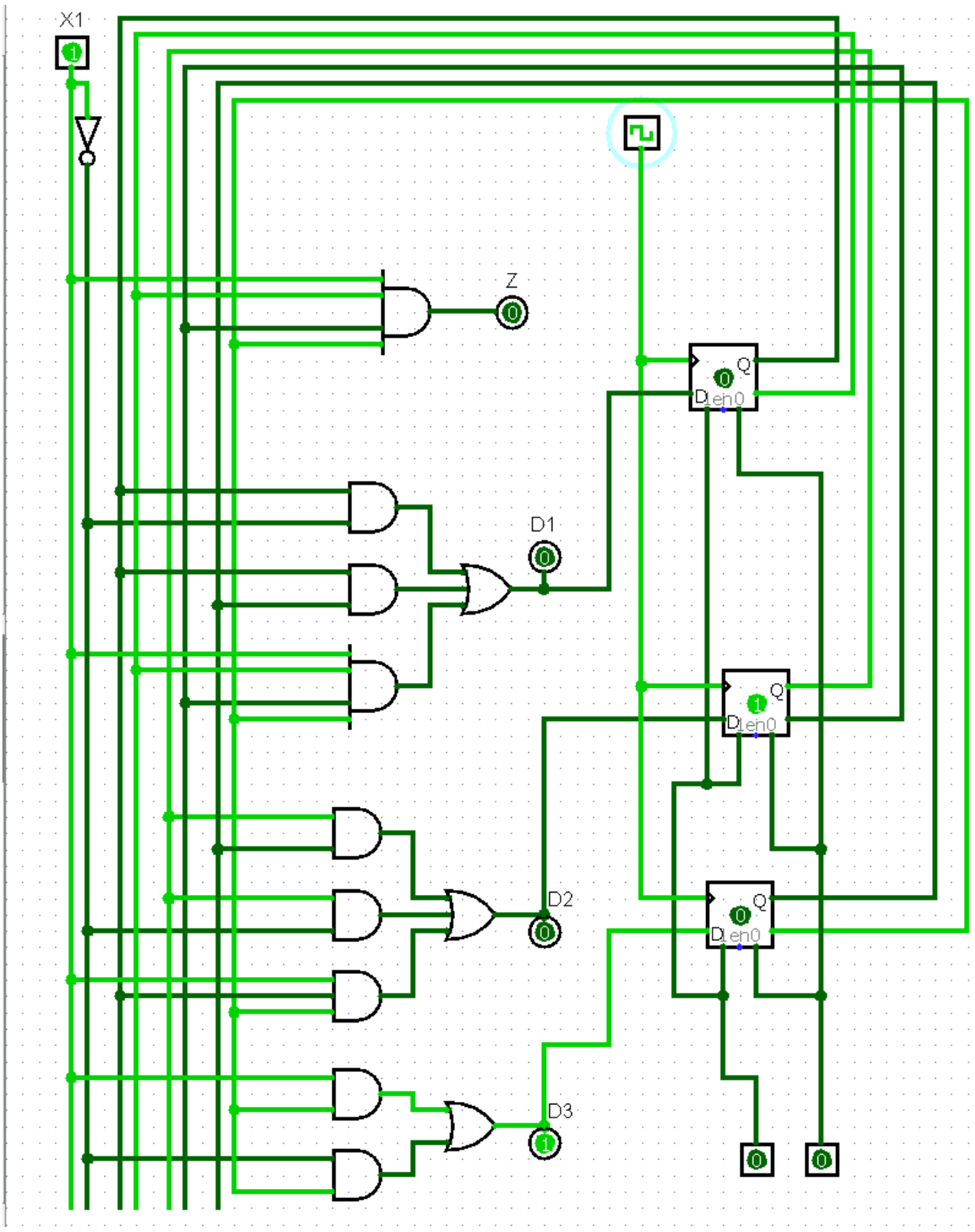



X1
Z
D1
D2
D3
Q
D
en
0


X1
Z
D1
D2
D3
Q
D
en
0
1


X1
Z
D1
D2
D3
Q
D
en
Q
D
en
Q
D
en


X1
Z
D1
D2
D3
Q
D
en
Q
D
en
Q
D
en


X1
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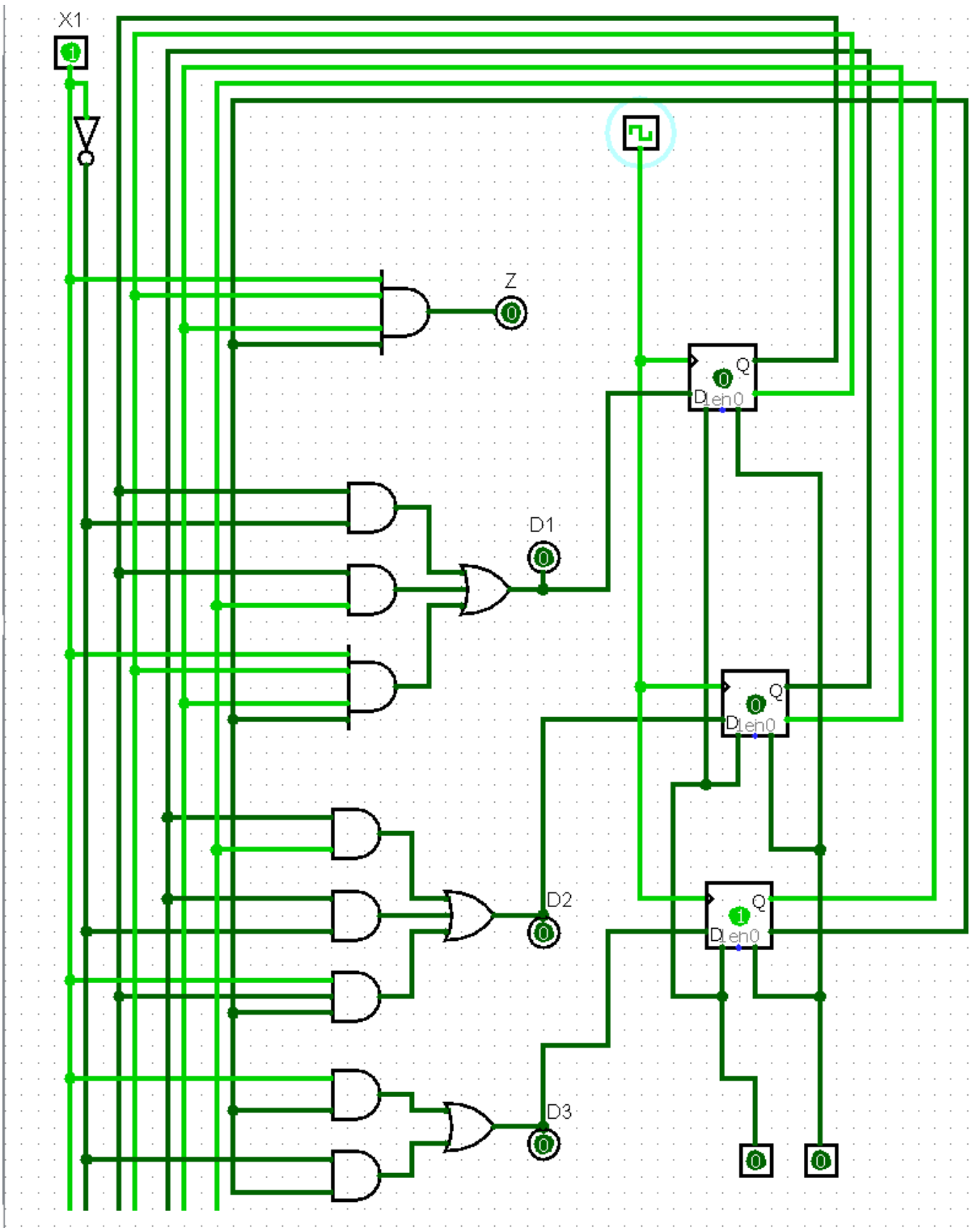
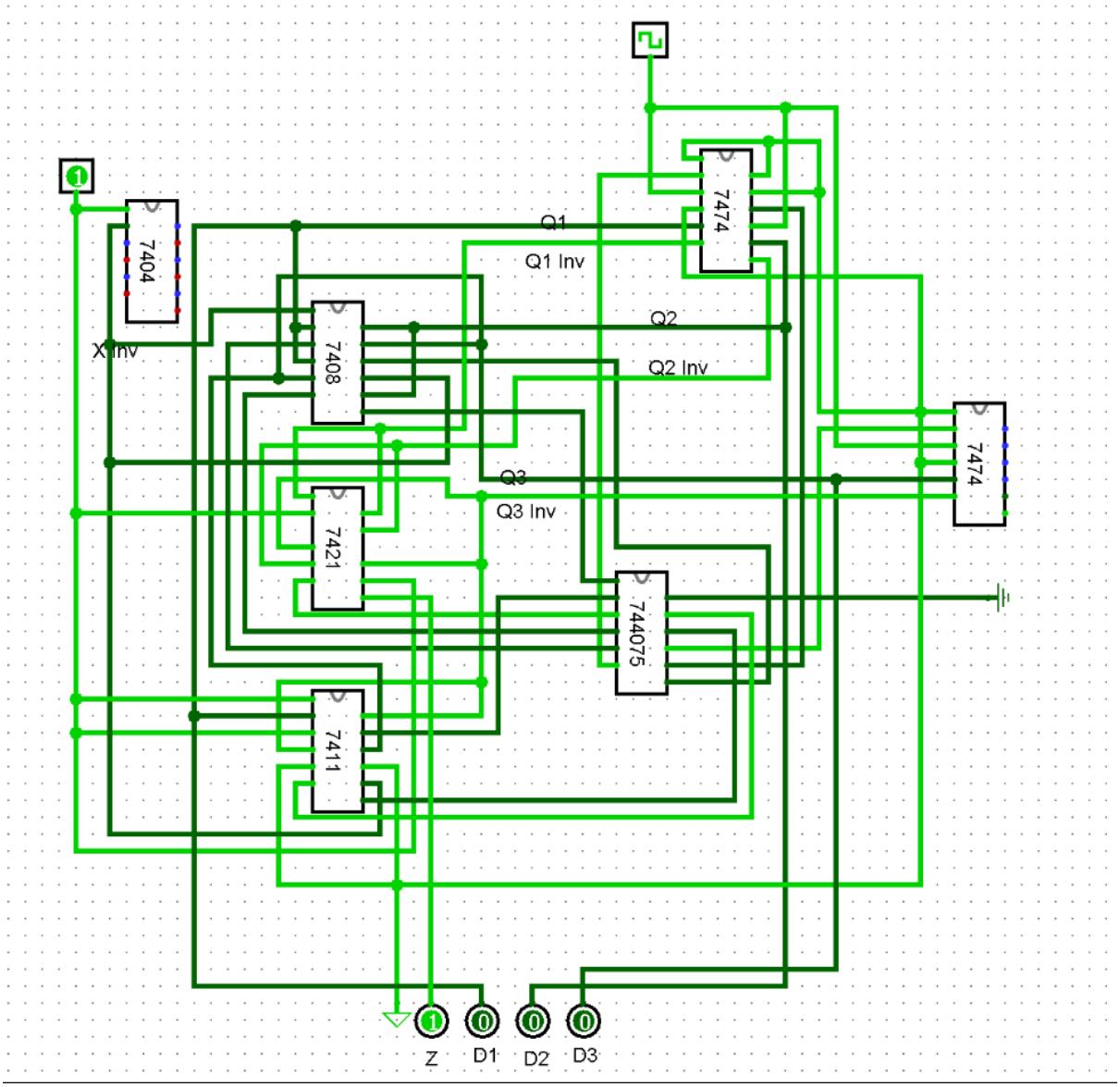
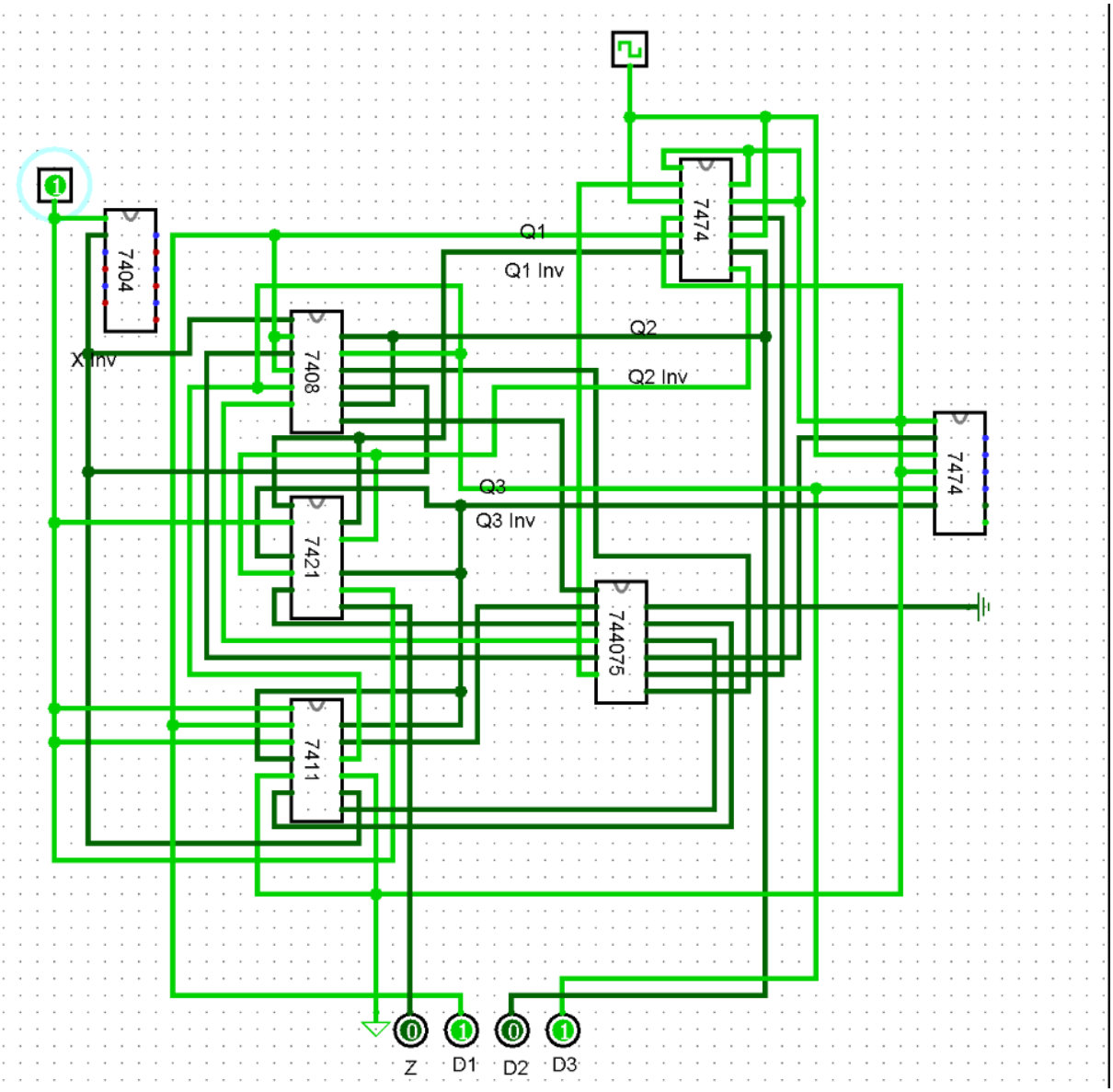
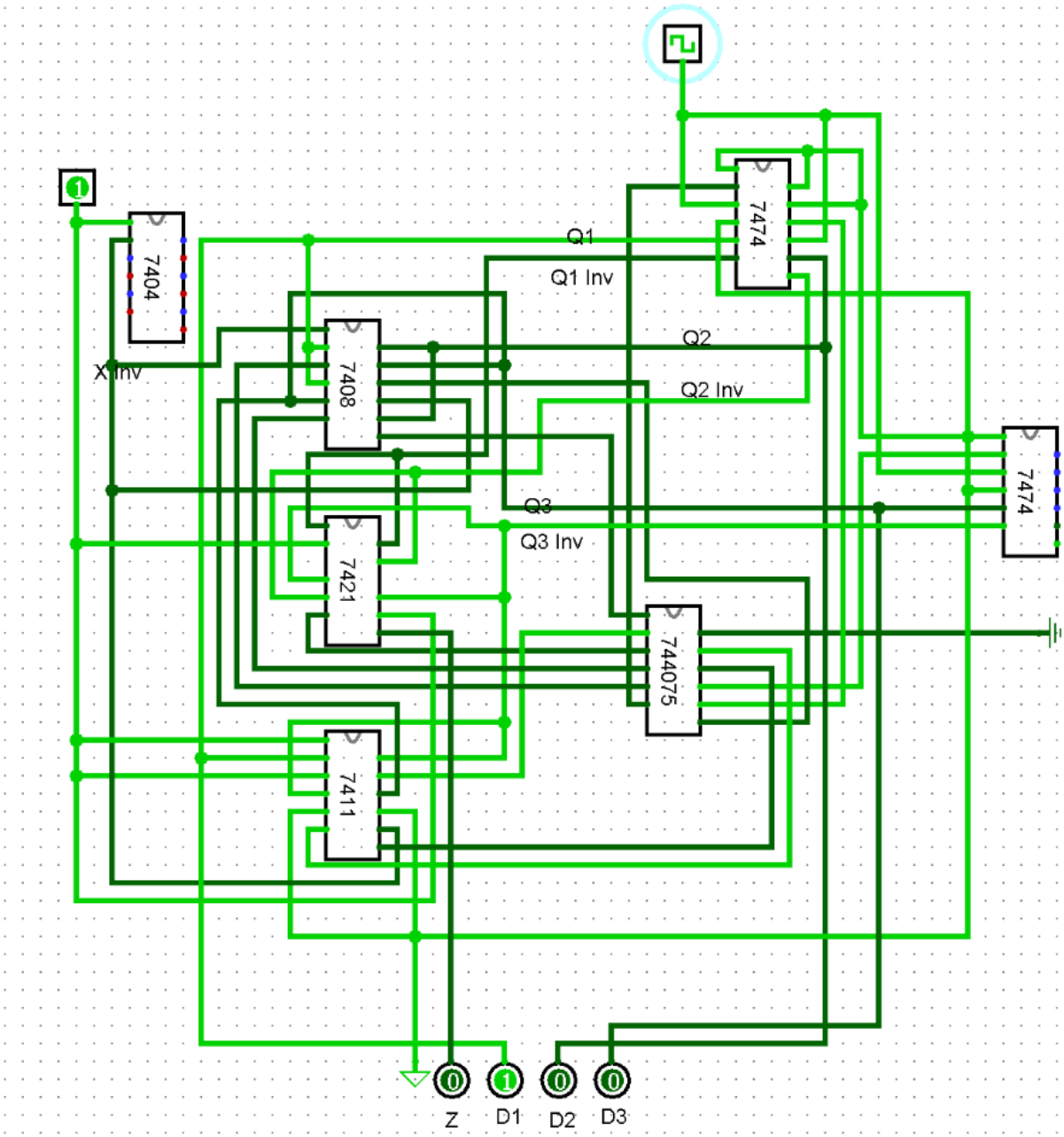
D1
D2
D3
Q
D
en
Q
D
en
Q
D
en

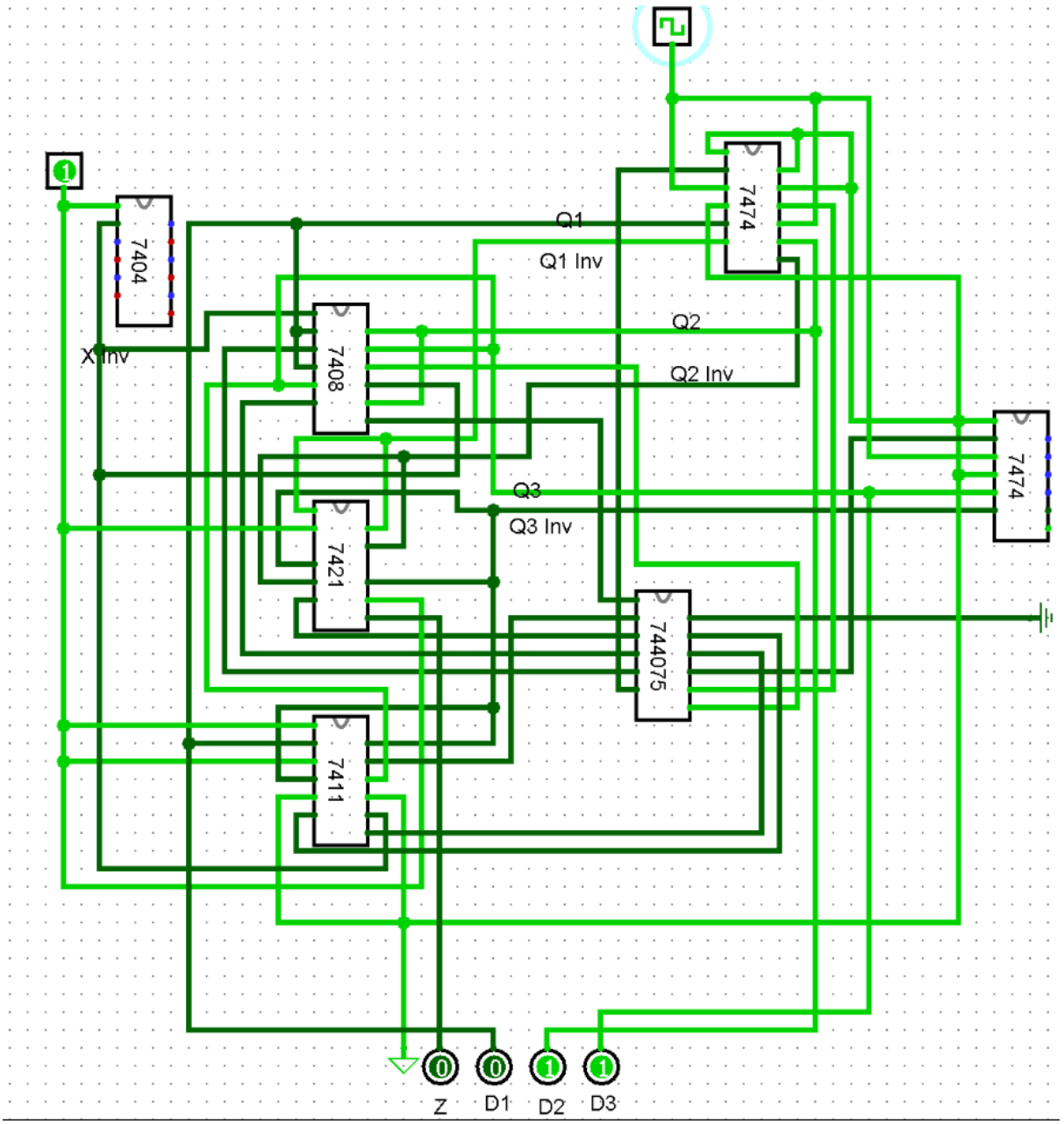

X1
Z
D1
D2
D3
Q
D
en
0

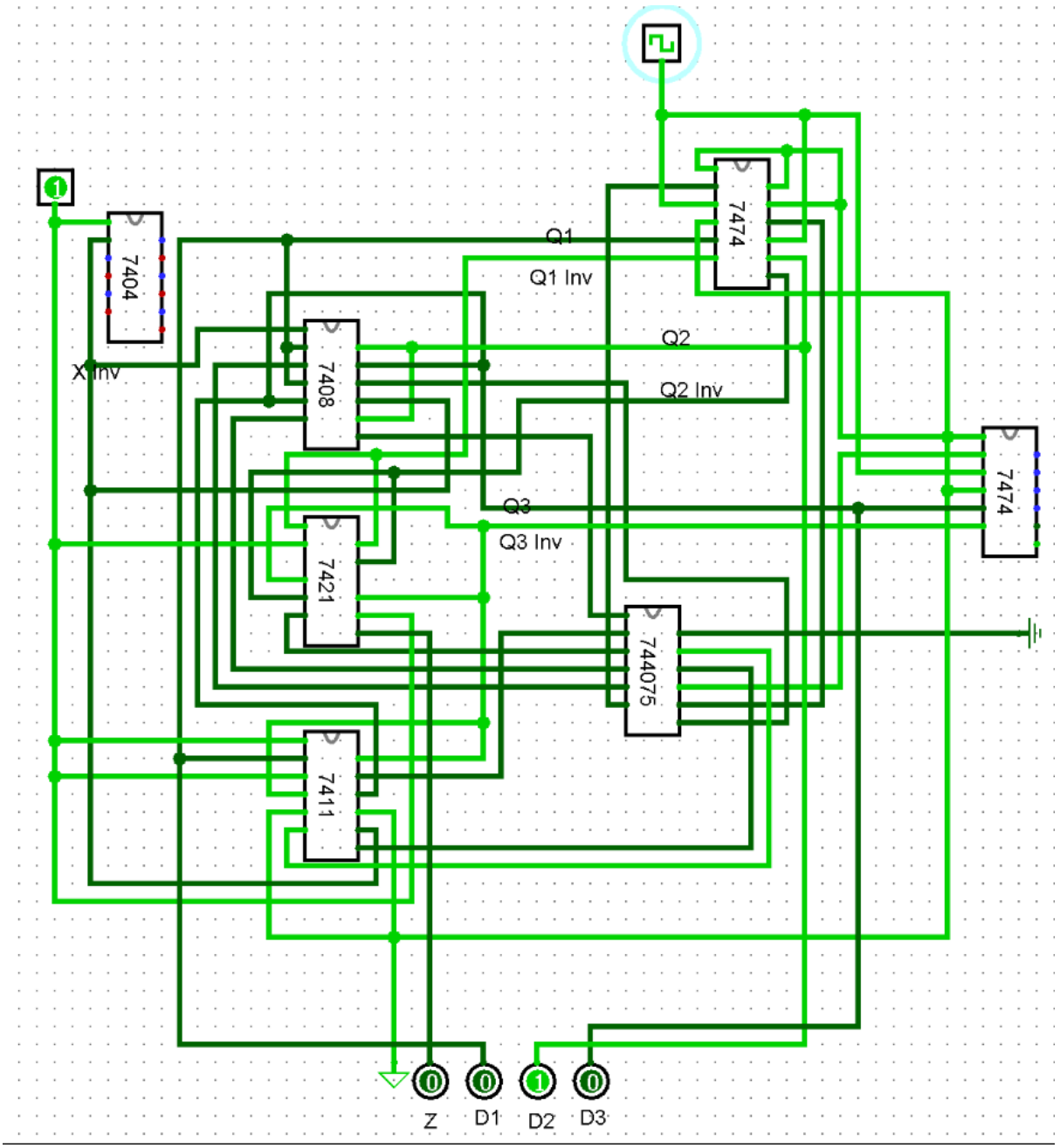
6) Схема използваща библиотеката 7400

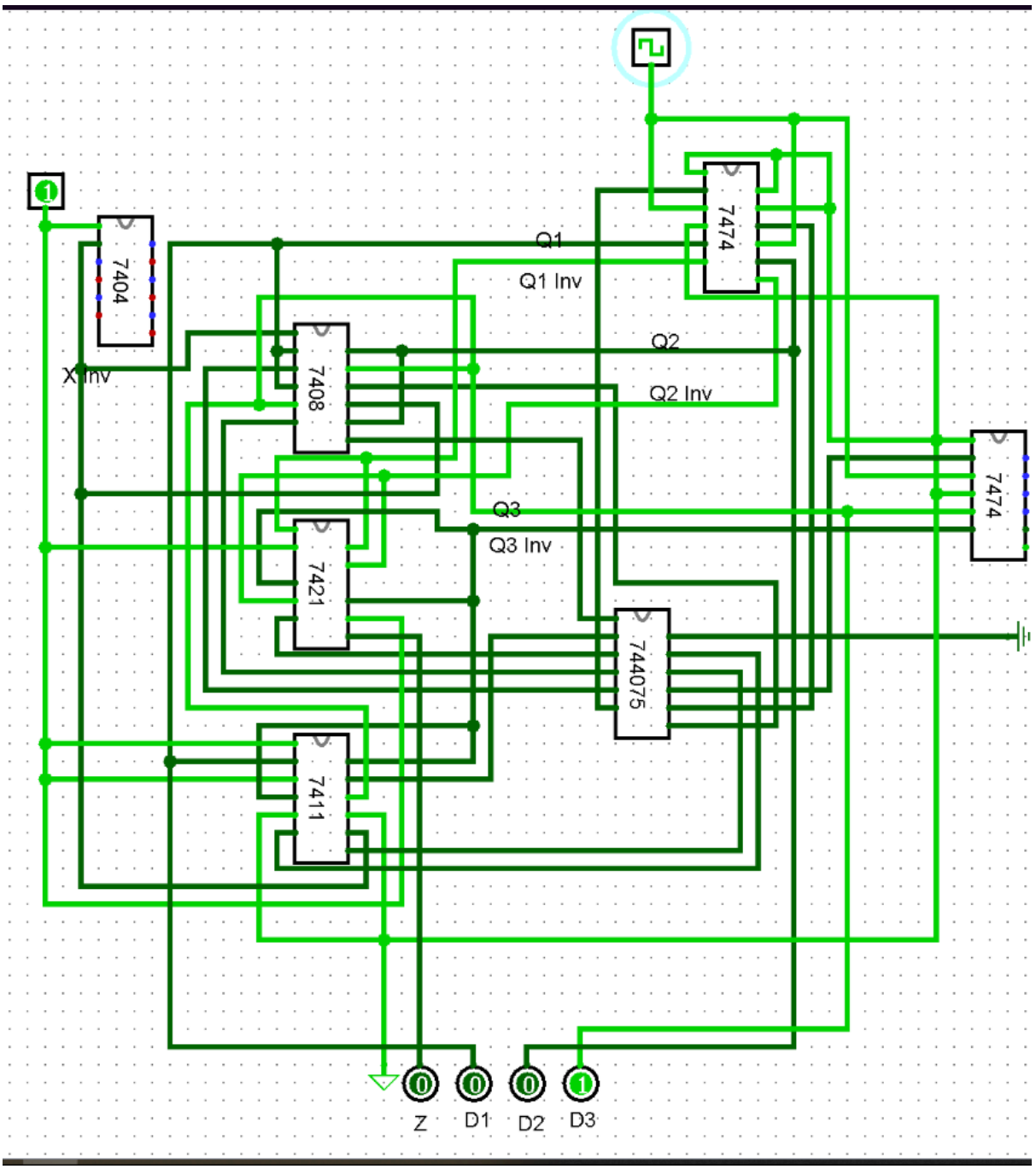



7404
X Inv
7408
7421
7411
7474
Q1
Q1 Inv
Q2
Q2 Inv
Q3
Q3 Inv
7474
744075
Z
D1
D2
D3


7404
X Inv
7408
7421
7411
7474
Q1
Q1 Inv
Q2
Q2 Inv
Q3
Q3 Inv
744075
7474
Z
D1
D2
D3


7404
X Inv
7408
7421
7411
7474
Q1
Q1 Inv
Q2
Q2 Inv
Q3
Q3 Inv
744075
7474
Z
D1
D2
D3


7404
7474
Q1
Q1 Inv
7408
Q2
Q2 Inv
X Inv
7474
Q3
Q3 Inv
7421
744075
7411
Z
D1
D2
D3


7404
X Inv
7408
7421
7411
7474
Q1
Q1 Inv
Q2
Q2 Inv
Q3
Q3 Inv
744075
7474
Z
D1
D2
D3