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ENGINEERING FACULTY OF ENGINEERING

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# LTspice Simulation of Sequential Circuits

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Author:  
George Downing

Student Number:  
20273662

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## Question 1

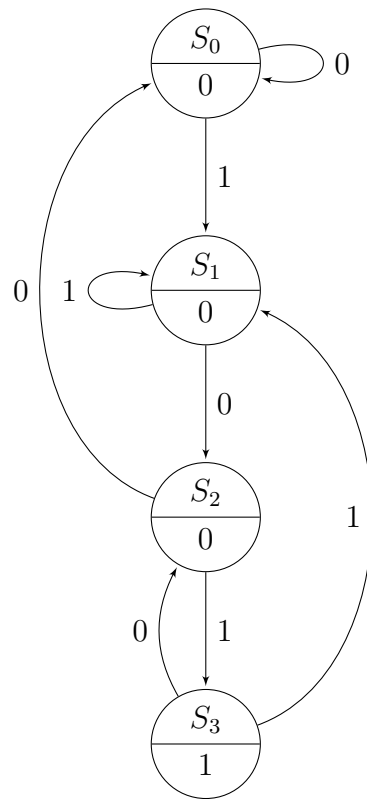


Figure 1: State Diagram for Q1

## Question 2

<i>Present State</i> ( <i>n</i> )	Next State (n+1)		Present Output Z
	X=0	X=1	
$S_0$	$S_0$	$S_1$	0
$S_1$	$S_2$	$S_2$	0
$S_2$	$S_0$	$S_3$	0
$S_3$	$S_2$	$S_1$	1

Table 1: State Transition Table in terms of  $S_0$  and  $S_1$ 

Present State ( <i>n</i> )		Next State ( <i>n</i> +1)				D-inputs required				Output Z
		X = 0		X = 1		X = 0		X = 1		
<i>Q<sub>n</sub><sup>A</sup></i>	<i>Q<sub>n</sub><sup>B</sup></i>	<i>Q<sub>n+1</sub><sup>A</sup></i>	<i>Q<sub>n+1</sub><sup>B</sup></i>	<i>Q<sub>n+1</sub><sup>A</sup></i>	<i>Q<sub>n+1</sub><sup>B</sup></i>	<i>D<sub>A</sub></i>	<i>D<sub>B</sub></i>	<i>D<sub>A</sub></i>	<i>D<sub>B</sub></i>	
0	0	0	0	0	1	0	0	0	1	0
0	1	1	0	0	1	1	0	0	1	0
1	0	0	0	1	1	0	0	1	1	0
1	1	1	0	0	1	1	0	0	1	1

Table 2: State Transition Table in terms of  $Q_n^A$  and  $Q_n^B$

### Question 3

		$Q_n^A \cdot Q_n^B$			
		00	01	11	10
X	0	0	1	1	0
	1	0	0	0	1

Figure 2: Karnaugh map for the Input of flip-flop  $D_A$ 

		$Q_n^A \cdot Q_n^B$			
		00	01	11	10
X	0	0	0	0	0
	1	1	1	1	1

Figure 3: Karnaugh map for the Input of flip-flop  $D_B$ 

$$D_A = Q_n^B \cdot \overline{X} + Q_n^A \cdot \overline{Q_n^B} \cdot X \quad (1)$$

$$D_B = X \quad (2)$$

$$Z = Q_n^A \cdot Q_n^B \quad (3)$$

Eq. 1 is the input of flip-flop  $D_A$  derived from the Karnaugh map as shown in figure 2. Eq. 2 is the input of flip-flop  $D_B$  derived from the Karnaugh map as shown in figure 3. Eq. 3 is the output of the flip-flop  $D_A$  as shown by Table 2.

## Question 4

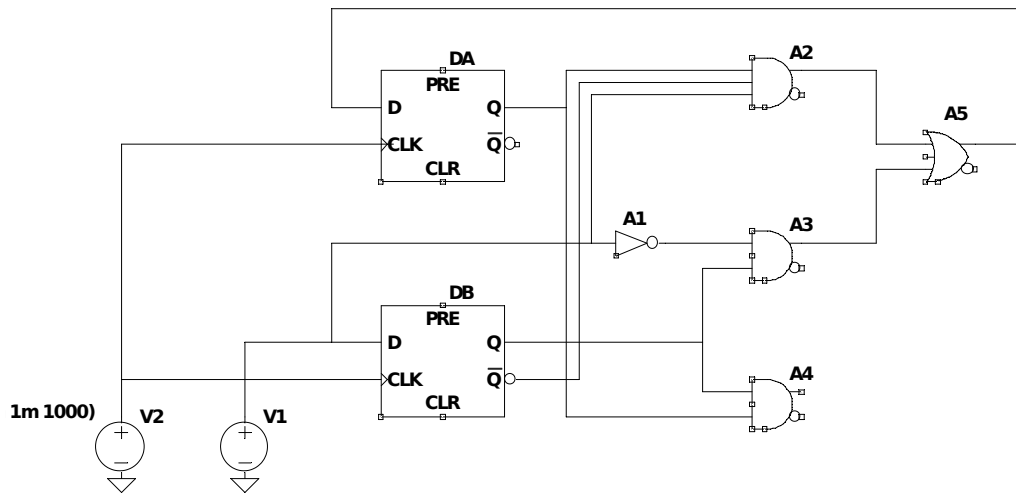


Figure 4: LTspice schematic for Q4

## Question 5

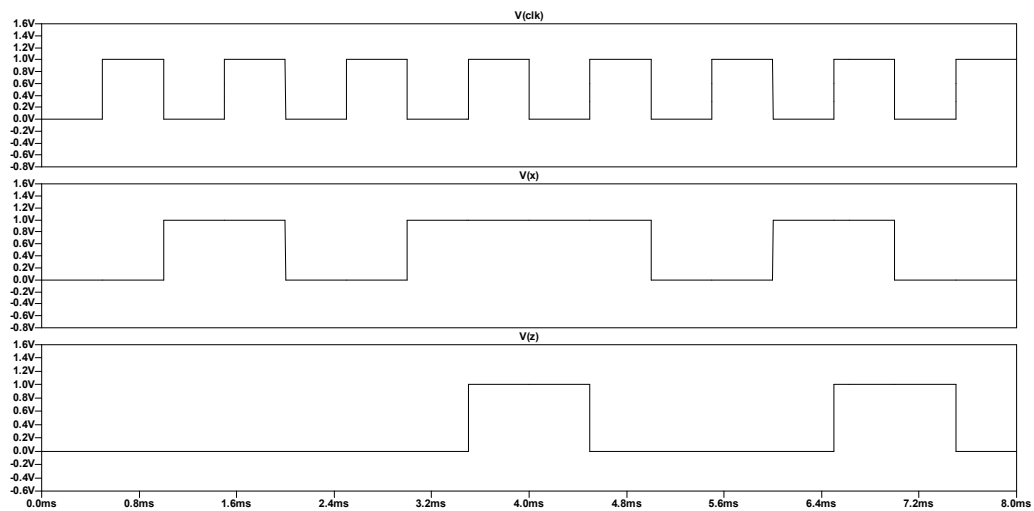


Figure 5: LTspice Simulation Traces V(CLK), V(X) and V(Z) for Q5

## Question 6

$$t_{AFGCD} = t_{pd} + t_{A1} + t_{A5} \quad (4)$$

$$t_{DGCD} = t_{pd} + t_{A1} + t_{A5} \quad (5)$$

Eq. 4 and 5 denote the delay through paths  $t_{DGCD}$  and  $t_{AFGCD}$ .

## Question 7

$$t_{JGCD} = t_{A1} + t_{A5} \quad (6)$$

Eq. 6 denotes the delay through path  $t_{JGCD}$ .

## Question 8

$$\begin{aligned} t_{AEBCD} &= t_{pd} + t_{A2} + t_{A5} \\ &= 40ns + 27ns + 22ns \\ &= 89ns \end{aligned} \quad (7)$$

$$\begin{aligned} t_{AFGCD} &= t_{pd} + t_{A1} + t_{A5} \\ &= 40ns + 27ns + 22ns \\ &= 89ns \end{aligned} \quad (8)$$

$$\begin{aligned} t_{DGCD} &= t_{pd} + t_{A1} + t_{A5} \\ &= 40ns + 27ns + 22ns \\ &= 89ns \end{aligned} \quad (9)$$

Eq. 7, 8 and 9 denote the delay through paths  $t_{AEBCD}$ ,  $t_{AFGCD}$  and  $t_{DGCD}$  respectively. The maximum delay of these three paths is  $t_{min} = 89ns$ .

## Question 9

$$\begin{aligned}
 t_{JHBCD} &= t_{A4} + t_{A2} + t_{A5} \\
 &= 22ns + 27ns + 22ns \\
 &= 71ns
 \end{aligned} \tag{10}$$

$$\begin{aligned}
 t_{JGCD} &= t_{A1} + t_{A5} \\
 &= 27ns + 22ns \\
 &= 49ns
 \end{aligned} \tag{11}$$

Eq. 10 and 11 denote the delay through paths  $t_{JHBCD}$  and  $t_{JGCD}$  respectively. the maximum delay of these two paths is  $t_{min} = 71ns$ .

## Question 10

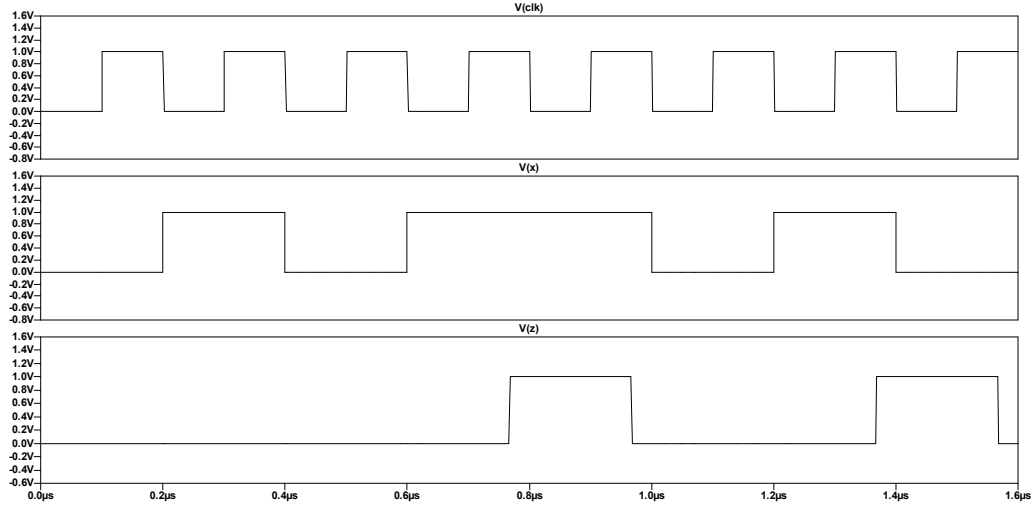


Figure 6: LTspice Simulation Traces V(CLK), V(X) and V(Z) for Q10



## Question 11

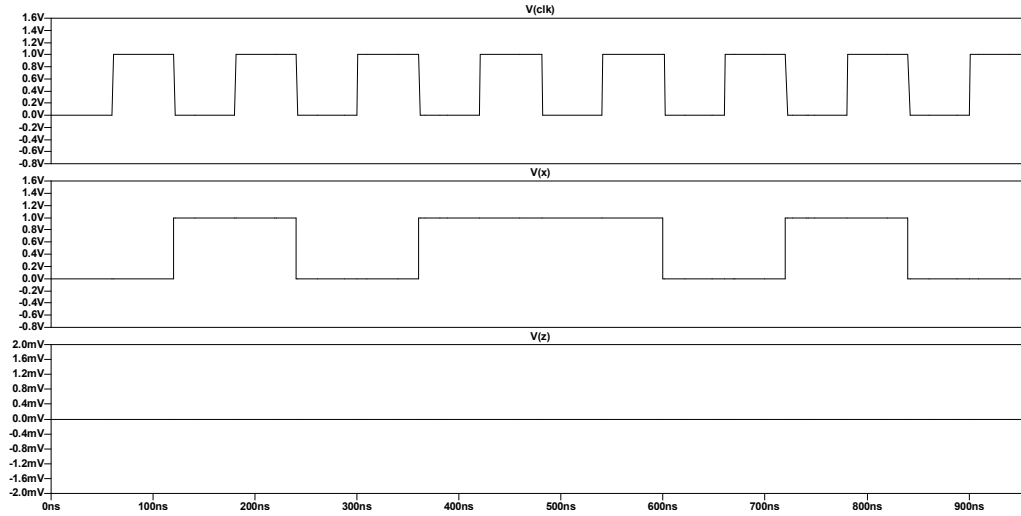


Figure 7: LTspice Simulation Traces V(CLK), V(X) and V(Z) for Q11

Figure 8 shows the output V(Z) as a flat line indicating the circuit is not operating correctly due to being clocked too fast.

V(X) clocked on the falling edge of V(CLK) and V(Z) is clocked on the rising edge of V(CLK). This means any change in V(X) only has half a clock cycle to propagate to the the input of  $D_a$ .  $t_{JHBCD} = 71ns$  which is more than half of the clock cycle (60ns) when  $t_{CLK} = 120ns$ . This means the circuit is not operating correctly due to being clocked too fast.

## Question 12

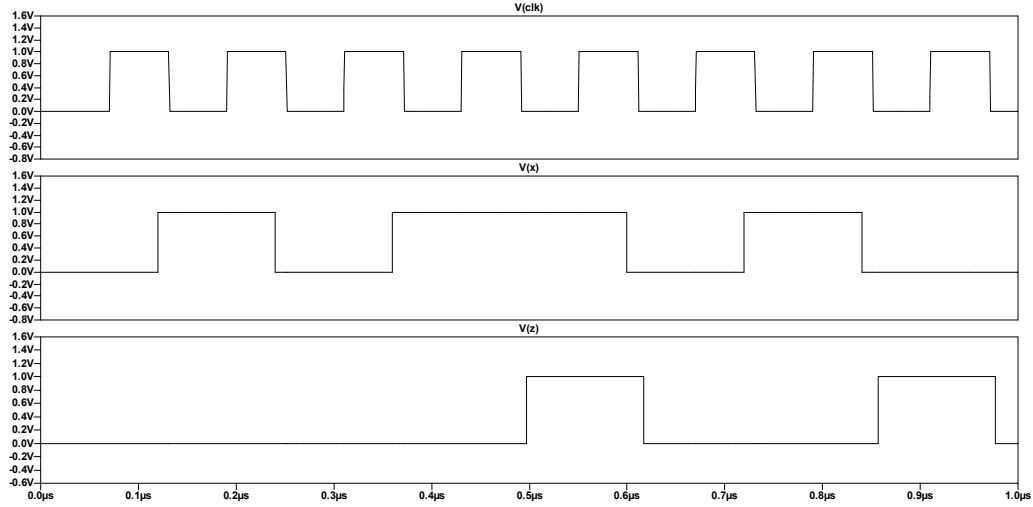


Figure 8: LTspice Simulation Traces V(CLK), V(X) and V(Z) for Q12

Figure 8 shows the output V(Z) now producing the correct output when clocked at 120ns. Introducing a delay of 10ns, the time between a change in V(x) and the rising edge of V(CLK) now becomes  $60ns + 10ns + 0.5ns = 70.5ns$ , where the 10ns is the additional delay and 0.5ns, the delay caused by a 1ns rise time. the mesured value of  $t_{JHBCD} = 70.36$  which is less than 70.50ns therefore will propegate in time V(Z) to be clocked.

## Question 13

State	Description of state
$S_0$	Initial State/Last bit is '0'
$S_1$	Detect '1' in most recent bit.
$S_2$	Detect '10' in most recent two bit.
$S_3$	Detect '100' in most recent two bit.
$S_4$	Detect '1000' in most recent two bit.

Table 3: State description table for mealy machine to detect the sequence 10001

## Question 14

ID	20273662
Test sequence	10001
Test stream	1111110001100111010001110

Table 4: Data for Q14

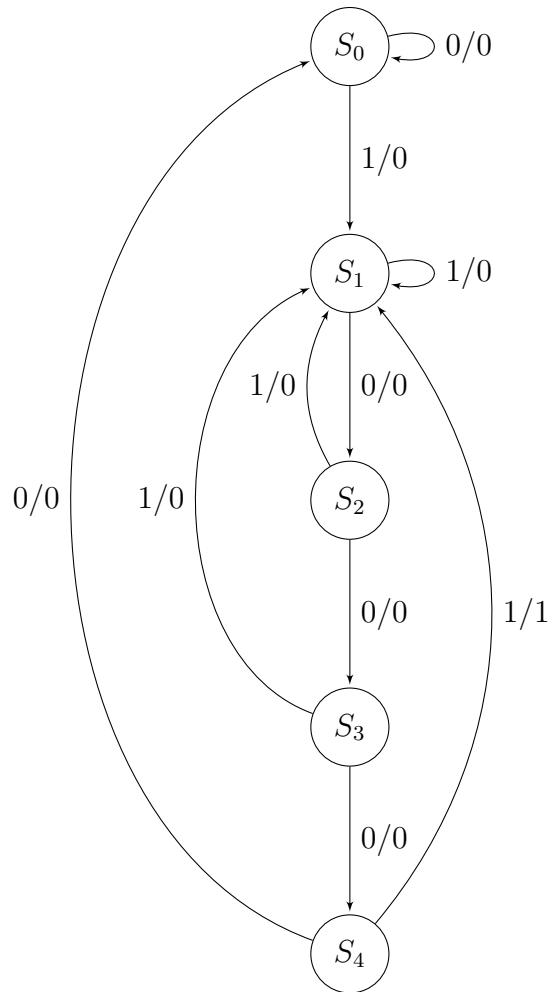


Figure 9: State Diagram for Q14

## Question 15

The number of flip flops required is  $\lceil \sqrt{n} \rceil$  where  $n$  is the number of states. In this case,  $n = 5$  so  $\lceil \sqrt{5} \rceil = 3$  flip flops are required. The flip-flop state allocation is shown in table 5 below.

State	Flip Flop Output		
	$Q^A$	$Q^B$	$Q^C$
$S_0$	0	0	0
$S_1$	0	0	1
$S_2$	0	1	0
$S_3$	0	1	1
$S_4$	1	0	0

Table 5: Flip Flop State Allocation

## Question 16

Present State (n)	Next state (n+1)		Output $Z(n)$	
	X=0	X=1	X=0	X=1
$S_0$	$S_0$	$S_1$	0	0
$S_1$	$S_2$	$S_1$	0	0
$S_2$	$S_3$	$S_1$	0	0
$S_3$	$S_4$	$S_1$	0	0
$S_4$	$S_0$	$S_1$	0	1

Table 6: State Transition Table in terms of  $S_0$  and  $S_1$ 

State (n)			Next State (n+1)						Output (Z)	
			X=0			X=1				
$Q_n^A$	$Q_n^B$	$Q_n^C$	$Q_n^A$	$Q_n^B$	$Q_n^C$	$Q_n^A$	$Q_n^B$	$Q_n^C$	X=0	X=1
0	0	0	0	0	0	0	0	1	0	0
0	0	1	0	1	0	0	0	1	0	0
0	1	0	0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	1	0	1
1	0	1	x	x	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x

Table 7: State Transition Table in terms of  $Q_n^A$  and  $Q_n^B$

## Question 17

		$Q_n^B \cdot Q_n^C$			
		00	01	11	10
$X \cdot Q_n^A$	00	0	0	1	0
	01	0	x	x	x
	11	0	x	x	x
	10	0	0	0	0

Figure 10: Karnaugh map for the Input of flip-flop  $D_A$ 

$$D_A = \overline{X} \cdot Q_n^B \cdot Q_n^C \quad (12)$$

Figure 10 shows the Karnaugh map for the input of flip-flop  $D_A$ . The Karnaugh map was created using the state transition table shown in Table 7. The input of flip-flop  $D_A$  is given by Eq. 12.

		$Q_n^B \cdot Q_n^C$			
		00	01	11	10
$X \cdot Q_n^A$	00	0	1	0	1
	01	0	x	x	x
	11	0	x	x	x
	10	0	0	0	0

Figure 11: Karnaugh map for the Input of flip-flop  $D_B$ 

$$\begin{aligned}
 D_B &= \overline{X} \cdot \overline{Q_n^B} \cdot Q_n^C + \overline{X} \cdot Q_n^B \cdot \overline{Q_n^C} \\
 &= \overline{X} \left( \overline{Q_n^B} \cdot Q_n^C + Q_n^B \cdot \overline{Q_n^C} \right) \\
 &= \overline{X} (Q_n^B \oplus Q_n^C)
 \end{aligned} \quad (13)$$

Figure 11 shows the Karnaugh map for the input of flip-flop  $D_B$ . The Karnaugh map was created using the state transition table shown in Table 7. The input of flip-flop  $D_B$  is given by Eq. 13.

		$Q_n^B \cdot Q_n^C$			
		00	01	11	10
$X \cdot Q_n^A$	00	0	0	0	1
	01	0	x	x	x
	11	1	x	x	x
	10	1	1	1	1

Figure 12: Karnaugh map for the Input of flip-flop  $D_C$

$$D_C = X + Q_n^B \cdot \overline{Q_n^C} \quad (14)$$

Figure 12 shows the Karnaugh map for the input of flip-flop  $D_C$ . The Karnaugh map was created using the state transition table shown in Table 7. The input of flip-flop  $D_C$  is given by Eq. 14.

		$Q_n^B \cdot Q_n^C$			
		00	01	11	10
$X \cdot Q_n^A$	00	0	0	0	0
	01	0	x	x	x
	11	1	x	x	x
	10	0	0	0	0

Figure 13: Karnaugh map for the Output  $Z$

$$Z = X \cdot Q_n^A \quad (15)$$

Figure 13 shows the Karnaugh map for the output  $Z$ . The Karnaugh map was created using the state transition table shown in Table 7. The output  $Z$  is given by Eq. 15.

## Question 18

```

0m 1
0.999999m 1
1m 1
1.999999m 1
2m 1
2.999999m 1
3m 1
3.999999m 1
4m 1
4.999999m 1
5m 1
5.999999m 1
6m 0
6.999999m 0
7m 0
7.999999m 0
8m 0
8.999999m 0
9m 1
9.999999m 1
10m 1
10.999999m 1
11m 0
11.999999m 0
12m 0
12.999999m 0
13m 1
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14m 1
14.999999m 1
15m 1
15.999999m 1
16m 0
16.999999m 0
17m 1
17.999999m 1
18m 0
18.999999m 0
19m 0
19.999999m 0
20m 0
20.999999m 0
21m 1
21.999999m 1
22m 1
22.999999m 1
23m 1
23.999999m 1
24m 0
24.999999m 0

```



## Question 19

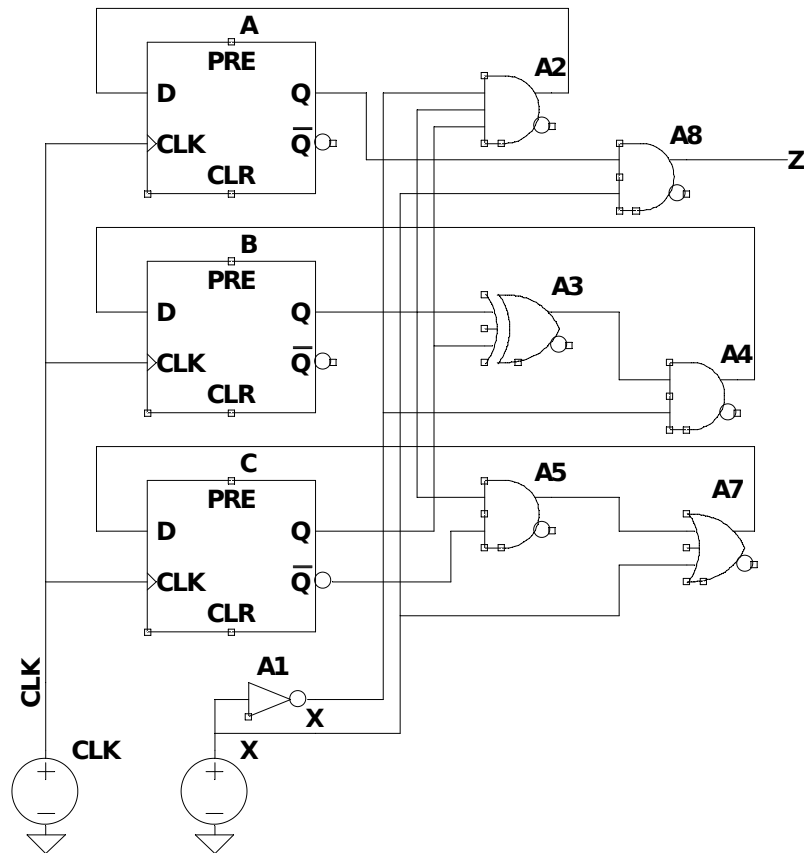


Figure 14: LTspice schematic for Q19

## Question 20

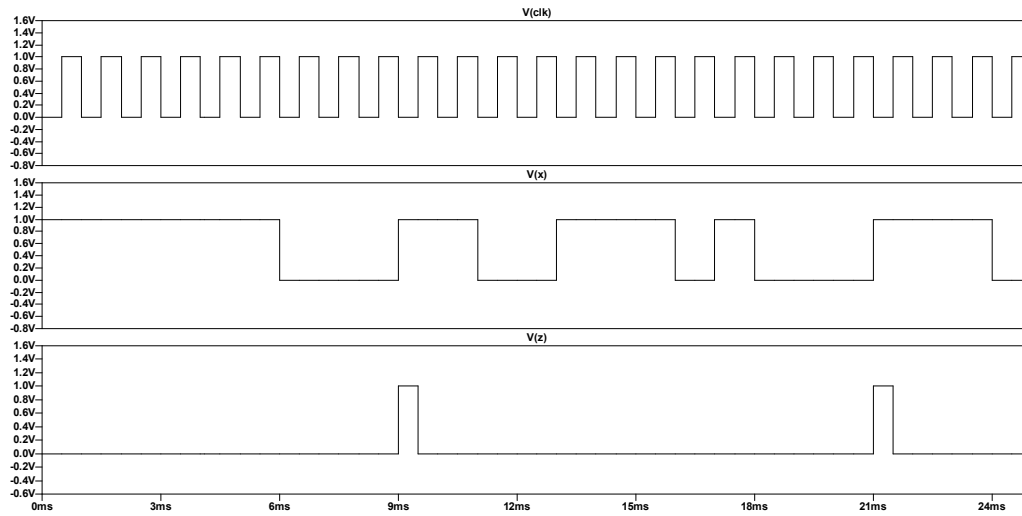


Figure 15: LTspice Simulation Traces V(CLK), V(X) and V(Z) for Q20