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ELECTRONIC PROCESSING AND COMMUNICATIONS

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LTspice Simulation of Sequential Circuits

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Question 1

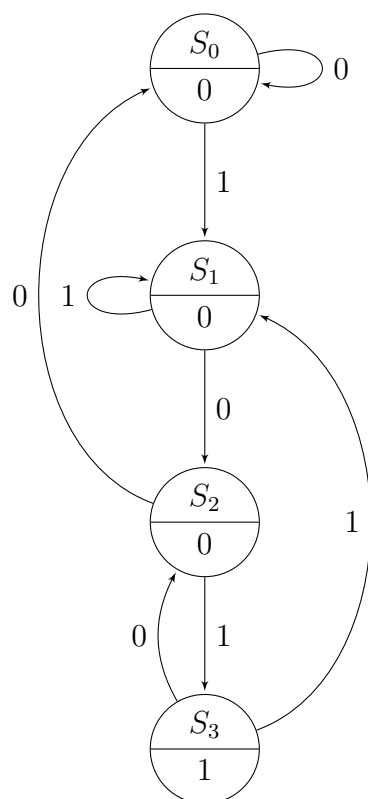


Figure 1: State Diagram for Q1

Question 2

<i>Present State</i> (<i>n</i>)	Next State (<i>n</i> +1)		Present Output <i>Z</i>
	X=0	X=1	
S_0	S_0	S_1	0
S_1	S_2	S_2	0
S_2	S_0	S_3	0
S_3	S_2	S_1	1

Table 1: State Transition Table in terms of S_0 and S_1

<i>Present State (n)</i>		Next State (n+1)				D-inputs required				Output Z
		X = 0		X = 1		X = 0		X = 1		
Q_n^A	Q_n^B	Q_{n+1}^A	Q_{n+1}^B	Q_{n+1}^A	Q_{n+1}^B	D_A	D_B	D_A	D_B	
0	0	0	0	0	1	0	0	0	1	0
0	1	1	0	0	1	1	0	0	1	0
1	0	0	0	1	1	0	0	1	1	0
1	1	1	0	0	1	1	0	0	1	1

Table 2: State Transition Table in terms of Q_n^A and Q_n^B

Question 3

		$Q_n^A Q_n^B$			
X		00	01	11	10
	0	0	1	1	0
	1	0	0	0	1

Figure 2: Karnaugh map for the Input of flip-flop D_A

		$Q_n^A Q_n^B$			
X		00	01	11	10
	0	0	0	0	0
	1	1	1	1	1

Figure 3: Karnaugh map for the Input of flip-flop D_B

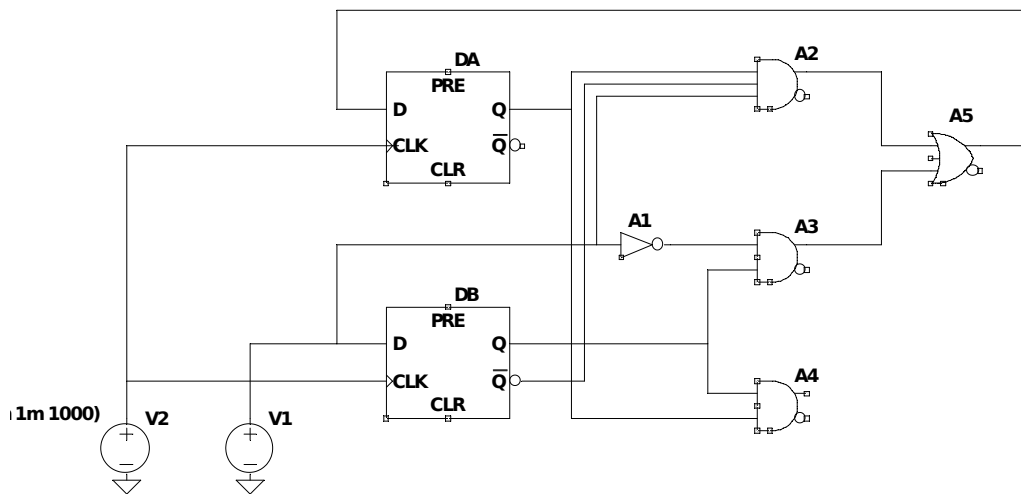
$$D_A = Q_n^B \cdot \overline{X} + Q_n^A \cdot \overline{Q_n^B} \cdot X \quad (1)$$

$$D_B = X \quad (2)$$

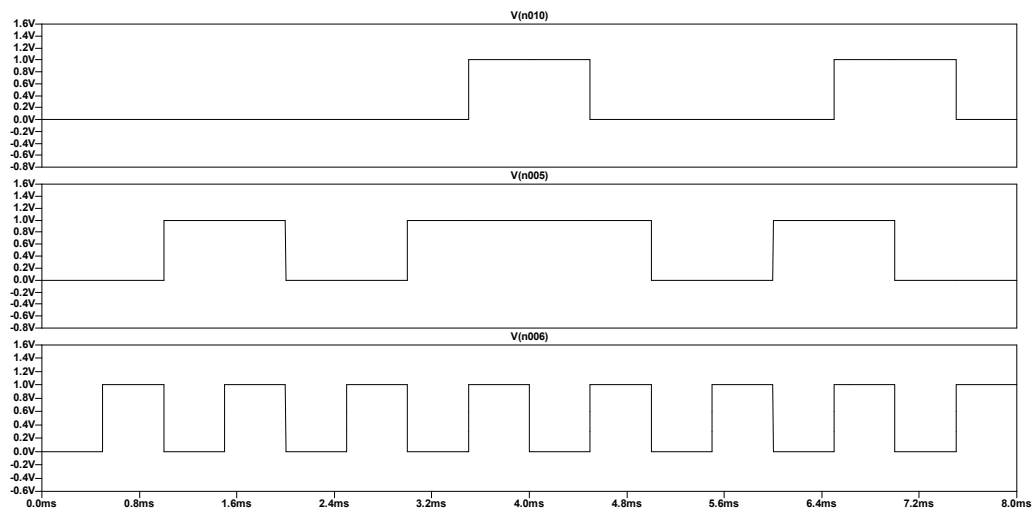
$$Z = Q_n^A \cdot Q_n^B \quad (3)$$

Eq. 1 is the input of flip-flop D_A derived from the Karnaugh map as shown in figure 2. Eq. 2 is the input of flip-flop D_B derived from the Karnaugh map as shown in figure 3. Eq. 3 is the output of the flip-flop D_A as shown by Table 2.

Question 4



Question 5



Question 6

Question 7

Question 8

Question 9

Question 10

Question 11

Question 12

Question 13

Question 14

Question 15

Question 16

Question 17

Question 18

Question 19

Question 20

References