The University of Nottingham

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Department of Electrical and Electronic Engineering Faculty of Engineering

Electronic Processing and Communications

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LTspice Simulation of Sequential Circuits

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Question 1

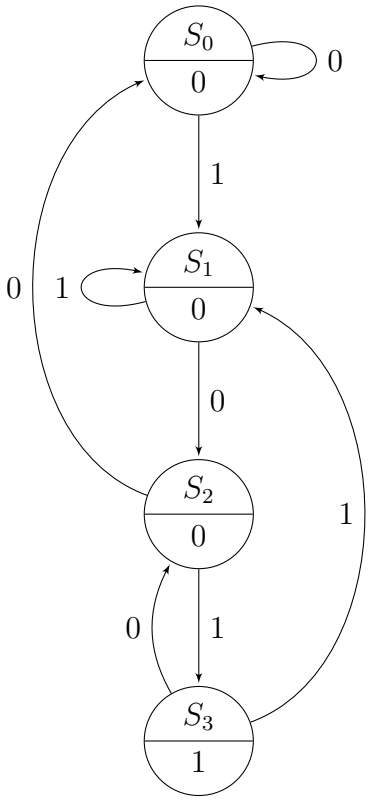


Figure 1: State Diagram for Q1

Question 2

Present State (n)	Next State (n+1)		Present Output
	X=0	X=1	Z
S_0	S_0	S_1	0
S_1	S_2	S_2	0
S_2	S_0	S_3	0
S_3	S_2	S_1	1

Table 1: State Transition Table in terms of S_0 and S_1

Present State (n)		Next State (n+1)				D-inputs reqired				Output Z
		X = 0		X = 1		X = 0		X = 1		
Q_n^A	Q_n^B	Q_{n+1}^A	Q_{n+1}^B	Q_{n+1}^A	Q_{n+1}^B	D_A	D_B	D_A	D_B	
0	0	0	0	0	1	0	0	0	1	0
0	1	1	0	0	1	1	0	0	1	0
1	0	0	0	1	1	0	0	1	1	0
1	1	1	0	0	1	1	0	0	1	1

Table 2: State Transition Table in terms of Q_n^A and Q_n^B

Question 3

X \ $Q_n^A Q_n^B$	00	01	11	10
0	0	1	1	0
1	0	0	0	1

Figure 2: Karnaugh map for the Input of flip-flop D_A

X \ $Q_n^A Q_n^B$	00	01	11	10
0	0	0	0	0
1	1	1	1	1

Figure 3: Karnaugh map for the Input of flip-flop D_B

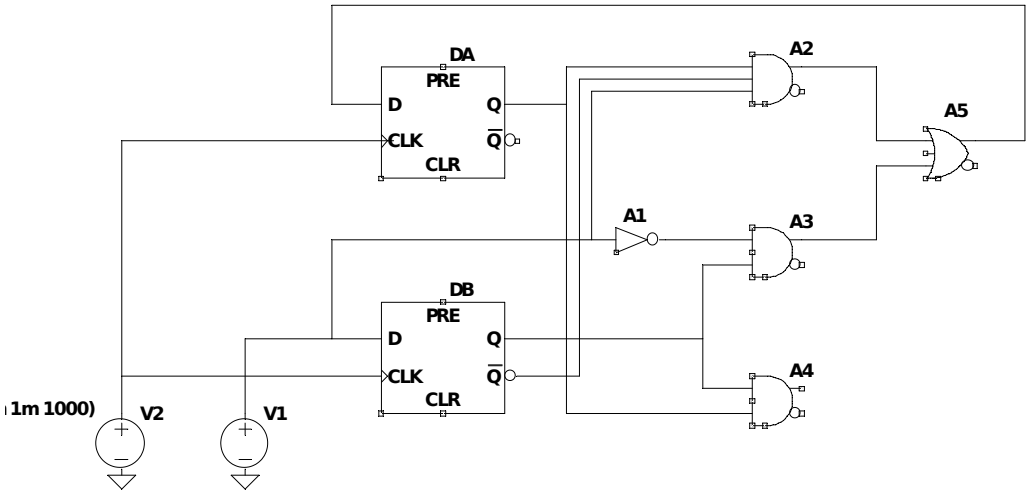
$$D_A = Q_n^B \cdot \overline{X} + Q_n^A \cdot \overline{Q_n^B} \cdot X \tag{1}$$

$$D_B = X \tag{2}$$

$$Z = Q_n^A \cdot Q_n^B \tag{3}$$

Eq. 1 is the input of flip-flop D_A derived from the Karnaugh map as shown in figure 2. Eq. 2 is the input of flip-flop D_B derived from the Karnaugh map as shown in figure 3. Eq. 3 is the output of the flip-flop D_A as shown by Table 2.

Question 4



Question 5

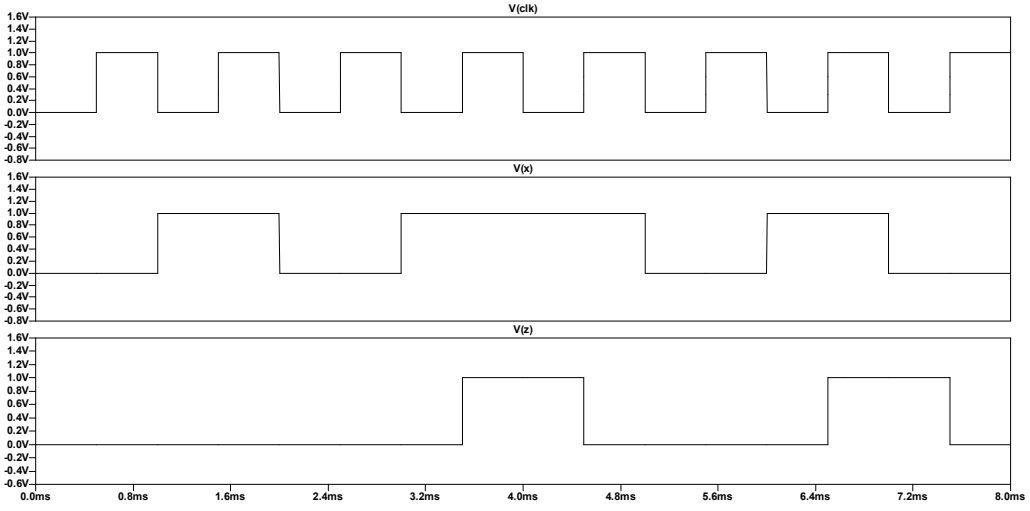


Figure 4: LTspice Simulation Traces V(CLK), V(X) and V(Z) for Q5

Question 6

$$t_{AFGCD} = t_{pd} + t_{A1} + t_{A5} \tag{4}$$

$$t_{DGCD} = t_{pd} + t_{A1} + t_{A5} \tag{5}$$

Eq. 4 and 5 denote the delay through paths t_{DGCD} and t_{AFGCD}.

Question 7

$$t_{JGCD} = t_{A1} + t_{A5} \tag{6}$$

Eq. 6 denotes the delay through path t_{JGCD}.

Question 8

$$\begin{aligned} t_{AEBCD} &= t_{pd} + t_{A2} + t_{A5} \\ &= 40ns + 27ns + 22ns \\ &= 89ns \end{aligned} \tag{7}$$

$$\begin{aligned} t_{AFGCD} &= t_{pd} + t_{A1} + t_{A5} \\ &= 40ns + 27ns + 22ns \\ &= 89ns \end{aligned} \tag{8}$$

$$\begin{aligned} t_{DGCD} &= t_{pd} + t_{A1} + t_{A5} \\ &= 40ns + 27ns + 22ns \\ &= 89ns \end{aligned} \tag{9}$$

Eq. 7, 8 and 9 denote the delay through paths t_{AEBCD}, t_{AFGCD} and t_{DGCD} respectively. The maximum delay of these three paths is $t_{min} = 89ns$.

Question 9

$$\begin{aligned} t_{JHBCD} &= t_{A4} + t_{A2} + t_{A5} \\ &= 22ns + 27ns + 22ns \\ &= 71ns \end{aligned} \tag{10}$$

$$\begin{aligned} t_{JGCD} &= t_{A1} + t_{A5} \\ &= 27ns + 22ns \\ &= 49ns \end{aligned} \tag{11}$$

Eq. 10 and 11 denote the delay through paths t_{JHBCD} and t_{JGCD} respectively. the maximum delay of these two paths is $t_{min} = 71ns$.

Question 10

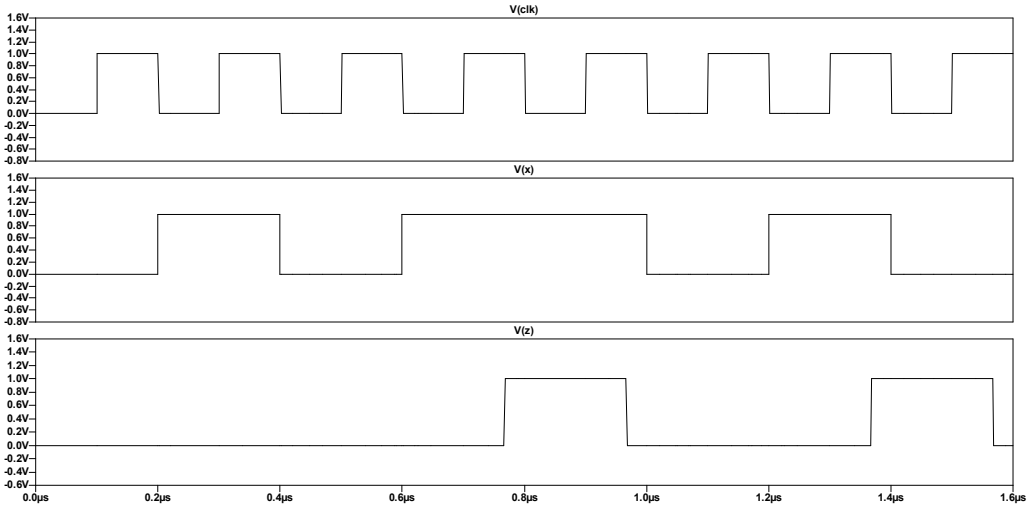


Figure 5: LTspice Simulation Traces V(CLK), V(X) and V(Z) for Q10

Question 11

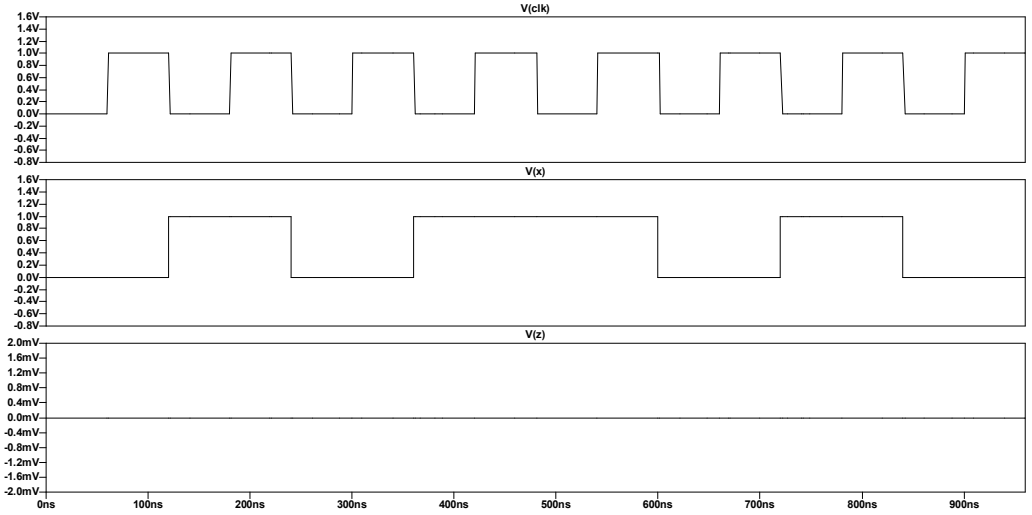


Figure 6: LTspice Simulation Traces V(CLK), V(X) and V(Z) for Q11

Figure 7 shows the output V(Z) as a flat line indicating the circuit is not operating correctly due to being clocked too fast.

V(X) clocked on the falling edge of V(CLK) and V(Z) is clocked on the rising edge of V(CLK). This means any change in V(X) only has half a clock cycle to propagate to the the input of D_a. $t_{JHBCD} = 71ns$ which is more than half of the clock cycle (60ns) when $t_{CLK} = 120ns$. This means the circuit is not operating correctly due to being clocked too fast.

Question 12

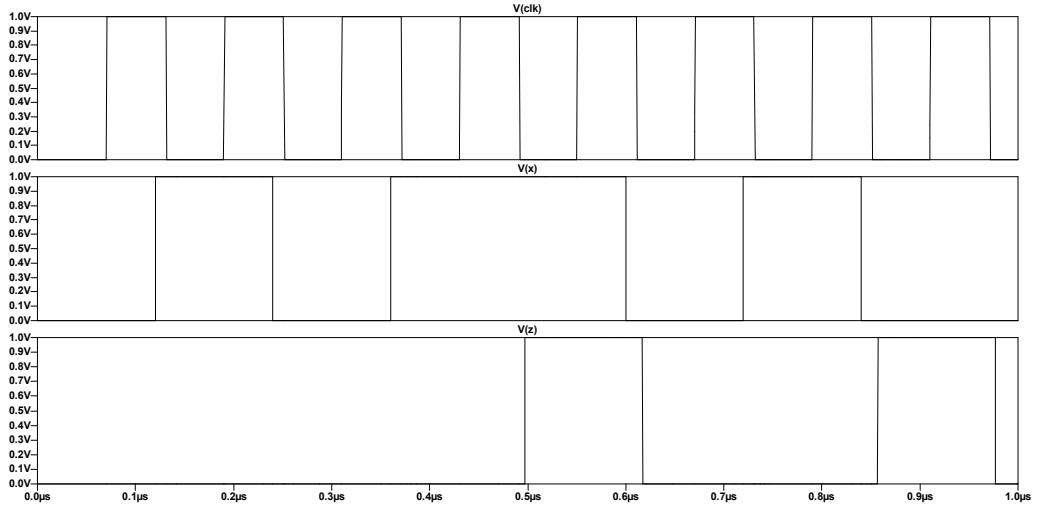


Figure 7: LTspice Simulation Traces V(CLK), V(X) and V(Z) for Q12

Figure 7 shows the output V(Z) now producing the correct output when clocked at 120ns. Introducing a delay of 10ns, the time between a change in V(x) and the rising edge of V(CLK) now becomes $60ns + 10ns + 0.5ns = 70.5ns$, where the 10ns is the additional delay and 0.5ns, the delay caused by a 1ns rise time. the mesured value of $t_{JHBCD} = 70.36$ which is less than 70.50ns therfore will propergate in time V(Z) to be clocked.

Question 13

State	Description of state
S_0	Initial State/Last bit is '0'
S_1	Detect '1' in most recent bit.
S_2	Detect '10' in most recent two bit.
S_3	Detect '100' in most recent two bit.
S_4	Detect '1000' in most recent two bit.

Table 3: State description table for mealy machine to detect the sequence 10001

Question 14

ID	20273662
Test sequence	10001
Test stream	11111100011001110100011110

Table 4: Data for Q14

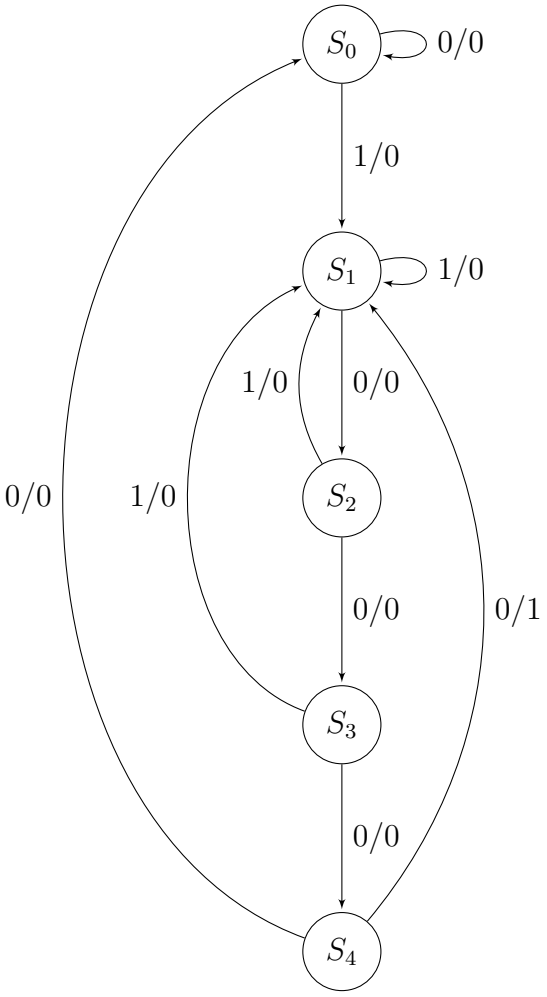


Figure 8: State Diagram for Q14

Question 15

The number of flip flops required is $\lceil \sqrt{n} \rceil$ where n is the number of states. In this case, $n = 5$ so $\lceil \sqrt{5} \rceil = 3$ flip flops are required. The flip-flip state allocation is shown in table 5 below.

State	Flip Flop Output		
	Q^A	Q^B	Q^C
S_0	0	0	0
S_1	0	0	1
S_2	0	1	0
S_3	0	1	1
S_4	1	0	0

Table 5: Flip Flop State Allocation

Question 16

Question 17

Question 18

Question 19

Question 20

References