TECHNICAL NOTE

INTERFACING SDRAM DEVICES WITH MOTOROLA'S MPC8XX

INTRODUCTION

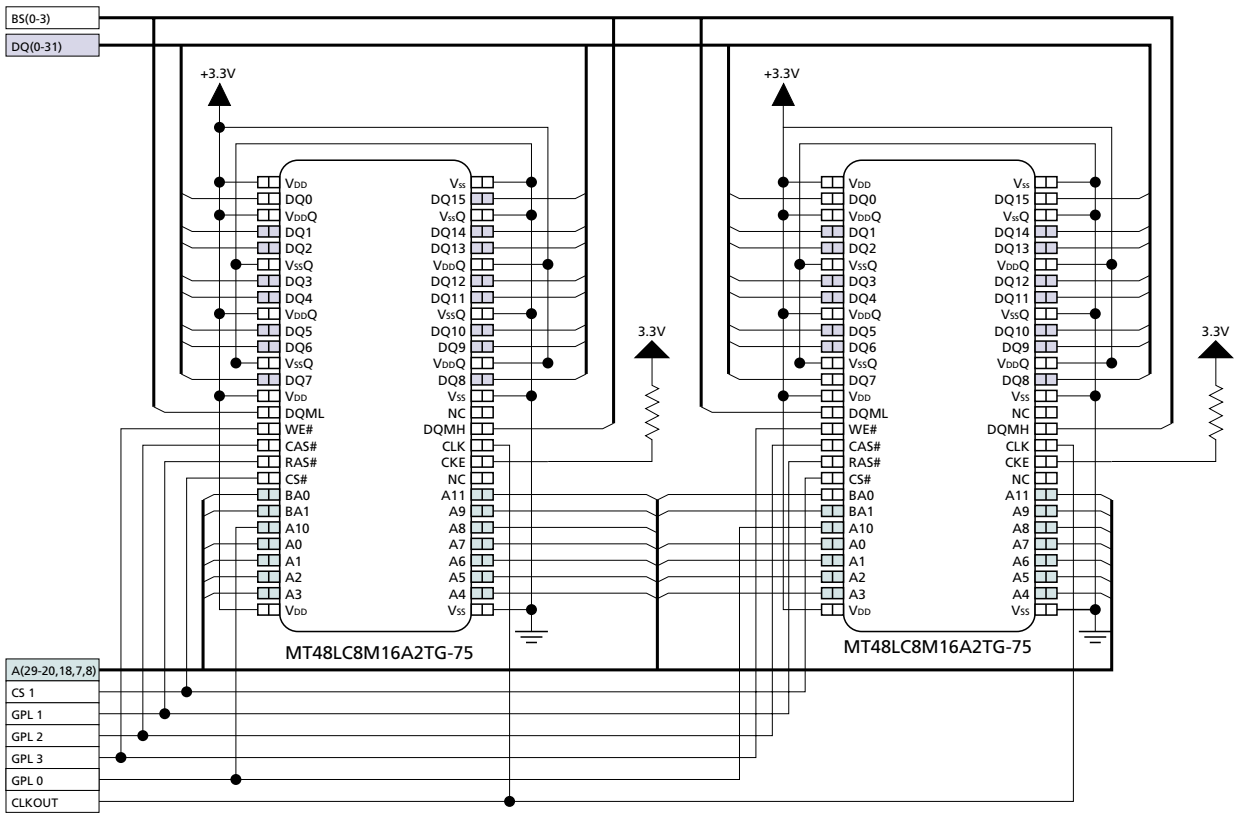
The Motorola MPC8xx integrated PowerPC™ microprocessor is designed for embedded solutions. The interface between this device and an SDRAM is done through one of the two UPMs (User Programmable Machines) to provide a glueless interface. The UPM is a RAM based programmable machine controlling the external signals connected to the SDRAM supporting both single and burst READs and WRITEs.

INTERFACE

The hardware interface from SDRAM to the MPC8xx family requires a complete understanding of how the address multiplexing is done by the UPM. Diagram 1 illustrates this interface using two MT48LC8M16A2 SDRAM devices in a 32-bit wide configuration.

The addressing for the MCP8xx uses A0 as the Most Significant Bit (MSB), while the MSB for the SDRAM are the bank address lines BA1 and BA0 followed by A11. For the MPC8xx the Least Significant Bits (LSB), A31 and A30, are left unconnected when implementing a 32-bit wide bus. For a 16-bit wide bus, A31 is left unconnected. Table 1 shows the address multiplexing for two of the MT48LC8M16A2 devices with two bank address lines, 12 row addresses, and 9 columns. From Table 1, the physical hardware connection scheme can be derived as displayed in Table 2. Note that address pin A19 for the MPC8xx is not connected to the SDRAM. Instead, the pin A10 for the SDRAM is connected to GPL0 on the MPC8xx for Auto Precharge control during READ and WRITE sequences. Setting the MxMR bits 16-18 in the UPM to 0b001 will mux A10 to GPL0 for addressing control during ACTIVE commands pre-

Diagram 1
MPCxx/SDRAM Hardware Interface



formed by the UPM. Refer to page 16-15 of the Motorola MPC860 User's Manual, Rev 1 for more detailed information.

The address multiplexing is done in a similar way for all SDRAMs regardless of the densities and/or configuration. For example, if the design requires two 256Mb (MT48LC16M16A2) components, the only change would be adding A12 mapped to A17 for the MPC8xx which also moves the Bank Address pins on the SDRAM to A7 and A6. This is on the hardware side only. The UPM will have to be programmed for the different densities and memory configurations. This is done in the MxMR[AMx] register bits. For the 128Mb: x16 example in Table 2, address bits A20-A9 have to be multiplexed to A29-A18 of the MPC8xx for the Row address. Table 16-17 on page 16-44 of the Motorola MPC860 User's Manual Rev1, notes that the MxMR[AMx] register must be set to 0b001.

Table 1
Address Multiplexing

	LSB	COLUMN ADDRESS	ROW ADDRESS	BANK ADDRESS
Number	2	9	12	2
MPC8xx Address	A(31-30)	A(29-21)	A(20-9)	A(8-7)

Table 2
Address Multiplexing

8xx Address	SDRAM/8xx Map	8xx Mux	8xx Pin	SDRAM Pin
A31				
A30				
A29	Column A0	A20	A29	A0
A28	A1	A19	A28	A1
A27	A2	A18	A27	A2
A26	A3	A17	A26	A3
A25	A4	A16	A25	A4
A24	A5	A15	A24	A5
A23	A6	A14	A23	A6
A22	A7	A13	A22	A7
A21	A8	A12	A21	A8
A20	Row A9	A11	A20	A9
A19	A10	A10	GPL0	A10
A18	A11	A9	A18	A11
A17	A12			
A16	A13			
A15	A14			
A14	A15			
A13	A16			
A12	A17			
A11	A18			
A10	A19			
A9	A20			
A8	BA0		A8	BA0
A7	BA1		A7	BA1

The RAS#, CAS#, and WE# pins for the SDRAM should be connected to GPL1, GPL2, and GPL3 on the MPC8xx controller. The CS# for the SDRAM is connected to one of the eight CS lines on the MPC8xx, typically starting with CS1. CS0 is usually reserved for the boot ROM.

There are a few key points to remember when designing an interface between the MPC8xx PowerPC and SDRAM. The width of the SDRAM part is only indirectly related to how the address multiplexing is accomplished in the MPC8xx. The total width of the bus is the key. Each bank in the MPC8xx Memory Controller can support an 8, 16, or 32-bit wide bus from almost any combination of SDRAM components. From the previous example, the last two LSBs are left as No-Connects. This is always done for a total bus width of 32. For a bus width of 16, only the LSB is left as a No-Connect. For a bus width of 8 there are no No-Connects, the addressing starts with the LSB A31.

Word of caution: under no circumstances should the 60x Bus signals be used with the Memory Controller signals, especially the 60x R/W signals.

UPM OPERATIONS

The UPM RAM array controls all of the signals connecting the MPC8xx to the SDRAM devices, which include the Chip Selects [0-7], Byte Selects [0-3], and GPLs [0-5]. The UPM will assume control over these signals when one of two of the following events takes place:

1. When a bus access is automatically initiated by the MPC8xx or other external bus master.
2. When a RUN command is initiated in the MCR (Memory Command Register) by MPC8xx software.

The UPM RAM array can be written to or read from by issuing the appropriate command in the MCR register by software. This is how the RAM array, as seen in Figures 1, 2, and 3 is initially built—using the MDR (Memory Data Register) as a source of data used to build the array and the WRITE command from the MCR. Each SDRAM command, such as ACTIVATE, READ, or WRITE, is stored into the RAM array individually to set up the appropriate command sequence to be executed by the UPM. Careful attention should be given to make sure the sequences adhere to all of the AC timing parameters as defined in the SDRAM data sheet. In Figures 1-3 some of the NOP commands can be eliminated or added depending on the speed of the SDRAM being used. Please refer to the SDRAM data sheet for AC timing specifications.

Most SDRAM operating sequences that are programmed from the MCR start from a location predefined in the UPM RAM array. The operation will continue until the last bit command unless there is a loop programmed into the sequence. The starting locations in the RAM array for the specific access types are predefined and cannot be changed. See Table 3 for a list of these accesses and their staring locations. The UPM will automatically begin at these starting points when the memory controller detects a bus access involving the SDRAM and continue until the LAST bit is detected in the RAM word. This is the reason the starting locations are set and cannot be changed.

Table 3
Predefinded Starting Locations for the UPM RAM Array

0x00 for read single beat access
0x08 for read burst access
0x18 for write single beat access
0x20 for write burst access
0x30 for periodic timer access
0x3c for exception access

The MPC860 UPM Programming Tool found on Motorola's web page is useful when developing the UPM RAM array. This can be found on the Netcom Tools page, http://www.mot.com/SPS/RISC/netcomm/tools/. The MPC860 UPM Programming Tool has a wave editor window that graphically displays the internal RAM array in the UPM and how it is programmed. The RAM word bit settings can be found in the MPC860 Users Manual, Rev 1 on page 16-36 through 16-39.

Note that any unused portion of the RAM array can be used to store any sequence to be initiated by software in the MCR register to address operations such as Mode Register Settings, Self Refresh, and Power Down. The following locations are left free in this example and illustrated in gray on Figures 1-3. This does not mean there might be more free locations depending on the SDRAM device and speed grade. RAM array accesses from the MCR register using the RUN command is exactly the same as the MPC8xx bus accesses.

Table 4
Open Locations in the UPM RAM Array

0x03 to 0x07 (5 locations)
0x0d to 0x17 (11 locations)
0x1b to 0x1f (5 locations)
0x25 to 0x2f (11 locations)
0x34 to 0x3b (8 locations)
0x3d to 0x3f (4 locations)

The Mode Register setting uses both the MCR and the MAR registers on the MPC8xx. The hex code needed to program the SDRAMs MODE REGISTER is loaded into the MAR register and the RUN command is initiated in the MCR with the appropriate starting location in the UPM RAM array. Another note of caution, be sure to make adjustments to the value placed in the MAR to take into account whether A30 and/or A31 on the MPC8xx are no-connects depending on the bus width. This is done by shifting the value left one or two places before loading the MAR register.

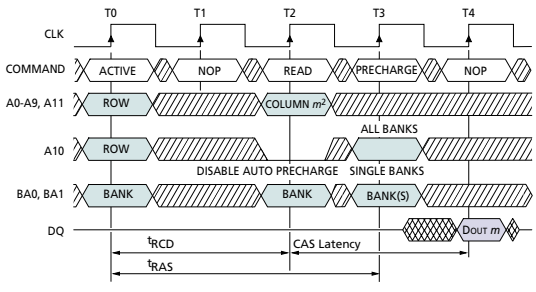
Figure 1
Single Bit and Burst Read UPM Code

		Ram Array Location and Bit Location																						
	DRAM Commands	ACTIVATE	NOP	READ	PRECHARGE	NOP				ACTIVATE	NOP	READ	NOP	NOP	NOP	PRECHARGE	NOP							
NAME	DESCRIPTION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CST4	Defines the CS# state	0	0	0	0	0				0	0	0	0	0	0	0	0								
CST1		0	0	0	0	0				0	0	0	0	0	0	0	0								
CST2		0	0	0	0	0				0	0	0	0	0	0	0	0								
CST3		0	0	0	0	1				0	0	0	0	0	0	0	1								
BST4	Defines the DQM state	1	1	0	1	1				1	1	0	0	0	0	1	1								
BST1		1	1	0	1	1				1	1	0	0	0	0	1	1								
BST2		1	1	0	1	1				1	1	0	0	0	0	1	1								
BST3		1	1	0	1	1				1	1	0	0	0	0	1	1								
G0L	Defines the state of A10	0	1	1	1	1				0	1	1	1	1	1	1	1								
G0L		0	1	0	1	1				0	1	0	1	1	1	1	1								
G0H		0	1	1	1	1				0	1	1	1	1	1	1	1								
G0H		0	1	1	1	1				0	1	1	1	1	1	1	1								
G1T4	RAS# Control	0	1	1	0	1				0	1	1	1	1	1	0	1								
G1T3		1	1	1	1	1				1	1	1	1	1	1	1	1								
G2T4	CAS# Control	1	1	0	1	1				1	1	0	1	1	1	1	1								
G2T3		1	1	1	1	1				1	1	1	1	1	1	1	1								
G3T4	WE# Control	1	1	1	0	1				1	1	1	1	1	1	0	1								
G3T3		1	1	1	1	1				1	1	1	1	1	1	1	1								
G4T4/DLT3	GPL4 Control	1	1	1	1	1				1	1	1	1	1	1	1	1								
G4T3/WAEN	GPL4 Control	1	1	1	1	1				1	1	1	1	1	1	1	1								
G5T4	GPL5 Control	1	1	1	1	1				1	1	1	1	1	1	1	1								
G5T3	GPL5 Control	1	1	1	1	1				1	1	1	1	1	1	1	1								
-	Reserved	0	0	0	0	0				0	0	0	0	0	0	0	0								
-	Reserved	0	0	0	0	0				0	0	0	0	0	0	0	0								
Loop	Loop Control	0	0	0	0	0				0	0	0	0	0	0	0	0								
EXEN	Exception Bit for Reset	0	0	0	0	0				0	0	0	0	0	0	0	0								
AMX	Defines the Address Multiplexing	0	0	0	0	0				0	0	0	0	0	0	0	0								
AMX		0	0	0	0	0				0	0	0	0	0	0	0	0								
NA	Enables address incrementing	0	0	0	0	0				0	0	0	0	0	0	0	0								
UTA	Data Transfer Acknowledge	1	1	1	0	1				1	1	1	0	0	0	0	1								
TODT	Disables UPM Timer	0	0	0	0	0				0	0	0	0	0	0	0	0								
LAST	Defines last DRAM command in the Ram Array	0	0	0	0	1				0	0	0	0	0	0	0	1								
	Hex Value	0x0f07fc04	0x0ffffc04	0x00bdfc04	0x0ff77c00	0x1ffffc05				0x0f07fc04	0x0ffffc04	0x00bdfc04	0x00fffc00	0x00fffc00	0x00fffc00	0x0ff77c00	0x1ffffc05								

UPM RAM Array Starting Location

UPM RAM Array Last Bit

Figure 1a
Single Bit and Burst Read Diagrams For UPM Code



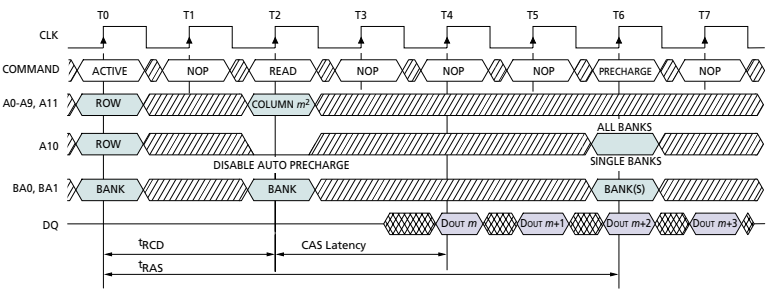


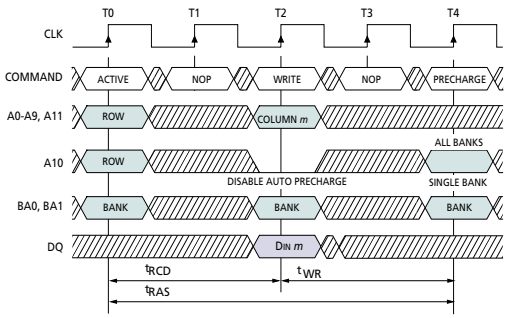
Figure 2
Single Bit and Burst WRITE UPM Code

		Ram ArrayLocation and Bit Location																						
	DRAM Commands	ACTIVATE	NOP	WRITE	NOP	PRECHARGE	NOP			ACTIVATE	NOP	WRITE	NOP	NOP	NOP	NOP	PRECHARGE	NOP						
NAME	DESCRIPTION	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CST4	Defines the CS# state	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
CST1		0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
CST2		0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
CST3		0	0	0	0	0	1			0	0	0	0	0	0	0	0	1							
BST4	Defines the DQM state	1	1	0	1	1	1			1	1	0	0	0	0	1	1	1							
BST1		1	1	0	1	1	1			1	1	0	0	0	0	1	1	1							
BST2		1	1	0	1	1	1			1	1	0	0	0	0	1	1	1							
BST3		1	1	0	1	1	1			1	1	0	0	0	0	1	1	1							
G0L	Defines the state of A10	0	1	1	1	1	1			0	1	1	1	1	1	1	1	1							
G0L		0	1	0	1	1	1			0	1	0	1	1	1	1	1	1							
G0H		0	1	1	1	1	1			0	1	1	1	1	1	1	1	1							
G0H		0	1	1	1	1	1			0	1	1	1	1	1	1	1	1							
G1T4	RAS# Control	0	1	1	1	0	1			0	1	1	1	1	1	1	0	1							
G1T3		1	1	1	1	1	1			1	1	1	1	1	1	1	1	1							
G2T4	CAS# Control	1	1	0	1	1	1			1	1	0	1	1	1	1	1	1							
G2T3		1	1	1	1	1	1			1	1	1	1	1	1	1	1	1							
G3T4	WE# Control	1	1	0	1	0	1			1	1	0	1	1	1	1	0	1							
G3T3		1	1	1	1	1	1			1	1	1	1	1	1	1	1	1							
G4T4/DLT3	GPL4 Control	1	1	1	1	1	1			1	1	1	1	1	1	1	1	1							
G4T3/WAEN	GPL4 Control	1	1	1	1	1	1			1	1	1	1	1	1	1	1	1							
G5T4	GPL5 Control	1	1	1	1	1	1			1	1	1	1	1	1	1	1	1							
G5T3	GPL5 Control	1	1	1	1	1	1			1	1	1	1	1	1	1	1	1							
-	Reserved	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
-	Reserved	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
Loop	Loop Control	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
EXEN	Exception Bit for Reset	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
AMX	Defines the Address Multiplexing	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
AMX		0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
NA	Enables address incrementing	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
UTA	Data Transfer Acknowledge	1	0	1	1	1	1			1	0	0	0	0	1	1	1	1							
TODT	Disables UPM Timer	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0							
LAST	Defines last DRAM command in the Ram Array	0	0	0	0	0	1			0	0	0	0	0	0	0	0	1							
	Hex Value	0x0f07fc04	0x0ffffc00	0x00bd7c04	0x0ffffc04	0x0ff77c04	0x1ffffc05			0x0f07fc04	0x0ffffc00	0x00bd7c00	0x00fffc00	0x00fffc00	0x00fffc04	0x0ffffc04	0x0ff77c04	0x1ffffc05							

UPM RAM Array Starting Location

UPM RAM Array Last Bit

Figure 2a
Single Bit and Burst WRITE Diagrams For UPM Code



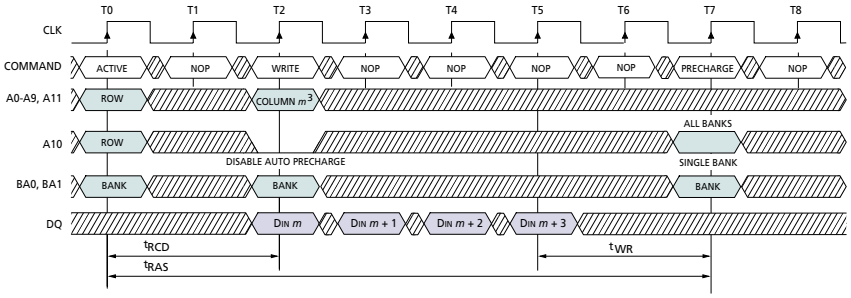


Figure 3
AUTO REFRESH UPM Code

		Ram Array Location and Bit Location															
	DRAM Commands	PRECHARGE ALL	NOP	AUTO REFRESH	NOP	NOP	NOP	NOP									
NAME	DESCRIPTION	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CST4	Defines the CS# state	0	0	0	0	0	0	0									
CST1		0	0	0	0	0	0	0									
CST2		0	0	0	0	0	0	0									
CST3		0	0	0	0	0	0	1									
BST4	Defines the DQM state	1	1	1	1	1	1	1									
BST1		1	1	1	1	1	1	1									
BST2		1	1	1	1	1	1	1									
BST3		1	1	1	1	1	1	1									
G0L	Defines the state of A10	1	1	1	1	1	1	1									
G0L		1	1	1	1	1	1	1									
G0H		1	1	1	1	1	1	1									
G0H		1	1	1	1	1	1	1									
G1T4	RAS# Control	0	1	0	1	1	1	1									
G1T3		1	1	1	1	1	1	1									
G2T4	CAS# Control	1	1	0	1	1	1	1									
G2T3		1	1	1	1	1	1	1									
G3T4	WE# Control	0	1	1	1	1	1	1									
G3T3		1	1	1	1	1	1	1									
G4T4/DLT3	GPL4 Control	1	1	1	1	1	1	1									
G4T3/WAEN	GPL4 Control	1	1	1	1	1	1	1									
G5T4	GPL5 Control	1	1	1	1	1	1	1									
G5T3	GPL5 Control	1	1	1	1	1	1	1									
-	Reserved	0	0	0	0	0	0	0									
-	Reserved	0	0	0	0	0	0	0									
Loop	Loop Control	0	0	1	0	0	1	0									
EXEN	Exception Bit for Reset	0	0	0	0	0	0	0									
AMX	Defines the Address Multiplexing	0	0	0	0	0	0	0									
AMX		0	0	0	0	0	0	0									
NA	Enables address incrementing	0	0	0	0	0	0	0									
UTA	Data Transfer Acknowledge	1	1	1	1	1	1	1									
TODT	Disables UPM Timer	0	0	0	0	0	0	0									
LAST	Defines last DRAM command in the Ram Array	0	0	0	0	0	0	1									
	Hex Value	0ff77c04	0x0ffffc04	0x0ff5fc84	0x0ffffc04	0x0ffffc04	0x0ffffc84	0x1ffffc05									

UPM RAM Array Starting Location

UPM RAM Array Last Bit

UPM Loop

UPM SPECIFIC REGISTERS

The MPC8xx microprocessor has four specific registers to define the interface and functionality for the SDRAM components.

1. Machine x Mode Register, MxMR defines the global features for each UPM (MAMR and MBMR).
2. Memory Command Register, MCR executes READs and WRITEs to the UPM Ram array. It is also used to access the UPM RAM array for operations such as loading the SDRAMs Mode Register.
3. Memory Data Register, (MDR) is programmed with data to be written to the UPM RAM array for the UPM MCR register when building the array.
4. Memory Address Register is used to specify the address driven on the external bus when the RUN command is issued from the MCR register to the UPM RAM array.

The additional two registers are the Base Register, BRx and the Option Register, ORx. There are eight pairs [0-7] of the BRx and ORx registers, one pair for each bank of the MPC8xx. Both of these registers are used with the UPM and the GPCM memory controllers. The GPCM will not be covered in this document because it cannot be used to interface to SDRAM components. The BRx is used to define the Base Address for the particular Bank and other general addressing issues such as the selection of which controller will be used for a specific bank of memory (UPMA or UPMB). The reference to bank is not in relation to the SDRAM internal banks but to the multiple banks of memory that the MPC8xx supports. The ORx is used to set up the address comparison for the external bus.

GENERAL OPERATION

General operation of the PowerPC and SDRAM is fairly straight forward once the UPM RAM array is setup and the registers are defined. As described earlier, the RAM array is programmed using the MCR[OP] and the MCR[MAD] register bits. The binary data word to be programmed into the RAM array is loaded into the Memory Data Register, MDR. This would correspond to a command on the SDRAM side such as an ACTIVE command. The MCR[MAD] bits identify the location where the data in the MDR is to be written in the RAM array. The WRITE opcode field in the MCR[OP] is then set to 0b0,0 to initiate a WRITE transfer. This is done for each SDRAM command in the RAM array word to build the timing sequences as illustrated on pages 4 through 6.

The MxMR register can then be programmed followed by the ORx and BRx registers. The ORx and BRx registers should always be programmed after all of the UPM specific registers are set up. Once the UPM specific register are set the ORx register should be initialized prior to the BRx register. The one exception is after hardware reset the BR0 register is programmed before the OR0 register when programming the boot chip select.

The MPC8xx UPM controller does not keep track of row or bank addresses for the READ and WRITE bus accesses so every access needs to start over with a new ACTIVE command. This prevents any interleaving between internal SDRAM banks.

SELF-REFRESH

Placing the SDRAM components into Self Refresh mode can be accomplished by connecting CKE to GPL5 on the MPC8xx. The CKE pin in this case should be viewed as one more command pin like the RAS# or CAS# pins. Self-Refresh is initiated by programming the UPM RAM with an AUTO REFRESH command in one of the unused locations of the RAM array which forces GPL5 (CKE) low during the AUTO REFRESH command. For exiting Self Refresh, a NOP command needs to be stored in another unused area of the RAM array which forces GPL5 (CKE) high for that NOP command.

As an example, starting in address 0x0d program the SELF REFRESH command as described above and its last word should include the LAST bit set. In a similar way, the Self Refresh Exit sequence can be stored (as an example) starting in address 0x1b, and again, its last word should include the LAST bit set.

Use the RUN command in the MCR register to execute these UPM RAM array location for the desired command.

Table 5
Self Refresh

SDRAM COMMAND	UPM RAM WORD
SELF REFRESH Entry	0x08000200D
SELF REFRESH Exit	0x08000201B

Table 6
MxMR Register Descriptions

BITS	NAME	DESCRIPTION
0-7	PTx	Periodic Timer period, PTx bits will set the UPMs internal counter to make sure Refresh is taken care of at in the appropriate amount of time.
8	PTxE	Periodic Timer enable, PTXE bit will enable the refresh counter in the UPM. PTxE disable = 0, PTXE enable = 1
9-11	AMx	Address Multiplex Size, AMx bits set the address multiplexing refer to table 16-17 in the MPC860 users manual and Table 2 in this document. In reference to the first row address in relation the MPC8xx address pin.
12	–	Reserved, Do not use
13-14	DSx	Disable Timer Period, DSx sets the ^{t}RAS(MIN) requirement in clock cycles for the UPM. 00 – 1 clock 01 – 2 clocks 10 – 3 clocks 11 – 4 clocks
15	–	Reserved, Do not use
16-18	G0CLx	General Line 0 Control, G0CL selects the Auto precharge pin on the SDRAM. 010 = A10
19	GPLx4DIS	GPL out put line disable, GPLx4DIS is set to either freeze the UPM or use GPL4 as the WE# pin in the SDRAM 0 - defines GPL4 1 – defines UPWAIT
20-23	RLFx	Read Loop Field x, RLFx specifies the number of times a read loop is executed in binary with 0001=1....1111=15. Note 0000=16
24-27	WLFx	Write Loop Field x, WLFx specifies the number of times a write loop is executed in binary similar to the RLFx
28-31	TLFx	Timer Loop Field x, TLFx defines the number of times a loop is executed by the UPM RAM word in binary.

Table 7
MCR Register Descriptions

BITS	NAME	DESCRIPTION
0-1	OP	Command Opcode, OP defines the operation to be executed by the UPM. 00 – WRITE, 01 – 01 READ, 10 – RUN, 11 – Reserved
2-7	–	Reserved, Do not use
8	UM	User Machine, UM defines which UPM machine the command is entended 0 – UPMA, 1 - UPMB
9-15	–	Reserved, Do not use
16-18	MB	Memory Bank, MB defines which Chip Select (CS#) pin is to used in binary CS0 – 000, CS1 – 001…..
19	–	Reserved, Do not use
20-23	MCLF	Memory Command Loop Field, MCLF defines how many times the UPM is executed for a run command in binary.
24-25	–	Reserved, Do not use
26-31	MAD	Memory array index, MAD is an index to the starting location for the 64 RAM words in the array

Table 8
MDR Register Descriptions

BITS	NAME	DESCRIPTION
0-31	MD	Memory Data, MD defines the data to be written to the RAM array

Table 9
MAR Register Descriptions

BITS	NAME	DESCRIPTION
0-31	MA	Memory Address, MA specify the address driven on the external bus when the RUN command is issued from the MCR. Used to define contact of the SDRAM Mode Register.

Table 10
MPTPR Register Descriptions

BITS	NAME	DESCRIPTION
0-7	PTP	Periodic Timer Prescaler, PTP contains the division factor needed to define the Refresh interval
8-15	–	Reserved, Do not use

Table 11
BRx Register Descriptions

BITS	NAME	DESCRIPTION
0-16	BA	Base Address. Used for access to multiple external memory banks in conjunction with ORx[AM] register.
17-19	AT	Address Type: Used to limit access to curtain address in the SDRAM if needed
20-21	PS	Port Size: Specifies the total external bus width. 00 – 32 Bits Wide 01 – 8 Bits Wide 10 – 16 Bits Wide 00 – Reserved
22	PARE	Parity Enable: Enables parity for error detection. 0 – Disable 1 - Enable
23	WP	Write Protect: Sets a portion of the memory in a READ only state within a defined address space 0 – Disable 1 – Enable
24-25	MS	Machine Select: Selects the Memory controller that is being used 00 – GPCM not used for SDRAM 01 – Reserved 10 – UPM A 11 – UPM B
26-30	–	Reserved
31	V	Valid: Indicates the contents of the BRx and the ORx registers are valid

Table 12
ORx Register Descriptions

BITS	NAME	DESCRIPTION
0-16	AM	Address Mask: Used for multiple external memory bank interfaces. The AM bits work in conjunction with the BRx[BA] register bits. 0 – Address is Masked 1 – Address Bit is Used in the Comparison with BRx[BA]
17-19	ATM	Address Type Mask: Restricts access to desired memory addresses in the external memory bank
20	SAM	Start Address Multiplex: Determines the address multiplexing as defined in the MxMR[AMx] register. Should be set to 1 for SDRAM 0 – Not Multiplexed internally 1 – Reflects Address in the MxMR[AMx] Register
21-22	G5LA	General Purpose Line 5: Determines the control of the GPL5 control pin on the MPC 8xx. GPL5 is typically not used unless there is a need for control of CKE for the SDRAM device 0 – Output driven on GPL_B5 1 – Output driven on GPL_A5
	G5LS	0 – GPL5 Low on the falling edge of GCLK1_50 1 – GPL5 High on the falling edge of GCLK1_50
23	BIH	Burst Inhibit: Indicates if the memory device supports burst accesses. All SDRAM devices support burst access. 0 – Burst Support 1 – No Burst Support
24-27	SCY	Only used for the GPCM machine
28	SETA	Only used for the GPCM machine
29	TRLX	Only used for the GPCM machine
30	EHTP	Only used for the GPCM machine
31	–	Reserved

CONCLUSION

There are a few key points to remember when interfacing the MPC8xx microprocessor with SDRAM.

The address multiplexing is one area in the implementations that should not deviate from the example. While this was not the case with older DRAM technologies such as EDO or Fast Page mode DRAMs, with SDRAM devices the address connections are also used to program the MODE REGISTER to define the device's operation. Deviation from the standard address multiplexing can cause unknown values in the mode register causing the SDRAM device to not function properly.

When dealing with multiple external SDRAM banks it is important to remember the LOAD MODE REGISTER command needs to be done for both banks of memory. The periodic timer also needs to be adjusted to compensate for the added memory.

When programming the UPM it is important to have the GOL0, GOL1, GOH0, and GOH1 bits in the RAM array set low during all SDRAM ACTIVE commands. This will allow the UPM to use the A10 line as a row address during ACTIVE command for the SDRAM.

Finally, this document covers only one way to implement the MPC8xx microprocessor with SDRAM and is by no means the only way it can be done.

REFERENCES

1. Rick Nelson at Motorola
2. MPC860 Users Manual Rev. 1
3. Motorola SDRAM MPC8xx Application Note

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992