

ASR8601 Brief Specification

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Table of Content

OVERVIEW.....	4
1 SOC DEVICE FEATURES	5
1.1 PLATFORM FEATURES	5
1.2 MULTIMEDIA FEATURES.....	7
1.3 MODEM FEATURES.....	9
REVISION HISTORY	10

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Overview

ASR8601 is a System on Chip (SoC) device which highly integrates both application processing subsystem, the baseband modem and cellular RF to enable 4G LTE multimedia smartphone applications. The application subsystem integrates quad-Core 64-bit processors ARM Cortex A55 operating up to 1.5 GHz. It also integrates multimedia sets, include GPU, Video codec, Image processing engine, Audio system, Display system and Camera system for advanced multimedia services such as streaming video, audio, a multitude of decoders and encoders and ISP processing.

On the connectivity, it integrated GNSS/FM module with RF on chip. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays, MMC/SD cards, various sensors such as accelerometer, gravity, gyros sensors etc., and external Bluetooth, Wi-Fi, NFC modules.

An ARM Cortex-R5, and 2G/3G/4G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 4, WCDMA R7.

The highlighted SoC device block diagram is shown in Figure 1.

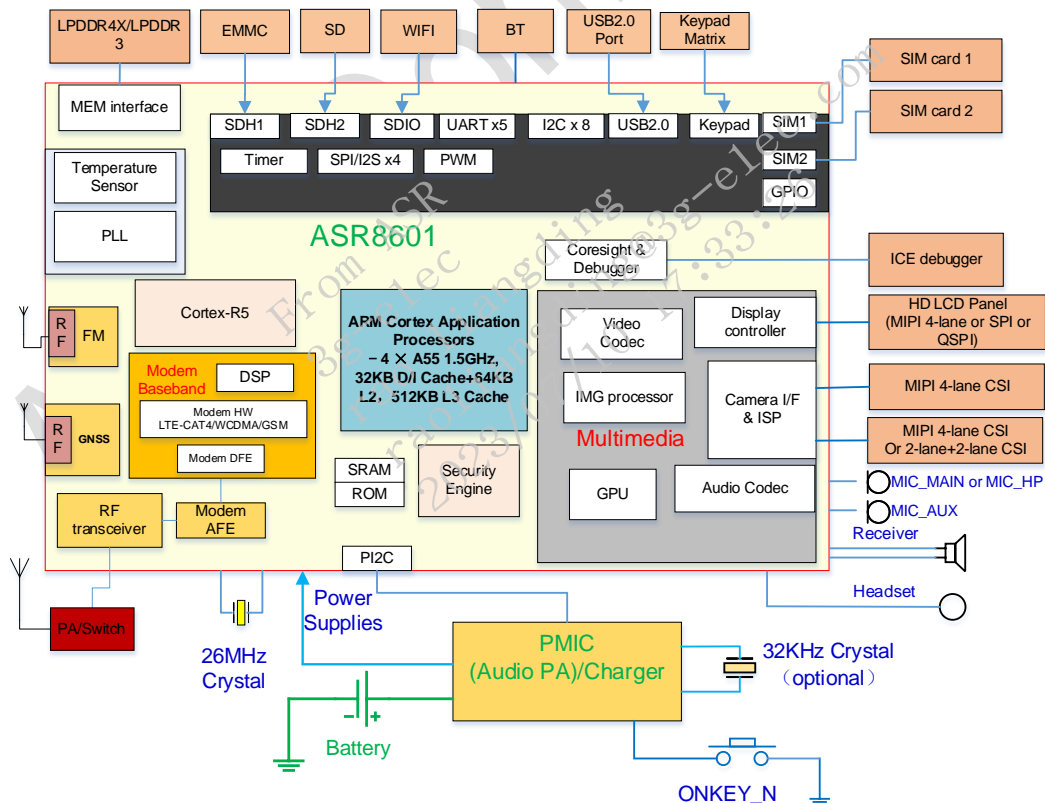


Figure 1 SoC Device Block Diagram

1 SoC device features

1.1 Platform features

- General
 - TSMC 22nm process
 - Operation temperature: -20~70°C
- Application Processor
 - ARM CortexA55×4 64-bit Quad-core processors
 - Quad-Core with 1.5 GHz clock
 - 32K I-Cache per core
 - 32K D-Cache per core
 - 64K L2-Cache per core
 - 512KB L3 Cache
 - TrustZone® Extension (protect storage/RAM for payment/DRM)
 - DVFS with adaptive operating voltage from 0.6V to 1.0V
- DDR Memory
 - Dual chip select 32-bit LPDDR4x SDRAM with 2400Mbps operation and a total of up to 6GB of RAM.
 - Dual chip select 32-bit LPDDR3 SDRAM with 1866Mbps operation and a total of up to 6GB of RAM.
- Sensor-Hub
 - 2x SHUB I2C
 - 2x SHUB SSP
 - 1x SHUB UART
- Peripheral Controller
 - GPIO (×128)
 - 128 pins
 - Pull-up/pull-down programmable
 - 1.8V IO
 - UART (×5)
 - AP/CP/BT/print
 - I2C (×9)
 - for camera, G-Sensor/ E-COMPASS/ Proximit-Sensor/ Light-Sensor/Gyro and Fingerprint/NFC,PMIC, touch etc.
 - SPI(×4)
 - To support both master and slave mode
 - For Bluetooth, codec etc.
 - Platform has 2 SPI and audio system has 2 SPI.
 - USB (×1)
 - USB 2.0
 - Support USB2.0 High speed, OTG
 - SDIO (×1 for WIFI)
 - compatible for 4-bit SDIO 3.0 UHS-I protocol, up to SDR104(208MHz)
 - SD (×1 for TF card)

- compatible for 4-bit SD3.0 UHS-I protocol, up to SDR104(208MHz)
- eMMC (×1)
 - compatible for 8bit eMMC5.1, up to HS400(200MHz)
- MIPI CSI(CSI-2 v1.1) 4 lane(×2)
 - 4 Lane + 4 Lane mode
 - 4 Lane + 2 Lane mode
 - 4 Lane + 2 Lane + 2 Lane mode(triple sensor)
- MIPI DSI(DSI v1.1) (×1)
 - 4 Lane DSI
- PWM (×4)
- Dual SIM/USIM card controller
- Security System
 - ARM TrustZone® Security
 - Secure Boot/Strap/Bonding
 - Secure EFUSE 2K bits
 - Cryptographic engine (TRNG/AES/RSA/ECC/SHA2/HMAC)
- GNSS
 - Support both TSX and TCXO
 - Support multi-GNSS
 - GPS L1
 - BDS B1
 - GLONASS L1
 - QZSS L1
- FM
 - CMOS single-chip fully-integrated FM tune
 - Support worldwide frequency band 65~108 MHz
 - Support flexible channel spacing mode 100KHz, 200KHz, 50KHz and 25KHz
 - Digital low-IF tuner
 - Image-reject down-converter
 - High performance A/D converter
 - Digital Auto Gain Control(AGC)
- Debug System
 - 2 JTAG for all CPU/MCU sub-system
 - UARTs
 - ETM/ETB
 - CPU/IO register dump after watchdog reboot
- Boot System
 - Initial AP boot from UART/USB/eMMC
 - 64KB boot-ROM size
- Aided System
 - Watchdog design for each CPU/MCU system

1.2 Multimedia features

- GPU
 - IMG BXE-2-32 @819MHz, 32KB SLC
 - Support OpenGL ES 3.2
- VPU (video processing unit)
 - ARM Mali-V5 @819MHz clock
 - H.265/H.264/VP8/VP9/MPEG4/MPEG2 decoder 1080p@30fps
 - H.265/H.264/VP8/VP9 encoder 1080p@30fps
- Display
 - 1 MIPI DSI-4lane or SPI interface
 - Support up to HD+(1600x720@60fps)
 - Embedded LCD gamma correction
 - Color/contrast enhancement
 - support up to 4-full-size-layer composer and maximum 8 layer composer by up-down layer reuse in rdma channel
 - support cmdlist mechanism, which can configure register parameters by HW
 - support concurrent write back, with both raw and afbc format, also support dither/crop/rotation in write back path
 - support advanced mmu (virtual address) mechanism, with nearly no page missing in 90/270 degree rotation
 - support color key and solid color
 - support both advanced error diffusion and pattern based dither for panel
 - support both afbc/raw format image source
 - Color saturation/contrast enhancement
 - Support both video mode and cmd mode for panel
 - Support ddr frequency dynamic changing with embedded dfc buffer
- Camera
 - Dual-ISP
 - 16M(max.) 30fps Dual ISP
 - One 4 Lane CSI + one 4 Lane CSI or 4 Lane + 2 lane + 2 lane
 - RAW sensor, output YUV data to DRAM
 - Hardware JPEG encoder(hardware, up to 23M is supported)
 - support YUV/EXIF/JFIF format
 - AF/AE/AWB
 - Face detection
 - digital zoom, panorama view
 - PDAF
 - PIP(picture in picture)
 - support HDR
 - continuous video AF

- Video stabilization
 - HW 3D denoise
- Audio
 - Integrated High quality audio codec and audio front-end
 - ADC: 90dB SNR@20~20kHz
 - DAC: 95dB SNR@20~20kHz
 - Class-G: 95dB SNR@20~20kHz, 31mW@32-ohm, THD - 90dB
 - ClassAB: 95dB SNR@20~20kHz, 75mW@32-ohm, THD- 90dB
 - Line-out to support external Class-D audio amplifier (Class-D in PMIC: 95dB SNR@20~20kHz, 800mW@4.2Vbat, 8-ohm speaker)
 - Two MICs input
 - Stereo inputs path for noise cancellation
 - Stereo headphone output
 - Audio content sampling rates: 8kHz to 48kHz
 - Microphone bias for headphone plug-in and hook-key detection
 - Quad vocoders for adaptive multi-rate (AMR)
 - Noise suppression and echo cancellation
 - Digital side tone generator with programmable gain
 - Voice power amplifier with programmable gain

1.3 Modem features

- Modem
 - FDD/TDD LTE
 - 3GPP Cat-4: DL 150Mbps, UL 50Mbps
 - VoLTE, ViLTE
 - WCDMA release 7
 - Class 12 EDGE
 - ASR supported 4G/3G/2G protocol stack compliant with world's leading carriers
 - Fully-integrated platform solution validated via extensive IOT, GCF, and field trial testing
 - FR/EFR/HR/AMR (Both AFS/AHS)
 - A5/1, A5/2, A5/3, f8/f9, GEA2 and GEA3 encryption
 - SNOW3 G/ZUC cipher offload engine
 - Dual-SIM with dual standby
 - Echo cancellation and noise suppression
- Communication Processors
 - ARM Cortex R5 with packet processing accelerators up to 832MHz
 - Micro-Signal Architecture VLIW DSP core
- RF Solution
 - LTE FDD/TDD support
 - Multi-band 3G support
 - Quad-band EDGE support
 - Support all bands from 450MHz~2.7GHz
 - 10 single end Rx Primary ports
 - 10 single end Rx Diversity ports
 - 6 Tx ports
- Multi-radio Platform Capabilities
 - Enables support for IMS, VoIP and other advanced carrier services

Revision History

Table 1 **Revision History**

Revision	Date	Description
V1.0	Nov.29, 2022	ASR8601 Brief Initial Release
V1.1	June 26, 2023	Update some parameter info.

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