ASR8601 BB Design Guide V1P0 20221201

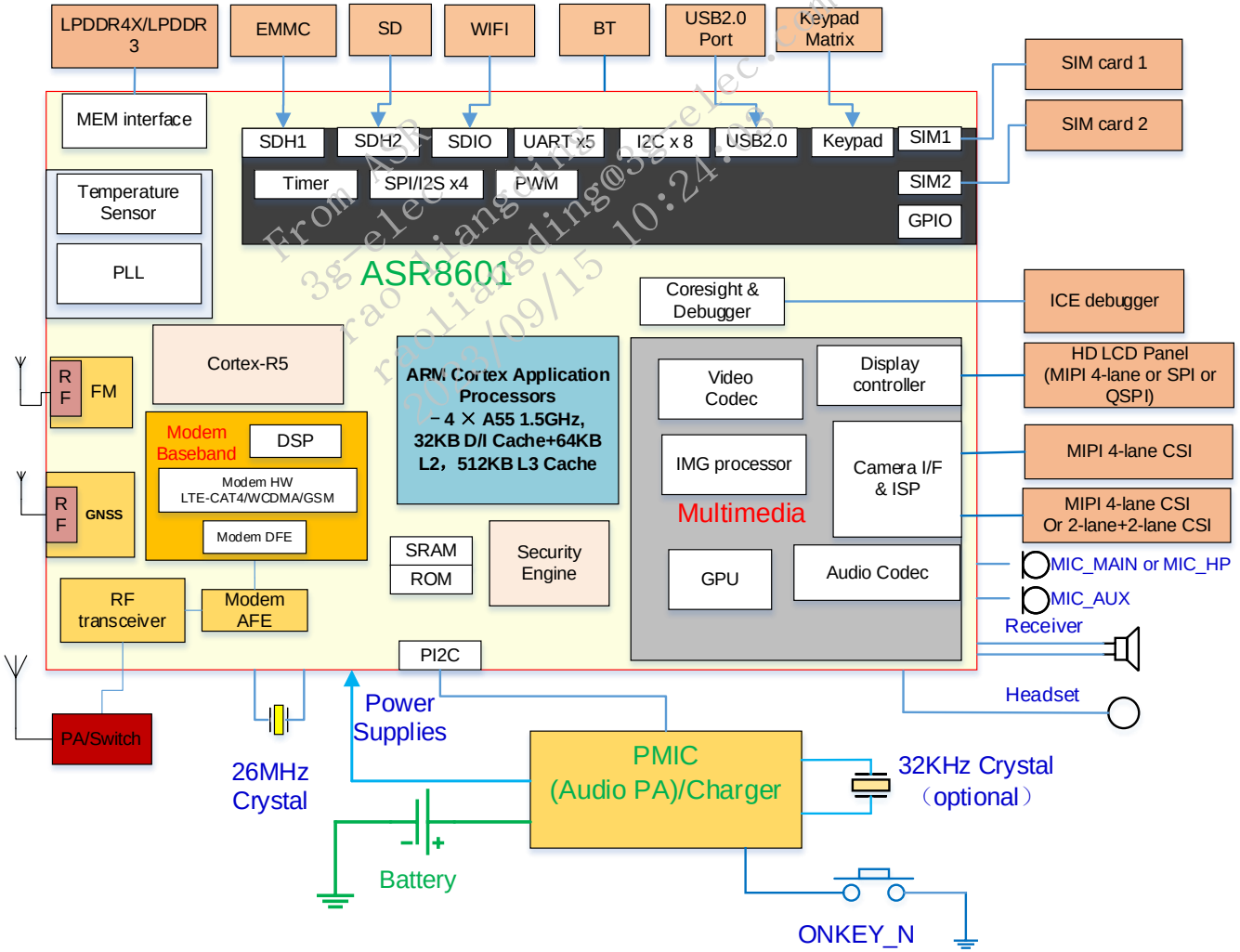
ASR-AE-Team

2022/12/01

BB Design Guide Version

VERSION	OWNER	DATE	NOTE	REMARKS
V1P0	AE/BB	20221201	First edition	

Platform Block Diagram



Overview of Contents

NO.	FEATURES	REMARKS
1	SYSTEM CLOCK	
2	SYSTEM CONTROL	
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4	EMMC/LPDDR	
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1.SYSTEM CLOCK 1/3

System Clock Scheme With GNSS：

- **DCS Mode: 26MHz TCXO+32.768KHz Crystal.**
- **DCS Mode: 26MHz TSX+32.768KHz Crystal.**
- **SCS Mode: 26MHz TSX. 26MHz Generate 32.786KHz.**

System Clock Scheme Without GNSS：

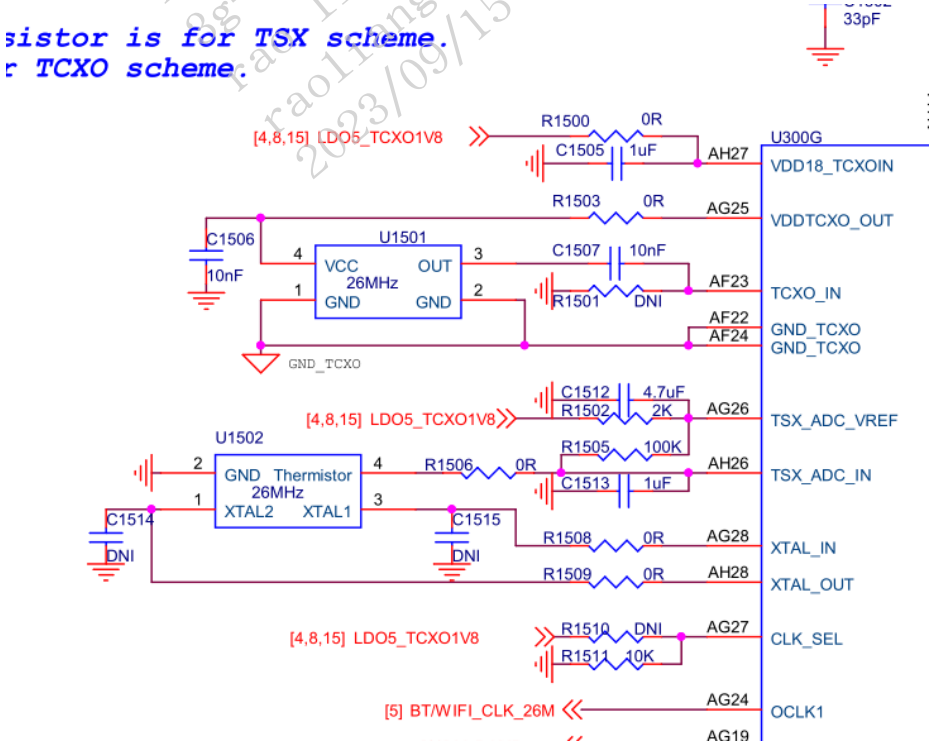
- **DCS Mode: 26MHz DCXO+32.768KHz Crystal.**
- **SCS Mode: 26MHz DCXO. 26MHz Generate 32.786KHz。**

- **The clock scheme is selected according to the specific product definition, mainly based on power consumption and function.**
- **Select the same TSX/DCXO crystal. The average power consumption of SCS mode is about 100uA higher than that of DCS mode.**
- **In particular, if TCXO crystal oscillator is selected, 32K crystal must be added.**

1.SYSTEM CLOCK 2/3

Sketch map of 26MHz clock scheme

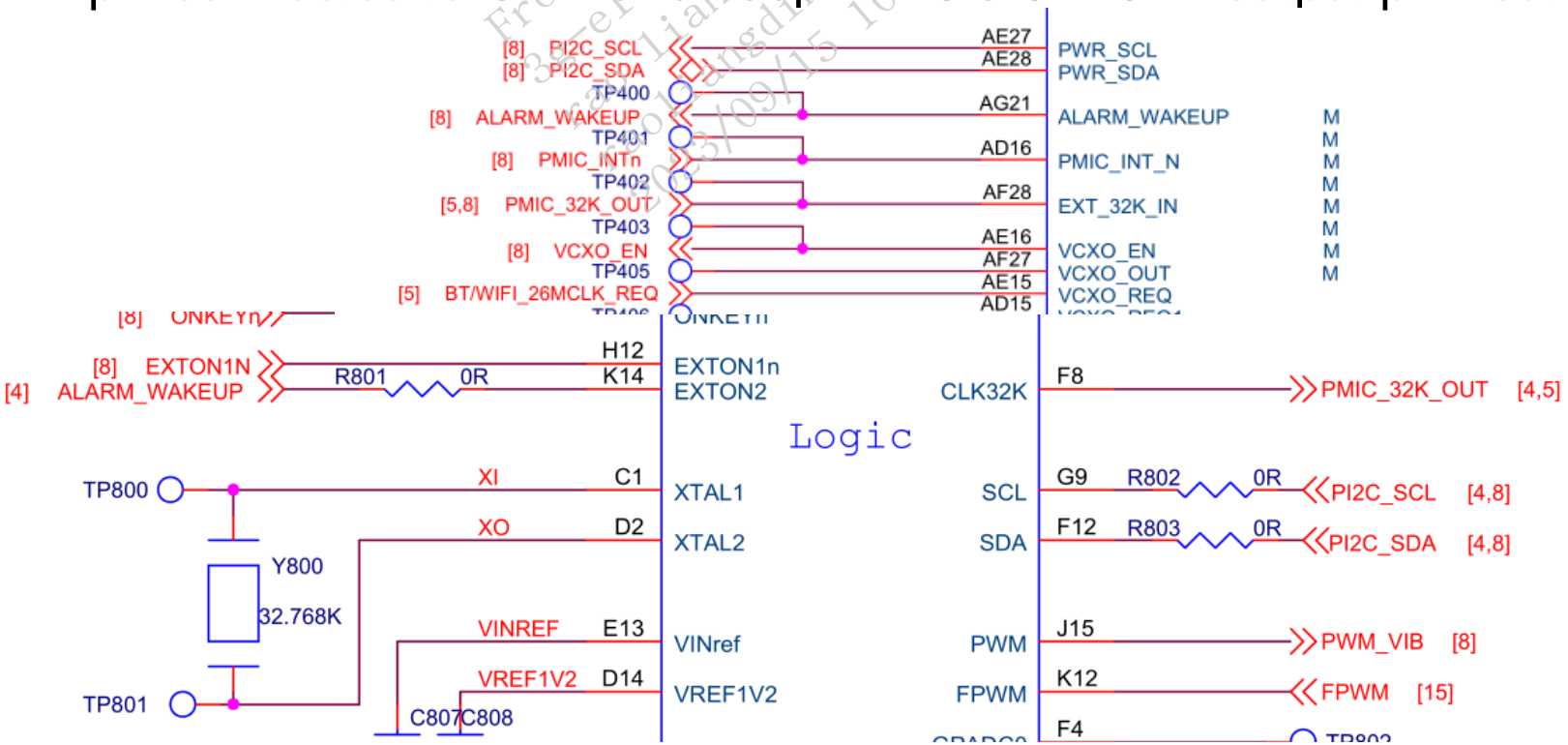
- TSXADC is a 16 bit ADC with sufficient precision.
- The peripheral device design of TSXADC sampling circuit is subject to the reference design of release schematic diagram.



1.SYSTEM CLOCK 3/3

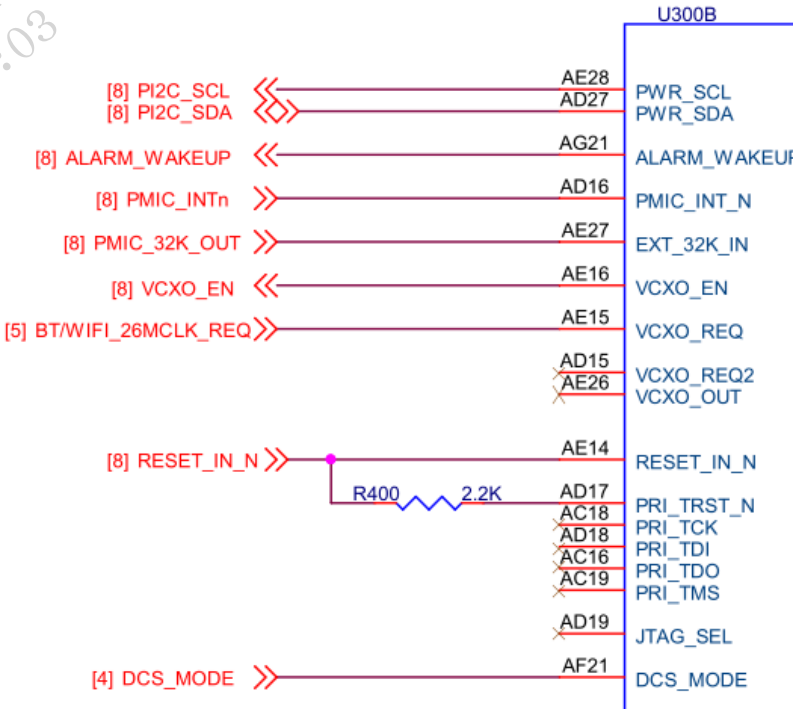
Sketch map of 32KHz clock scheme

- 32K crystal is added according to product definition.
- If SCS mode is selected for the product, please keep SOC's EXT+32K_IN pin connected to GND and keep PMIC's CLK32K output pin floating.



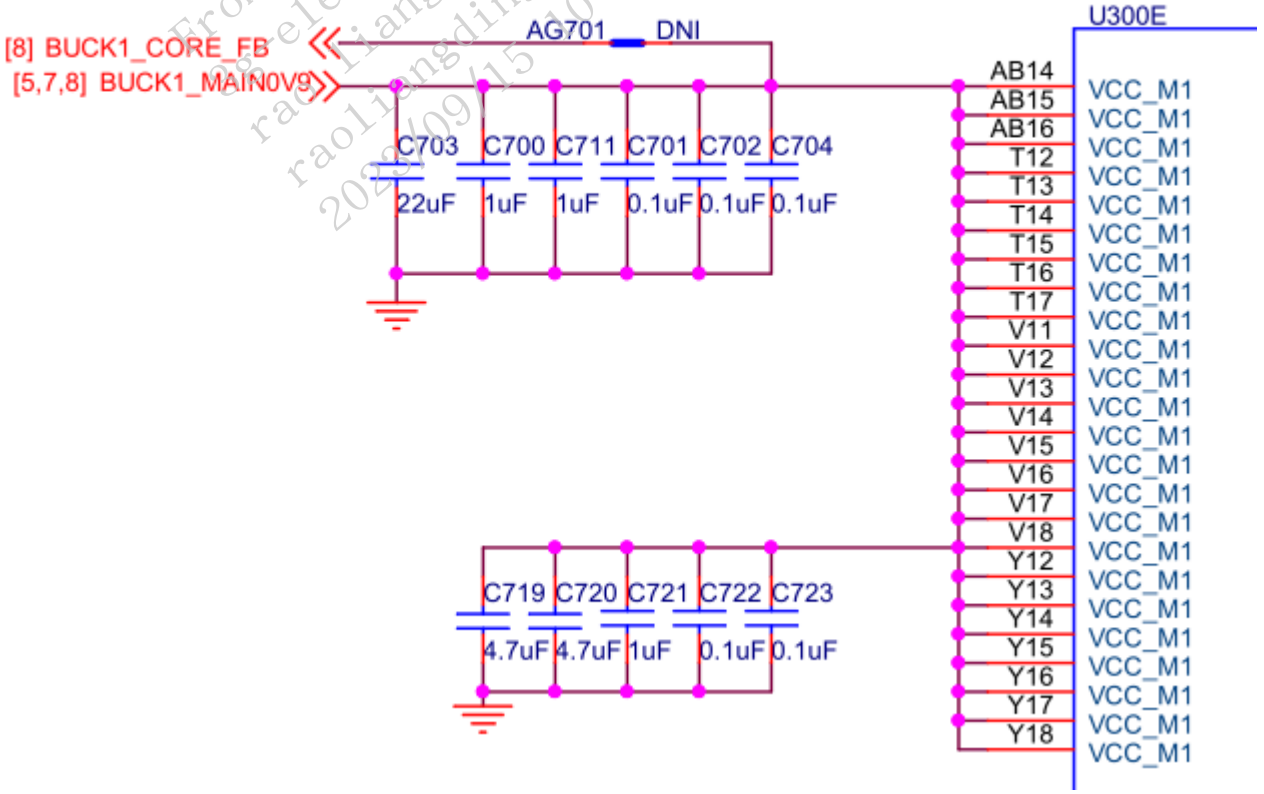
2. SYSTEM CONTROL

- PWR_I2C is used to communicate with PMIC.
- ALARM is used for RTC wake-up PMIC in SCS's power off mode.
- PMIC_INTn is an interrupt request sent by PMIC to the SOC.
- EXT_32K_IN is the 32KHz clock input provided by PMIC to SOC in DCS mode.
- VCXO_EN: The SOC informs the PMIC to sleep.
- VCXO_REQ: OCLK output request signal. Used for BT/WIFI.
- VCXO_REQ2: VCXO_OUT output request signal. Used for digital 26MHz scene.
- RESET_IN_N: SOC reset signal.
- DCS_MODE: For the solution with 32K crystal, This pin is pulled up by 510KΩ to system clock power, otherwise it is directly pulled down to GND.



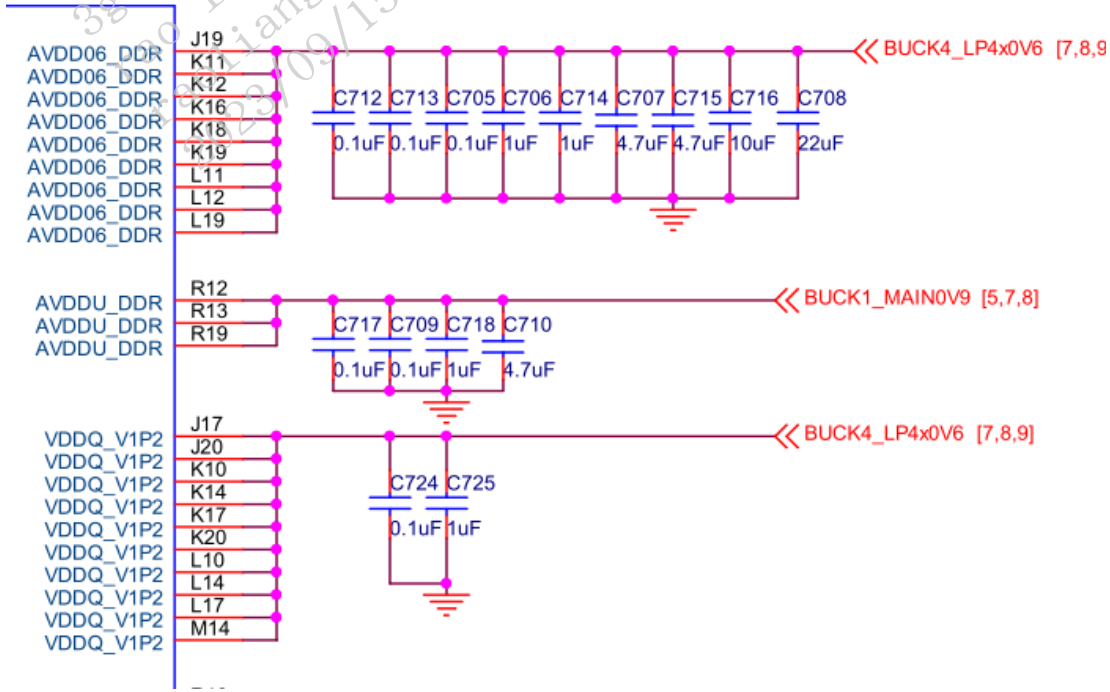
3. POWER DOMAIN 1/8

- VCC_ M1s are the core power supply of the SOC.
- BUCK1 is designed for remote feedback.
- The power supply design of BUCK1 shall meet the requirements of PDN.



3. POWER DOMAIN 2/8

- Power supplies of LPDDR4x's PHY on SOC side.
- These power supply design shall meet the requirements of PDN.
- Avoid the high current or high voltage power supply in the system when routing.



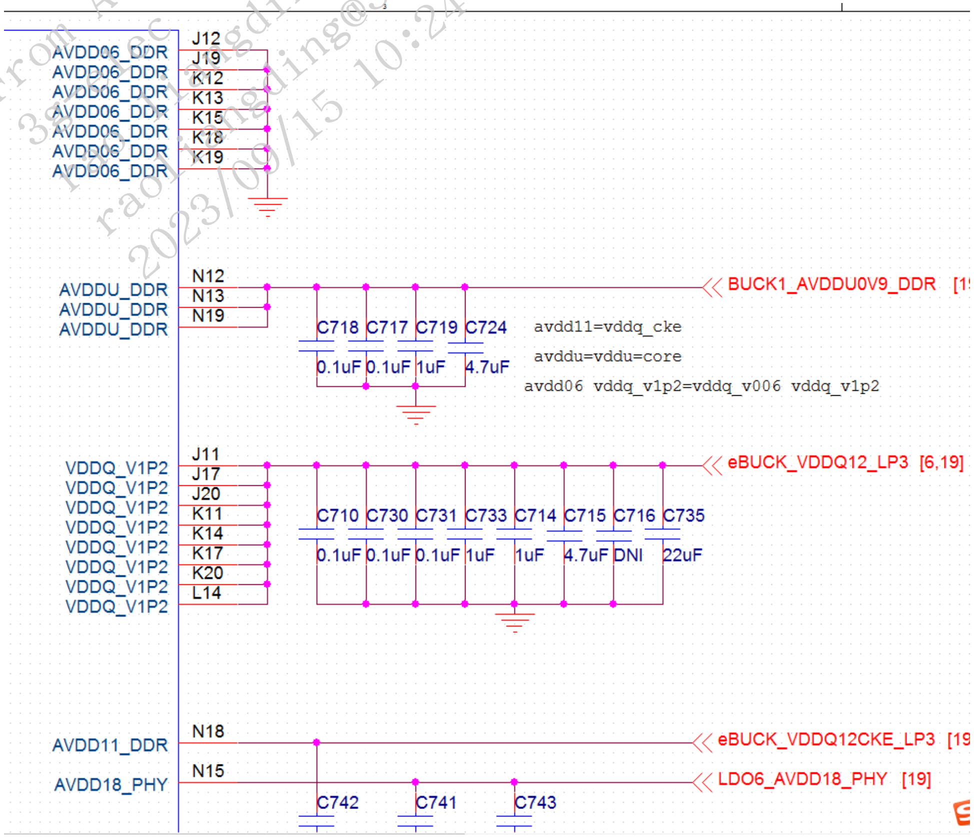
3. POWER DOMAIN 3/8

When matching with LPDDR4x,

- AVDD06_ DDR is the SOC's VDDQ_PHY_V0P6 (0.6V) power supply, which is the key power supply network.
- AVDD11_ DDR is the SOC's VDDQ_PHY_CKE(1.1V) power supply.
- AVDD18_ PHY is powered by AVDD1V8(1.8V).
- AVDDU_ DDR is the power supply of the PHY's digital logic core, witch should be connected to BUCK1.
- VDDQ_ V1P2 should be connected to AVDD06_ DDR with two small capacitors in parallel.

3. POWER DOMAIN 4/8

- Power supplies of LPDDR3's PHY on SOC side.
- These power supply design shall meet the requirements of PDN.
- Avoid the high current or high voltage power supply in the system when routing.



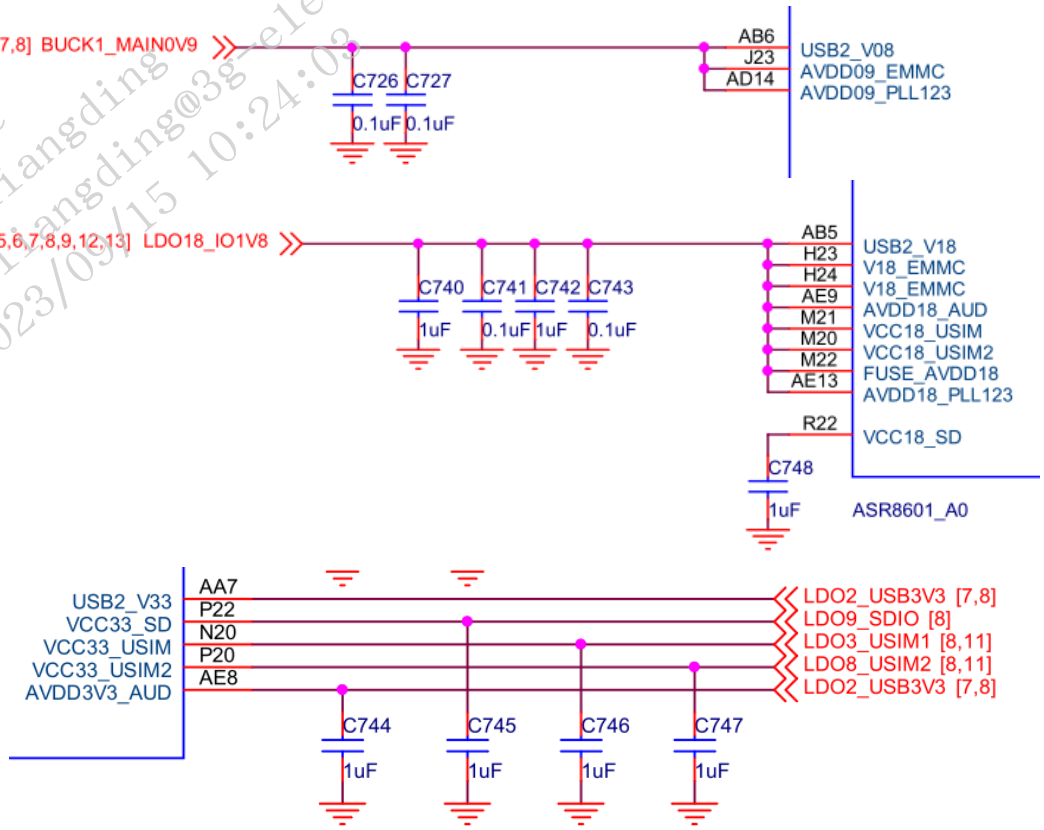
3. POWER DOMAIN 5/8

When matching with LPDDR3,

- AVDD06_ DDR should be connected to GND.
- AVDD11_ DDR is the SOC's VDDQ_PHY_CKE(1.2V) power supply.
- AVDD18_ PHY is powered by AVDD1V8(1.8V).
- AVDDU_ DDR is the power supply of the PHY's digital logic , witch should be connected to BUCK1.
- VDDQ_ V1P2 is the SOC's VDDQ_PHY_V1P2(1.2V) power supply, which is the key power supply network.

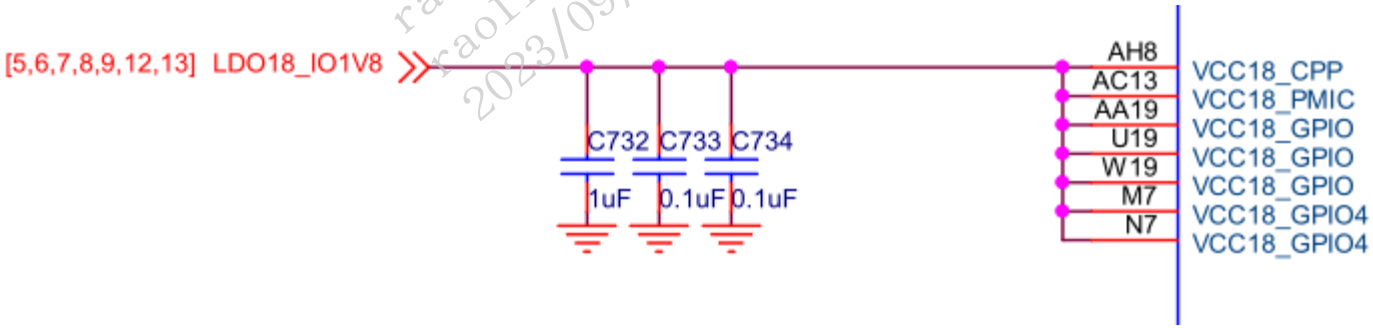
3. POWER DOMAIN 6/8

- Power supplies for eMMC, USB, SIMs, SD, PLL, Audio and fuse on the SOC.
- Please note that the position of the swing part of the decoupling capacitor should be as close to the corresponding pin as possible.



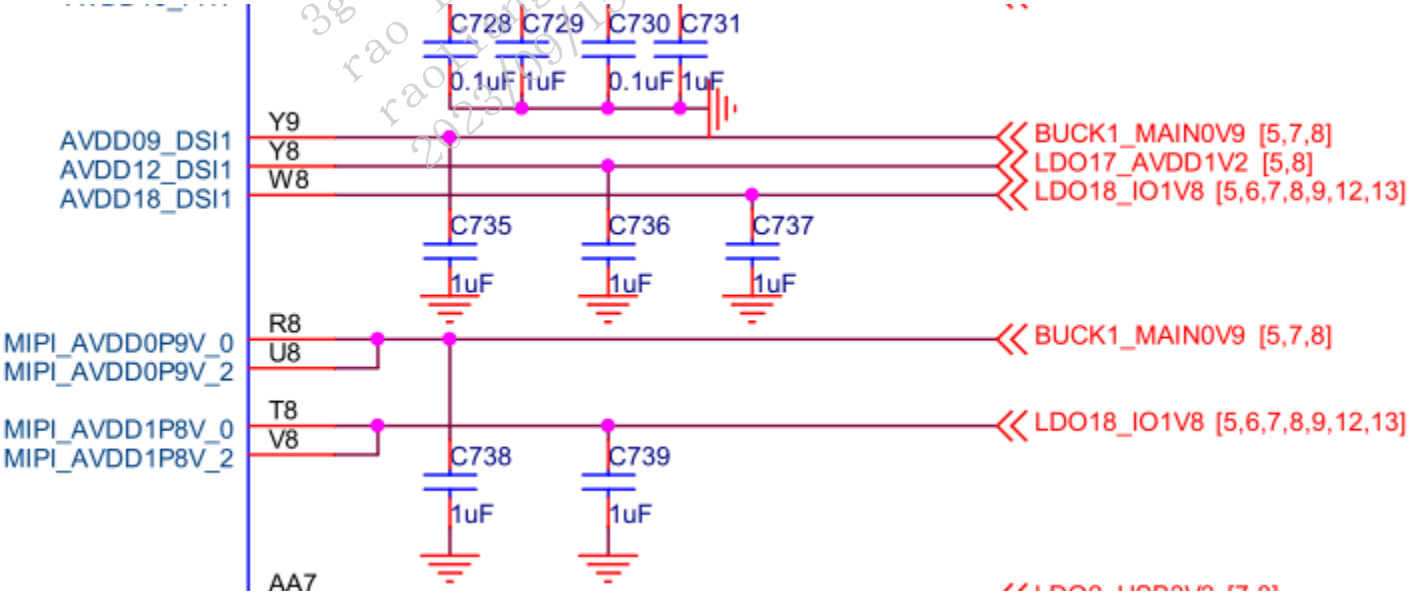
3. POWER DOMAIN 7/8

- Power supplies of GPIOs on SOC side.
- Please refer to the design schematic diagram for actual design.



3. POWER DOMAIN 8/8

- Power supplies of DSI&CSI MIPI on SOC side.
- Please pay attention to wiring protection for these power supplies. Avoid high current or high voltage power supply in the system.



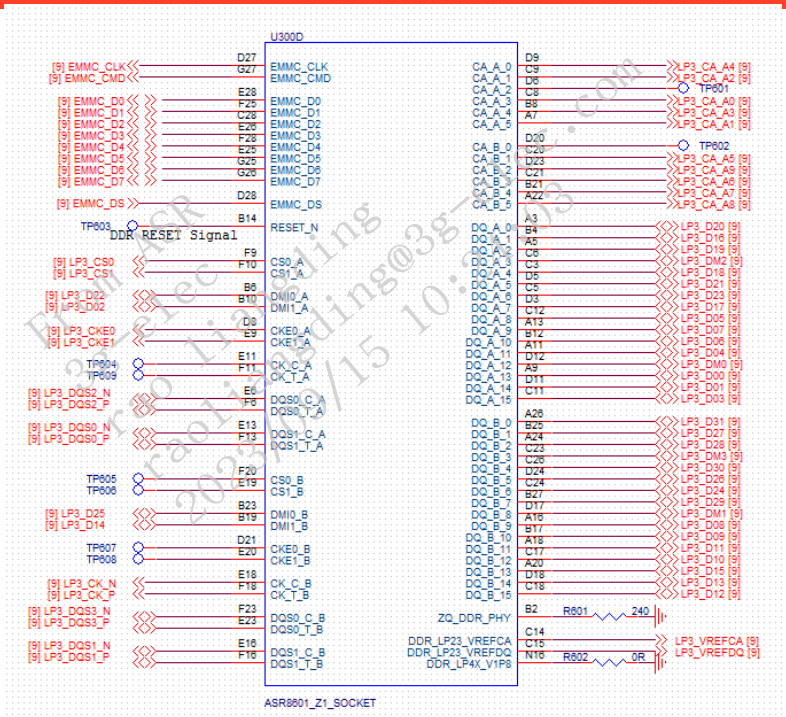
4. EMMC/LPDDR 1/4

- The PCB routing shall comply with the SI routing rules.

When matching with LPDDR4x,

- ZQ_DDR_PHY is PHY's R-calibration resistor PAD. Connect it to GND through a 240Ω1% resistor .
- DDR_LP4x_V1P8 should be connect to AVDD18 through a 10K resistor.
- DDR_LP23_ VREFCA/DQ should be kept disconnection.

4. EMMC/LPDDR 2/4

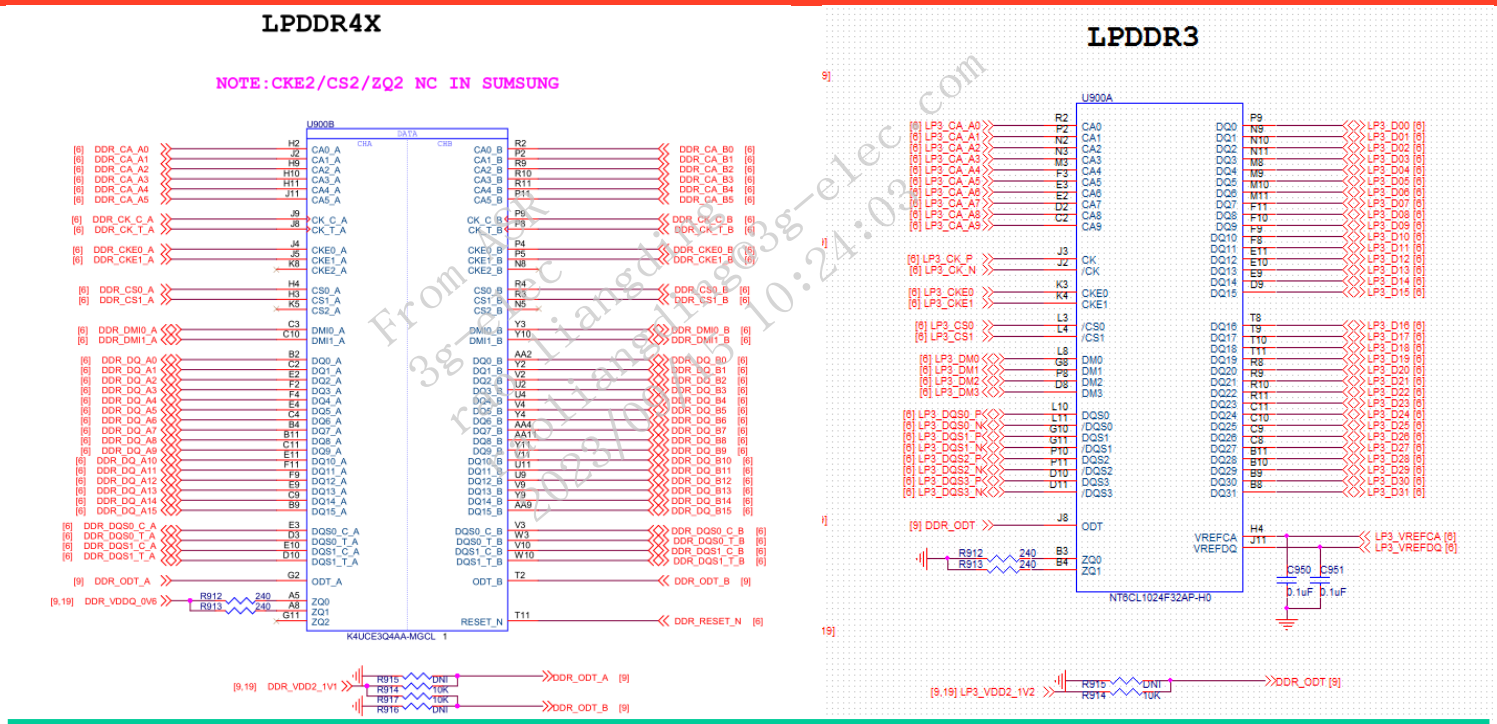


- The PCB routing shall comply with the SI routing rules.

When matching with LPDDR3,

- ZQ_DDR_PHY is PHY's R-calibration resistor PAD. Connect it to GND through a 240Ω1% resistor .
- DDR_LP4x_V1P8 should be connect to GND.
- DDR_LP23_ VREFCA/DQ should be connected to LPDDR3.

4. EMMC/LPDDR 3/4

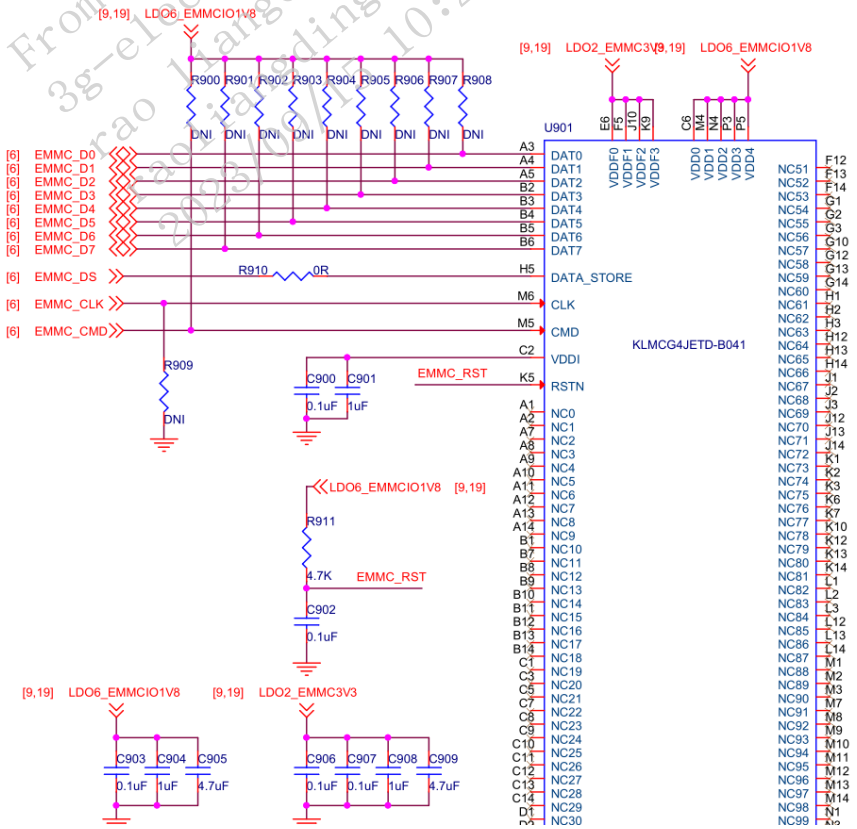


Device ZQ&ODT connection index

LP	ZQ PAD	ODT PAD	
	connection	connection	description
LPDDR3	RZQ to VSS	tie to VDD2	enable ODT
LPDDR4x	RZQ to VDDQ	tie to VDD2 or VSS	ignored ODT

4. EMMC/LPDDR 4/4

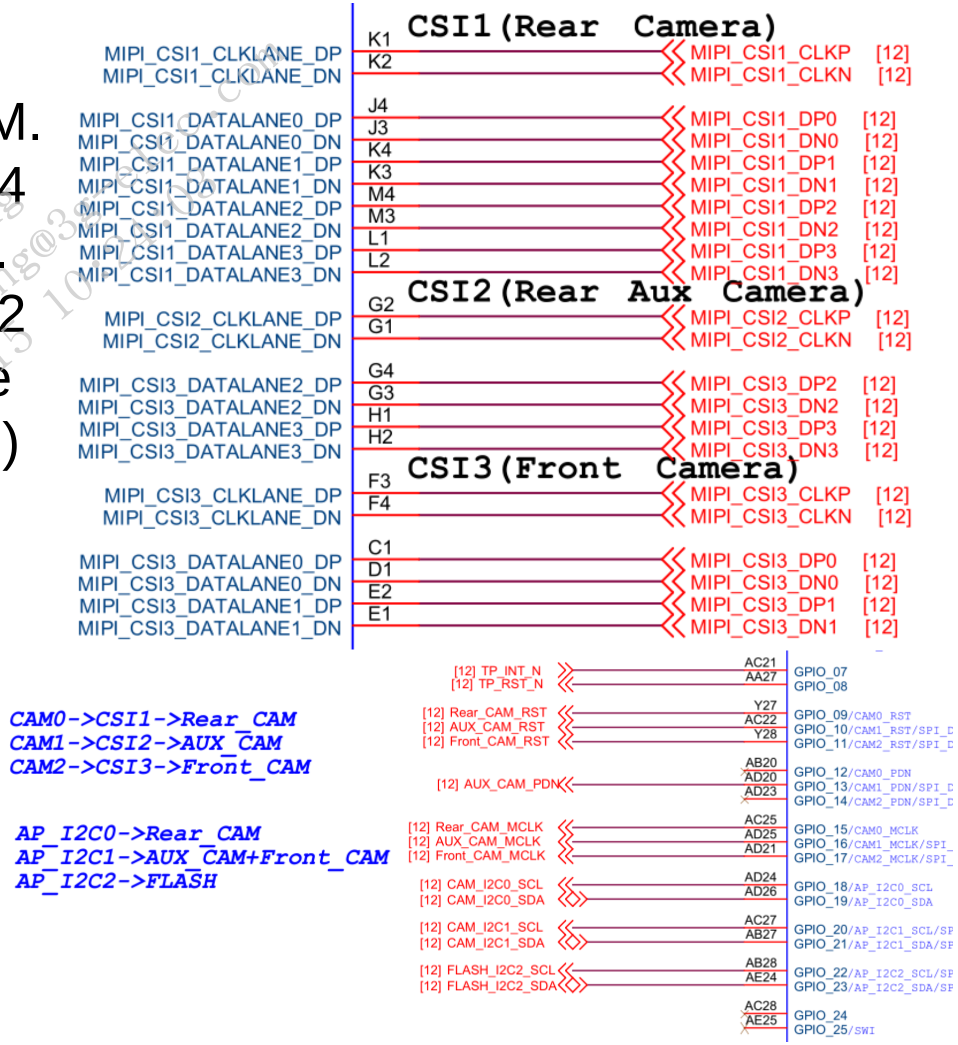
- sketch map of eMMC. The actual design is subject to the schematic reference design.
- The PCB routing shall comply with the SI routing rules.



5. CAMs

- 16M(max.) 30fps Dual ISP. RAW sensor, output YUV data to DRAM.
- Support One 4 Lane CSI1 + one 4 Lane CSI3 cameras combination.
- Support One 4 Lane CSI1 + one 2 Lane CSI3(Lane0,1)+ one 2 Lane CSI2_CLK&CSI3_DATA(Lane2,3) cameras combination.
- Add common mode filters according to the actual product needs.

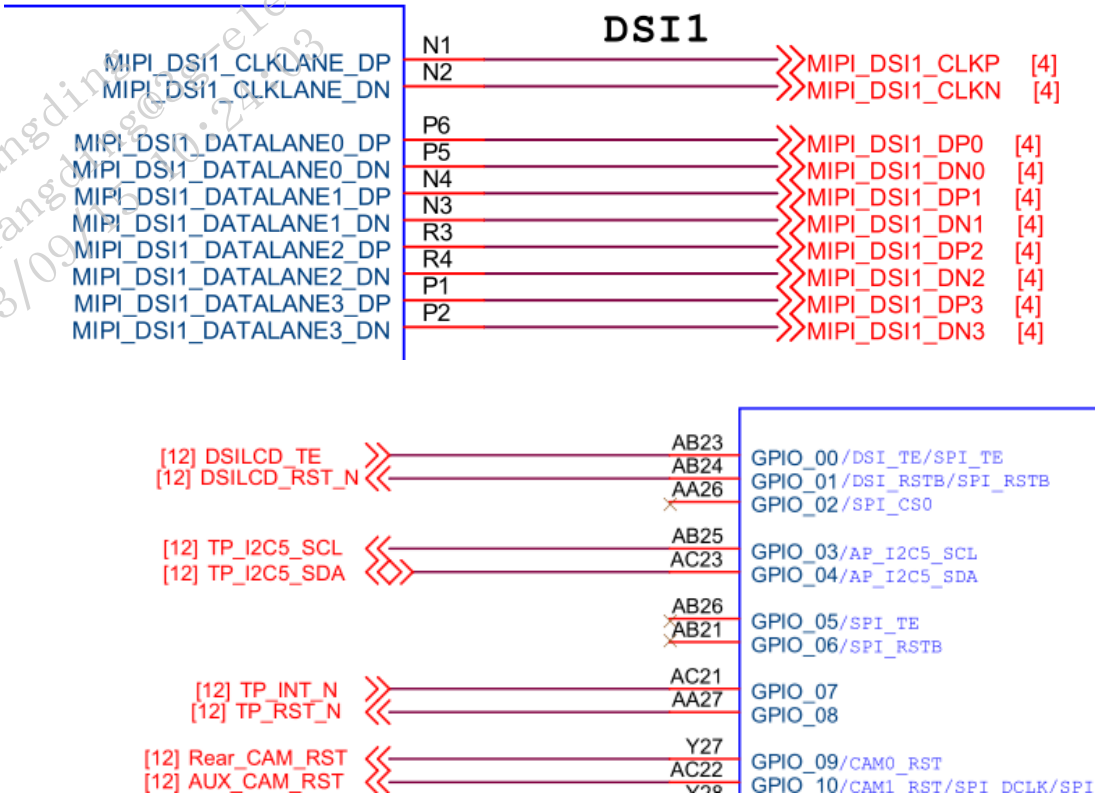
    - Cameras clock and control signals part.
    - CSI routing shall meet MIPI routing rules.



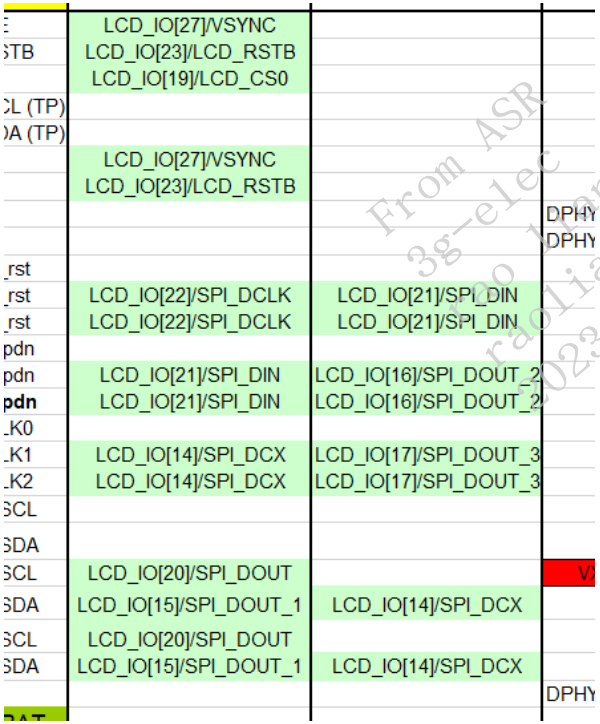
6. LCD/OLED 1/2

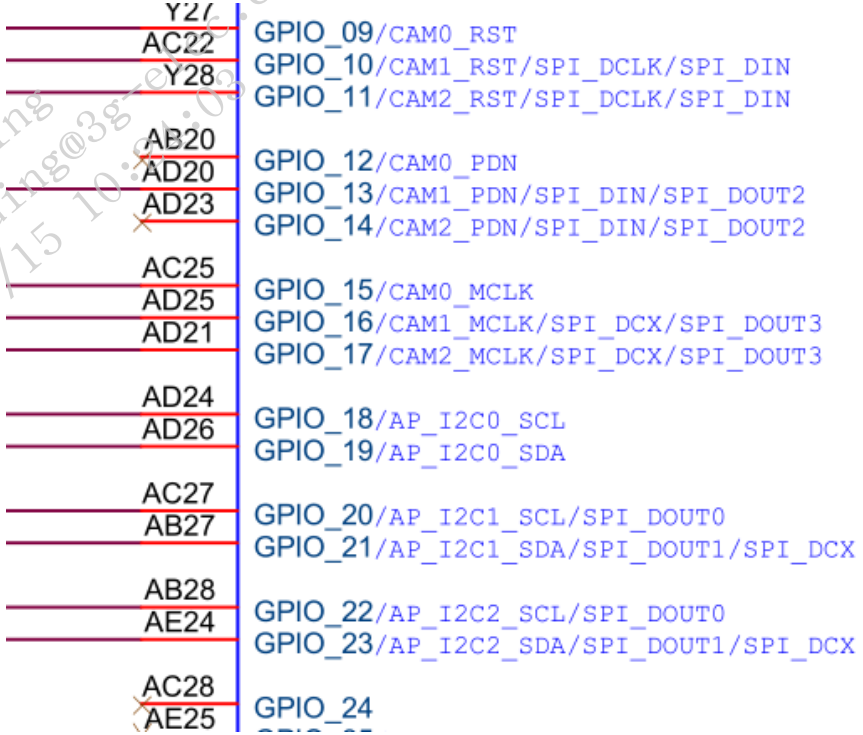
- 1 MIPI DSI-4lane support up to HD+(1600x720@60fps).
- DSI routing shall meet MIPI routing rules.
- Add common mode filters according to the actual product needs.

  - TP and LCD control signals part.



6. LCD/OLED 2/2

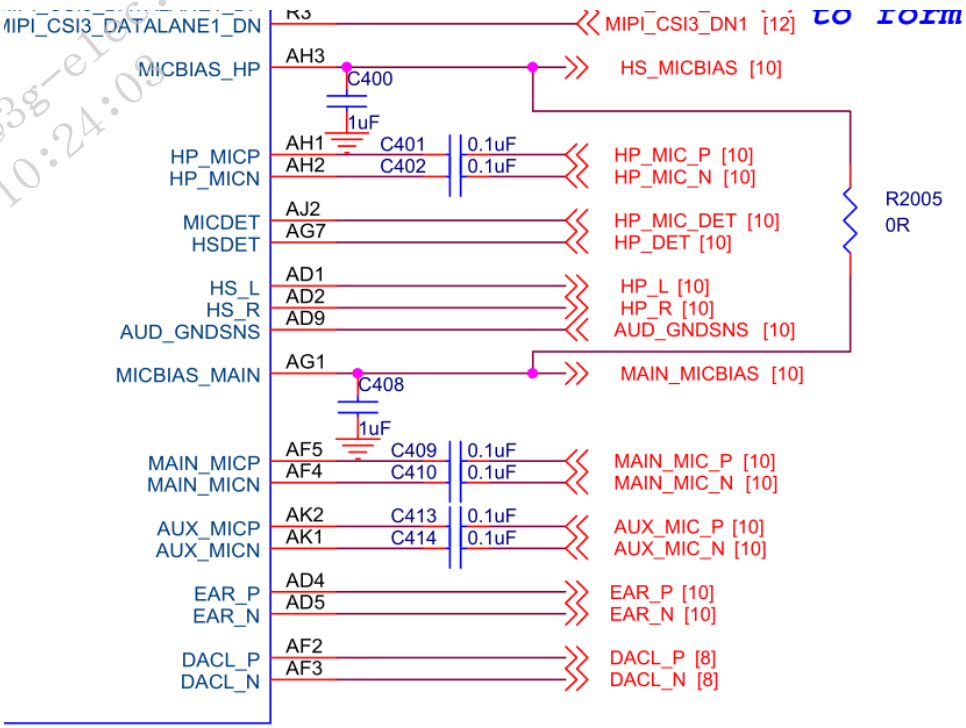




- 1 SPI-1/2lane support up to 320x240@30fps.
- 1 QSPI-4lane support up to 640x480@30fps

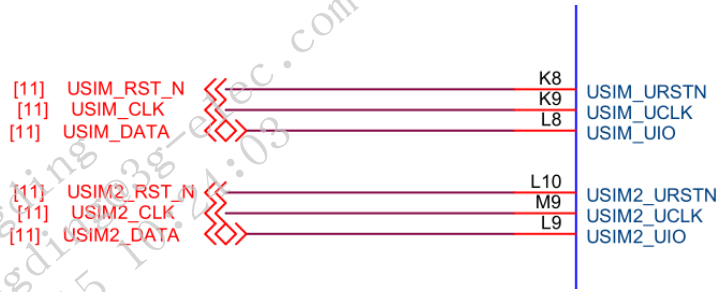
7. AUDIO

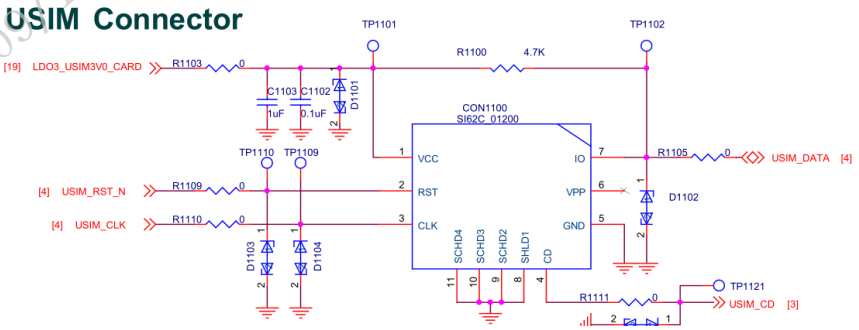
- MICBIAS_ MAIN is used for both main and auxiliary boards.
- MICBIAS_ HP is for headphones
- AUD_VPOS/VNEG: the power supply for headphone.
- HS_L/R: Class-G: 95dB SNR@20~20kHz,31mW@32Ω,THD -90dB.
- EAR_P/N： ClassAB,95dB SNR@20 ~20kHz,75mW@32Ω,THD-90dB.
- DACL_P/N: support external Class-D audio amplifier （Class-D in PMIC: 95dB SNR@20~20kHz, 800mW@4.2Vbat,8Ω speaker.

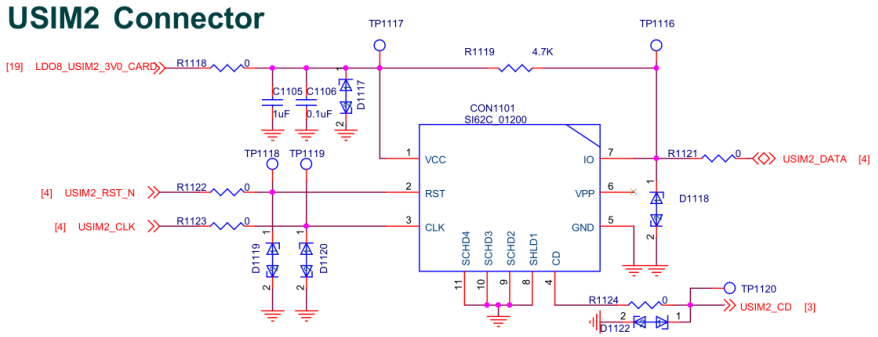


8. PERIPHERAL INTERFACE 1/4

- Dual SIM/USIM card.
- Support dual card dual standby.
- Please reserve static protective devices.
- Please avoid interference sources when routing.

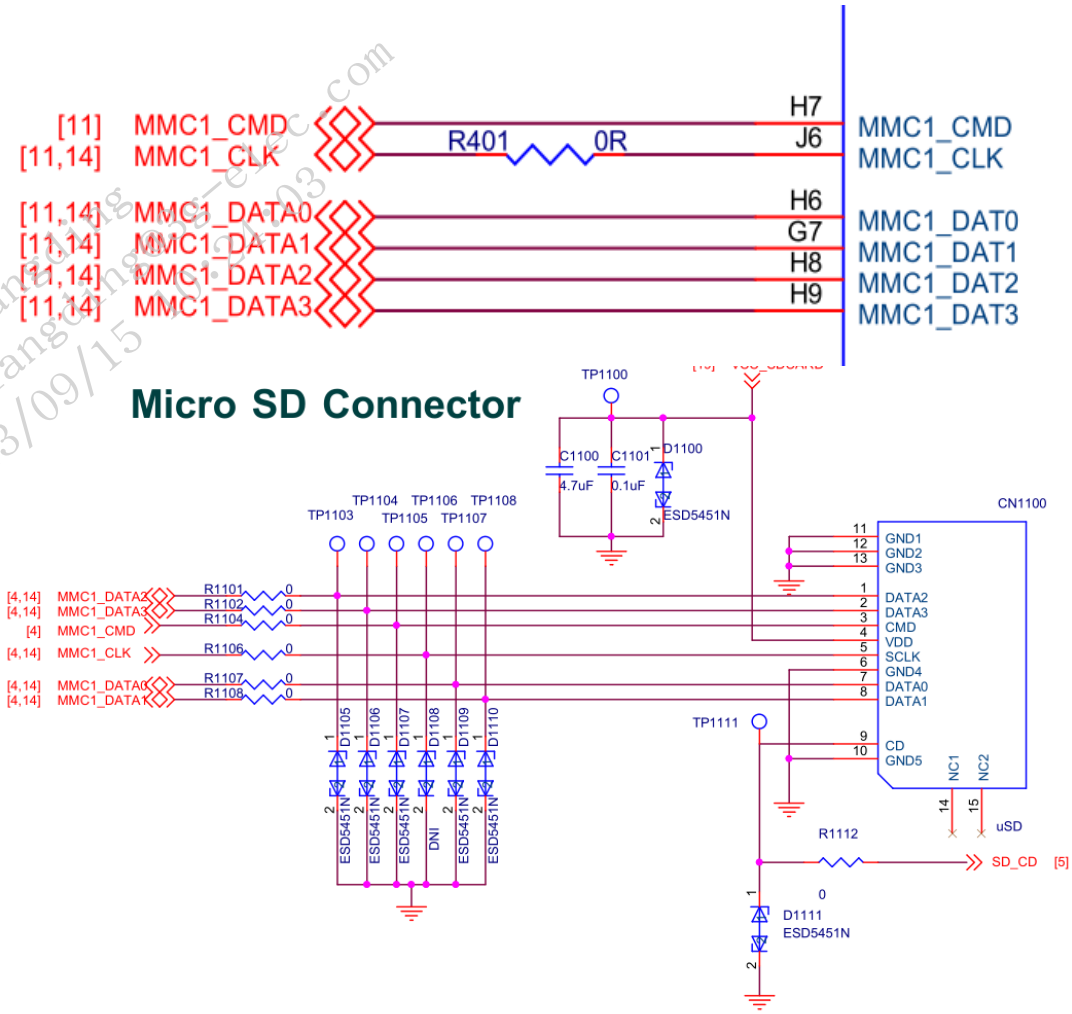






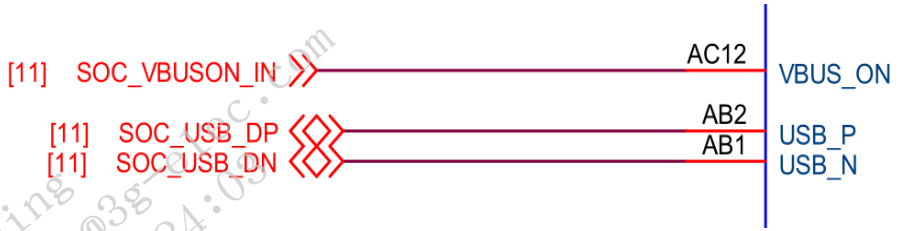
8. PERIPHERAL INTERFACE 2/4

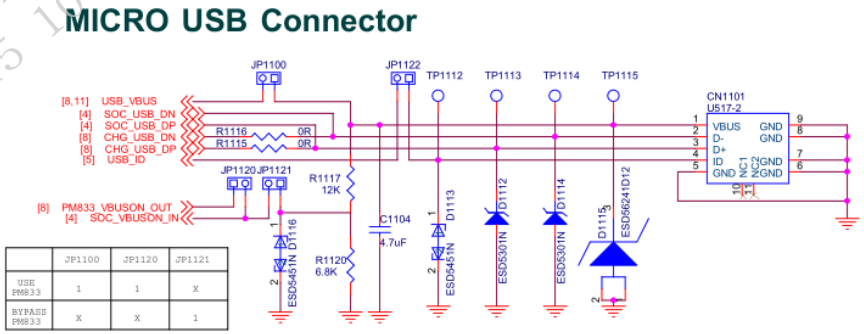
- SD card.Support 4-bit SD3.0 UHS-I protocol, up to SDR104(208MHz)
- Please reserve static protective devices.
- Please avoid interference sources when routing.

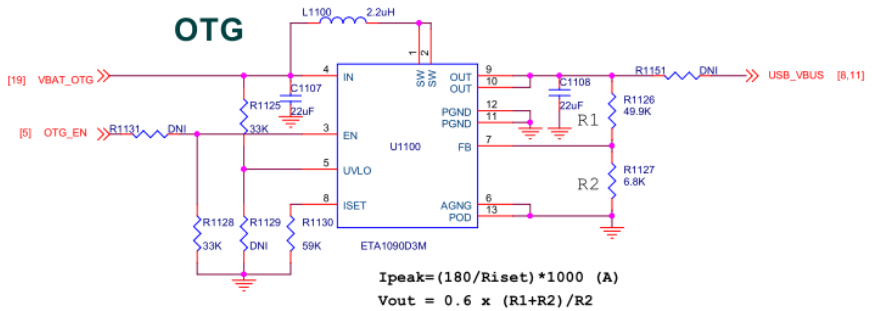


8. PERIPHERAL INTERFACE 3/4

- Support USB2.0 High speed，OTG
- Please avoid interference sources when routing.
- Please ensure differential line impedance control and protection.



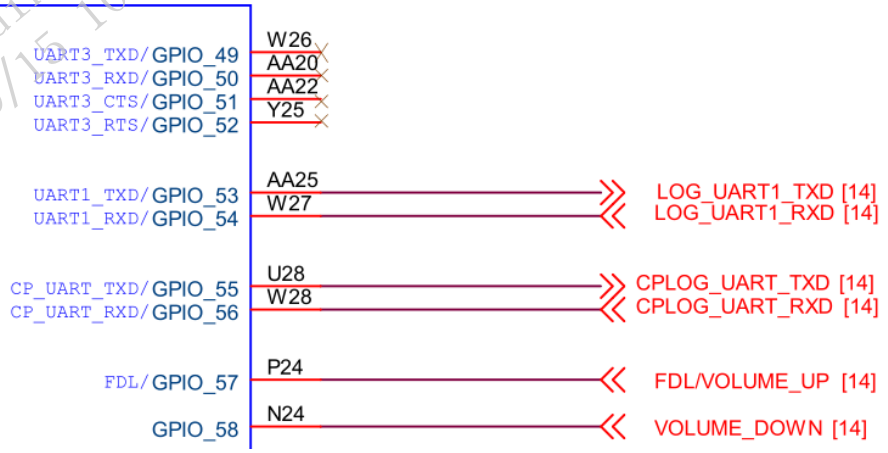




8. PERIPHERAL INTERFACE 4/4

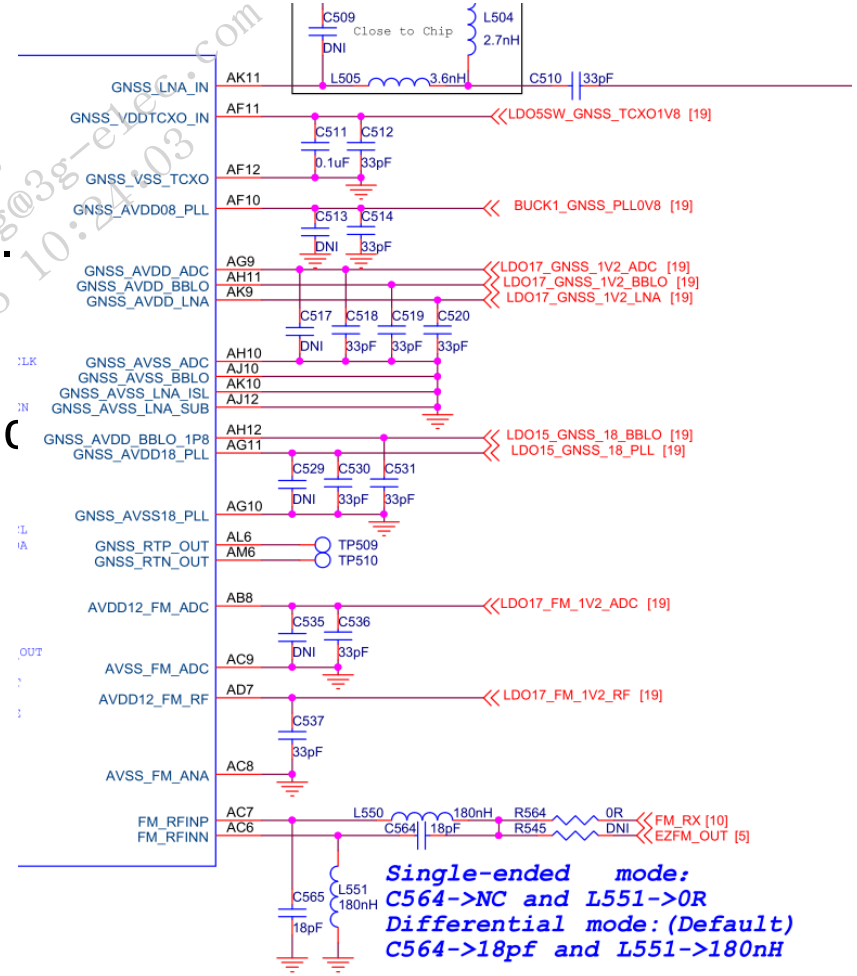
- AP log port. Frequently used debug LOG output port.
- FDL&Volume signal
- Please reserve static protective devices.

- CP log port. The debug LOG output port of the MODEM part.
- It is not frequently used, but it is recommended to reserve measuring points. Especially the first project.



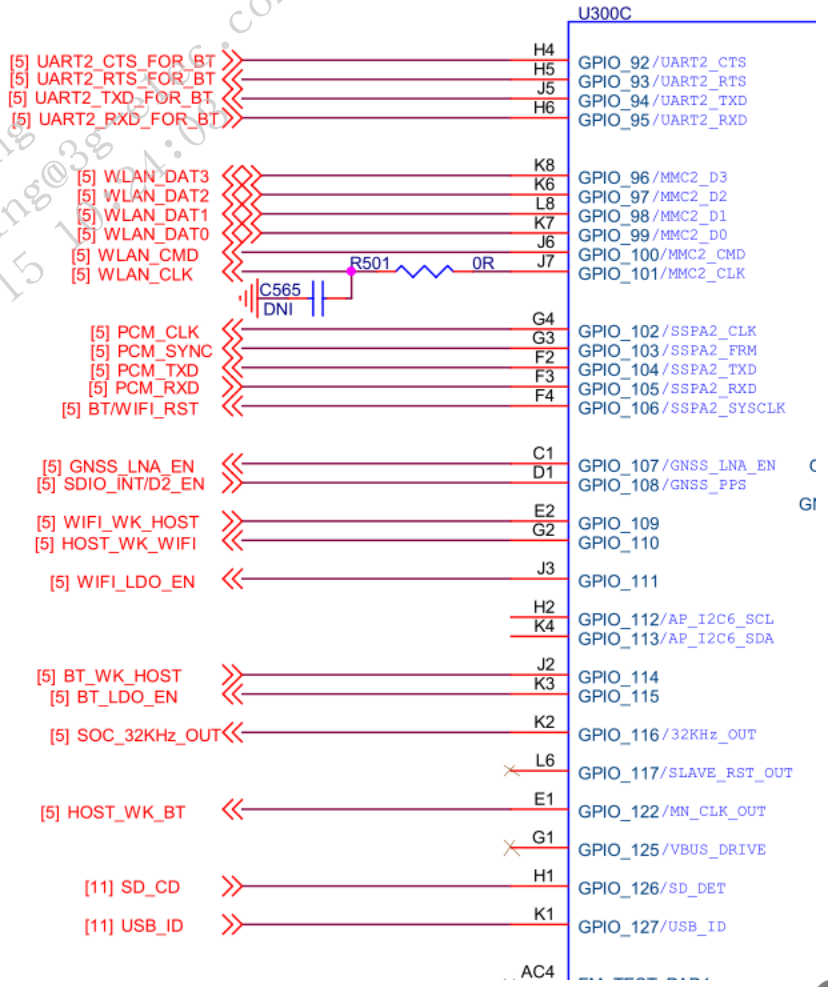
9. WCN 1/2

- GNSS and FM are built in SOC.
- GNSS: support GPS L1,BDS B1,GLONASS L1,QZSS L1.
- FM: Support worldwide frequenc band 65~108 MHz. Support flexible channel spacing mode 100KHz, 200KHz, 50KHz and 25KHz.



9. WCN 2/2

- This functional design is realized by carrying ASR5803F.
- BT and Wifi interfaces (UART/SDIO/PCM/WAKE/INT/RST) are shown in the right figure.
- Support 802.11a/b/g/n Wi-Fi.
- Support Bluetooth 5.0.



谢谢

欢迎您选择ASR8601