ASRPM813S

Power Management IC

Datasheet

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PRODUCT OVERVIEW

The ASR® ASRPM813S is a high efficiency Power Management IC (PMIC), integrating a 1.2-Watt Class D audio amplifier, RTC and measurement unit.

The ASRPM813S power section is designed to supply high performance multi-core processor systems. The ASRPM813S high efficiency step-down regulators support the latest multi-core mobile and tablet platform power requirements.

Interface to Host Processor

- Flexible fast power-up sequences
- I2C host control interface supporting standard and fast modes
- Simple and no-latency two pin DVC interface to host processor for step-down regulator voltage control
- Long OnKey power on/off controls
- Low-power sleep mode
- Fault detection (over voltage, over current, and over temperature), safety controls and watch dog timer
- One dedicated interrupt line to host processor
- Supports many system events and status interrupts

Power supplies

- Three high-efficiency step-down buck regulators
  - Programmable output voltages
  - One 1600mA processor core power supply with fine resolution of 12.5mV steps
  - One general purpose 800mA bucks for system, RF, and I/O power supplies
  - One General purpose 1200mA buck for system and PA power supply
  - Support analog Buck3 input tracking mode
- Thirteen Low Dropout regulators
  - Two low noise LDOs
  - Eleven general purpose remote cap LDOs
- Dynamic Voltage Control for core buck.
- Vibrator driver operating in switch mode and LDO mode with PWM control
- Charger
  - Linear Charger with 1 A max current with fully charge management function. The charger input blocking up to 12V. Programmable fast charge current.

RTC and Clocks

- Low power 32.768kHz crystal oscillator
- RTC domain LDO circuit to support RTC functions
- Low power SRAM retention regulator from VAON domain
- Power up sequence selected by OTP trim

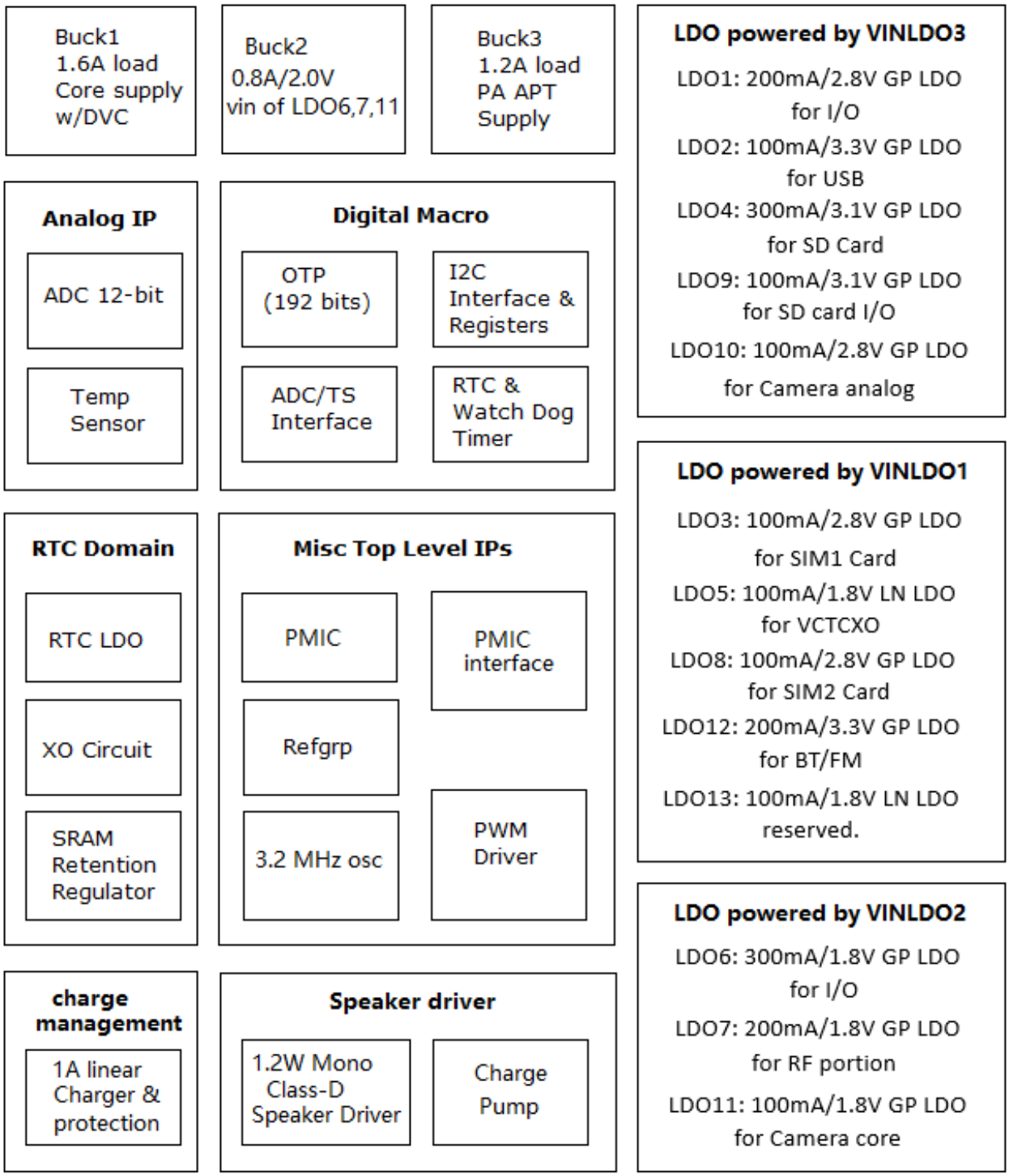
Measurement Unit

- General purpose 12 bit ADC with automatic sampling capability
- Supports system battery voltage, buck/LDO output-voltage and PMIC internal regulator voltage_measurement, etc.
- Four general purpose independent measurement inputs with high-accuracy built-in current source
- 1uA-76uA programmable accurate current source
- Supports battery temperature and battery ID detection
- Programmable measurement thresholds and interrupts
- On-chip temperature sensor to monitor PMIC temperature

Audio

- 1.2W at 8Ω (1%THD) high efficiency Class D amplifier.
- Analog Class-D with analog differential inputs.

Figure 1: PM813S block diagram



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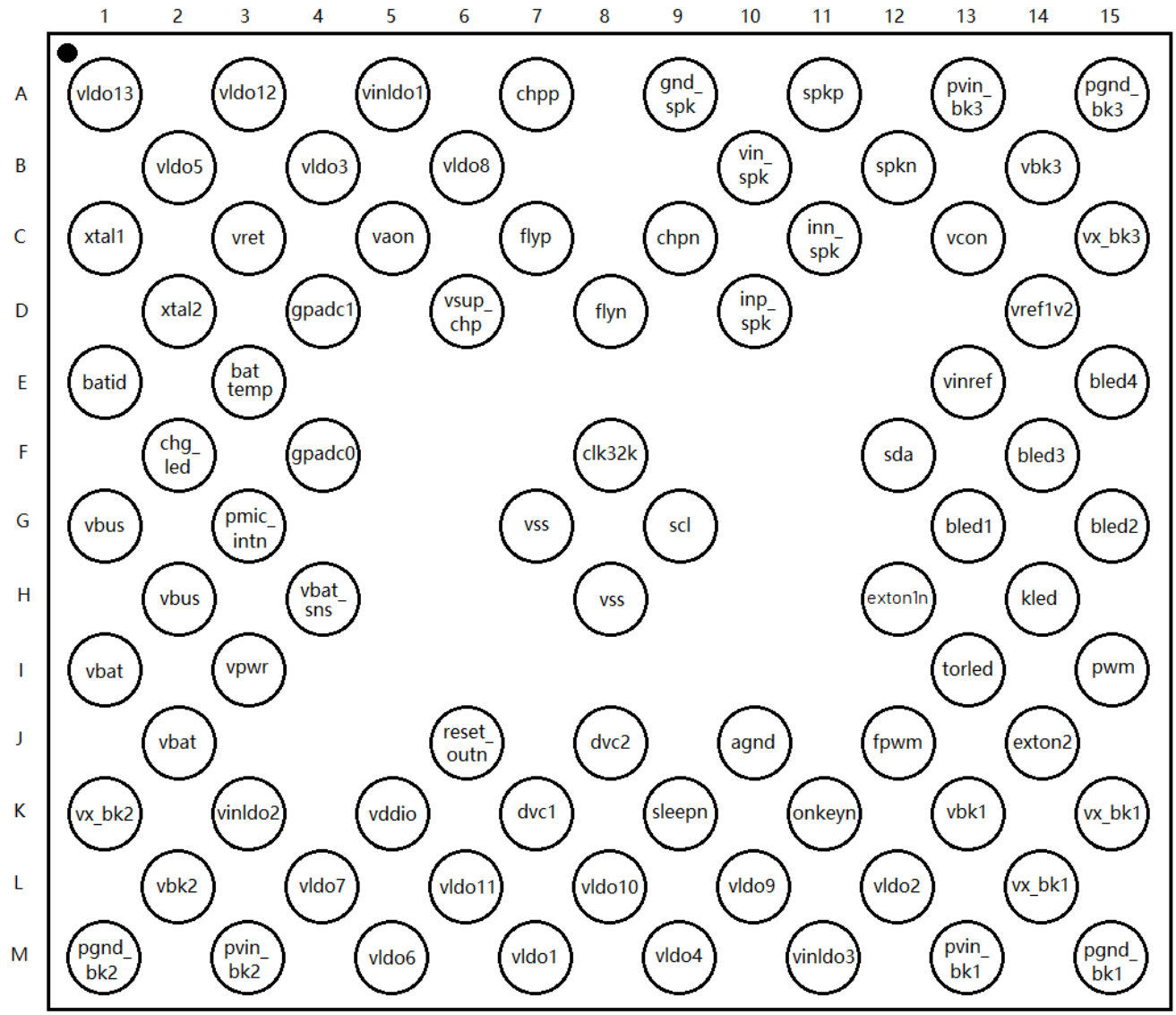
1. Signal Description

1.1. Pin Configurations

PM813S project has one package:

PM813S in 4.093mm×3.533mm WLCSP package, ball pitch 0.35mm with 45 degree angle direction.

Figure 2: PM813S ball map



1.2. Pin Descriptions

Table 1: ASR PM813S pin types

Pin Type	Description
VDD	Supply
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
AI/DI	Analog Input and/or Digital Input
AI/DO	Analog Input and/or Digital Output
DI/DO	Digital Input and/or Digital Output
GND	Ground
NC	Not Connected

Table 2: ASRPM813S Pin Descriptions

Pin Ref.	Pin Name	Pin Type	Ground	Function
A1	VLDO13	AO	AGND	Output of LDO13
A3	VLDO12	AO	AGND	Output of LDO12
A5	VINLDO1	VDD	AGND	Input power supply for LDO3, 5, 8, 12, 13.
A7	CHPP	AO	GND_SPK	Positive charge pump output
A9	GND_SPK	GND		Power ground for loudspeaker.
A11	SPKP	AO	GND_SPK	Loudspeaker amplifier positive output
A13	PVIN_BK3	VDD	PGND_BK3	Supply input for Buck3
A15	PGND_BK3	GND		Power ground for Buck3
B2	VLDO5	AO	AGND	Output of LDO5
B4	VLDO3	A/O	AGND	Output of LDO3
B6	VLDO8	A/O	AGND	Output of LDO8
B10	VIN_SPK	VDD	VSS	Power supply for speaker
B12	SPKN	AO	AGND	Loudspeaker amplifier negative output
B14	VBK3	AI	AGND	Buck 3 feedback input
C1	XTAL1	AO	AGND	32kHz crystal oscillator terminal 1
C3	VRET	AO	VSS	Output of SRAM retention regulator
C5	VAON	AO	AGND	VRTC regulator output
C7	FLYP	AO	GND_SPK	positive charge pump flying capacitor
C9	CHPN	AO	GND_SPK	Negative charge pump output
C11	INN_SPK	AI	AGND	Negative input of the loudspeaker
C13	VCON	AI	AGND	Buck3 analog tracking input
C15	VX_BK3	AO	PGND_BK3	SW output of buck3
D2	XTAL2	AI	VSS	32kHz crystal oscillator terminal 2
D4	GPADC1	AI	AGND	GP ADC auxiliary input 1 with programmable current bias
D6	VSUP_CHP	VDD	AGND	Power supply for charge pump
D8	FLYN	AO	GND_SPK	negative charge pump flying capacitor
D10	INP_SPK	AI	AGND	Positive analog input of the loudspeaker
D14	VREF1V2	AO	AGND	1.2V reference output

Table 2 ASRPM813S Pin Descriptions (Continued)

Pin Ref.	Pin Name	Pin Type	Ground	Function
E1	BAT_ID	AI	AGND	battery id detection input
E3	BATTEMP	AI	AGND	Battery temperature sense
E13	VINREF	VDD	AGND	Filtered supply for reference
E15	BLED4	DO	VSS	Backlight LED4 open drain output
F2	CHG_LED	AO	VSS	Charge LED open drain output
F4	GPADC0	AI	AGND	GP ADC auxiliary input 0 with programmable current bias
F8	CLK32K	DI	VSS	Buffered crystal output
F12	SDA	DI	VSS	I2C serial data
F14	BLED3	DO	VSS	Backlight LED3 open drain output
G1	VBUS	VDD	AGND	Power input VBUS
G3	PMIC_INTN	AI	VSS	PMIC interrupt signal to host
G7	VSS	DI		digital ground
G9	SCL	DI	VSS	I2C serial clock
G13	BLED1	DO	VSS	Backlight LED1 open drain output
G15	BLED2	DO	VSS	Backlight LED2 open drain output
H2	VBUS	VDD	AGND	Power input VBUS
H4	VBAT_SNS	AI	AGND	VBAT sense input
H8	VSS	GND		digital ground
H12	EXTON1N	AI	VSS	enableN signal
H14	KLED	AO	VSS	Keyboard LED open drain output
J1	VBAT	AI/AO	AGND	Battery input
J3	VPWR	AO	AGND	Power supply for charger generated internally from VBUS
J13	TORLED	AO	VSS	Torch LED open drain output
J15	PWM	AO	VSS	Vibrator driver PWM output
K2	VBAT	VDD	AVSS	Battery connection
K6	RESET_OUTN	DO	VSS	Reset signal
K8	DVC2	AI	VSS	DVC port 2
K10	AGND	GND		Analog ground for the whole chip

Table 2 ASRPM813S Pin Descriptions (Continued)

Pin Ref.	Pin Name	Pin Type	Ground	Function
K12	FPWM	AI	VSS	Forced PWM control signal
K14	EXTON2	AI	VSS	Enable signal
L1	VX_BK2	AO	PGND_BK2	SW output of buck2
L3	VINLDO2	VDD	AGND	Power supply input for LDO6, 7, 11
L5	VDDIO	VDD	VSS	Power supply for I/O
L7	DVC1	AI	VSS	DVC port pin 1
L9	SLEEPN	AI	VSS	Sleep control input pin.
L11	ONKEYN	AI	VSS	On Key button pin. 50kΩ pull-up.
L13	VBK1	AI	AGND	Buck1 feedback input
L15	VX_BK1	AO	PGND_BK1	SW output of buck1
M2	VBK2	AI	AGND	Buck2 feedback input
M4	VLDO7	AO	AGND	Output of LDO7
M6	VLDO11	AO	AGND	Output of LDO11
M8	VLDO10	AO	AGND	Output of LDO10
M10	VLDO9	AO	AGND	Output of LDO9
M12	VLDO2	AO	AGND	Output of LDO2
M14	VX_BK1	AO	PGND_BK1	SW output of buck1
N1	PGND_BK2	GND		Power ground for buck2
N3	PVIN_BK2	VDD	PGND_BK2	Power supply input for buck2
N5	VLDO6	AO	AGND	Output of LDO6
N7	VLDO1	AO	AGND	Output of LDO1
N9	VLDO4	AO	AGND	Output of LDO4
N11	VINLDO3	VDD	AGND	Power supply input for LDO1, 2, 4, 9, 10
N13	PVIN_BK1	VDD	PGND_BK1	Power supply input for buck1
N15	PGND_BK1	GND		Power ground for buck1

2. Electrical Specifacations

2.1. Absolute Maximum Ratings

The following applies unless otherwise stated: V_{IN}=VINLDO=2.7 to 4.8V, -30°C<T_A<85°C. Typical values are at T_A=25°C.

Table 3: Absolute Maximum Ratings

Parameters	Condition	Min	Max	Unit
Charger Input	VBUS	-0.3	+12	V
Power Supply Input	VINLDO1, VINLDO2, VINLDO3, VBAT, VBAT_SNS, PVIN_BKx, VIN_SPK	-0.3	+6	V
	VSUP_CHP		2.1	V
Power Supply Output	VLDO1-13, VAON, VX_BK1, VX_BK2, VX_BK3 VPWR, VINREF	-0.3	VBAT+0.3	V
Power I/O Inputs	ONKEYN, EXTON1N, EXTON2	-0.3	VBAT+0.3	V
Power Supply Output	FLYP, FLYN	CHPN-0.3	CHPP+0.3	V
	CHPP	-0.3	VSUP_CP+0.3	
	CHPN	-VSUP_CP-0.3	0.3	V
Analog Inputs	VBK1, VBK2, VBK3, BATTEMP BLED1, BLED2, BLED3, BLED4 TORLED, KLED	-0.3	VBAT+0.3	V
	CHG_LED	-0.3	+12	V
	VREF1P2V	-0.3	2	V
Digital I/O Power Supply	VDDIO, VSUP_CHP	-0.3	+2	V
Digital I/O	RSTn, CLK32K, PMIC_INTN DVC1, DVC2, SLEEPN, I2C_SCL, I2C_SDA, RESET_OUTN, FPWM, PWM	-0.3	VDDIO+0.3	V
Low Voltage Analog I/O	GPADC0, GPADC1	-0.3	+2.0	V
	XTAL1, XTAL2, VRET	-0.3	+2.0	V
All Other Pins	Except GND	-03	+6	V
Storage Temperature		-40	+150	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure.

2. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

2.2. Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameters	Condition	Min	Max	Unit
Charger Input	VBUS	4.5	+5.5	V
Power Supply Input	VINLDO1, VINLDO2, VINLDO3, VBAT, VBAT_SNS, PVIN_BKx, VIN_SPK,	2.7	4.8	V
	VSUP_CHP		2.0	V
Power I/O Inputs	PWM	-0.3	VBAT+0.3	V
Digital I/O	RSTn, CLK32K, PMIC_INTN, GPIO1, GPIO2, DVC1, DVC2, SLEEPN, I2C_SCL, I2C_SDA, RESET_OUTN, FPWM	-0.3	VDDIO+0.3	V
Digital I/O	ONKEYN, EXTON1N, EXTON2	-0.3	VBAT+0.3	V
Low Voltage Analog I/O	GPADC0, GPADC1	-0.3	+1.3	V
	XTAL1, XTAL2, VRET	-0.3	+1.2	V
Operating Temperature (T_{AMB})	Ambient	-30	+85	°C
Operating Junction Temperature (T_J)		-30	+125	°C
I2C Power Supply Input	VDDIO	+1.7	+1.98	V

1. This device is not guaranteed to function outside the specified operating range.

2. Ambient temperature, typical power supplies, unless otherwise noted.

2.3. Package Dissipation Ratings

Table 5: Package Dissipation Ratings

Parameters	Condition	Min	Max	Unit
Maximum Power Dissipation	Device soldered on 4 layer PCB		1	W
Package Thermal Resistance	Device soldered on 4 layer PCB		35	°C/W

1. This device is not guaranteed to function outside the specified operating range.

2. Derate 28mW/C above 85°C.

2.4. Current Consumption

Table 6: Current Consumption Scenarios1

State	Test Conditions	Min	Typ	Max	Unit
'Power-down' State	VINLDO>2.8V		9		μA
'Active' State, Normal Mode	All bucks and LDOs turned on. Load is zero on all supplies. SLEEPn='1'. VBUS=0V		500		μA
'Active' State, Sleep Mode	All bucks and LDOs turned on and in sleep mode. Load is zero on all supplies. SLEEPn=0. VBUS=0V		200		μA

Ambient temperature, typical power supplies, unless otherwise noted.

2.5. Digital I/O Characteristics

The PMIC has one I/O power domain, VDDIO. It is expected to be connected to a 1.8V (±10%) supply.

All pins that can be input or output are set in POR default as inputs.

All pins that are defined as output are set in POR default at low level.

The following applies unless otherwise stated: V_{IN}=VINLDO=2.7V to 4.8V, -30°C<T_A<85°C. Typical values are at T_A=25°C. Refer to schematic shown in Figure 1.

Table 7: Digital I/0 Signals Electrical Characteristics1

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIL	ONKEYn		0		0.3 x VINLDO	V
VIH			0.7 x VINLDO		VINLDO	V
RIN		In parallel to CIN. Internal pull-up to VINLDO	35	50		kΩ
CIN		In parallel to RIN			6	pF
VIL	EXTON1n		0		0.3 x VINLDO	V
VIH			0.7 x VINLDO		VINLDO	V
RIN		In parallel to CIN. Internal pull-up to VINLDO	35	50		kΩ
CIN		In parallel to RIN			6	pF
VIL	EXTON2		0		0.3 x VINLDO	V
VIH			0.7 x VINLDO		VINLDO	V
RIN		In parallel to CIN	200			kΩ
CIN		In parallel to RIN			6	pF
VOL	RSTn	ILOAD = 20kΩ | 10pF	0		0.2 x VDDIO	V
VOH		ILOAD = 20kΩ | 10pF	0.8 x VDDIO		VDDIO	V
Pull-up		When pin is grounded externally			5	mA

Current						
VOL	CLK32K	ILOAD = 5kΩ | 30pF	0		0.2 x VDDIO	V
VOH		ILOAD = 5kΩ | 30pF	0.8 x VDDIO		VDDIO	V
VOL	PMIC_INTn	ILOAD = 20kΩ | 10pF	0		0.2 x VDDIO	V
VOH		ILOAD = 20kΩ | 10pF	0.8 x VDDIO		VDDIO	V
VIL	I2C_SCL		0		0.3 x VDDIO	V
VIH			0.7 x VDDIO		VDDIO	V
RIN		In parallel to CIN. Internal pull up to VDDIO		5	10	kΩ
CIN		In parallel to RIN			6	pF
VIL	I2C_SDA		0		0.3 x VDDIO	V
VIH			0.7 x VDDIO		VDDIO	V
RIN		In parallel to CIN. Internal pull up to VDDIO		5		KΩ
CIN		In parallel to RIN			6	pF
VOL		ILOAD = internal pull up to VDDIO2 5kΩ | 100pF	0		0.2 x VDDIO	V
VIL	DVC1, DVC2		0		0.3 x VDDIO	V
VIH			0.7 x VDDIO		VDDIO	V
RIN		In parallel to CIN	200			kΩ
CIN		In parallel to RIN			6	pF
VOL		ILOAD = 20kΩ | 10pF	0		0.2 x VDDIO	V
VOH		ILOAD = 20kΩ | 10pF	0.8 x VDDIO		VDDIO	V
VIL	SLEEPN		0		0.3 x VDDIO	V
VIH			0.7 x VDDIO		VDDIO	V
RIN		In parallel to CIN	200			kΩ
CIN		In parallel to RIN			6	pF

VOL		ILOAD = 20kΩ | 10pF	0		0.2 x VDDIO	V
VOH		ILOAD = 20kΩ | 10pF	0.8 x VDDIO		VDDIO	V
VIL	FPWM		0		0.3 x VDDIO	V
VIH			0.7 x VDDIO		VDDIO	V
RIN		In parallel to CIN	200			kΩ
CIN		In parallel to RIN			6	pF

3. Power Supplies

3.1. Power Supply Overview

The PM813S includes five buck converters and six low dropout voltage regulators (LDOs).The LDOs and bucks low power mode and active mode are defined in 3.2 and 3.3 . The conditions that set the bucks, LDOs and the switch into their different modes are detailed in LDOs and Bucks States.

Table 8: Buck Power Supply Summary

Power Supply	Typical Usage	Default output(V)	Output Selection(V)	IMAX (mA)	Ilim (mA)	Rdson_p (mOHM)	Rdson_n(mOHM)	Frequency (MHz)	L(uH)	Cout (uF)	Features
Buck1	Host Core voltage	1.05V	0.6-1.6V(12.5mv) 1.6V-1.8V(50mV)	1600	2800	50	25	1.6	1.0~1.2	44	With DVC
Buck2	2.0V I/O	2.0V	0.6-1.6V(12.5mv) 1.6V-3.3V(50mV)	800	1400	80	35	1.6	1.0-2.2	10	
Buck3	General Purpose, RF PA	1.2V	0.3-1.6V(12.5mv) 1.6V-3.3V(50mV)	1200	2100	65	30	1.6	1.0-2.2	10	With APT

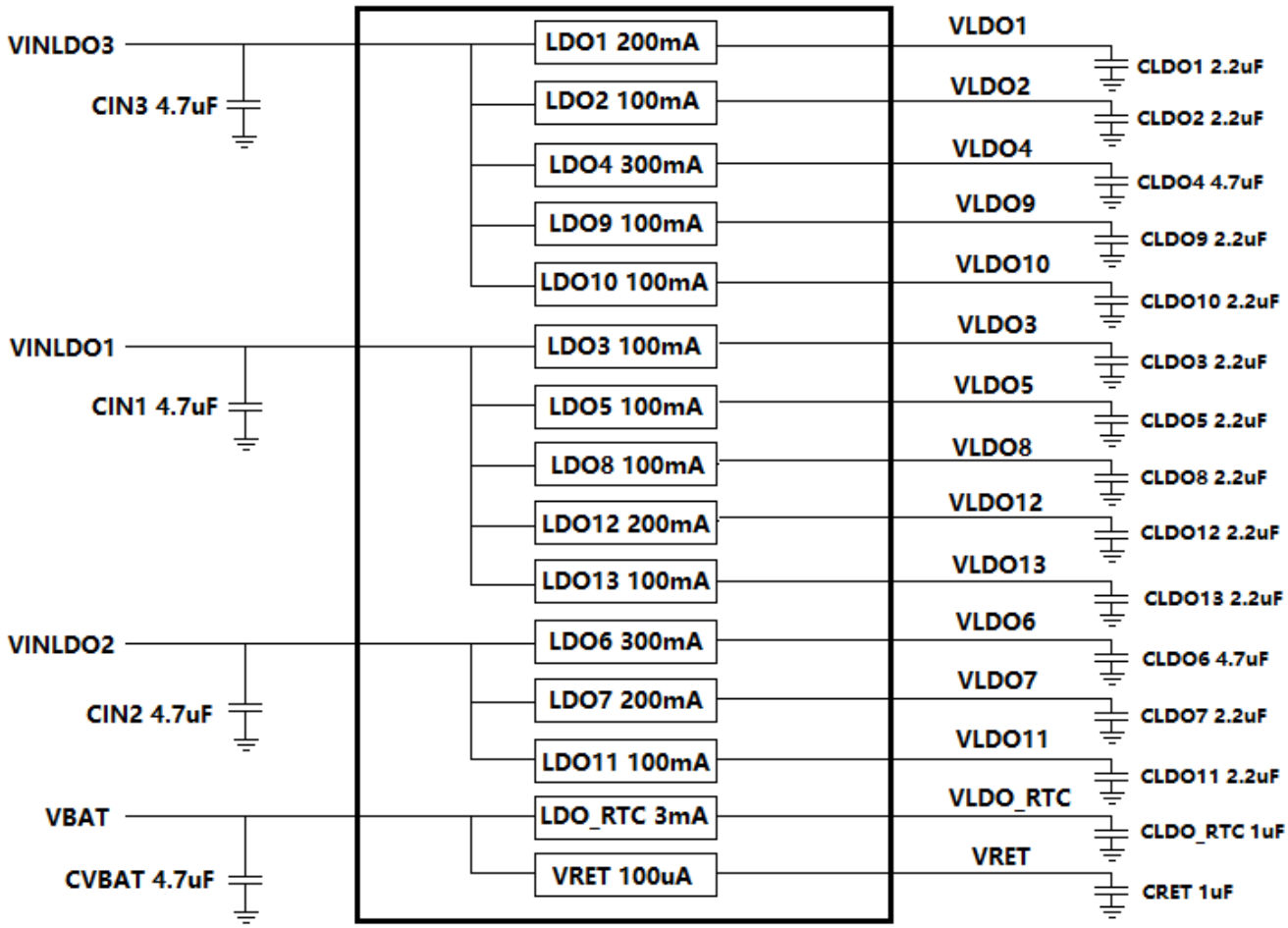
Table 9: LDO Supply Summary

Power Supply	Typical Usage	Output Selection (V)	IMAX	ILIM	Accuracy	Cout	Feature
LDO1	2.8V I/O	1.2~3.3V	200mA	600mA	±3%	2.2~4.7uF	Remote load cap
LDO2	3.3V USB	1.2~3.3V	100mA	600mA	±3%	2.2~4.7uF	Remote load cap
LDO3	2.8V SIM1	1.2~3.3V	100mA	300mA	±3%	2.2~4.7uF	Remote load cap
LDO4	3.1V SD Card Core	1.2~3.3V	300mA	600mA	±3%	2.2~4.7uF	Remote load cap
LDO5	1.8V VCTCXO	1.7~3.3V	100mA	300mA	±3%	2.2~4.7uF	Low noise
LDO6	1.8V I/O	1.2~3.3V	300mA	450mA	±3%	2.2~4.7uF	Remote load cap
LDO7	1.8V RF portion	1.2~3.3V	200mA	600mA	±3%	2.2~4.7uF	Remote load cap
LDO8	2.8V SIM2	1.2~3.3V	100mA	300mA	±3%	2.2~4.7uF	Remote load cap
LDO9	3.1V SD Card IO	1.2~3.3V	100mA	600mA	±3%	2.2~4.7uF	Remote load cap
LDO10	2.8V Camera analog	1.2~3.3V	100mA	600mA	±3%	2.2~4.7uF	Remote load cap
LDO11	1.8V Camera core	1.2~3.3V	100mA	600mA	±3%	2.2~4.7uF	Remote load cap
LDO12	3.3V BT/FM	1.2~3.3V	200mA	300mA	±3%	2.2~4.7uF	Remote load cap
LDO13	1.8V reserved	1.7~3.3V	100mA	300mA	±3%	2.2~4.7uF	Low noise
LDO_RTC	RTC Domain	3.0~3.5V	3mA		±3%	1uF	Low I_Q
VRET	0.675V	0.675V to 0.850V	100uA		+5%	1uF	SRAM retention supply, 25mV a step

3.2. Supply LDOs

Figure 3 shows the supply LDOs application diagram.

Figure 3: Supply LDOs Application Diagram



LDO output voltages are programmable through separate VLDOx_SET registers. The output voltage settings are in listed in the following table.

Table 10: LDO voltage mapping

VLDOx_SET[3:0]	LDO1~4, LDO6~12	LDO5,LDO13
0x0	1.2	1.7
0x1	1.25	1.8
0x2	1.7	1.9
0x3	1.8	2.5
0x4	1.85	2.8
0x5	1.9	2.9
0x6	2.5	3.1
0x7	2.6	3.3
0x8	2.7	N/A
0x9	2.75	N/A
0xA	2.8	N/A
0xB	2.85	N/A
0xC	2.9	N/A
0xD	3	N/A
0xE	3.1	N/A
0xF	3.3	N/A

Table 11: General Purpose LDO(LDO1~LDO4，LDO6~12) Electrical Characteristics

The following applies unless otherwise stated: VIN=VINLDO1,2,3= 2.7V to 4.8V, -30°C <TA<85°C.Typical values are at TA= 25°C. Refer to schematic shown in Figure 3.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Input Voltage Range	VINLDO pins	2.7	3.6	4.8	V
CLDO	Load Impedance	Use capacitor with ±30% tolerance or better [1]	2.2		4.7	μF
		PCB trace resistance to CLDO	0		150	mΩ
CIN1-13	Input Capacitor per LDO if Input Capacitor is Shared	Use capacitor with ±30% tolerance or better	1			μF
IMAX (LDO2/3/8 /9/10/11)	Max Load Current	Active mode	100			mA
		Sleep mode	3			
IMAX (LDO1/7/12)	Max Load Current	Active mode	200			mA
		Sleep mode	3			
IMAX (LDO4/6)	Max load Current	Active mode	300			mA
		Sleep mode	3			
VOUT	Output Voltage Range	Nominal output voltage at output pin (VINLDO > VOUT + 0.3V)	1.2		3.3	V
	Output Voltage Accuracy	Active mode, ILOAD = 50mA	-3		3	%
		Sleep mode, ILOAD = 1mA	-5		5	
VLDREG	Load Regulation	ILOAD from 1mA to 100mA		0.005		%/mA
VLNREG	Line Regulation	VIN from VOUT+0.5V to 4.8V. VOUT = 2.8V ILOAD = 10mA		0.01		%/V
	PSRR[2]	ILOAD = 50mA, F = 100Hz VIN = 3.6V, VOUT = 1.8V		90		dB
		ILOAD = 50mA, F = 10kHz VIN = 3.6V, VOUT = 1.8V		55		

		ILOAD = 50mA, F = 100kHz VIN = 3.6V, VOUT = 1.8V		35		
		ILOAD = 50mA, F = 1MHz VIN = 3.6V, VOUT = 1.8V		25		
	Output Noise	10Hz<f<100kHz, ILOAD = 50mA, VIN = 3.6V, VOUT = 2.8V		70		μVrms
	Short Circuit Current	Current limit in active state (LDO3/8/12). Programmable.	-40%	300	40%	mA
		Current limit in active state (LDO1/2/4/7/9/10/11). Programmable.	-40%	600	40%	
		Current limit in active state (LDO6). Programmable.	-40%	450	40%	
		Current limit in supplies power-up state during LDO power-up, CLDO= 2.2μF		45		
VDROP	Drop Out Voltage	VOUT = 2.8V; ILOAD = IMAX(LDO1,2,3,4,8,9,10,12)			200	mV
		VOUT = 1.8V; ILOAD = IMAX(LDO6,7,11)			200	mV
	Discharge Resistance	LDO_EN = 0		240		Ω
IQ	Quiescent current	Off mode, ILOAD = 0mA		0.1		μA
		Sleep mode, ILOAD=0mA		1		
		Active mode, ILOAD = 0mA (LDO3/8/12)		15		
		Active mode, ILOAD = 0mA (LDO1/2/4/7/9/10/11)		18		
		Active mode, ILOAD = 0mA (LDO6)		21		
PGOOD (Rising)	Power Good Rising			95		%/Vout
PGOOD (Falling)	Power Good Falling			90		%/Vout
	Turn ON Time	From turn on command (I2C or SOD) to 90% of VOUT nominal level; VOUT = 2.8V; CLDO = 2.2μF		0.2		ms

	Turn OFF Time	From turn off command (I2C) to 10% of VOUT nominal level; VOUT=2.8V; Cldo=2.2uF		1.6		ms

1. Using larger CLDO can help reduce load transients.

Guaranteed by design. Not production tested.

Table 12: Low Noise LDO (LDO5 and LDO13) Electrical Characteristics

The following applies unless otherwise stated: VIN= VINLDO=2.7V to4.8V,-30°C<TA<85°C.Typical values are at TA= 25°C. Refer to schematic shown in Figure3.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Input Voltage Range	VINLDO pin	2.7	3.6	4.8	V
CLDO	Load Impedance	Use capacitor with ±30% tolerance or better[1]		4.7		µF
		PCB trace resistance to CLDO	0		150	mΩ
CIN5_6	Input Capacitor per LDO if Input Capacitor is Shared	Use capacitor with ±30% tolerance or better	1			µF
IMAX	Max Load Current	Active mode	200			mA
		Sleep mode	3			
	Output Voltage Range	Nominal output voltage at output pin (VINLDO > VOUT + 0.3V)	1.7		3.3	V
	Output Voltage Accuracy	Active mode, ILOAD = 50mA	-3		3	%
		Sleep mode, ILOAD = 1mA	-5		5	
VLDREG	Load Regulation	ILOAD from 1mA to IMAX		0.002		%/mA
VLNREG	Line Regulation	VIN from VOUT+0.5V to 4.8V VOUT = 2.8, ILOAD = 10mA		0.01		%/V
	PSRR[2]	ILOAD = 50mA, F = 100Hz VIN = 3.6V, VOUT = 1.8V		95		dB
		ILOAD = 50mA, F = 10kHz VIN = 3.6V, VOUT = 1.8V		60		
		ILOAD = 50mA, F = 100kHz VIN = 3.6V, VOUT = 1.8V		35		
		ILOAD = 50mA, F = 1MHz VIN = 3.6V, VOUT = 1.8V		25		

	Output Noise	10Hz < f < 100kHz, ILOAD = 50mA, VOUT = 2.8V		45		µVrms
	Short Circuit Current	Current limit in active state. Programmable with 100mA steps	-40%	300	40%	mA
		Current limit in supplies power-up state during LDO power-up, CLDO = 1µF		45		
VDROP	Drop Out Voltage	VOUT = 2.8V, ILOAD = IMAX			200	mV
	Discharge Resistance	LDO_EN = 0		240		Ω
IQ	Quiescent Current	Off mode, ILOAD = 0mA		0.1		µA
		Sleep mode, ILOAD = 0mA		2		
		Active mode, ILOAD = 0mA		32		
PGOOD (Rising)	Power Good Rising			95		%/Vout
PGOOD (Falling)	Power Good Falling			90		%/Vout
	Turn ON Time	From turn on command (I2C or SOD) to 90% of VOUT nominal level; VOUT = 2.8V; CLDO = 2.2µF		0.2		ms
	Turn OFF Time	From turn off command (I2C) to 10% of VOUT nominal level; VOUT=2.8V; Cldo=2.2uF		1.6		ms

Using larger CLDO can help reduce load transients.

Guaranteed by design. Not production tested.

Table 13: LDO RTC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Input Voltage Range	VINLDO pin	3	3.6	4.8	V
CLDO	Load Impedance	Use capacitor with ±30% tolerance or better	1			µF
IMAX	Maximum Load Current	Active mode, VINLDO >VOUTV+0.5V	3			mA

VOUT	Output Voltage Range	Nominal output voltage at output pin	3		3.5	V
	Step Size			100		mV
	Output Voltage Accuracy	ILOAD = 1mA, VINLDO > VOUTV+0.5V	-5		5	%
VLDREG	Load Regulation	ILOAD from 0.1mA to IMAX		1		%
VLNREG	Line Regulation	VIN from VOUT+0.5V to 4.8V. ILOAD = 1mA		1		%
	PSRR1	ILOAD = 1mA to IMAX, F = 20kHz VIN>VOUT+0.5V		40		dB
VDROP	Drop Out Voltage	VOUT = 2.8V; ILOAD = 3mA		100		mV
IQ	Quiescent Current	Off mode		0.2	2	μA
		Active mode, ILOAD = 0mA		2.4		
	Reverse Leakage Current	VINLDO = 0V; VOUT = 2.9V		0.1	1	μA

Notes:

This LDO is always on to drive the RTC domain.It is active whenever VINLDO is sufficiently high to drive this LDO(VINLDO> V_{OUT}+0.1V).

There is no sleep mode for LDORTC.

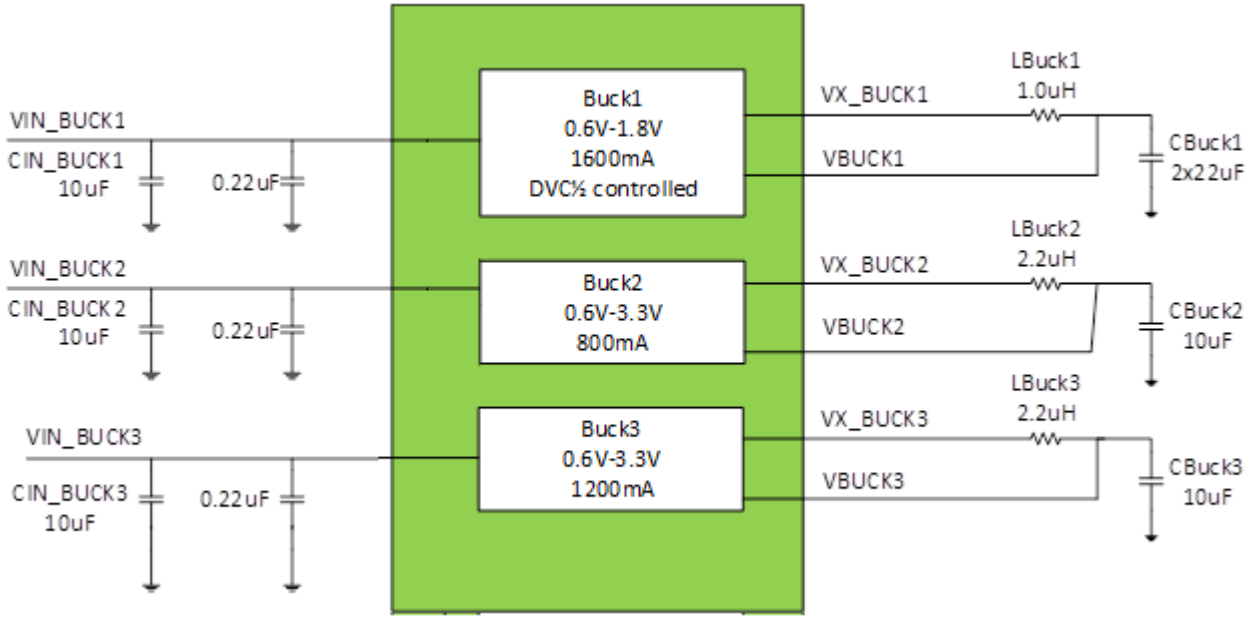
This LDO is not turnedoffbyI2C command.

3.3. Supply Buck Converters

3.3.1. Core Supply Step Down Regulator

Buck1, buck2 and buck3 have different switching phase. Buck2 swithcing phase has 180 degree shift to buck1 and buck3 has 90 degree shift to buck2. The switching frequency is 1.6MHz.

Figure 4: Supply Buck Converters Application Diagram



The following applies unless otherwise stated: V_{IN}=VIN_BUCK1,2,3=2.7V to 4.8V, -30°C<T_A<85°C. Typical values are at T_A=25°C. Refer to schematic shown in Figure 4.

Table 14: Core Supply Step Down Regulator (buck1) Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CIN1_BUCK1	External components		0.22			µF
CIN2_BUCK1	External components		10			µF
L_{BUCK1}			1.0		1.2	µH
L_{BUCK1_ESR}					100	mΩ
C_{OUT_BUCK1}			2x22		4x22	µF
V_{IN_BUCK}	Input Voltage Range	VIN_BUCK1 Pin	2.7	3.6	4.8	V
FSW	Switching Frequency			1.6		MHz
I_{MAX}	Maximum Load Current	PWM mode, V_{IN}=>3.0V	1600			mA
		Sleep mode	5			mA
$I_{PWM2PFM}$		Vin = 3.6V, Vout = 1.05V		180		mA
$I_{PFM2PWM}$		Vin = 3.6V, Vout = 1.05V		350		mA
V_{OUT}	Output Voltage Range	Programmable range	0.6		1.8	V
	Step Size	V_{OUT}=0.6V to 1.6V		12.5		mV
		V_{OUT}=1.6V to 1.8V		50		mV
	DVC Step	Time step	1, 2, 4, 16			µs/step
	Soft Start Time		500, 1000			µs
	Output Voltage Accuracy	PWM mode, I_{LOAD}=10mA	-2		2	%/V_{OUT}
		PFM=1, I_{LOAD}=10mA	-3		+3	%/V_{OUT}
		Sleep mode, I_{LOAD}=5mA	-5		+5	%/V_{OUT}
PGOOD_R	Power Good Rising			95		%/V_{OUT}
PGOOD_F	Power Good Falling			90		%/V_{OUT}
V_{LDREG}	Load Regulation	PWM mode: I_{LOAD}=10mA to I_{MAX}		0.1		%/A
V_{LNREG}	Line Regulation	I_{LOAD}=1000mA, V_{IN}=2.7V to 4.8V		0.2		%/V
I_{LIM}	High-side FET current limits	PWM mode, VIN=2.7V to 4.8V	2500	3000	3400	mA
	Quiescent Current Consumption	Off mode		0.1	10	µA
		Sleep mode		6		µA
		PFM mode		25		µA
		PWM mode (Buck1 only)		10		mA
Rdson_P	High-side: V_{IN}=3.6V FULL_DRIVE=1			50		mΩ
Rdson_N	Low-side: V_{IN}=3.6V			25		mΩ

	FULL_DRIVE=1					
	Internal discharge resistance in off mode	I discharge = 3.5mA		165		Ω
T_turnoff	Turn OFF Time	From turn off command (I2C or power-down event) to 10% of VBUCK1 nominal output voltage level; CBUCK=2x22μF		30		ms

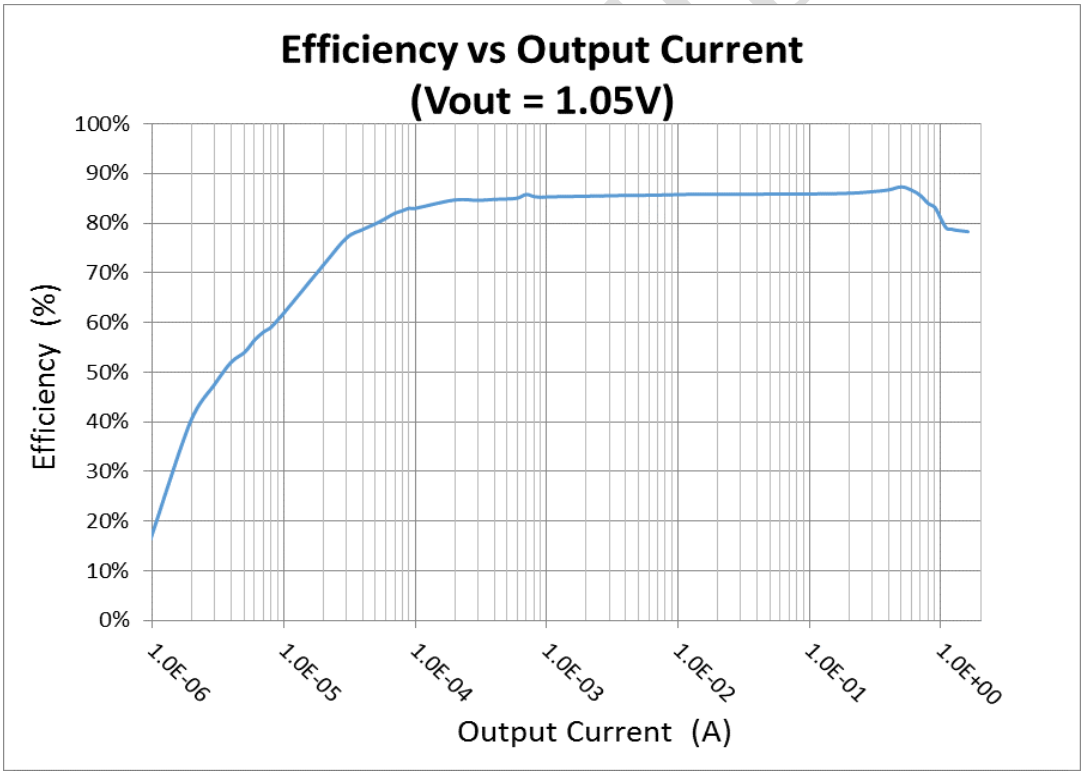
1. All bucks have Dynamic Voltage Control (DVC) to control the slope of the voltage when changing from one voltage setting to another and when the buck converter turns on (soft start).

2. For Buck1, the actual voltage is programmed into the VBUCK1_SETy (y = 0, 1, 2, 3) selected using the DVC1 and DVC2 pins as described in Section 9.7.6, DVC1 and DVC2.

Figure 5: Core Supply Buck1 Typical Efficiency Curve

VIN = 3.6V; VOUT = 1.05V; FSW= 1.6MHz; LBUCK = 1uH

Temperature = 25°C; COUT = 2x22uF, with the Buck1 quiescent only.



3.3.2. General Purpose Step Down Regulator Buck2

Table 15: General Purpose Step Down Regulator (Buck2) Electrical Characteristics

The following applies unless otherwise stated: VIN=VINLDO=2.7V to 4.8V, -30°C<TA<85°C. Typical values are at TA=25°C. Refer to schematic shown in Figure 4.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CIN1_BUCK2	External components		0.22			µF
CIN2_BUCK2	External components		10			µF
LBUCK2			2.2		3.3	µH
LBUCK_ESR2					100	mΩ
COUT_BUCK2			10		50	µF
VIN_BUCK2	Input Voltage Range	VIN_BUCK2 Pin	2.7	3.6	4.8	V
FSW	Switching Frequency			1.6		MHz
IMAX(Buck2)	Maximum Load Current	PWM mode, VIN=>3.0V	800			mA
		Sleep mode	5			mA
IPWM2PFM		Vin = 3.6V, Vout = 1.8V		180		mA
IPFM2PWM		Vin = 3.6V, Vout = 1.8V		340		mA
VOUT	Output Voltage Range	Programmable range	0.6		3.3	V
	Step Size	VOUT=0.6V to 1.6V		12.5		mV
		VOUT=1.6V to 3.3V		50		mV
	DVC Step	Time step	1, 2, 4, 16			µs/step
	Soft Start Time		500, 1000			µs
	Output Voltage Accuracy	PWM mode, ILOAD=10mA	-2		2	%/VOUT
		PFM=1, ILOAD=10mA	-3		+3	%/VOUT
		Sleep mode, ILOAD=5mA	-5		+5	%/VOUT
PGOOD_R	Power Good Rising			95		%/VOUT
PGOOD_F	Power Good Falling			90		%/VOUT
VLDREG	Load Regulation	PWM mode: ILOAD=10mA to IMAX		0.1		%/A
VLNREG	Line Regulation	ILOAD=1000mA, VIN=2.7V to 4.8V		0.2		%/V
ILIM	High-side FET current limits	PWM mode, VIN=2.7V to 4.8V	1300	1550	1800	mA
	Quiescent Current	Off mode		0.1	10	µA

	Consumption	Sleep mode		5		μA
		PFM mode		24		μA
		PWM mode		6		mA
Rdson_P	High-side: VIN=3.6V FULL_DRIVE=1			80		mΩ
Rdson_N	Low-side: VIN=3.6V FULL_DRIVE=1			40		mΩ
	Internal discharge resistance in off mode	I discharge = 3.5mA		165		Ω
	Turn OFF Time	From turn off command (I2C or power-down event) to 10% of VBUCK1 nominal output voltage level; CBUCK=10μF		10		ms

All bucks have Dynamic Voltage Control (DVC) to control the slope of the voltage when changing from one voltage setting to another and when the buck converter turns on (soft start).

For Bucks 2, the target value of the voltage change is programmed into the VBUCK2_SET fields.

Figure 6: General Purpose Buck Typical Efficiency Curve

VIN = 3.6V; VOUT = 1.2V; FSW = 1.6MHz; LBUCK = 2.2uH

Temperature = 25°C; COUT = 10uF, with the Buck quiescent only.

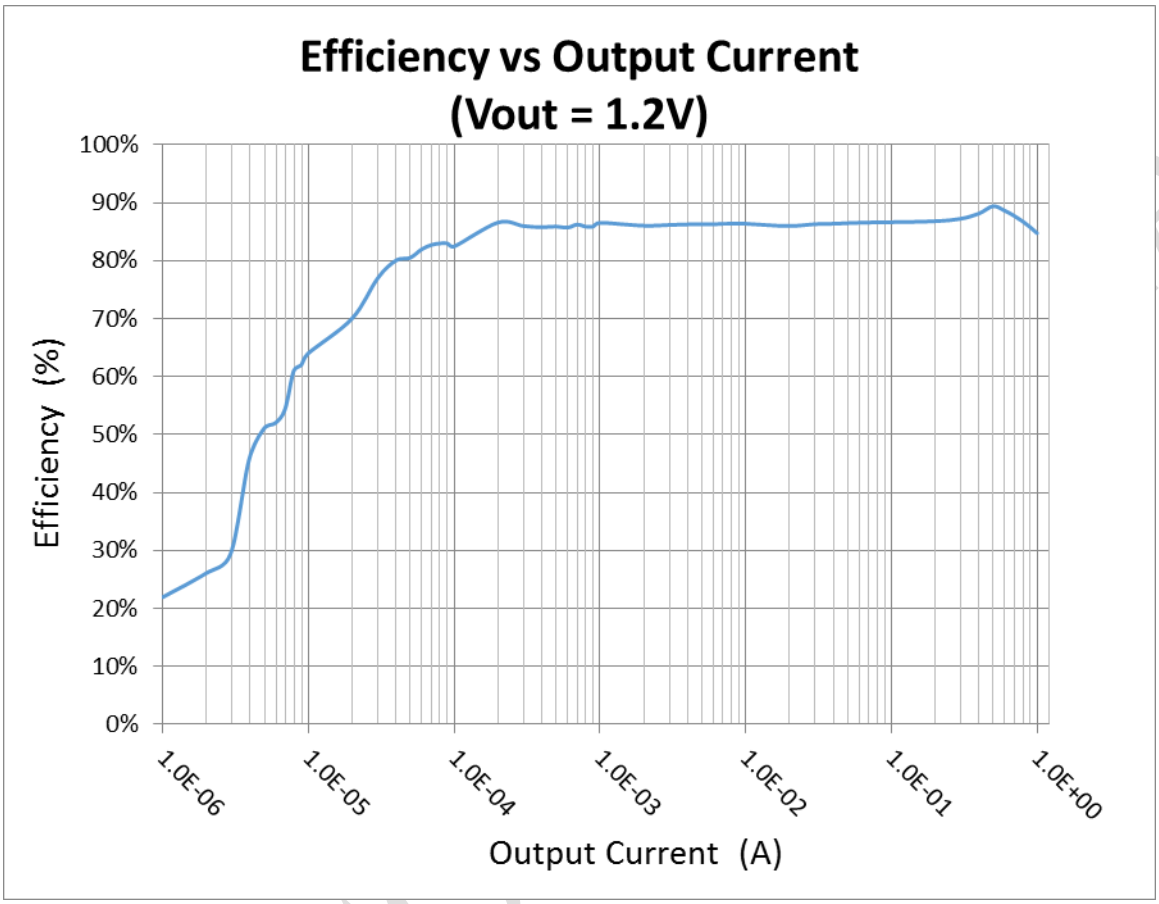
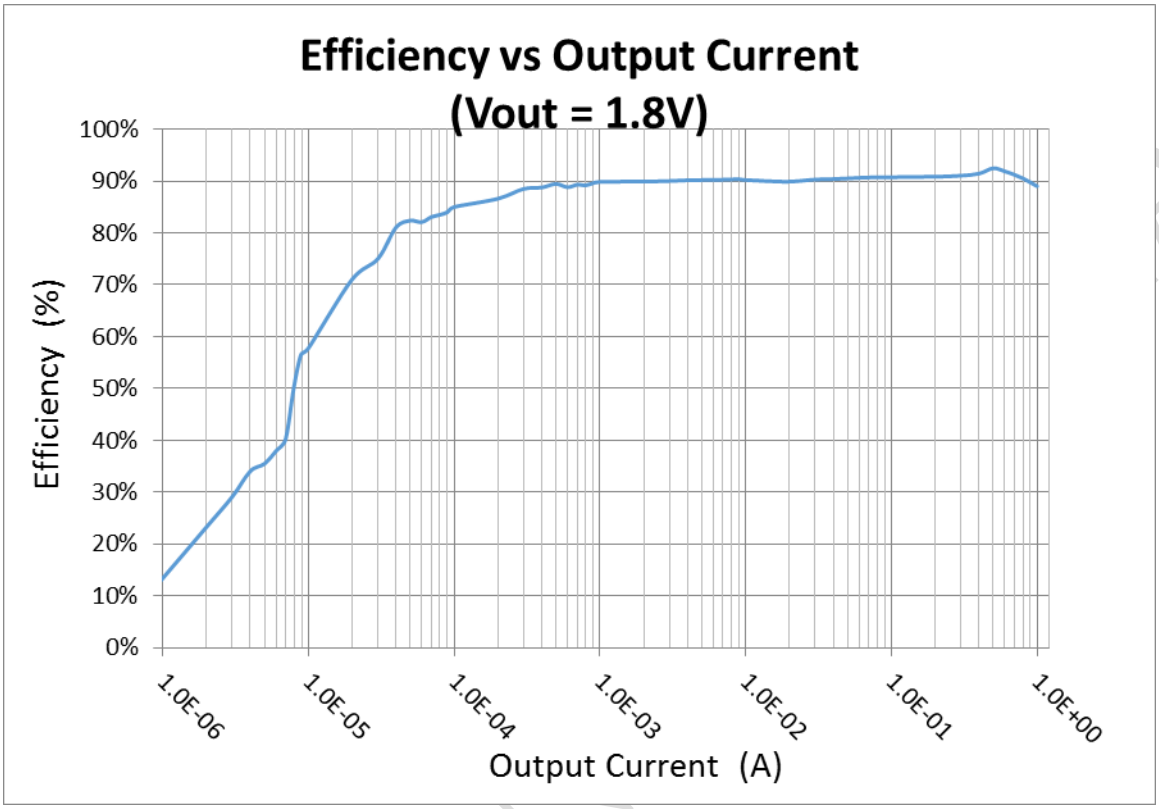


Figure 7: General Purpose Buck Typical Efficiency Curve

VIN = 3.6V; VOUT = 1.8V; FSW = 1.6MHz; LBUCK = 2.2uH

Temperature = 25°C; COUT = 10uF, with the Buck quiescent only.



3.3.3. General Purpose Step Down Regulator Buck3

Table 16: General Purpose Step Down Regulator (Buck3) Electrical Characteristics

The following applies unless otherwise stated: VIN=VIN_BUCK3=2.7V to 4.8V, -30°C<TA<85°C. Typical values are at TA=25°C. Refer to schematic shown in Figure 4.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN1_BUCK3}	External components		0.22			µF
C_{IN2_BUCK3}	External components		10			µF
L_{BUCK3}			2.2		3.3	µH
L_{BUCK_ESR3}					100	mΩ
C_{OUT_BUCK3}			10		50	µF
V_{IN_BUCK3}	Input Voltage Range	VIN_BUCK3 Pin	2.7	3.6	4.8	V
FSW	Switching Frequency			1.6		MHz
$I_{MAX(BUCK3)}$	Maximum Load	PWM mode,	1200			mA

	Current	V_{IN}=>3.0V				
		Sleep mode	5			mA
$I_{PWM2PFM}$		Vin = 3.6V, Vout = 1.1V		180		mA
IPFM2PWM		Vin = 3.6V, Vout = 1.1V		320		mA
VOUT	Output Voltage Range	Programmable range	0.6		3.3	V
	Step Size	VOUT=0.6V to 1.6V		12.5		mV
		VOUT=1.6V to 3.3V		50		mV
	DVC Step	Time step	1, 2, 4, 16			µs/step
	Soft Start Time		500, 1000			µs
	Output Voltage Accuracy	PWM mode, I_{LOAD}=10mA	-2		+2	%/V_{OUT}
		PFM=1, I_{LOAD}=10mA	-3		+3	%/V_{OUT}
		Sleep mode, I_{LOAD}=5mA	-5		+5	%/V_{OUT}
PGOOD_R	Power Good Rising			95		%/V_{OUT}
PGOOD_F	Power Good Falling			90		%/V_{OUT}
V_{LDREG}	Load Regulation	PWM mode: I_{LOAD}=10mA to I_{MAX}		0.1		%/A
V_{LNREG}	Line Regulation	I_{LOAD}=1000mA, V_{IN}=2.7V to 4.8V		0.2		%/V
I_{LIM}	High-side FET current limits	PWM mode, VIN=2.7V to 4.8V	1900	2200	2500	mA
	Quiescent Current Consumption	Off mode		0.1	10	µA
		Sleep mode		5		µA
		PFM mode		24		µA
		PWM mode		6		mA
Rdson_P	High-side: V_{IN}=3.6V FULL_DRIVE=1			65		mΩ
Rdson_N	Low-side: V_{IN}=3.6V FULL_DRIVE=1			30		mΩ
	Internal discharge resistance in off mode	I discharge = 3.5mA		165		Ω
	Turn OFF Time	From turn off command (I2C or power-down event) to 10% of V_{BUCK1} nominal output voltage level; C_{BUCK}=10µF		10		ms

Buck3 have Dynamic Voltage Control (DVC) to control the slope of the voltage when changing from one voltage setting to another and when the buck converter turns on (soft start).

Buck3 the target value of the voltage change is programmed into the VBUCK3_SET fields.

Buck3 RF PA Mode

Buck3 can be configured to track an analog voltage applied to the GPIO1/BUCK3_ADC pin. . The input voltage applied to the GPIO1/BUCK3_ADC pin is expected to have a range from 0.10 to 1.4V. The relationship between input and output is Buck3_PA_OUT=2.5x GPIO1.

Table 17: BK3_ADC pin

BK3_ADC is analog input pin as VCON for buck3 operation. In this operation, Buck3 behaves in APT mode which generates output Vbk3=2.5 x VCON to support PA operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCON	Input voltage range		0.12		1.4	V
Gain	BK3_ADC gain			2.5		
VCON_PFM	Vcon threshold to go to PFM mode. If VCON is below the threshold, buck3 goes to PFM mode.	VCON_PFM_TH[1:0]=00		0.4		V
		VCON_PFM_TH[1:0]=01		0.44		
		VCON_PFM_TH[1:0]=10		0.48		
		VCON_PFM_TH[1:0]=11		0.52		
	Hysteresis for VCON_PFM threshold to go to PWM mode			20		mV

This APT feature is enabled by programming register EN_APT_BK3. During this APT mode, buck3 can transition from PFM to PWM mode based on VCON value. If VCON is below VCON_PFM_TH, then buck3 stays in PFM mode, otherwise Buck3 stays in PWM mode. The threshold is programmable by I2C interface. For example, when VCON_PFM_TH[1:0]=00, VCON voltage below 0.4V makes buck3 go to PFM mode, VCON voltage above 0.42V makes buck3 go to PWM mode.

3.3.4. FPWM function

FPWM pin is digital input pin to force buckx(x=1,2,3) into FPWM mode during PMIC operation. When FPWM=1, buckx goes to FPWM mode immediately. This function is much faster than I2C program therefore it can prepare buckx faster for heavy load application.

To enable buckx's FPWM function, the internal register FPWM_en_buckx should be set to 1 by I2C program.

FPWM_en_buckx default value is 0.

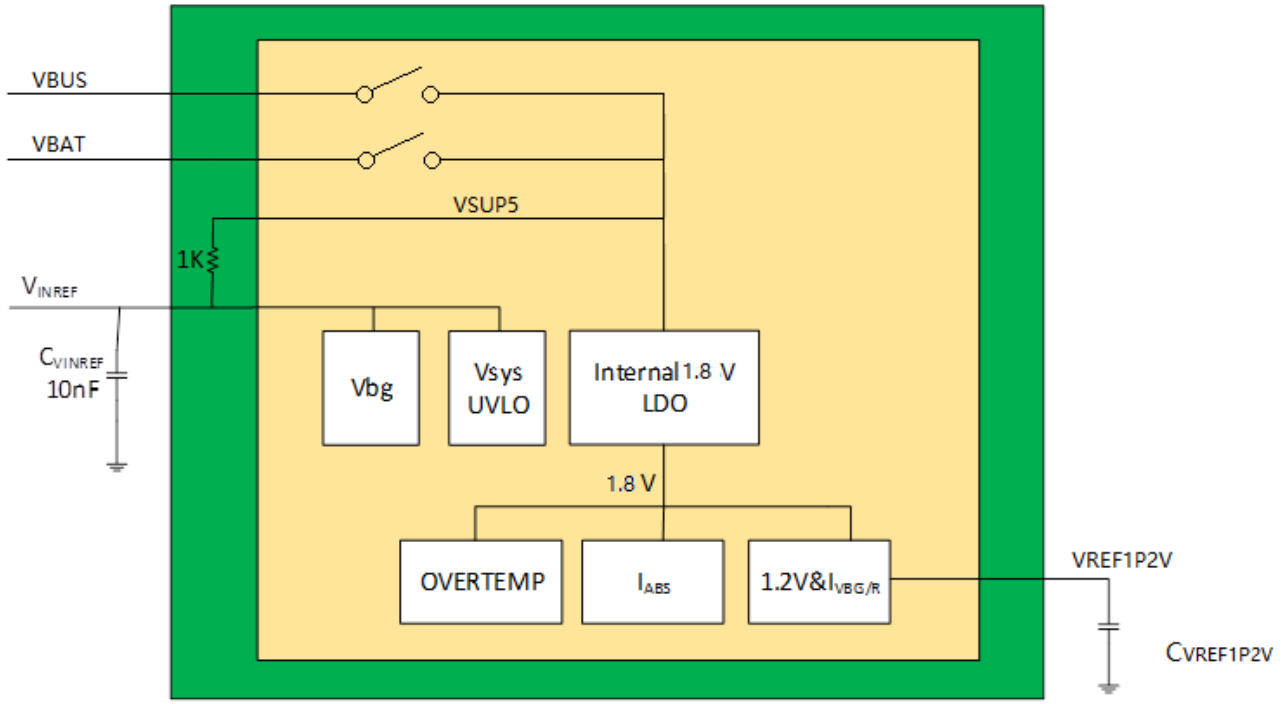
Table 18: FPWM pin

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIL	FPWM		0		0.3xVDDIO	V
VIH			0.7xVDDIO		VDDIO	V
RIN		In parallel to CIN to ground	200			KΩ
CIN		In parallel to RIN			6	pF

3.4. ReferenceGroup

Reference Groupincludes trimmed bandgap,precise1.2V voltage generation for bucks andLDOs,voltage to current(V2I)block,1.2V logic core supply,1.8V analog circuits supply and fault detection circuitry.The VINREF input pin requires a10nFcapacitor.The1.2V reference output has a low pass filter which requires an external 220nF bypass capacitor at the VREF1V2 output pin,as shown in Figure 8.

Figure 8: Reference Group Block Diagram



The fault detection circuitry includes over temperature protection (OVER_TEMP detector), over and under voltage protection (OV_VSYS, UV_VSYS2 detectors) and under voltage lock out (UV_SYS1 detector).

Bandgap generates the reference voltage for all the circuits. Trim circuit makes sure that 1.2V output has an error less than 1% (@25°C). The 1.2V reference output is followed by a Low Pass Filter (LPF) to reduce noise. "V to I converter" generates stable currents over temperature and power supply voltage variations. The LPF is enabled when POWER_HOLD is set.

Fault detection circuits, for Over Temperature, Over Voltage Protection and Under Voltage protection provides signaling to the digital section. There are a total of 5 protection signals sent from the reference group to the digital (OV_TEMP140, OV_TEMP160, UV_VSYS1 UV_VSYS2, OV_VSYS).

Table 19: Reference Group Electrical Characteristics

The following applies unless otherwise stated: $V_{IN=}$ VINLDO=2.7V to4.8V,-30°C<T_A<85°C.Typical valuesareatT_A=25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{VINREF}	External Components	CVINREF, Output load capacitor	-30%	100	+30%	nF
$C_{VREF1P2V}$	External Components	CREF, Output load capacitor	-30%	220	+30%	nF
VREF1P2V	VREF1P2V output voltage	No Load.		1.200		V
UVSYS_R	System Under voltage protection rising edge threshold votlager	programmable		2.9V		V
UVSYS_F	System under voltage protection falling edge threshold voltage	programmable		3.0V		V
T_UVSYS	UVSYS debounce time	Entering UVSYS or Exiting from UVSYS		30		ms
OT	Over temperature protection threshold			120		°C

When VBAT voltage decreases below UVSYS _R and last longer than T_UVSYS, the PMIC shuts down with power off sequence. If VBAT keeps below UVSYS_R for shorter than T_UVSYS, PMIC keeps in active state. This is useful to filter glitches on VBAT when VBAT is close to UVSYS_R and avoid PMIC shutdown unexpectedly.

For over discharged battery, after VBUS pluggin VBAT voltage begin to rise. PMIC will power up after VBAT rises above UVSYS_F and lasts for T_UVSYS. If VBAT voltage drops below UVSYS_F again within T_UVSYS, PMIC will not power up.

4. Charger

PM813S device integrates the charge function and can charger the battery from VBUS power souce connected to USB. The charge current is monitored inside the chip. The current monitored by the charger is the VBUS input current. The charger regulates the VBUS input current during tricle charge, pre-charge and fast charge.

In a typical application the battery is supplying the system. The charge current into the battery will be

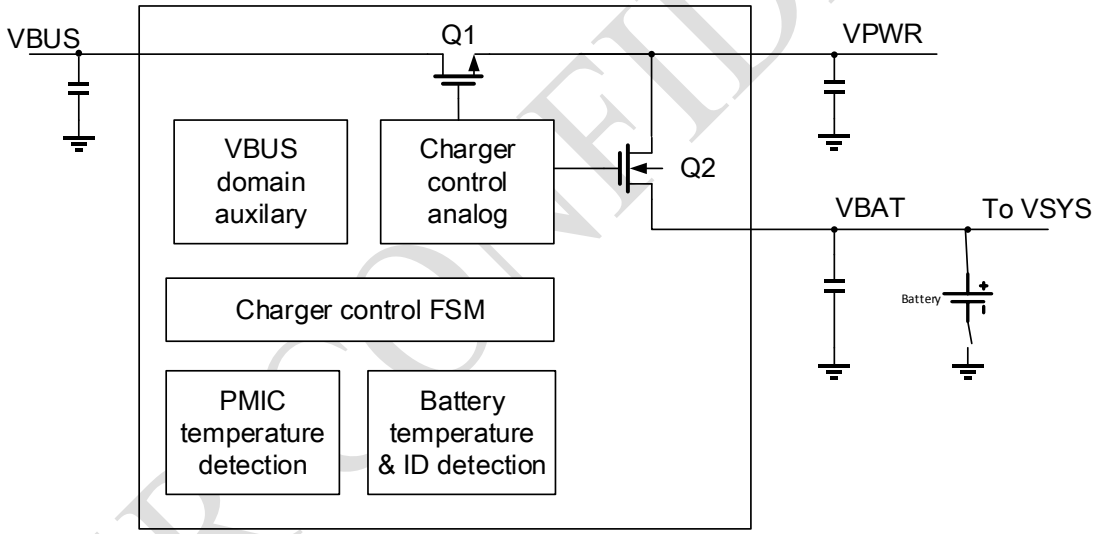
I(VBAT) =I(VBUS)-I(VSYS).

Where I(VBUS) is the VBUS input current, I(VSYS) is the current to the system.

ASR PM813S also provides function to sense the charge current into the battery by GPADC channel 9 (GPADC0 channel) and an external current sense resistor connected at the negative side of the battery. The charger's state is automatically controlled by PMIC charger control, depending on input VBUS voltage, battery voltage, battery temperature, PMIC chip temperature etc.

The following figure shows PM813S charge function diagram.

Figure 9: Charger function diagram



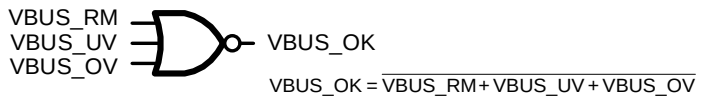
4.1. Charger Power Source

When USB is plugged in, the charger is powered by VBUS. In order for a VBUS power source to be validated (VBUS_OK=1) three conditions must hold

1. VBUS > VBUS_UV
2. VBUS < VBUS_OV

3. VBUS – VBAT > VTH_VBUSRM

Figure 10: VBUS detection diagram (VBUS_OK)



The detection of VBUS remove is implemented by detecting the voltage drop between VBUS and VBAT. If VBUS is removed VBUS voltage will decrease. When VBUS-VBAT is less then VTH_VBUSRM and VBUS remove is detected, the charger will switch to shutdown mode and the charger MOSFET is turned off.

Table 20: Threshold of VLRDY/VBUS_UV/VBUS_OV/VBUS_RM is shown in the following table

	0=>1 Threshold(default)	1=>0 Threshold(default)	Program Field
VLRDY	VBUS>3.3V	VBUS<3.2V	None
VBUS_RM	VBUS<VBAT+22.5mV	VBUS>VBAT+180mV	BP 0x28 bit<2:0>
VBUS_UV	VBUS<3.7V	VBUS>3.8V	BP 0x29 bit<5:4>
VBUS_OV	VBUS>6.3V	VBUS<6.2V	None

The device Q1 between VBUS and VPWR is a 12V HV-NMOS, so VBUS can sustain surge voltage up to 12V. When VBUS voltage is higher than VBUS_OV, Q1 will turn off and protect VPWR and circuits powered by VPWR.

4.2. Charger control

The device Q2 between VPWR and VBAT is a 5V PMOS for the charge control. The bulk of Q2 is always selecting the max voltage node of VPWR and VBAT. When VBUS is off, Q2 can reverse blocking the current from VBAT to VPWR (and then to VBUS).

The charge current is controlled according to the following charge states.

- Trickle charge. When VBAT < VTH_trk, the charge current is Ichg_trk.
- Pre-charge. When VTH_trk < VBAT < VTH_pre, the charge current is Ichg_pre.
- Fast charge. When VTH_pre < VBAT < VTH_fast, the charge current is Ichg_fast.
- Constant volage charge. When VBAT > VTH_fast, the max charge current is Ichg_cv. the voltage V(VBAT) is regulated to VREGCV.

The charger state machine diagram is:

Figure 11: Charger State Machine

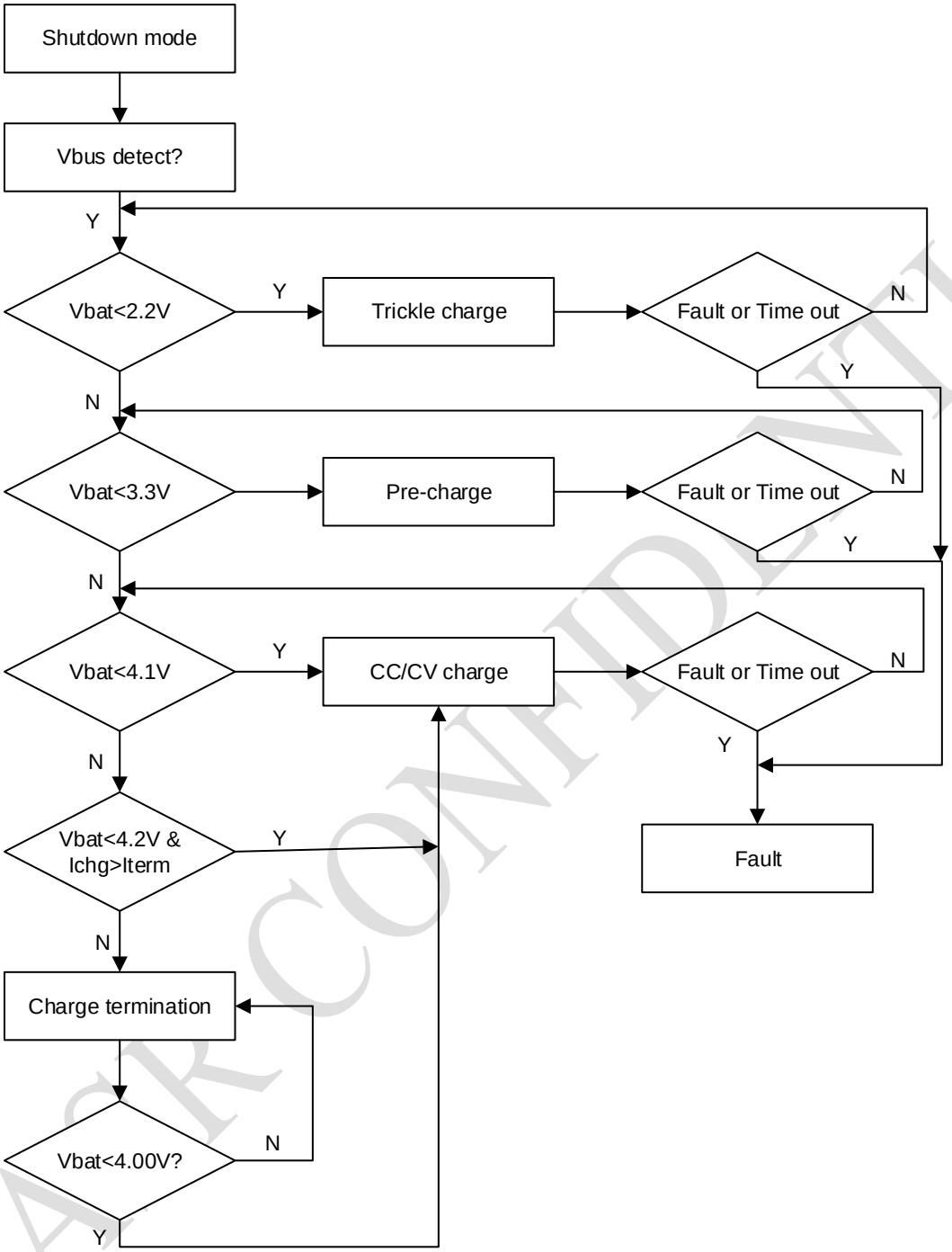


Table 21: Charger electronic characteristics

Charger Electronic characteristics

Symbol	Description	Condition	Value			Unit
			Min	Typical	Max	
Vbus	Vbus detection range		4.4		6.2	V
Vbus_ovp_rise	Vbus OVP rising threshold			6.3		V
Vbus_ovp_fall	Vbus OVP falling threshold			6.2		V
Vbus_uvlo_rise	Vbus UVLO rising threshold			4.4		V
Vbus_uvlo_fall	Vbus UVLO falling threshold			4.3		V
VTH_VBUSRM_rise	VBUS-VBAT rising edge			60		mV
VTH_VBUSRM_fall	VBUS-VBAT falling edge			20		mV
Vth_trickle	Trickle charge threshold	Vbat < Vth_trickle		2.2V		V
$I_{TRICKLE}$	Trickle charge current	Vbat < Vth_trickle		50		mA
TO_trickle	Trickle charge timeout	Programmable from 6 min to 15min		15		min
VTH_{PRECHG_RISE}	Pre-charge battery threshold (rise edge)	Need to be the same as PMIC UVLO_Vsys		3.0		V
VTH_{PRECHG_FALL}	Pre-charge battery threshold (fall edge)			2.7		V
I_{PRECHG}	Pre-charge current (programmable)	ICC_PRE<1:0>=00 ICC_PRE<1:0>=01 ICC_PRE<1:0>=10 ICC_PRE<1:0>=11		75 50 100 150		mA
TO_{PRECHG}	Precharge timeout	Programmable from 24 to 60 Minutes.		60		Min
ICC	CC mode charge current	ICC_sel<4:0>=00000		50		mA
		ICC_sel<4:0>=00001		100		
		ICC_sel<4:0>=00010		150		
		ICC_sel<4:0>=00011		200		
		ICC_sel<4:0>=00100		250		
		ICC_sel<4:0>=00101		300		

		ICC_sel<4:0>=00110		350		
		ICC_sel<4:0>=00111		400		
		ICC_sel<4:0>=01000		450		
		ICC_sel<4:0>=01001		500		
		ICC_sel<4:0>=01010		550		
		ICC_sel<4:0>=01011		600		
		ICC_sel<4:0>=01100		650		
		ICC_sel<4:0>=01101		700		
		ICC_sel<4:0>=01110		750		
		ICC_sel<4:0>=01111		800		
		ICC_sel<4:0>=10000		850		
		ICC_sel<4:0>=10001		900		
		ICC_sel<4:0>=10010		950		
		ICC_sel<4:0>= 10011~11111		1000		
	Charge current accuracy		-5%		+5%	
VREGCV	CV mode regulation voltage: (programmable)	Vreg_cv[1:0]=000 Vreg_cv[1:0]=001 Vreg_cv[1:0]=010 Vreg_cv[1:0]=011 Vreg_cv[1:0]=100 Vreg_cv[1:0]=101 Vreg_cv[1:0]=110 Vreg_cv[1:0]=111		4.20 4.25 4.30 4.35 4.40 4.45 4.15 4.10		V
	CV voltage accuracy		-0.6%		+0.6%	
	Battery over voltage protection	For 4.2V VREGCV setting		4.3		V
ITERM	CC/CV mode termination current	programmable to 25/50/75/100mA		50		mA
VRECHG	Battery voltage for re-charge			VREGCV-150mV		V
TOCCCV	CC/CV mode timeout			120		min

IBAT_NOCHG	Battery leakage with no Vbus attach			1	10	uA
PMICTEMP	PMIC temp during charging	reduce Ichg		115		C
BATTEMP	Battery temp during charging		0		60	C
ICHGLED	Charger LED current	Programmable 5mA or 10mA		5 or 10		mA

Comparator in Charger IP (total 7 comparators)

Mode	**Comparators in Charger IP**							**Note**
	VBATTCHG	**VBATPCHG**	**VBATFCHG**	**IBATTERM**	**OVP**	**UVLO**	**Vbat OVP**	
Shutdown (000)	2.2	3.3	4.1	50mA	6.2	4.4	4.3	Charger HIZ
Check (001)	2.2	3.3	4.1	50mA	6.2	4.4	4.3	Charger HIZ
Trickle CHG (010)	2.1	3.3	4.1	50mA	6.3	4.3	4.3	ICHG=50mA
PreCharge (011)	2.1	3.3	4.1	50mA	6.3	4.3	4.3	ICHG=100mA
CC/CV (100)	2.1	3.2	4.1	50mA	6.3	4.3	4.3	ICHG=500 ~ 1000mA
Terminate (101)	2.2	3.2	4.05	60mA	6.3	4.3	4.3	ICHG=0mA
CHG_Fault (110)	2.2	3.3	4.1	50mA	6.2	4.4	4.3	ICHG=0mA

Battery temperature and battery ID detection are done inside ADC block. During charging, battery temperature and PMIC temperature are monitored to control charging process. To improve safety of charging Li-ion battery, JEITA compliance can be enabled by I2C (register base page 0x15[7]). Once enabled, Battery charging is only allowed from 0C to 60C of battery temperature. Within this temp range, charging is regulated by JEITA standard. Below is the recommendation in PM813S PMIC. The following algorithm is controlled by hardware. This feature can also be overrided to allow AP to take control of charging process.

Table 22: Battery temperature detection

Battery Temp	Charging current and voltage setting
0C to 10C	Roughly halve the charging current setting.

	Regulation voltage is the same as I2C setting
10C to 45C	Default setting. Charging current and voltage are controlled by I2C
45C to 60C	Current is the same as I2C setting Reduce the regulation voltage by 0.1V~0.2V, i.e. reduce regulation voltage from 4.2V to 4.1V

For the same reason, when PMIC temperature is too high (>110C), the charging current will be reduced per I2C setting to improve safety. If PMIC temperature is higher than 150C, charging process will be stopped.

On top of supporting 4.2V/4.35V battery voltage, the charger function also supports 4.4V battery voltage per I2C programming (base page F1, bit 6).

4.3. MPPT function

When extenral power supply is connected to VBUS, it provides the current to PM813S via VBUS pin. In CC/CV charge state, the charge current is usually big. If the charge current is set higher than the external power supply's current limit threshold, VBUS voltage will decrease until it drops below VBUS_UV threshold and turn off the charger. PM813S provides MPPT function to automatically perform the maximum power point tracking, and get the optimized charge current setting.

MPPT funciton is useful when VBUS input current cannot reach ICC. One possible reason is the external power supply current capacity is smaller than ICC. Another possible reason is resistance of the connection bus from external power supply to VBUS pinof PM813S is too big. Without MPPT function the charger may not work properly in these 2 cases.

4.3.1. MPPT starts condition

MPPT function will start each of the following conditions:

1. The charger enters CC/CV state.
2. VBUS decreases below VTH_MPPT_VMIN.
3. I2C write register bit MPPT_RESTART=1 (GP 0x8B bit[6])

When write MPPT_RESTART=1, MPPT function restarts, and the bit MPPT_RESTART will automatically reset to 0.

4.3.2. MPPT disable

MPPT function can be disabled by I2C write register MPPT_DISABLE=1 (GP 0x8B bit[6]).

4.3.3. MPPT function

When MPPT starts, the charge current is initially reset to 0, then ramp the charge currrent step by step. The following are the MPPT cases:

1. The charge current reaches ICC (the constant charge current) and VBUS voltage keeps above VTH_MPPT_MAX. MPPT stops with charge current set to ICC. This is the normal case.

2. VBUS voltage drops below VTH_MPPT_MAX before the charge current reaches ICC. Then the charge current will ramp down by 1 step and stops MPPT.

3. VBUS voltage drops below VTH_MPPT_MIN during MPPT period or in CC/CV mode. MPPT will restart.

Considering cases 3, if VTH_MPPT_MIN and VTH_MPPT_MAX are too close, MPPT may not stop properly. So prpper set the value of VTH_MPPT_MIN and VTH_MPPT_MAX is necessary.

Figure 12: MPPT and done with charge current reaches ICC

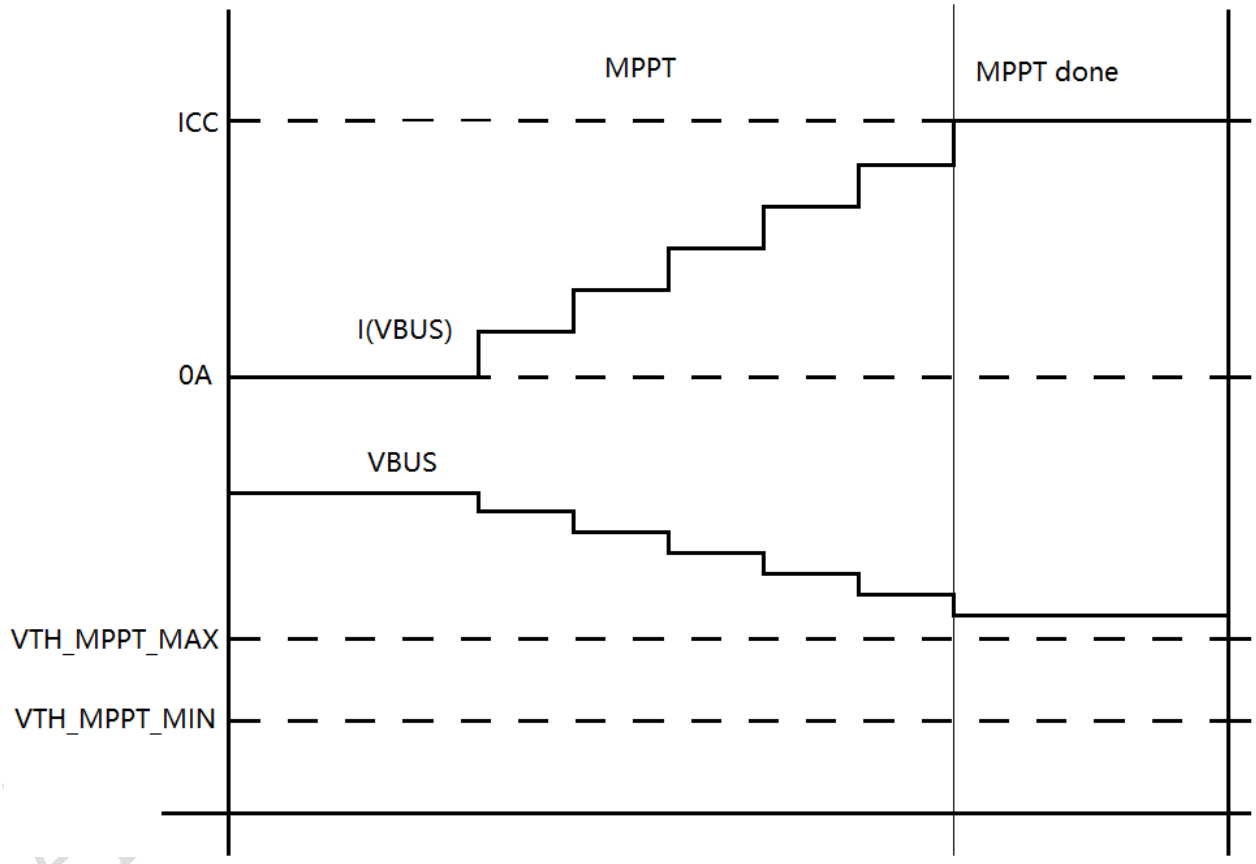


Figure 13: MPPT and done with charge current lower than ICC

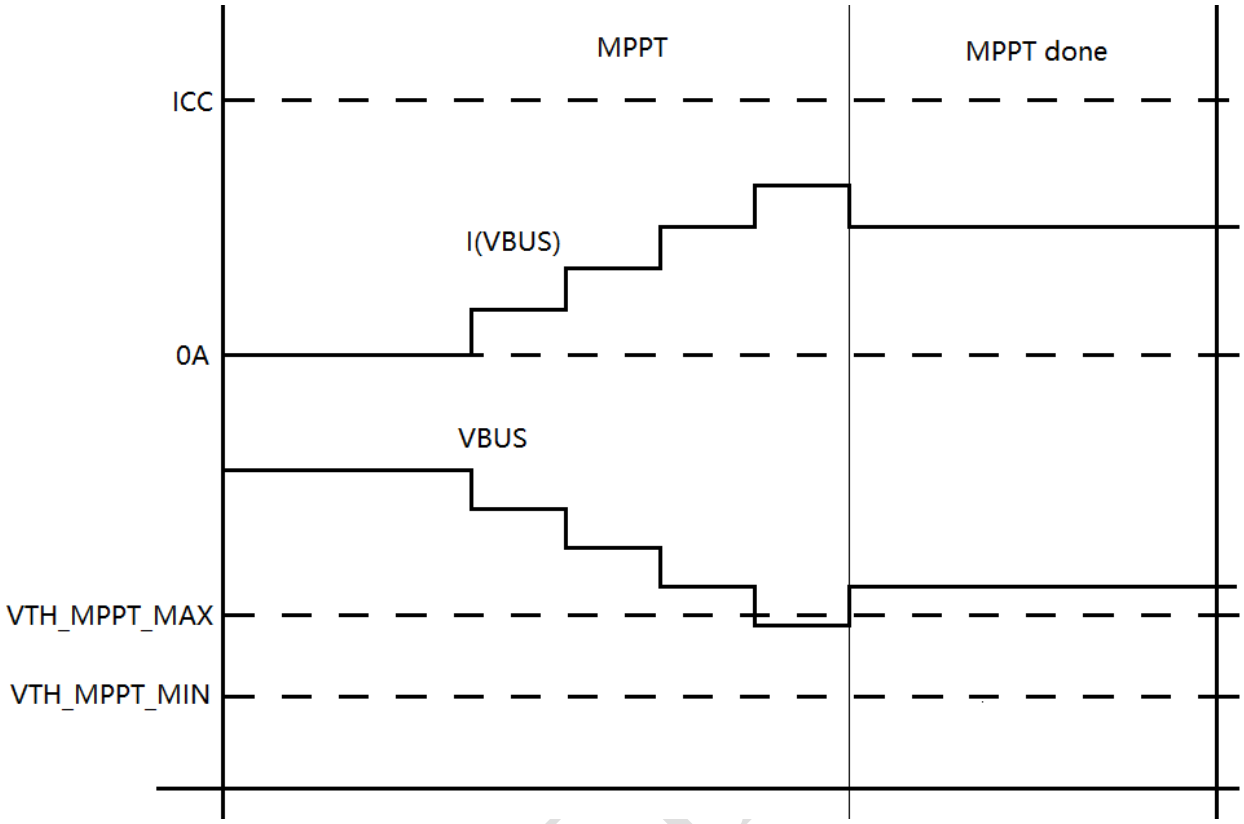
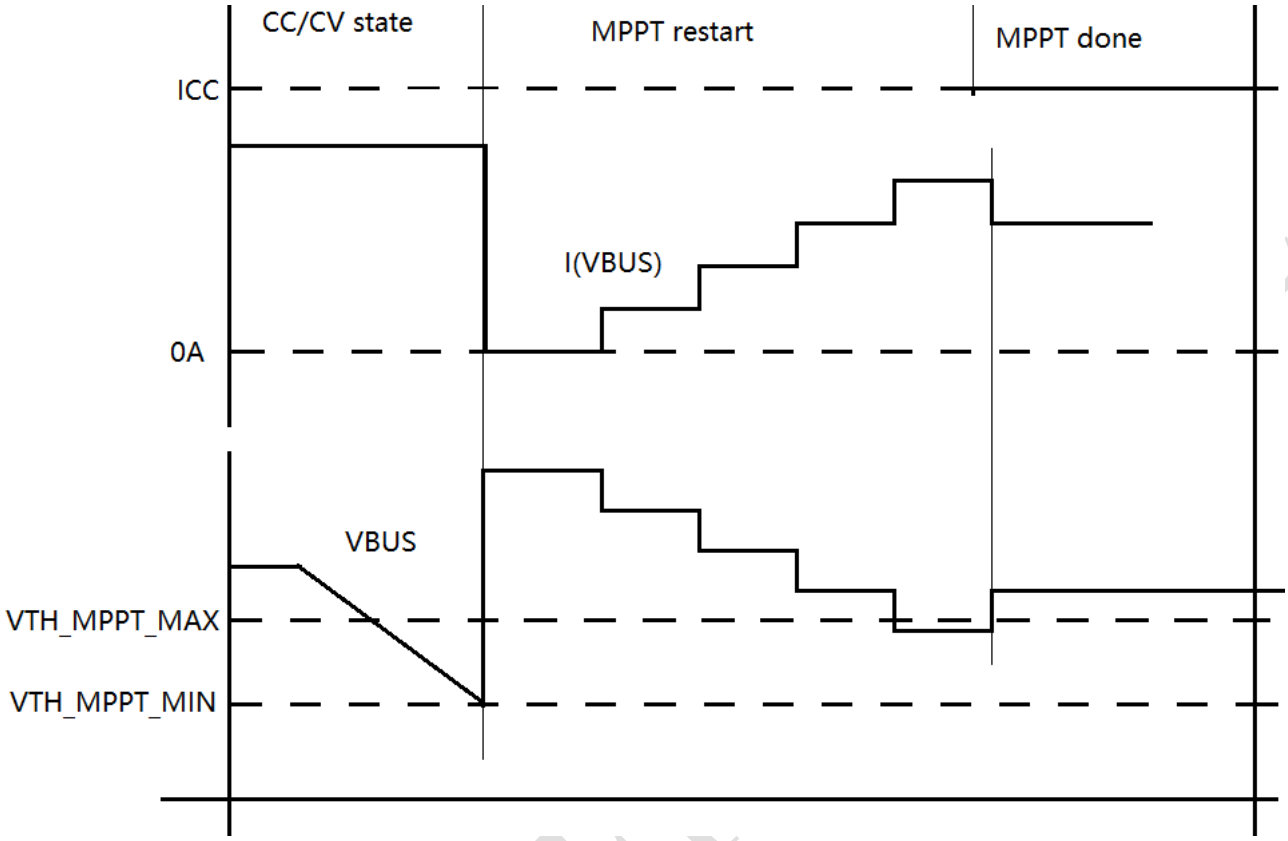


Figure 14: MPPT restart by VBUS decreases below VTH_MPPT_MIN during CC/CV state



The MPPT threshold voltage VTH_MPPT_MAX and VTH_MPPT_MIN are programmable.

4.4. VBUS voltage limit function

PM813S also provides VBUS voltage limit funciton to make the charger work properly when external power supply cannot provide current up to ICC. This function is impelemnted by the charger loop adjustment. When external power supply output current reaches its limit threshold and VBUS decreases to VTH_VBUS_MIN, the charger loop senses VBUS votlage and reduces the charge current to keep VBUS no less than VTH_VBUS_MIN.

The VBUS voltage limit funciton is disabled by default. It could be enabled by set register EN_VBUSMIN to 1. The threshold VTH_VMUS_MIN can be selectd by S_VBUS_MIN[1:0]

Table 23: VBUS voltage limit function

Register	Parameter
EN_VBUSMIN	0: disable vbus voltage limit function (default) 1: enable vbus voltage limit function

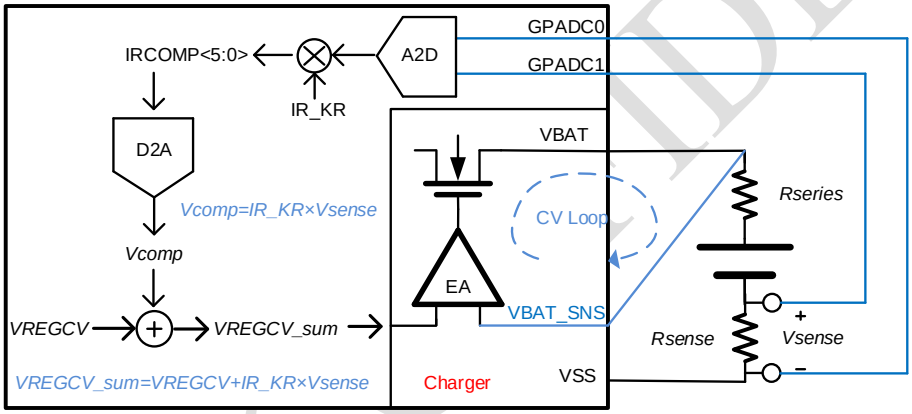
S_VBUS_MIN[1:0]	00: 3.9V; 01: 4.1V; 10: 4.3V; 11: 4.5V

4.5. IR compensation function

Series resistance (including PCB routing, battery connector, sense resistor in the battery pack) may slow down charge speed. To speed up charging cycle, charger should stay in constant current mode as long as possible. Purpose of IRCOMP is to increase constant voltage regulation target, so that charger can stay in constant current mode longer in charging cycle. Constant voltage regulation target of charger with IRCOMP is VREGCV_sum, we have VREGCV_sum=VREGCV+Vcomp, where VREGCV is constant voltage regulation target without IRCOMP and Vcomp is the compensation voltage.

As shown as following figure, voltage on Rsense, i.e. Vsense, is sensed by GPADC1/0 and calculated to generate compensation voltage Vcomp: Vcomp=Vsense*IR_KR (limited by Vcomp_limit, see below for detail).

Figure 15: IR Compensation



- IR_KR (GP 0x8A bit<5:0>) is the compensation resistance ratio: IR_KR=Rcomp/Rsense.

If Rsense=20mohm，range of compensation resistance is 0mohm~1260mohm（IR_KR=000000~111111）, step is 20mohm. Rcomp should be smaller than Rseries+Rsense, IR_KR is recommended to be smaller than 0.5*(Rseries+Rsense)/Rsense

- Total Range of Vcomp is 0~315mV (000000~111111). Step of Vcomp is 5mV.
- Vcomp is limited by Vcomp_limit =5mV*IRCOMP_LIMIT<5:0> (GP 0x88 bit<5:0>)：

  Vcomp=Vcomp_limit (Vsense*IR_KR>Vcomp_limit),

  Vcomp=Vsense*IR_KR (Vsense*IR_KR≤Vcomp_limit)

  Default value of Vcomp_limt is 100mV（010100），maximum value of Vcomp_limt is 315mV（111111）

- Accuracy of Vcomp is ±10%.

5. Clock and RTC Management

5.1. Clock group

The internal clock group generates all clock signals for PMIC. It powers up after PMIC wakeup. The block diagram is below.

Figure 16: Clock group

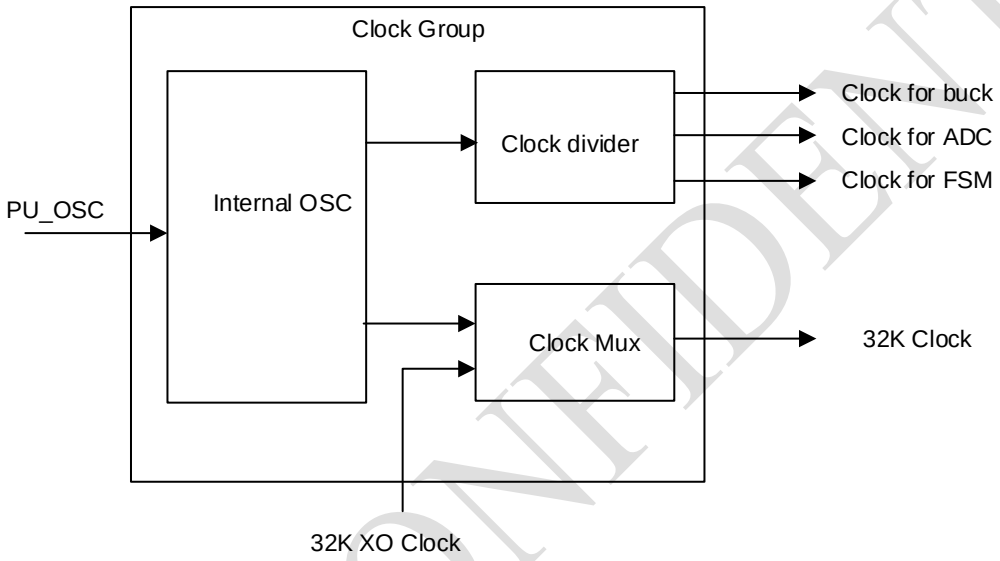


Table 24: Internal Clock Electrical Characteristics

The following applies unless otherwise noted: VIN=1.8V,-30 ℃<T_A<85 ℃. Typical values are at T_A=25 ℃. Refer to schematic shown in Figure 3.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VINLDO	Input voltage range	VINLDO Pin	2.7	3.6	4.8	V
	Quiescent current	'Active' state		4.5	7	μA
		'Power-down' state		0	0.5	
	Frequency	VINLDO = 3.6V @ room temperature	-5%	32.768	5%	kHz
		Over supply and temperature	-15%	32.768	15%	

The 32k clock output "clk32k" can be set to two different clock sources: internal OSC clock or 32K crystal oscillator

output by register programming (see table below). Once PMIC is powered up, and XO output is ready, SOC can program register bit reg_use_xo high to use 32K XO clock, which will remain active even when PMIC is in shutdown mode. During sleep mode, the OSC will run in low power mode to reduce Iq. All other clocks will be either gated off or running in low power mode.

5.2. 32K Crystal Oscillator (CLK_XO)

32K XO uses a crystal to generate the 32.768kHz clock.

CLK_XO turns on after SOD power-up. It supplies the clock CLK32K once the host processor switches the source to the 32K XO (CLK_XO), usually after the startup time defined in Figure3. to reach the clock accuracy required by the platform.

Chapter 4.1 describes the application diagram of 32.768kHz XO connectivity to the PMIC. The crystal capacitances are integrated and can be selected through the XO_CAP_SEL field as described in Table20.

Table 25: 32K XO Electrical Characteristics

The following applies unless other wise noted:V_{IN}=1.8V,-30°C<T_A<85°C. Typical values are at T_A=25°C. Refer to schematic shown in Figure3 .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VRTC	Input voltage range	VRTC Pin	1.8	3.0		V
IQ	Quiescent current (XO + complete RTC block)	Oscillator running		2		µA
TSTART	Start-up time	From VRTC rise to oscillator running at specified frequency		1		Sec
RF	Feedback resistor	Integrated resistor between XTAL1 and XTAL2 pins	-30%	12		MΩ
CXTAL	Internal capacitance for crystal oscillator	One capacitor CXTAL on XTAL1 and one on XTAL2, selected through XO_CAP_SEL[2:0] field		No internal cap,10,15,20,25,30,35,45		pF
XO Frequency	XTAL1,2 input accuracy				100	ppm

5.3. CLK32K Outputs

PM813S has one 32kHz output buffers. Each buffer can output either a'0', a 32 kHz internal freerunning clock,32kHz XOclock or HiZ.

The output signal ofthe CLK32K buffer is definedin Table below.

Table 26: CLK32K Output Signal

Output	Condition		
CLK32K Signal	**Reg_clk_32K_SEL<1:0>**	**RSTn**	**Reg_USE_XO Field**
'0'	Xx	0	x
'0'	00	1	x
32.768kHz clock from the 32K free running oscillator	01	1	0
32.768kHz clock from 32K XO	01	1	1
32.768kHz clock from 32K XO	10	1	1
Hi-Z	11	1	x

The CLK32K signal can output either a '0', a 32 kHz free running clock, 32 kHz XO clock or HiZ.

The output signal of CLK32K is defined as a function of the 32K_OUT1_SEL field and the RESET_OUTn signal level as detailed in 8.5.21.

When the USE_XO field is set, all clock buffers, if enabled output the XO version of the 32K clock.

Note: The transition of the signals CLK32K and CLK32K_2 from 32K free running oscillator to 32K XO and back is glitch free, at the expense of pausing the signals CLK32K for a maximum of one and a half clock cycles.

5.4. RTC Counter and Trimming

RTC_COUNTER is a 32 bit counter for seconds (it is a read only field).

In the transition from 'Power on Reset' state to 'RTC' state the RTC_COUNTER resets to zero, it starts counting and the event field RTC_RESET_EVENT is set to '1'.

The input clock to the RTC counter is either the internal clock divided by 100 or the 32K XO, as defined in 5.2.

In order to allow use of the I2C to read the RTC_COUNTER field is divided to four fields of eight bits each.

There are two trimming fields that correct the RTC counter to lower its frequency error.

RTC_TRIM_INT is a 10 bit field that trims integer 32 kHz clock cycles (2's complement format).

The value of RTC_TRIM_INT is added to 32767 and it is the reset value of the 32K_COUNTER. The 32K_COUNTER counts the cycles of the 32K XO oscillator. When it reaches the reset value it generates a pulse which is the raw 1-Hz signal that sources the RTC_COUNTER.

In the case that the 32 kHz clock is accurate to 32.768 kHz the RTC_TRIM_INT value will be set by the host processor as 0 and the 32K_COUNTER reset value is 32767.

- If the 32 KHZ clock frequency is lower than 32.768 kHz the RTC_TRIM_INT value is negative.
- If the frequency error is rounded to $-N*T_{32kHz}$ (where N is an integer number and T_{32kHz}=1/32768 [Sec]) the expected trimming field -N and the 32K_COUNTER reset value is 32767-N
- If the 32 KHZ clock frequency is higher than 32.768 kHz the RTC_TRIM_INT value is positive.
- If the frequency error is rounded to $+N*T_{32kHz}$ (where N is an integer number and
- T_{32kHz}=1/32768 [Sec]) the expected trimming field +N and the 32K_COUNTER reset value is 32767+N
- The minimum error that can be corrected with the integer trimming is: $T_{INT\ minimum\ error}$ $=(\pm 1cycle*T_{32kHz})/(32768cycles*T_{32kHz})=\pm 30.517ppm$
- The maximal error that can be corrected with the integer trimming is: $T_{INT\ maximum\ error}$ = $(\pm 2\text{^}9_{cycles}*T_{32kHz})/(32768_{cycles}*T_{32kHz})= \pm 1.56\%$

RTC_TRIM_FRAC is a 10 bit field that periodically deletes clocks cycle from the integer counter (32K_COUNTER). The period, called the trim interval, is hard wired to be (2^10-1) seconds (approximately 17 minutes). Every (2^10-1) seconds, the integer counter (32K_COUNTER) stops clocking for a number of clock cycles as the value of RTC_TRIM_FRAC.

- If this counter is programmed to a zero, then no trim operations will occur and the RTC will be clocked with the raw 32 kHz clock
- The fractional trimming can correct frequency errors to the integer trimmed clock that cause the frequency to be higher than 32.768kHz
- The minimum error that can be corrected with the fractional trimming is:

  $T_{FRAC\ minimum\ error} = -(1_{LSBs}*T_{32kHz})/((2\text{^}10-1)*32768_{LSBs}*T_{32kHz})= -0.0298ppm$
- The maximal error that can be corrected with the fractional trimming is:

  $T_{FRAC\ maximum\ error} = -((2\text{^}10-1)_{LSBs}*T_{32kHz})/((2\text{^}10-1)*32768_{LSBs}*T_{32kHz})= -30.517ppm$

5.5. RTC Alarm

The PM813S RTC supports two different alarm events, set through the RTC_EXPIRE1 and RTC_EXPIRE2 fields. RTC alarm event occurs when the RTC_COUNTER is equal to RTC_EXPIRE1and RTC_ALARM_SET1='1', or when the counter is equal to RTC_EXPIRE2 and RTC_ALARM_SET2='1'. When this event occurs, the interrupt fields RTC_ALARM and RTC_ALARM_WU are set to '1'.

RTC_ALARM_WU rising edge generates a wakeup event (RTC_WU) if the PMIC is at 'Power-down' state. If the PMIC is in active state it generates an interrupt event (see 8.5.3).

The RTC_ALARM field is an indication to the host processor, that an RTC alarm had occurred, regardless of RTC_ALARM_WU state, which can be reset in case of power-up failure. The RTC_ALARM field is cleared only if it is actively set to '1' by the host processor I2C write or by clearing the corresponding interrupt bit.

In order to allow use of the I2C to read and write RTC_EXPIRE1and RTC_EXPIRE2 fields are divided to 4 fields of 8 bits each. Each RTC_EXPIRE1/2 field must be atomically written by the host processor from least significant byte to most significant byte.

An additional status field RTC_ALARM_STATUS indicates the occurrence of an RTC_ALARM outside of the power-down window. This field is automatically reset at each system power-down or by when the RTC_ALARM interrupt is cleared.

Table 27: RTC Alarm Fields Summary Table

RTC_ALARM	RTC_ ALARM_WU	RTC_ALARM_STATUS	RTC_INT	Comments
1	0	0	0	Alarm triggered during power-down, failing power-up
1	1	0	0	Alarm triggered during power-down, successful power-up
1	1	1	1 if RTC_INT_EN=1; 0 if other	Alarm triggered during power-up

6. Measurement Unit

6.1. Overview

The measurement unit consists of a 12-bit General Purpose ADC and 16-bit temperature sense that measures several external signals and internel signals.

It provides readings of:

- Various voltages in the system (system and up to two external signals)
- Up to two external resistances by using internal accurate current source
- PMIC internal temperature reading, battery ID, and battery temperature reading.

The measurement unit, when enabled, can work in three modes: single trigger, non-stop mode and duty cycled mode:

- Single trigger mode - in this mode the GPADC performs a round of measurements initiated by a triggering event. Defined single triggers events are of three types: I2C field SW_TRIG, charger insertion event or any GPIO if configured in trigger mode.
- Non-stop mode - In this mode, the GPADC continuously repeats the enabled measurements, to provide the required accuracy and fastest update rate of the desired measurements. Single trigger events are ignored in this mode.
- Duty cycled mode - The GPADC wakes up for a short period of time with a programmable duty cycle and measures the enabled measurements. Single trigger events are active in this mode, causing the GPADC to restart a measurement loop.

6.2. Input Channels

The measurement unit can measure the voltage of internal and external signals. Table 22 defines the input signals to the measurement unit. Variables to be measured are selected through the MEAS_EN fields for PMIC in active state and MEAS_EN_SLP fields for PMIC in sleep mode .

There is one General Purpose ADC (GPADC) that measures the voltage of the input signals. Each input can be muxed into the GPADC.

Table 28: General Measurement Unit Block Diagram

ADC channel	ADC input signal name	Signal range	Note	Default	Divider value

1	Buck1	0v to 1.6V	Buck1 output voltage.	1.15V	/2
2	Buck2	0V to 1.8V	Buck2 output voltage	1.8V	/2
3	Buck3	0V to 3.5V	Buck3 output voltage	1.1V	/3
4	Vbus	0V to 7V	VBus voltage	5V	/5
5	VBat	0V to 5V	Vbat voltage	3.6V	/5
6	Tint	0V to 1.3V	PMIC internal temperature		/1
7	BATID	0V to 1.3V	Battery ID voltage		/1
8	BAT_TEMP	0V to 1.3V	Battery temperature voltage		/1
9	GPADC0	0V to 1.3V	Voltage drop betwen GPADC1 and GPADC0. Typically for current sense detection.		/1
10	LDO1	0V to 3.3V	LDO1 output voltage	2.8V	/3
11	LDO2	0V to 3.3V	LDO3 output voltage	3.3V	/3
12	LDO3	0V to 3.3V	LDO4 output voltage	2.8V	/3
13	LDO4	0V to 3.3V	LDO4 output voltage	3.1V	/3
14	LDO5	0V to 3.3V	LDO5 output voltage	1.8V	/3
15	LDO6	0V to 3.3V	LDO6 output voltage	1.8V	/3
16	LDO7	0V to 3.3V	LDO7 output voltage	1.8V	/3
17	LDO8	0V to 3.3V	LDO8 output voltage	2.8V	/3
18	LDO9	0V to 3.3V	LDO9 output voltage	3.1V	/3
19	LDO10	0V to 3.3V	LDO10 output voltage	2.8V	/3
20	LDO11	0V to 3.3V	LDO11 output voltage	1.8V	/3
21	LDO12	0V to 3.3V	LDO12 output voltage	3.3V	/3
22	LDO13	0V to 3.3V	LDO13 output voltage	1.8V	/3
23	VPWR	0V to 5.6V	VPWR voltage	5V	/5
24	VRTC	0V to 3.5V	RTC LDO output voltage	3.0V	/3
25	AVdd18	0 to 1.98V	Internal regulator voltage for analog circuit	1.8V	/2
26	DVDD18	0V to 1.98V	Internal regulator voltage for digital circuit	1.8V	/2
27	VSUP5	0V to 5V	Internal crude regulator voltage	5V	/5
28	GPADC1	0V to 1.3V	GPADC1 input votlage (reserved)	1V	/1
29-31	Reserved				

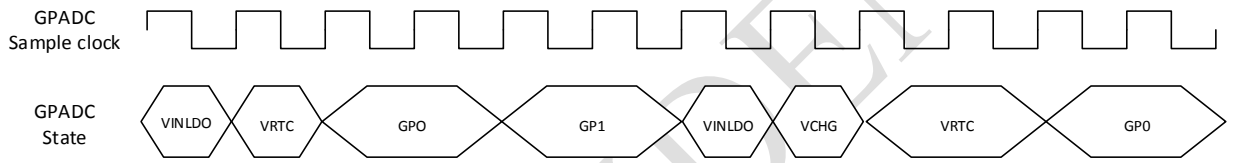
The table below also defines which input pins will include an internal bias to allow simple measurement of the load resistance of the input signal.

6.3. Operational Modes

6.3.1. Non-Stop Mode

In this mode the GPADC performs continuous measurements of the variables requested in a round robin fashion. This mode guarantees the fastest update rate of the desired variables at the cost of power consumption. This mode is enabled when the fields GPADC_EN and NON_STOP are both set.

Figure 17: Sample Non-Stop Timing Diagram1

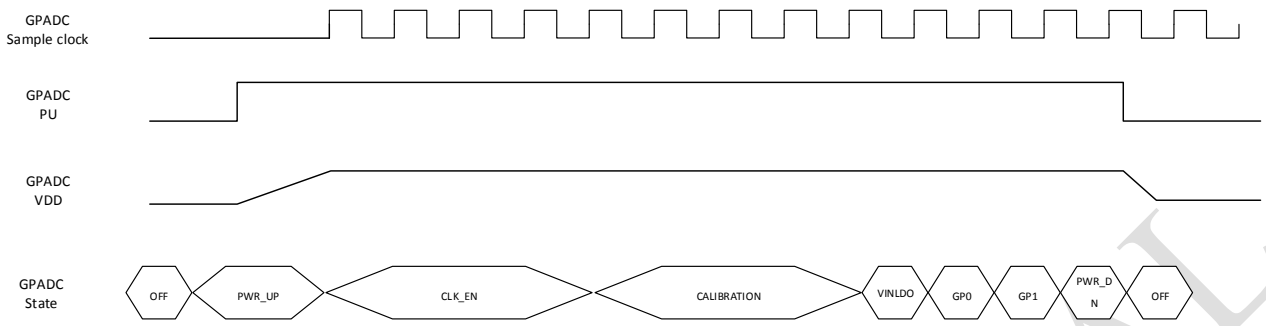


Duty Cycled Mode

When lower power consumption is desired, as it happens in sleep mode, the GPADC can be configured in a Duty Cycled mode. The GPADC wakes up periodically to perform the enabled measurements and turns off again. This is the default mode at power-up, and is enabled by setting the fields GPAD_EN = 1and NON_STOP = 0.

- The measurement unit wakes up and performs 20 sample clock periods of power-up and internal calibration.
- The enabled internal current sources turn on during the calibration sample periods and stay on until the measurement has completed.
- The enabled measurements are measured one after the other. The measurement unit turns off for programmable period of sample clock periods (MEAS_OFF_TIME field).

Figure 18: Sample Duty Cycle Timing Diagram1



6.4. Conversion Data Storage

Table 24 defines in which types of formats the data from each measurement can be read from the PMIC. The formats can be:

1. Last measurement reading
2. minimum value since last reading
3. Average value of the last four readings
4. Maximum value since last reading

Each measurement has its input range that is converted to full scale of the GPADC reading. The full scale number of bits is defined for each measurement field as detailed in Table24 .

Table 29: GPADC Conversion Formulas

Measurement	Range	Field	#Bits inRead	Conversion Formulas	ENOB (Typ)
VINLDO	0-5.6V	VINLDO_MEAS	12	Voltage[mV]=reading[lsb]*5*1.3[V]*1e3/(2^12)*128/129[lsb]	11
		VINLDO_AVG	12	Voltage[mV]=reading[lsb]*5*1.3[V]*1e3/(2^12) *128/129 [lsb]	
		VINLDO_MIN	12	Voltage[mV]=reading[lsb]*5*1.3[V]*1e3/(2^12) *128/129 [lsb]	
		VINLDO_MAX	12	Voltage[mV]=reading[lsb]*5*1.3[V]*1e3/(2^12) *128/129 [lsb]	
TINT	-30-140°C	TINT_MEAS	16	TINT[°C]=(Temp[15:6] *1.3/1.2*128/129 -273)℃	10
GPADC_IN0	0-1.3V	GPADC0_MEAS	12	Voltage[mV]=reading[lsb]*1.3[V]*1e3/(2^12) *128/129 [lsb]	11
GPADC_IN1	0-1.3V	GPADC1_MEAS			

Some of the measurements (VINLDO, TINT and GPADC0-1) include programmable upper and lower thresholds. When the measurement is above the upper threshold or below the lower threshold level (the threshold levels are programmable) an interrupt is asserted (Interrupt Events).

6.5. GPADC Electrical Characteristics

Table 30: GPADC Electrical Characteristics

The following applies unless otherwise stated: V_{IN} = VINLDO = 2.7V to 4.8V, -30°C < T_A < 85°C. Typical values are at T_A = 25°C.

Parameter	Condition	Min	Typ	Max	Unit
Supply			1.8		V
reference			1.3		V
Resolution			12		Bits
clock				800k	Hz
Conversion speed				50k	Hz
Input cap			1.8		pF
INL			±5		LSB
DNL			±2		LSB
Offset	1-sigma		2.3		LSB
gain			129/128		

ADC output code formula:

Code=Vin/Vref*4096*129/128

thus:

Vin=Code/4096*Vref*128/129

6.6. Differential voltage measurement for current sense

GPADC channel 9 is a differential input channel. The input is the votlage drop between GPADC1 and GPADC0.

If GPADC1>GPADC0, the measured output is positive.

If GPADC1<GPADC0, the measured output is negiatve.

Diffrerential channel (Channel 9) has a test mode. In test mode the differential inputs are short and measurement is done to get the differential channel offset. This measured offset could be used to cancel the offset when measure the input signals to get more accurate result.

Differential channel LSB is 0.65/2048*128/129=0.3149mV.

The output code vs. differential voltage is:

Table 31: Differential input voltage vs. code

Code	Voltage
000	-2048 LSB
001	-2047 LSB
…	…
7FD	-3 LSB
7FE	-2 LSB
7FF	-1 LSB
800	0 LSB
801	1 LSB
802	2 LSB
803	3 LSB
…	…
FFF	+ 2047 LSB

6.7. IDAC for measurement

In ASR PM813S there are 4 GPADC input pins (pin GPADC0, GPADC1, BAT_ID, BAT_TEMP). Each pin is configured with an IDAC. The IDAC's ouput range is from 1uA to 76uA with 5uA a step. In typical applicaton an external resistor is connected between the pin and ground. The resistor value could be calculated by GPADC measured pin voltage and IDAC's current setting. Usually pin GPADC1 and GPADC0 are configured for differential voltage measurement current sense. Pin BAT_ID is for battery ID measurement. Pin BAT_TEMP is for battery temperature measurement. The detail is described in the following figure. In application, set proper external resistor value to get the proper measuring range.

Figure 19: IDAC and GPADC input block

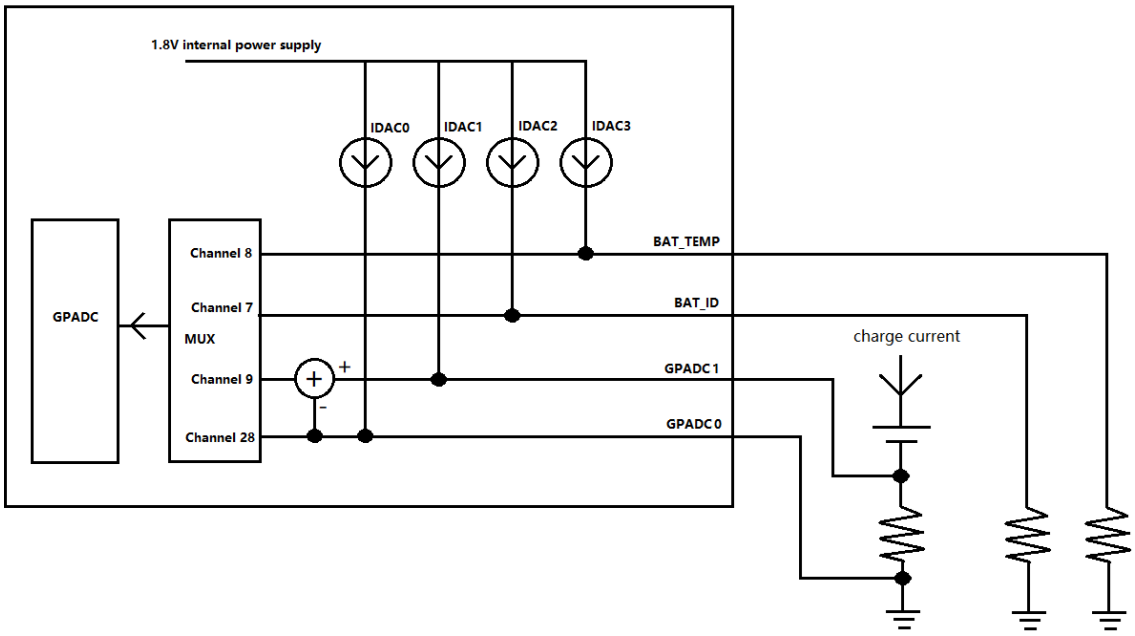


Table 32: GPADC input pin definition

GPADC0	GPADC1-GPADC0 differential voltage is configured to GPADC channel 9. Usually used for current sense.
GPADC1	Typically used with GPADC0 for differential voltage meassurement. Can also used as an independent measure channel (channel 28).
BAT_ID	BAT_ID is to detect battery ID and connected to PAD BAT_ID (channel 7)
BAT_TEMP	BAT_TEMP is to detect battery temperature and connected to PAD_TEMP (channel 8)

7. I2C Interface

7.1. I2C Overview

The I2C port supports Standard mode (up to 100 kHz), Fast mode (up to 400 kHz), and Fast mode plus (up to 1MHz). The I2C has internal pull-up resistors that automatically adapt to the interface speed, with a 5KΩ used in Standard and Fast modes.

7.2. I2C Device Address

The PM813S I2C bus 7-bit address ranges from 0[000]_000 to 0[000]_111. The three bits address in [] are OTP trim bits as {OTP0[39],OTP0[31],OTP0[23]}. In production it is trimmed to 110. The three least significant bits are used to select different internal devices, thus defining a field used throughout the register section called PAGE_ADDRESS, as shown in Table 27.

- Default slave write address is 0x60, 0x62, 0x64, 0x66, 0x68, 0x6A, 0x6C, 0x6E
- Default slave read address is 0x61, 0x63, 0x65, 0x67, 0x69, 0x6B, 0x6D, 0x6F

If a nonexistent I2C register address is read out, then PMIC returns data showing all zeros.

Page allocations are defined as follows:

Table 33: i2C Page Mapping

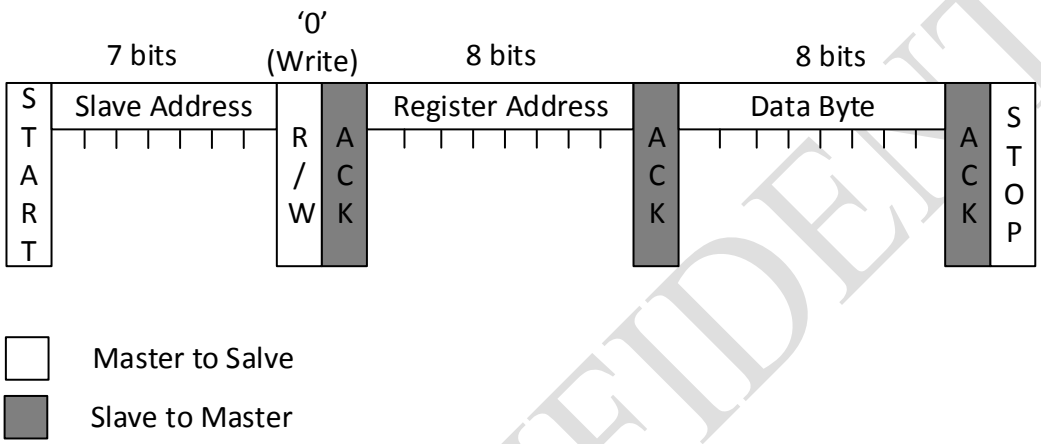
SLAVE ADDRESS [2:0] (PAGE_ADDRESS)	88PM813S PAGE SEL	Description
000	BASE	Contains all basic functions and misc functions including interrupts, status, fault, log, RTC, PWM, classD, oscillator references and low power related registers
001	POWER	Contains all buck and LDO related registers
010	GPADC	Contains all GPADC related registers
011	Reserved	
100	Reserved	
101	Reserved	
110	Reserved	
111	Test	

I2C Format

The following I2C formats are supported.

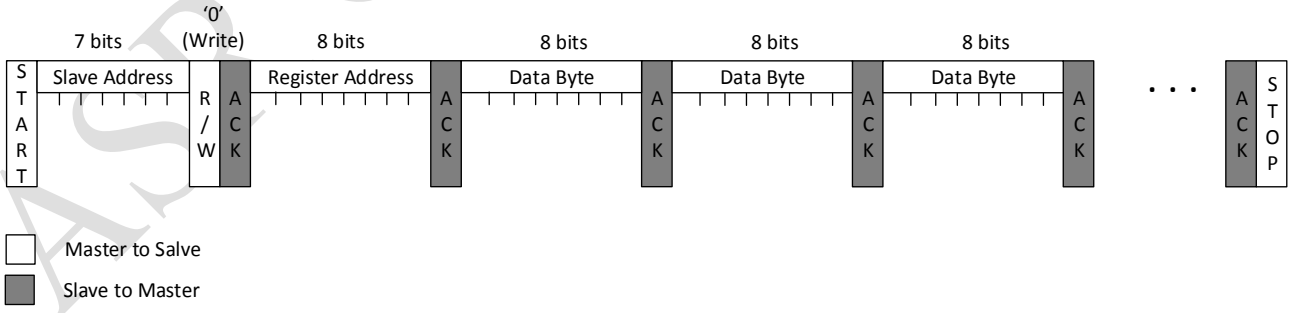
Master Write 1 Byte Format

Figure 20: Master Write 1 Byte Format



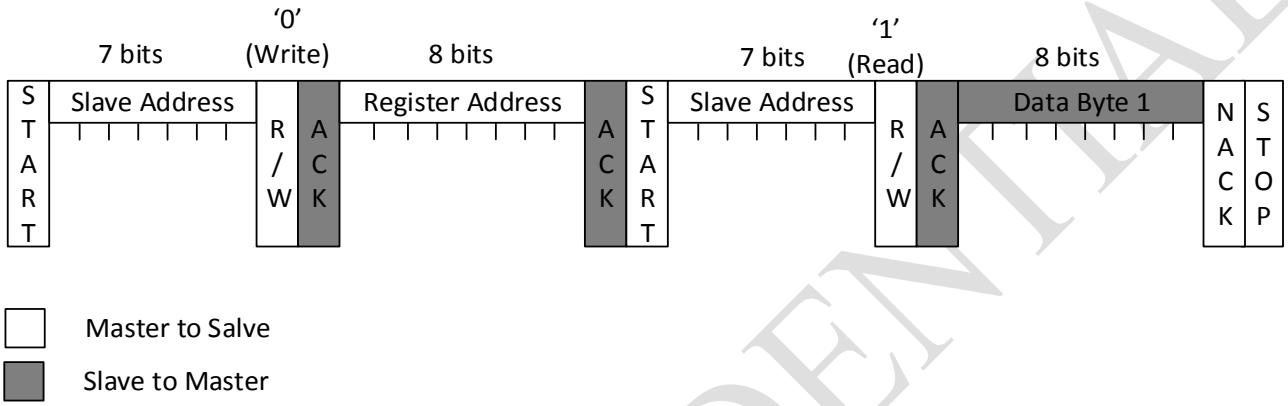
Master Write N Bytes Format

Figure 21: Master Write N Bytes Format



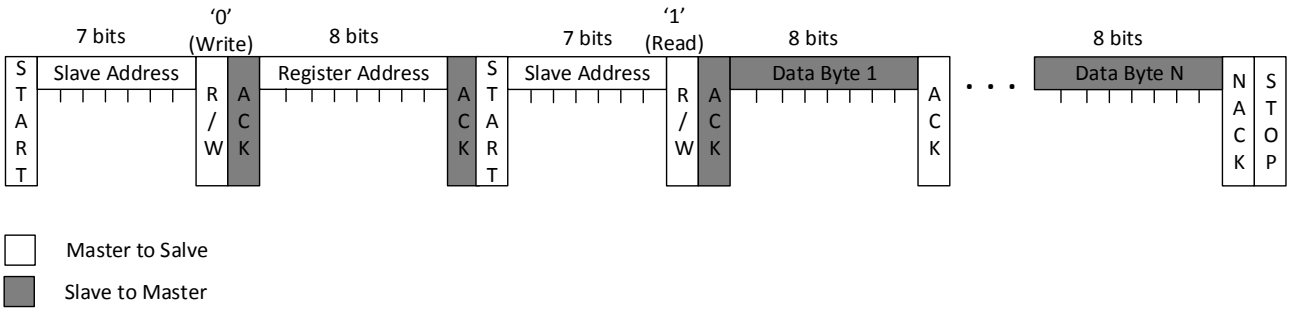
Master Read 1 Byte Format

Figure 22: Master Read 1 Byte Format



Master Read 1 Byte Format

Figure 23: Master Read N Bytes Format



8. Interface to Host Processor

8.1. Overview

The Power Management IC (PMIC) includes interface modes that work with ASR host processors.

In the PMIC there are several independent state machines.

The RTC section state machine, RTC State Machine

The main state machine, PMIC Main State Machine

8.2. PMIC Wake-up & Power-down Signals and Debounce Periods

There are three types of system events that can trigger the PMIC state machine:

- Wakeup events.
- Slow power-down events (PDOWN1): in case of power-down from 'active' state the power supplies are turned off in an orderly manner and allow a discharge time to the power supplies before any new wakeup event.
- Fast power-down events (PDOWN2): these events instantaneously turn off all power supplies, and allow a discharge time before any new wakeup event.
- Some wakeup and power-down signals are only valid if an external signal is stable for the duration of the debounce period.

Table 34: Wake-up and Power-down Events

Trigger Event	Type	Description	Digital Debounce Period Field
EXTON2	WAKEUP	EXTON2 input is asserted and the corresponding debounce timer is expired	EXTON2_DEBOUNCE
RTC_ALARM_WU	WAKEUP	Wakeup event when the one of RTC counters is enabled and expired	N/A
EXTON_WU	WAKEUP	EXTONn input is asserted and the corresponding debounce timer is	EXTON_DEBOUNCE

		expired	
ONKEY_WU	WAKEUP	When ONKEYn input is asserted and the corresponding debounce timer is expired	ONKEY_DEBOUNCE
SW_PDOWN_DETECT	PDOWN1	Normal power down sequence is initiated by software	N/A
LONG_ONKEY_DETECT1	PDOWN1	Occurs when ONKEYn is pressed (asserted low) and held for more than 8 seconds (default) if the corresponding detect enable register is enabled. A	LONKEY_DEBOUNCE
LONG_ONKEY_DETECT_RTC	PDOWN1	Occurs when ONKEYn is pressed (asserted low) for 4 seconds longer than LONG_ONKEY_DETECT1, causing the entire RTC digital domain to reset except the RTC counter itself, RTC alarms and RTC counter trimming registers.	N/A
WD_DETECT	PDOWN1	Watchdog timer is expired	N/A
OV_VSYS_DETECT	PDOWN1	Over Voltage is detected at the VINLDO power pin	N/A
UV_VSYS1_DETECT, UV_VSYS2_DETECT	PDOWN2	Under Voltage threshold 1 or threshold 2 is detected in VINLDO power input pin	N/A
PGOOD_PDOWN_DETECT	PDOWN1	A drop on the PMIC internal digital supply regulator input has been detected	N/A
OVER_TEMP_DETECT	PDOWN1	PM813S silicon junction temperature is over the limit	N/A
FAULT_WU	WAKEUP	When enabled, the PM813S will wakeup from power down events right away without any additional trigger	N/A
EXTON2_PD	PDOWN1	When enabled, the PM813S will power down if exton2 pad has a high to low transition	N/A
VBUS_DETECT	WAKEUP	When vbus_detect=1 (VBUS is detected to be >4.4V) and the PMIC is in power down mode, then it generate a wakeup event.	N/A

8.2.1. Debounce Period

When one of the wakeup external signals EXTON2, ONKEYn, EXTON1N is asserted active, two debounce mechanisms are in effect in order to define the signal as active.

The first debounce mechanism is analog in nature. It is an analog debounce circuitry that is relevant for all cases and required for the PMIC core LDO stabilization time, that is only applicable when the PMIC is at power-down state.

The second debounce mechanism checks whether the wakeup external signal is still valid after a time counting period of DB2 (programmable digital debounce delay). If the signal is still valid, then the PMIC defines the signal as passing the debounce period, and as stable. If a signal is defined as stable, then in the general state machine this wakeup signal can cause a change from 'POR&DB' state to 'check' state.

Table 35: Debounce Electrical Characteristics

The following applies unless otherwise stated: V_{IN} = VINLDO = 2.7V to 4.8V, -30°C < T_A < 85°C. Typical values are at T_A = 25°C.

Parameter	Conditions	Min	Typ	Max	Units
DB1 (Analog Debounce and Core LDO stabilization)	State = ’Power-down’		525		µs
	State other than ‘Power-down’		0		ms
	ONKEY_DEBOUNCE fields nominal length				
	Accuracy	-15		15	%
	Accuracy	-32		32	kHz

8.3. RTC State Machine

When there is sufficient voltage to supply the RTC domain (VAON higher than VRTC_MIN_TH) the RTC section turns on and performs POR.

In the 'RTC' state PMIC blocks RTC counter and logic and 32K_XO are active in this state. This state has an extremely low current consumption

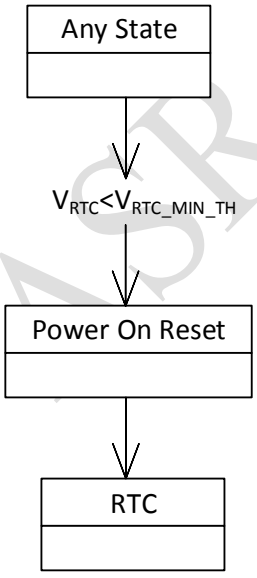
The supply to the RTC domain is from VAON pin.

LDO RTC is active and supplies regulated voltage in VAON pin if its input voltage (VINLDO pin) is higher than its output voltage (VRTC pin). If VAON pin voltage is higher than VINLDO pin there is no leakage current via LDO RTC.

The following activities are performed in the transition through the Power-On-Reset state in the RTC state Machine:

- Perform power on reset on RTC logic and RTC domain registers (register addresses 0xD0 to 0xEF)
- Turn on the 32K XO (for the 32K_XO clock to be used by the RTC block, the field USE_XO must be set by the host processor)
- Reset RTC counter to zero and activate the counter
- Set the RTC event field in the fault log register, RTC_RESET_EVENT = '1', to indicate that a reset had been performed on the RTC counter.

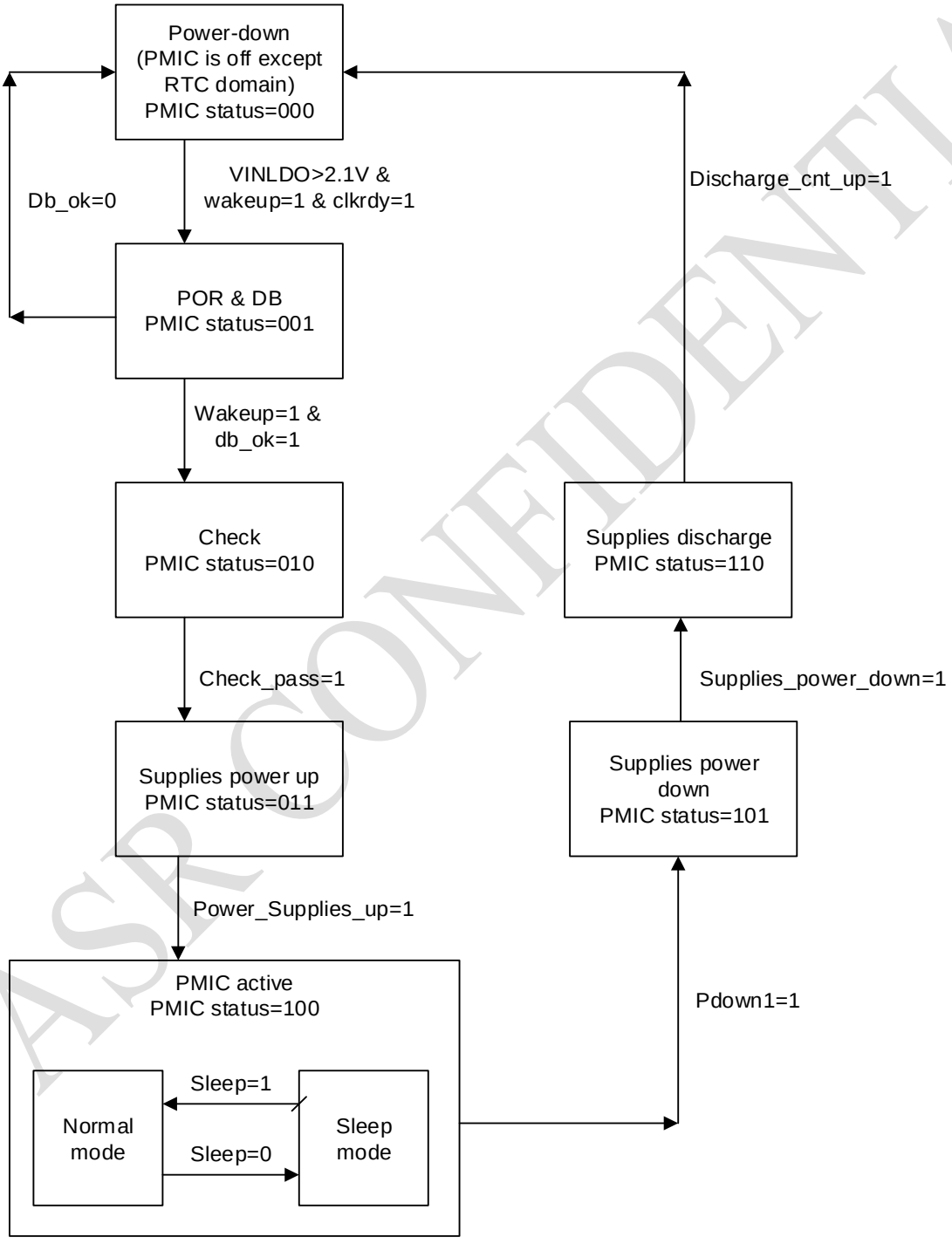
Figure 24: RTC State Machine



8.4. PMIC Main State Machine

The main state machine, shown in Figure 18, defines the main functionality of the interface signals and the PMIC blocks, except the RTC section that is controlled by the independent RTC state machine.

Figure 25: PM813S Main State Machine



8.4.1. Power-down State

In 'power-down' state the PMIC monitors for a wakeup event.

In the main state machine PMIC blocks LDO RTC and wake-up logic (monitors the pins VINLDO, EXTON2, ONKEYn, EXTONn) are active in this state.

8.4.2. POR&DB State

In 'POR&DB' state the PMIC performs POR on the main state machine and initialization activities. The PMIC does not continue the power-up process until it verifies that the wakeup signal is valid after a debounce period.

8.4.3. Check State

In 'check' state the PMIC monitors the internal temperature, input voltage VINLDO. The PMIC does not continue the power-up process until the specified conditions are met as in Figure 18, “PM813S Main State Machine.

If the main battery is below the threshold that will guarantee a successful power-up of the host processor, the PMIC will return to ‘power-down’ state.

In 'check' state the watchdog timer is activated in this state.

8.4.4. Supplies Power-up State

In 'supplies power-up' state the PMIC turns the supplies required to power-up the host processor. The supplies that turn on (buck converters and LDOs) and their turn on timing can be trimmed by OTP. Each LDO and buck that is enabled (LDOx_En, BUCKx_En) is turned on according to its turn on timing sequence.

Table 36: Supplies Power-up Timing

Time Interval	Min	Typ	Max	Unit	Description
TG		1		ms	Delay between each supplies group turn on time (assuming ±10% error on the clock frequency)
TG up total		7		ms	Total time from transition into ‘supplies power-up’ state until all enable supplies are turned on
Total number of startup groups		7			

Guaranteed by design. Not production tested.

8.4.5. Active State

In 'active' state the supplies to the host processor are turned on and the host processor can take control of the PMIC functionality through I2C writes. The first writes expected in active state are:

- Reset the watchdog
- Switching to XO clock as soon as XO is ready
- Program buck3 into APT mode

8.4.6. Supplies Power-down State

In 'supplies power-down' state the PMIC turns off the supplies in an orderly manner.

Upon entering the 'supplies power-down' state the supplies turn off in a reverse order to the supplies.

The time between each group turn off is ~30uS. At the end of the process all supplies except LDO RTC are off.

Table 37: Supplies Power-down Timing

Time Interval	Typ	Unit	Description
TG	30	us	Delay between each supplies group turn off time (assuming ±10% error on the clock frequency)
TG down total	210	µs	Total time until all supplies are turned off
Total number of turn off groups	7		

Guaranteed by design. Not production tested.

8.4.7. Discharge State

If all supplies (except LDO RTC) were not already turned off they are turned off (all of them at the same time).

The DISCHARGE_COUNTER is initiated to DISCHARGE_WAIT time (typically 2 Seconds).

The DISCHARGE_COUNTER Starts counting the timer down and waits in 'discharge' state until the DISCHARGE_COUNTER expires. The 'discharge' state enables all the power supplies to discharge.

8.4.8. Normal and Sleep mode

Normal mode and Sleep mode are part of PMIC active state. In normal mode, PMIC supports SOC to provide heavy current load. In sleep mode it is used to support light current load. Sleep mode is entered by falling edge of SLPN signal in PMIC active state.

8.5. Interface Signals to Host Processor

8.5.1. RSTn Signal

The RSTn signal initiates the host processor reset process. Initial value of RSTn in the RTC state Machine POR is '0'.

- The trigger to count the RESET_OUT_DELAY and then raise RSTn is the transition between ‘supply power-up’ state and ‘active’ state.
- RSTn falls low whenever the PMIC enters one of the power-down states ('supplies power-down' or 'discharge' or 'power-down')

Table 38: RESET_OUTn Signal

RESET_OUTn	Condition
Rising Edge	its rising edge is delayed, by the delay time defined in field RESET_OUT_DELAY (0-15 mSec), from the transition between ‘supplies power-up’ state and 'active' state
Falling Edge	state = 'supplies power-down' or 'discharge' or 'power-down'

8.5.2. CLK_32K Signal

PM813S has one 32 kHz output buffer. Each buffer can output either a '0', a 32 kHz free running clock, 32 kHz XO clock or HiZ. The output mode selection is performed through the 32K_OUT1_SEL fields.

The output signal of the CLK_32K buffers is defined in register map.

Table 39: CLK_32K_OUT1 Output Signal

Output	Condition		
CLK_32K Signal	**32K_OUT1_SEL Field**	**RSTn Singal**	**USE_XO Field**
'0'	xx	0	x
'0'	00	1	x
32.768kHz clock from the 32K free running oscillator	01 or 10	1	0
32.768kHz clock from 32K XO	01 or 10	1	1
Hi-Z	11	1	x

The setting of the field 32K_OUT_SEL is kept in 'power-down' state. It resets to its default only in RTC POR.

When the host processor has not written an indication that the 32K XO is settled (USE_XO = '0') then setting the field 32K_OUT_SEL = '01' will not output the 32K XO, but will output the internal free running clock.

8.5.3. PMIC_INTn Signal

The PMIC_INTn output signal is used to indicate that the PMIC needs to communicate an event or data to the host processor. The PMIC_INTn signal is active.

The complete list of interrupt events is described in Interrupt Events .

When the PMIC is in 'active' state and one or more of the enabled interrupt events are triggered, the PMIC_INTn signal is asserted low until all the interrupt event fields had been cleared via I2C (see Interrupt Events).

8.5.4. SLPn Signal

The SLPn signal when asserted low ('0') by the host processor, can change the mode of each power supply (LDO or buck), depending on its I2C settings, allowing each supply if desired to enter a low power consumption mode. This reduces significantly the PMIC quiescent current. The pin has an internal 50kΩ pull down. It can also modify automatically the GPADC duty cycle. SLPn signal de-assertion to high level ('1) is an indication to the PMIC to return to the normal mode of the power supplies and GPADC (same operational mode as before the SLPn assertion).

SLPn can rise high as soon as any of the PMIC supplies are turned on in the 'supplies power-up' state.

8.5.5. DVC1 and DVC2 Signals

The PM813S features Dynamic Voltage Control (DVC) on regulated supply Buck1. The host processor controls the DVC settings through pins DVC1 and DVC2. It has 4 dedicated voltage set control registers, selected by the value applied on the DVC1 and DVC2 pins, as represented in Table 34.

DVC1 and DVC2 are expected to be connected directly to host processor GPIO pins. This allows the fastest possible voltage selection change as there is no serialization (for example through I2C write) of the DVC change command. Default values of the four DVC registers for each supply are identical. DVC is activated after the power-up sequence has completed (PMIC main FSM in ACTIVE state) as they are gated by the POWER_HOLD field, so any value applied to the DVC1 and DVC2 pins is ignored before the host processor sets the POWER_HOLD field.

A simple deglitch mechanism based on matching two consecutive DVC1/DVC2 values as sampled by the internal 3MHz digital system clock avoids false DVC transitions. The DVC1/DVC2 pins control also the Buck1 power stage as configured through the BK1_DVC_DRIVE[1:0] fields. This allow fine grain buck efficiency optimization following each DVC1/DV2 pin setting.

Table 40: DVC Mapping

DVC2	DVC1	BUCK1
0	0	VBUCK1_SET0[6:0]
0	1	VBUCK1_SET1[6:0]
1	0	VBUCK1_SET2[6:0]
1	1	VBUCK1_SET3[6:0]

8.5.6. LDOs and Bucks States

Each LDO and buck can change its state as a function of the supplies setting fields.

The different LDOs and bucks in active and low power mode are defined in Table 37 and Table 38 .In SOD the default of the supplies that should turn on as part of the power-up are set as LDOx_EN and BUCKx_EN as '1'. The others supplies are set as '0' in default.

All these supplies are set by default as LDOx_SLEEP and BUCKx_SLP as '11' to guarantee these supplies will turn on in their active state regardless of the SLPn signal state. The voltage settings in the default for VLDOx_SET and VLDOx_SET_SLP are equal as well for these supplies.

LDO RTC is active all the time (when there is a valid VINLDO voltage). In 'active 'state the host processor can change the sleep fields settings.

Buck active, disabled and sleep modes are described in Supply Buck Converters. (PWM and PFM modes). LDO active, disabled and sleep modes are described in Supply LDOs.

Buck1 has DVC capability controlled through pins DVC1 and DVC2 as described in DVC1 and DVC2 Signals.

Note:

- Each LDO in sleep mode can supply at least 1mA (**See Supply LDSs**)
- Each buck in sleep mode can supply at least 5mA (**See Supply Buck Converters**)

Table 41: LDO Modes and Voltage Setting

LDOx_EN Field	SLPn Signal	LDOx_SLEEP Field	LDOx State
0	x	xx	LDOx is off
1	Rising	xx	LDOx is active (not in LDO sleep mode). Voltage is set as VLDOx_SET field (LDO1 will follow DVC pins as described in Table 36)
1	Falling	00	LDOx is off
1	Falling	01	Reserved state (LDOx is on)
1	Falling	10	LDO sleep mode. Voltage is set as VLDOx_SET_SLP field
1	Falling	11	LDOx is active (not in LDO sleep mode). Voltage is set as VLDOx_SET field

Table 42: BUCK modes and Voltage settings

BUCKx_EN Field	SLEEPn Signal	BUCKx_SLEEP Field	BUCKx State
0	X	xx	BUCKx is off
1	Rising	xx	BUCKx is active (PWM or PFM mode). Voltage is set as VBUCKx_SET field (Buck1 and 4 will follow DVC pins as described in Table 36)
1	Falling	00	BUCKx is off

1	Falling	01	BUCKx is active (automatic selection between PWM or PFM mode). Voltage is set as VBUCKx_SET_SLP field when SLPN = '0'.
1	Falling	10	BUCK sleep mode. Voltage is set as VBUCKx_SET_SLP field
1	Falling	11	BUCKx is active (automatic selection between PWM or PFM mode). Voltage is set as VBUCKx_SET field when SLPN = '0'

8.6. Watchdog Timer

The watchdog timer is enabled in 'check' state and loaded with the timer value as per WD_TIMER_ACT[2:0] field.

Every time that the host processor writes a '1' into the field WD_RESET the watchdog timer is re-triggered and WD_EXPIRE is set to the time defined by the field WD_TIMER_ACT.

Each time the SLPN pin toggles, the watchdog is automatically re-triggered, loading the WD_TIMER_ACT field timer on the SLPN rising edge transitions and the WD_TIMER_SLP field timer on the SLPN falling edge transitions. If the watchdog counter reaches zero, then an event called WD_DETECT is set (set to 1).

The WD_DETECT event (WD_DETECT rise to '1') causes the PMIC to enter into 'power-down' state from any state that the PMIC was.

Upon entering 'power-down' state the WD_DETECT event is cleared to '0' and the watchdog timer is not triggered (watchdog timer is not counting) until the PMIC enters the 'check' state.

Table 43: Wacth dog timer setting

WD_TIMER_ACT[3:0]	4'd0: 1 x 1024ms 4'd1: 2 x 1024ms 4'd2: 4 x 1024ms 4'd3: 8 x 1024ms 4'd4: 16 x 1024ms 4'd5: 32 x 1024ms 4'd6: 48 x 1024ms 4'd7: 64 x 1024ms 4'd8: 96 x 1024ms 4'd9: 128 x 1024ms 4'd10: 192 x 1024ms 4'd11: 256 x 1024ms
WD_TIMER_SLP[1:0]	2'b00: same as active 2'b01: 4x active 2'b10: 8x active 2'b11: 16x active

8.7. Analog Threshold Levels

Throughout the document there are different references to threshold levels of dedicated comparator circuitry in the PMIC. This next table summarizes all these threshold levels and their tolerances. Several timing counters are also detailed in this table with their tolerances.

The following applies unless otherwise stated: V_{IN} = VINLDO = 2.7V to 4.8V, -30°C < T_A < 85°C. Typical values are at T_A = 25°C. Refer to schematic shown in Figure3

Table 44: Interface to Host Processor Analog Threshold Levels Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units
VRTC_MIN_TH	Minimum voltage to operate the RTC state machine. Located in the RTC domain and active even in 'power-down' state. PMIC power down is forced when VRTC is below this threshold (see RSTn Signal) and to reset the RTC state machine.		1.8		V

VSYS_UNDER_RISE_TH1	Threshold for PMIC power-up when VINLDO is rising. Minimum voltage to operate the general state machine. Located in the reference group and is not active in 'power-down' state		2.6		V
VSYS_UNDER_FALL_TH1	Threshold for VINLDO under-voltage (UV_VSYS) event when VINLDO is falling. Minimum voltage to operate the general state machine. If VINLDO falls bellow it the PMIC powers down		2.5		V
VSYS_UNDER_RISE_TH2	Threshold for VINLDO under-voltage event when VINLDO is falling. If VINLDO falls bellow it the PMIC powers down		2.9V default, program-mable from 2.8		V
VSYS_UNDER_FALL_TH2	Threshold for VINLDO under-voltage event when VINLDO is falling. If VINLDO falls bellow it the PMIC powers down		2.8V default, program-mable from 2.8		V
VSYS_OVER_TH	Threshold for over-voltage power-down event (OV_VSYS). Programmable by OV_VSYS_SET field.		4.8		V
RSTn_PULSE	Delay in RSTn rising edge after long OnKey press		ONKEY_DB_SEL		ms
PMIC_INTn_PULSE	Pulse on PMIC_INT when not all status bits are cleared		6		ms
DISCHARGE_WAIT	Discharge timer initial value		2		Sec
TEMP_OVER_RISE_TH	Temperature rising		145		°C
TEMP_OVER_FALL_TH	Temperature falling		120		°C

9. Status and Interrupts

9.1. Power-up Log

The power-up log register retains a data log of any power-up event that triggers the PMIC wakeup and initialization of the power-up sequence. The power-up log can be accessed via register 0x10.

When the PMIC enters a Power-On Reset and Debounce (POR&DB) state, it stores data on the event that caused it to power-up in the power-up log register. Only one event would have caused the PMIC to power up.

The power-down-up register events are cleared every time the PMIC enters 'power-down' state .

Table 45: Power-up log

Event	Description
FAULT_WAKEUP	1=Power-up event is due to FAUT_WAKEUP event. This bit is cleared by writing a 1. Writing a 0 has no effect.
RTC_ALARM_WAKEUP	1=Power-up event is RTC_ALRAM expiry. This bit is cleared by writing a 1. Writing a 0 has no effect.
EXTON1_WAKEUP	1=Power-up event is ExtOn assertion low. This bit is cleared by writing a 1. Writing a 0 has no effect.
EXTON1N_WAKEUP	1=Power-up event is ExtOn1n assertion low. This bit is cleared by writing a 1. Writing a 0 has no effect.
ONKEY_WAKEUP	1=Power-up event is OnKey press. This bit is cleared by writing a 1. Writing a 0 has no
VBUS_WAKEUP	1=Power-up event is USB insertion. This bit is cleared by writing a 1. Writing a 0 has no effect.

9.2. Power-down Log

The power-down log register contains data of power-down events and RTC counter error.

When the PMIC enters a power-down state, the reason it powered down is recorded in one of the power-down log register fields located in base page registers 0xE5 and 0xE6. There could be only one event that caused the PMIC to enter the last power-down state in the main state machine.

The power-down log register events are updated each time the PMIC enters a power-down state. Its field contents do not change in the power-down state.

Table 46: Power-down log

Event	Description
LONG_ONKEY_EVENT	1=Entrance to 'power-down' state caused by long press of ONKEY
WD_EVENT	1=Entrance to 'power-down' state caused by PMIC watch dog expiry event
SW_PWDOWN_EVENT	1=Entrance to 'power-down' state caused by I2C write to field SW_PDOWN
OVER_TEMP_EVENT	1=Entrance to 'power-down' state caused by an internal over temperature in the internal PMIC temperature detector
UV_VSYS_EVENT	1=Entrance to 'power-down' state caused by VINLDO going lower than VSYS_UNDER_FALL_TH1 (such as battery removal without a connected charger)
OV_VSYS_EVENT	1=Entrance to 'power-down' state caused by VINLDO going above than VSYS_OVER_TH
UV_VSYS2_EVENT	1=Entrance to ‘power-down’ state caused by VINLDO going lower then VSYS_UNDER_FALL_TH2
RTC_CNT_ERROR	1=Entrance to ‘power-down’ state caused by VRTC falling below VRTC_MIN_TH
EXTON2_PDOWN EVENT	1=Entrance to ‘power-down’ state caused by EXTON2 turn to 0 when EXTON2 power down feature enabled
PGOOD_PDOWN EVENT	1=Entrance to ‘power-down’ state caused by PMIC internal digital supply voltage drop

9.3. Status Data

The status data fields contain the output of various detectors in the PMIC. Each field records the status of one of the pins of the PMIC. The value of the field changes when its relevant detector senses that the status of the pin has changed.

Table 47: Status Data

Status	Description
RTC_ALARM_CTRL	Indication of an RTC alarm event occurred outside of the power-down system state. 0 = no alarm event registered
BUCK_PGOOD	Indication that all the enabled buck supplies are within 5% (10%) of their target value on a rising (falling) supply voltage transient 0 = at least one buck supply is enabled and not within its target value
LDO_PGOOD	Indication that all the enabled LDO supplies are within 5% (10%) of their target value on a rising (falling) supply voltage transient 0 = at least one LDO supply is enabled and not within its target value
EXTON2_STATUS	Debounced status of the EXTON2 pin 0= EXTON2_DET = 0 1= EXTON2_DET = 1
ONKEY_STATUS	Debounced status of the ONKEYn pin 0=ONKEYn not pressed or not yet debounced. ONKEYn signal=’1’ 1=ONKEYn pressed.

EXTON1_STATUS	Debounced status of the EXTON1n pin 0=EXTON1n de-asserted or not yet debounced. EXTON1n signal=’1’ 1=EXTON1n
BAT_STATUS	Status of the BAT_DET signal 0=Battery is not present. BAT_DET signal='0' 1=Battery is present. BAT_DET signal='1'
VBUS_STATUS	Status of the VBUS_DET signal 0=VBUS is not present. VBUS_DET signal='0' 1=VBUS is present. VBUS_DET signal='1'

9.4. Interrupt Events

An interrupt event, as described in Table 41, results in the following:

- The PMIC signal PMIC_INTn is asserted low if the matching mask bit to that event in the interrupt mask registers is set to '1' (interrupt unmasked and enabled)
- The matching interrupt status bit in the Interrupt status registers is set to '1' unless INT_MASK_MODE field equals '0' and the matching mask bit to that event in the interrupt mask registers is set to '0' (interrupt masked and disabled)

The interrupt status bit and the PMIC_INTn signal are cleared by either of the following:

- Clear on Read. If the field INT_CLEAR_MODE=0, any of the interrupt status registers is cleared when it is read via the I2C port. The PMIC signal PMIC_INTn is de-asserted high when all the fields in the interrupt status registers are clear. If any interrupt status bit is still set after register INTERRUPT_STATUS is read, a short pulse, for the duration of PMIC_INT_PULSE, is asserted.
- Clear on Write. Any interrupt status bit is cleared by writing a '1' in this position.
- The PMIC signal PMIC_INTn is de-asserted high when all the fields in the interrupt status registers are clear.

Table 48: Interrupt Events

Interrupt	Description
ONKEY_INT	Field set to 1 when ONKEY pin input signal is rising high or falling low stays in that state for more than its debounce period
EXTON1_INT	Field set to 1 when EXTON1n pin input signal is rising high or falling low
EXTON2_INT	Field set to 1 when EXTON2_DET signal changes level
BAT_INT	Field set to 1 when BAT_DET signal changes level
RTC_INT	RTC alarm triggered
VINLDO_INT	VINLDO is exceeding either the upper or lower threshold range
TINT_INT	PMIC internal temperature (GPADC measurement) is exceeding either the upper or lower threshold range
GPADC0_INT	Differential voltage of GPADC1 and GPADC0 pin (typically for current sense) is exceeding either the upper or lower threshold range
GPADC1_INT	GPADC1 pin is exceeding either the upper or lower threshold range
VBUS_INT	Field set to 1 when VBUS_DET signal changes level
VBUS_OVP_INT	Field set to 1 when VBUS_OVP signal changes level
VBUS_UVLO_INT	Field set to 1 when VBUS_UVLO signal changes level
BAT_TEMP_INT	Field set to 1 when battery temperature is exceeding either the upper or lower threshold range
CP_START_DONE_INT	Field set to 1 when CP_START_DONE signal changes level
CP_START_ERROR_INT	Field set to 1 when CP_START_ERROR signal changes level
CLASSD_OCP_INT	Field set to 1 when CLASSD_OUT signal changes level

10. Class-D and Charge-pump

10.1.Class-D

10.1.1. Class-D overview

The Class-D consist of 2-stage filter, trig-wave generator, comparator and output driver; shown as Figure19. The input of Class-D is differential analog input, and with PWM out. The PWM frequency default is 625kHz, with the 2bit register CTRL_FREQ<1:0> for adjustment. The class-D has CTRL_SPD_EN to enable spectrum-spread function to reduce EMI. Register CTRL_SPD_RANGE can select week or strong spectrum-spread.

Class-D also has a Over-Current-Protection(OCP) function, when enable class-D, the OCP function should be also enable.

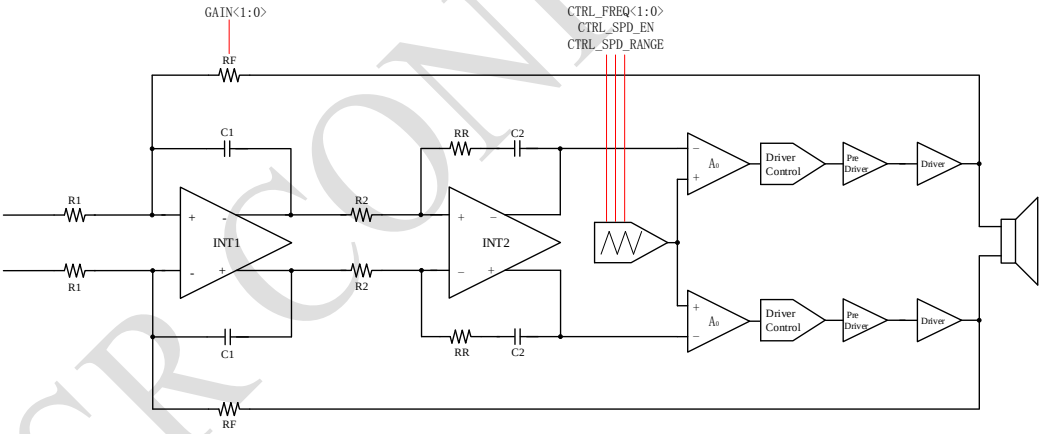
The class-D has 2bit register GAIN<1:0> gain option, we suggest to select high gain in higher power supply and select low gain in lower power supply to prevent cliping, as below.

PVDD=2.8~3.2V Gain<1:0>=00;

PVDD=3.2~3.6V Gain<1:0>=01;

PVDD=3.6~4.2V Gain<1:0>=10。

Figure 26: Overview of Class-D



10.1.2. Class-D SPEC

Table 49: Class-D Spec

Parameter	Condition	Min	Typ	Max	Unit
Supply(PVDD)			3~5		V
PWM frequency			625k		Hz

Dynamic Range			102.4		dB
SNR-peak	non-weighted @20~20kHz		98		dB
THD	@ output=6dBv PVDD=3.6V		-84		dB
Input Impedance			42k		ohm
Input common voltage		0.7	0.9	1.0	V
Gain	Gain<1:0>=00 Gain<1:0>=01 Gain<1:0>=10 Gain<1:0>=11		1.5 2 2.33 0		V/V
Max output power @THD=10%	PVDD=3.6 PVDD=4.2		0.7 1		W
Quiescent Current	AVDD+DVDD		782		uA
	PVDD		278		uA
	Total		1.06		mA

10.1.3. Regitster table of Class-D

Table 50: Class-D register table

Hex	Dec	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	default value
Identification										
		audio control								
30	48	SR				Ctrl_minimal_pulse		Gain		
		SR of output pulse. Time of output voltage from 0V to 4.2V (or 4.2V to 0) =1111, 10ns(Default) =1110, 20ns =1100, 35ns =1000, 50ns				Ctrl_minimal_pulse[1:0]. Default:11		Gain<1:0> =00, 1.5V/V =01, 2V/V (Default) =10, 2.33V/V =11, 0		8'b11111101
31	49	Reserved	PowerDown	Ctrl_spd_range	Ctrl_spd_en	Ctrl_freq		OCP_REST	ov_curr_prot	
		Reserved	1: PowerDown (Default) 0: PowerUp	Ctrl_spd_range 1: pwm_spd_strong (Default) 0: PWM_spd_weak	Ctrl_spd_en 1: Enable PWM_spd (Default) 0: Disable PWM_spd	Ctrl_freq<1:0> Frequency of triangular wave (PWM) =11, 710KHz =10, 625KHz (Default) =01, 625khz =00, 550KHz		OCP_REST = => 0V =>1.8V=>0V Defaut:0	Over current protection enable =1, enabled (Default) =0, disabled.	8'b00111001

10.1.4. Enable/disable sequence

- Enable Sequence

  1) set Gain<1:0>

  2) set OCP_REST=0; OCP_ENABLE=1

3) PD=0

- Disable Sequence

1) set PD=1

- OCP fucntion

If Over-current occur during Class-D operation, Class-D will self-protect; it will disable the output stage and generate an OCP_alram interrupt signal. If the user want to restart the class-D, you can set the OCP_REST=1. If the Over-current disappear, then the Class-D work normally, otherwise it will generate next OCP_alram interrupt signal and disable the output stage for self-protection.

10.2. Charge-pump

10.2.1. Charge-pump Overview

The charge-pump, which consists of SWITCH-array, SWITCH control logic, start done & oc detect, shown as Figure 11-2, supports two level positive and negative output voltage, +/-1.8V, +/-0.9V alternatively.

10.2.2. Charge-pump Application Diagram

Figure 27: Overview of Charge pump.

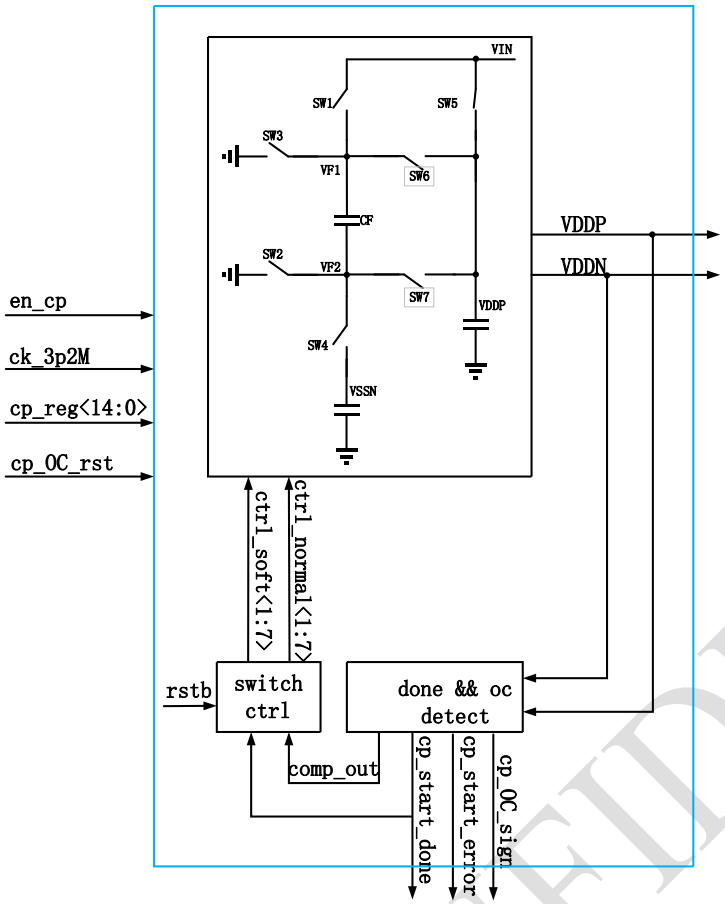
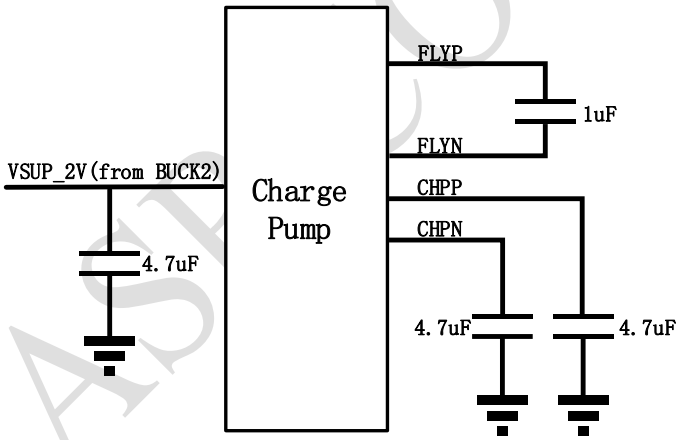


Figure 28: Charge-pump application diagram



10.2.3. Charge-pump Voltage Mapping

The positive and negative output voltage of charge-pump can be programmed by the registers of page 0 reg33,reg34. It lists in the following tables.

Table 51：Charge-pump CHPP mapping

page0 reg34 bit2:0	CHPP	
	page0 reg33 bit0=1'b0	page0 reg33 bit0=1'b1
000	1.8	0.98
001		0.96
010		0.94
011		0.92
100		0.9
101		0.88
110		0.86
111		0.84

Table 52: Charge-pump CHPN mapping

page0 reg33 bit6:4	CHPN	
	page0 reg33 bit0=1'b0	page0 reg33 bit0=1'b1
000	-1.96	-0.97
001	-1.92	-0.94
010	-1.88	-0.91
011	-1.84	-0.88
100	-1.8	-0.85
101	-1.76	-0.82
110	-1.72	-0.79
111	-1.68	-0.76

10.2.4. Charge-pump Spec

Table 53: Charge-pump Electrical Characteristics

The following applies unless otherwise stated: VIN=buck2= 2V, -30°C <TA<85°C.Typical values are at TA= 25°C.

Parameter	Conditions	Min	Typ	Max	Unit
VSUP_2V	from buck2		2		V
Cin	VSUP_2V capacitor		4.7		uF
Cfly	flying capacitor		1		uF
Cout	output capacitor		4.7		uF
CHHP	at +/-1.8V mode		1.8V		V
	at +/-0.9V mode		0.9		
CHHN	at +/-1.8V mode		-1.8		V
	at +/-0.9V mode		-0.9		

CHPP accuracy	at +/-1.8V mode, Iload=20mADC	-3		3	%
	at +/-0.9V mode, Iload=10mADC	-5		5	
CHPN accuracy	at +/-1.8V mode, Iload=20mADC	-3		3	
	at +/-0.9V mode, Iload=10mADC	-5		5	
CHPP load regulation	at +/-1.8V mode, Iload from 1mADC to 100mADC		0.021		%/mADC
	at +/-0.9V mode, Iload from 1mADC to 35mADC		0.03		
CHPN laod regulation	at +/-1.8V mode, Iload from 1mADC to 100mADC		0.025		
	at +/-0.9V mode, Iload from 1mADC to 35mADC		0.03		

10.2.5. Charge-pump Efficiency

Figure 29: Charge-pump Positive Output Voltage Efficiency at +/-1.8V Mode

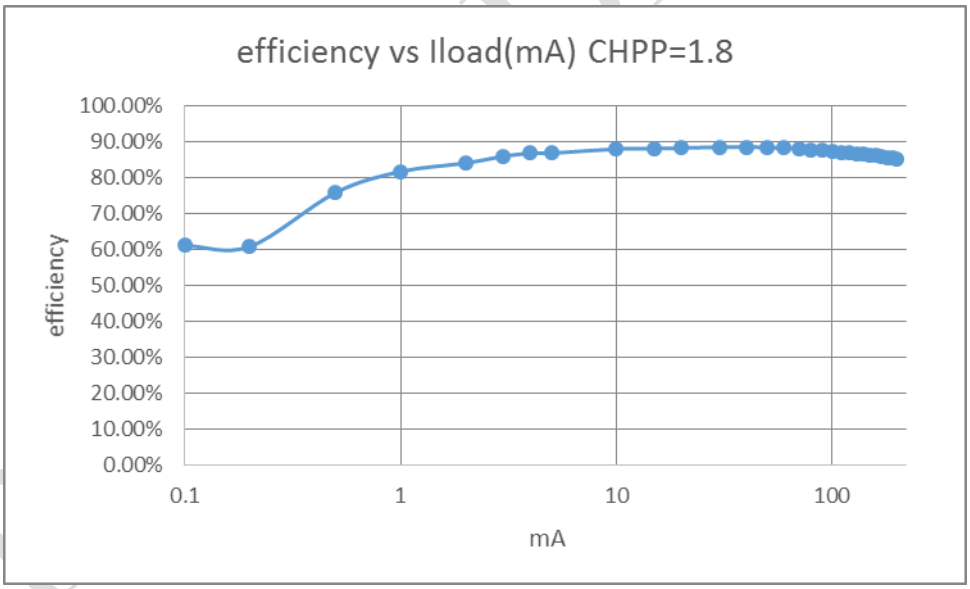


Figure 30: Charge-pump Negative Output Voltage Efficiency at +/-1.8V Mode

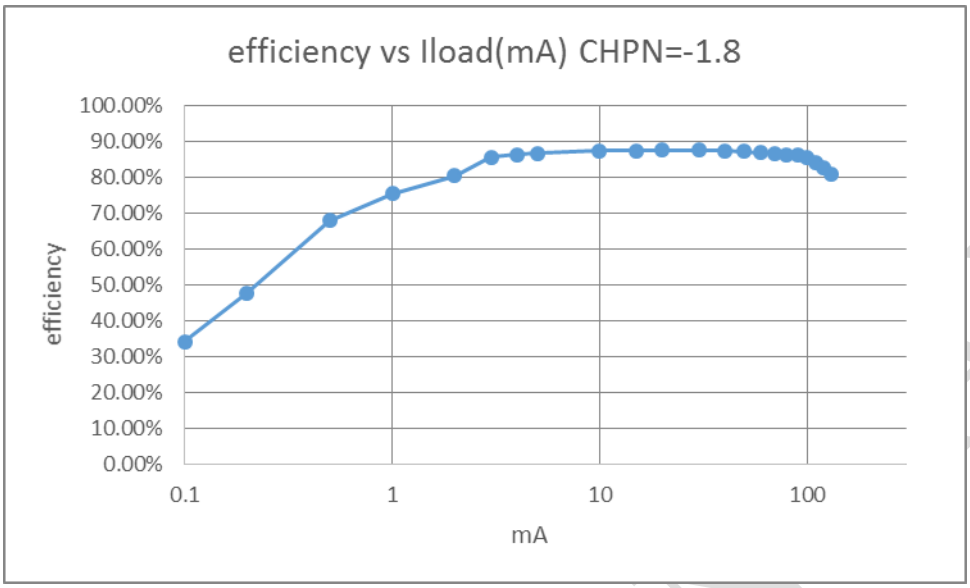


Figure 31: Charge-pump Positive Output Voltage Efficiency at +/-0.9V Mode

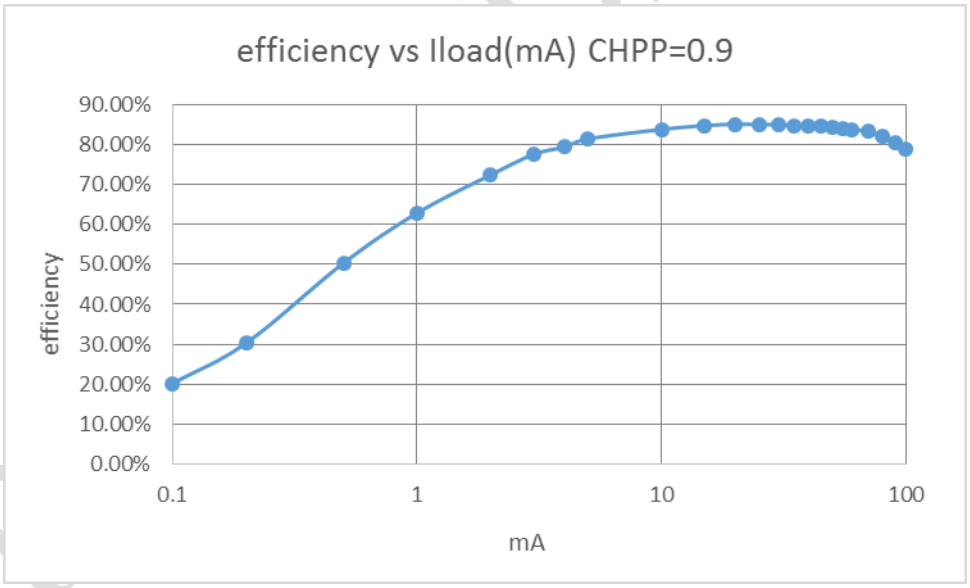
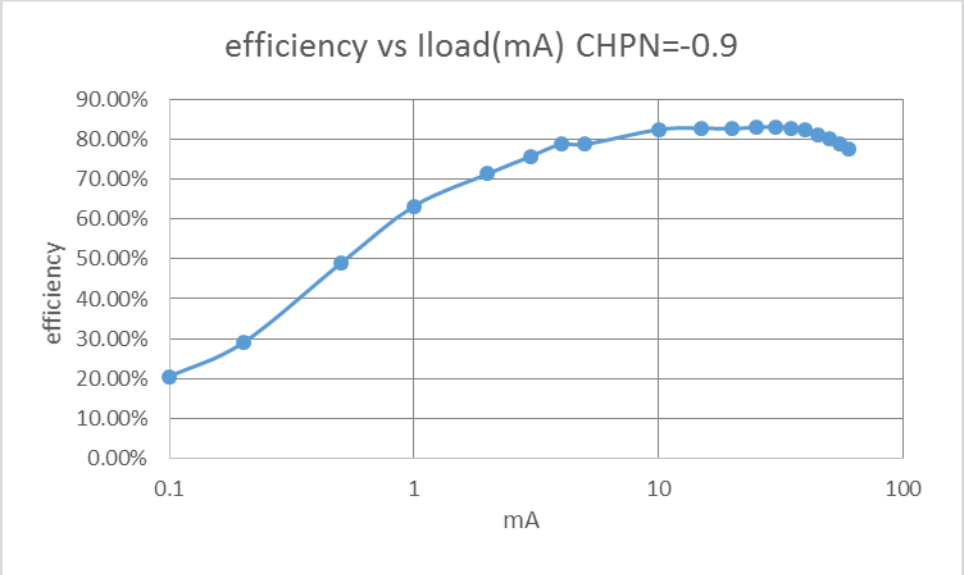


Figure 32: Charge-pump Negaive Output Voltage Efficiency at +/-0.9V Mode



10.2.6. Charge-pump Work Sequence

- Enable Sequence

  1) Make sure the potencial load current less than 20mA before charge-pump startup ok.

  2) Configure the registers from 0x33 to 0x35 to choose which work mode.

- Disable Sequence

  Set enable=0.

- Switch the ouput voltage: +/-0.9 vs +/-1.8

  Make sure the load current less than 37.5mArms before change the output voltage.

- OCP fucntion

If OCP occurred, charge-pump will shut down itself and give out the OCP alarm signal (cp_OC_sign). We need to set enable =0 first, and then set enable=1 to restart the charge-pump if we want to restart the charge-pump.

11. LED and vibrator driver

ASR PM813S supports backlight LED driver, key board LED driver, torch LED driver and vibrator driver

Table 54: LED and vibrator driver Summary

The following applies unless otherwise stated: V_{IN} = VINLDO = 2.7V to 4.8V, -30°C < T_A < 85°C. Typical values are at V_{IN}=3.6V, T_A = 25°C.

Parameter	Condition	Min	Typ	Max	Unit
Backlight BLEDn min current	duty cycle is 100%		0.75		mA
Backlight BLEDn max current	duty cycle is 100%		0.75*32		mA
Backlight BLEDn current step	duty cycle is 100%		0.75		mA
Backlight BLEDn driver duty cycle range			1/128 to 128/128		
Backlight BLEDn driver max frequency			25		kHz
Backlight BLEDn driver frequency selection			25/(1,2,4,8,16,32,64,128)		kHz
Keyboard LED current min value	duty cycle is 100%		2		mA
Keyboard LED current max value	duty cycle is 100%		64		mA
Keyboard LED current selection step	duty cycle is 100%		2		mA
Keyboard LED driver duty cycle range			1/128 to 128/128		
Keyboard LED driver max frequency			25		kHz
Keyboard LED driver frequency selection			25/(1,2,4,8,16,32,64,128)		kHz
Torch LED current min value	duty cycle is 100%		2		mA
Torch LED current max value	duty cycle is 100%		64		mA
Torch LED current selection step	duty cycle is 100%		2		mA
Torch driver duty cycle			1/128 to 128/128		

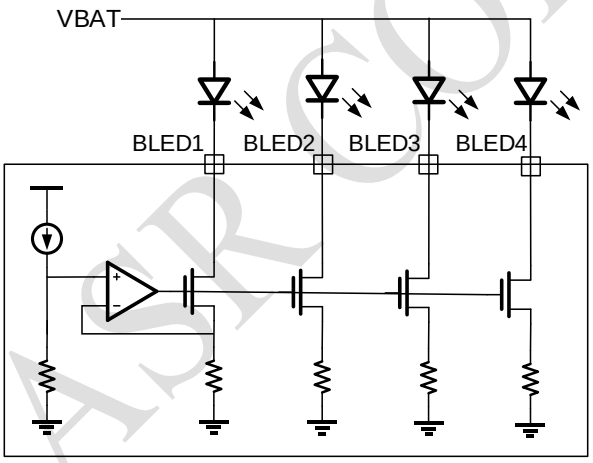
range					
Torch LED driver max frequency			25		kHz
Torch LED driver frequency selection			25/(1,2,4,8,16,32,64,128)		kHz
Vibrator driver on-resistance			0.8		Ohm
Vibrator driver duty cycle range			1/128 to 128/128		
Vibrator driver max frequency			25		kHz
Vibrator driver frequency selection			25/(1,2,4,8,16,32,64,128)		kHz

ASR PM813S has 4 current sink output for backlight LED on PIN BLED1, BLED2, BLED3 and BLED4. The channels BLED2, BLED3 and BLED4 matches with BLED1. These current sink dirvers can work with output votlage as low as 200mV. If BLED1,2,3,4 drops below 200mV, the BLED driver's output curent may decrease.

Each channel current is programmable from 0.75mA to 0.75mA*32 with step 0.75mA.

The BLED driver also supports PWM dimming function. The dimming frequency is programmable from 25kHz, 25kHz/2, 25kHz/4, 25kHz/8, 25kHz/16, 25kHz*/32, 25kHz/64 and 25kHz/128. The dimming duty cycle is programmable from 1/128, 2/128 … to 128/128. That is from 1/128 to 128/128 with step 1/128.

Figure 33: Backlight LED driver diagram

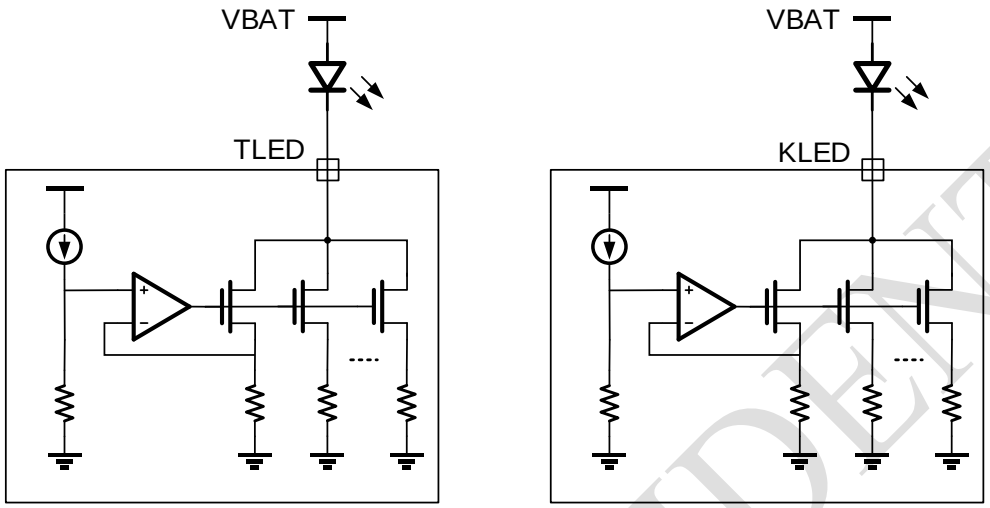


ASR PM813S has 1 current sink driver for TLED (Torch LED) and 1 current sink driver for KLED (Keyboard LED). These current sink dirvers can work with output votlage as low as 200mV. If TLED or KLED drops below 200mV, its output curent may decrease.

TLED and KLED have the same type of current sink driver. It supports 2mA to 64mA current output with 2mA a step.

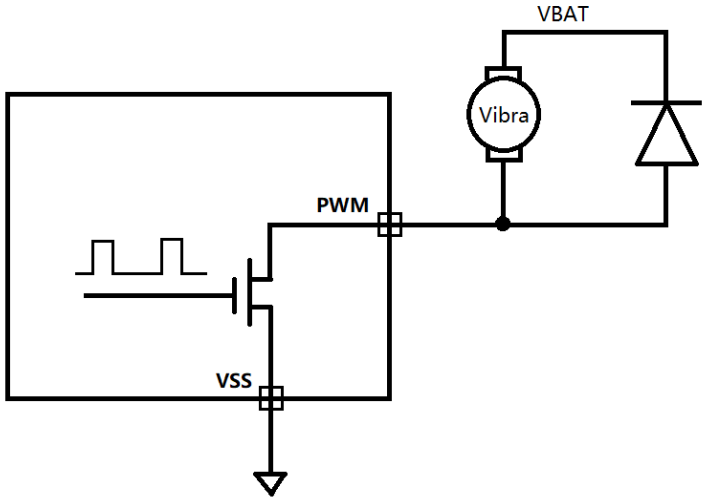
The TLED and KLED current sink driver also supports PWM dimming function. The dimming frequency is programmable from 25kHz, 25kHz/2, 25kHz/4, 25kHz/8, 25kHz/16, 25kHz*/32, 25kHz/64 and 25kHz/128. The dimming duty cycle is programmable from 1/128, 2/128 … to 128/128. That is from 1/128 to 128/128 with step 1/128.

Figure 34: Torch LED and Keyboard LED driver diagram



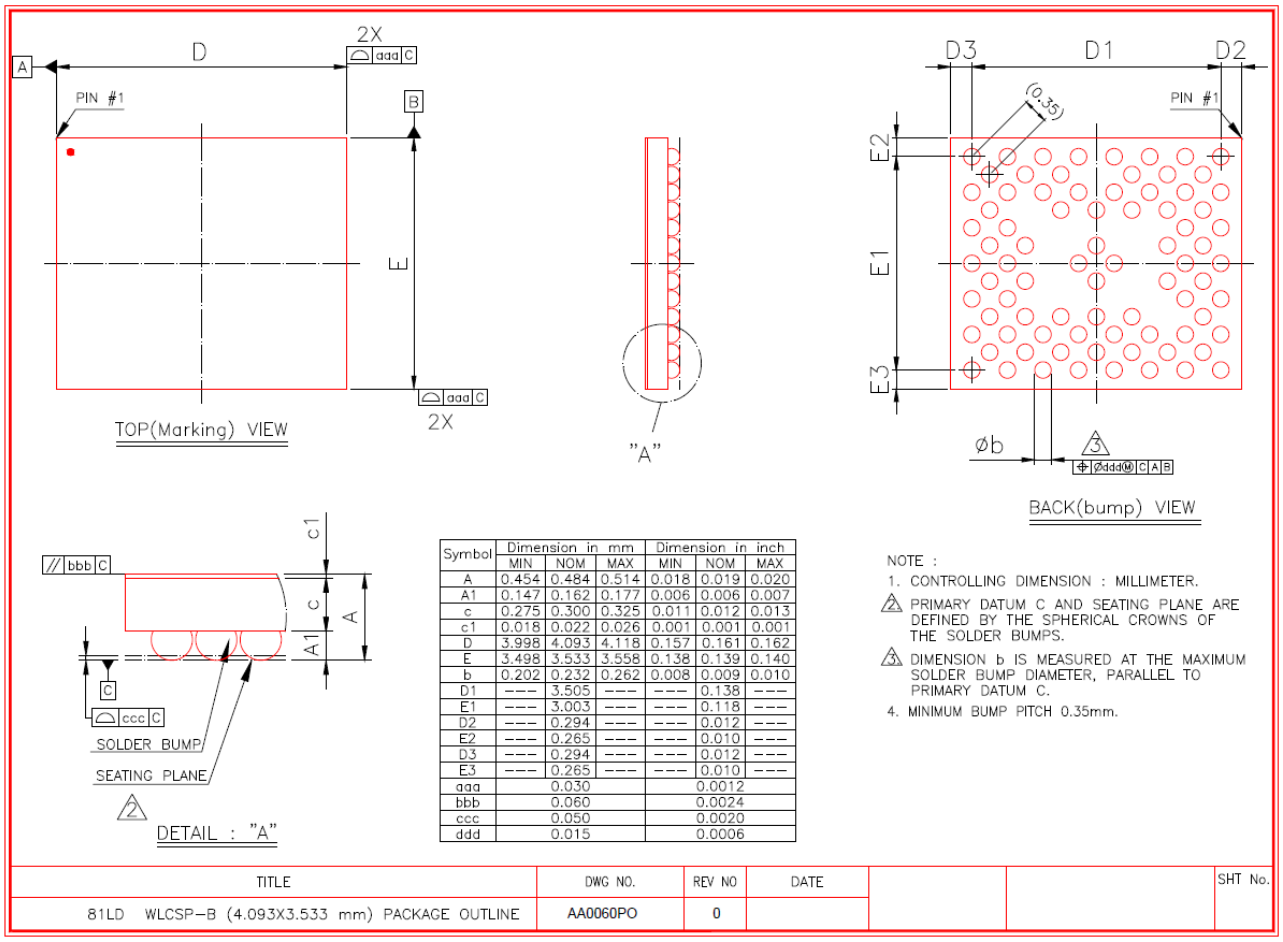
ASR PM813S has a vibrator driver and output at PWM pin. The vibrator driver diagram is as the following figure. The vibrator driver supports PWM function. The PWM frequency is selectable from 25kHz, 25kHz/2, 25kHz/4, 25kHz/8, 25kHz/16, 25kHz/32, 25kHz/64 and 25kHz/128. The PWM duty cycle is programmable from 1/128 to 128/128 by step 1/128.

Figure 35: Vibrator driver diagram



12. Mechanical Drawings

Figure 36: 81-pin 4.093 X 3.533 mm WLCSP Package



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.454	0.484	0.514	0.018	0.019	0.020
A1	0.147	0.162	0.177	0.006	0.006	0.007
c	0.275	0.300	0.325	0.011	0.012	0.013
c1	0.018	0.022	0.026	0.001	0.001	0.001
D	3.998	4.093	4.118	0.157	0.161	0.162
E	3.498	3.533	3.558	0.138	0.139	0.140
b	0.202	0.232	0.262	0.008	0.009	0.010
D1	---	3.505	---	---	0.138	---
E1	---	3.003	---	---	0.118	---
D2	---	0.294	---	---	0.012	---
E2	---	0.265	---	---	0.010	---
D3	---	0.294	---	---	0.012	---
E3	---	0.265	---	---	0.010	---
aaa	0.030			0.0012		
bbb	0.060			0.0024		
ccc	0.050			0.0020		
ddd	0.015			0.0006		

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. MINIMUM BUMP PITCH 0.35mm.

TITLE	DWG NO.	REV NO	DATE			SHT No.
81LD WLCSP-B (4.093X3.533 mm) PACKAGE OUTLINE	AA0060PO	0				

13. Part Order Numbering/Package Marking

13.1. Part Order Numbering

The current part order numbering scheme is the same as the package marking. Details see package marking。

Table 55: ASRPM813S Part Order Options

Package Type	Part Order Number	
81-pin WLCSP	ASRPM813S	

13.2. Package Marking

Figure 37: Shows a sample commercial package marking and pin 1 location.

Item	Content	Description
Line 1	ASR	ASR Company name
Line 2	PM813S	ASR Device
Line 3	XXXXXXX	Produce code

Line 4	YWW ASSY LOT	Date Code+Lot no.
Line 5	Pin1 dot	Pin1 dot

Note: The above drawing is not drawn to scale. Location of markings is approximate.

Revision History

Table 56: Revision History

Revision	Date	Description
Rev. A	Sep 17, 2020	Initial Release.

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