ASR5803 Datasheet

WLAN/Bluetooth SOC

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1. Product Overview

ASR5803 is a highly integrated, high performance, high cost-effective single-band (2.4GHz) IEEE802.11b/g/n 1x1 and Bluetooth (including BR/EDR and Low Energy) combo System on Chip (SoC) device, specially designed for high throughput.

The devices integrates the combined functions of Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and Orthogonal Frequency Division Multiplexing (OFDM) baseband modulation, Medium Access Controller (MAC), dual-MCUs, memories, RF transceivers and advanced host interfaces. The integrated RF system includes Tx/Rx switch, RF balun, power amplifier, low-noise amplifier, Dielectric Resonant Oscillators (DROs) and Phase Locked Loop (PLL) etc. Generic interfaces include an SDIO2.0 interface for connecting WLAN technologies and UART and PCM interface for connecting Bluetooth to the host processor.

The 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) are supported for security. Moreover, 802.11e Quality of Service (QoS) is supported.

The highlighted SoC device block diagram is shown in Figure 1-1.

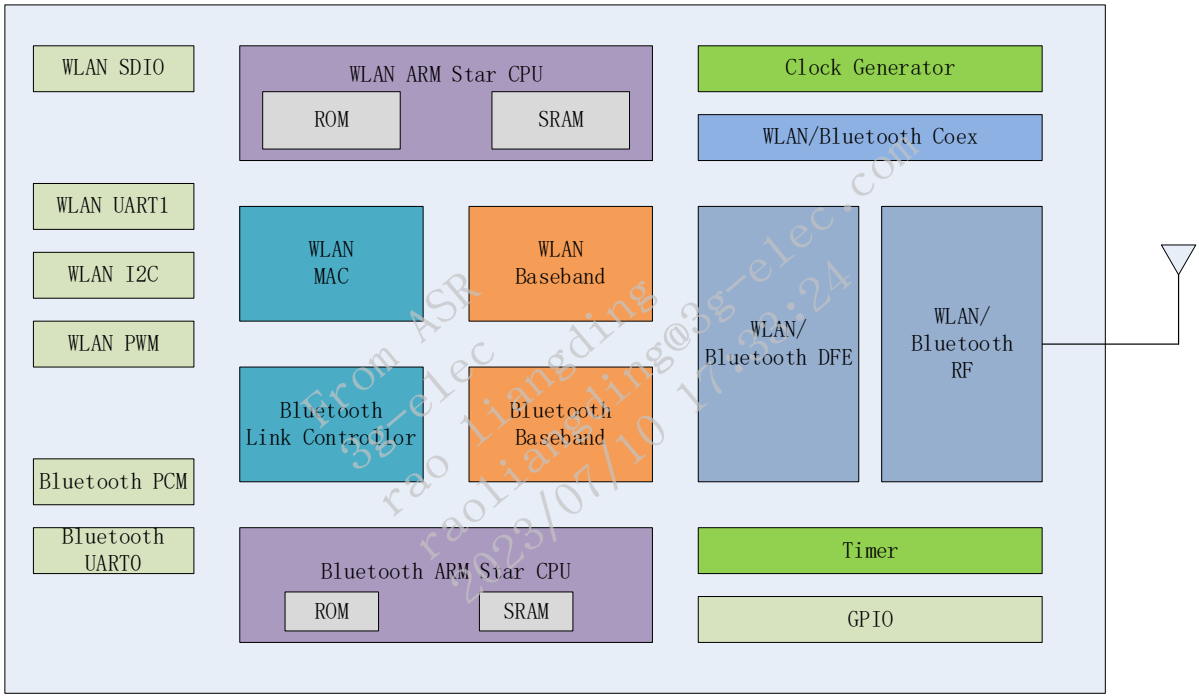


Figure 1-1 ASR5803 Block Diagram

1.1 Platform Features

- General
  - WLAN/Bluetooth combo
  - 1x1 SISO and HT20 operation
  - 26MHz analog reference clock support
  - Low-power clock 32.768KHz support deep sleep and standby modes
  - 22nm process, BGA83 3.3x4mm package.
  - Operation temperature: -20~70 (C grade), -40~85 (I grade)
- Application Processors
  - ARM Star CPU up to 120MHz clock for WLAN
  - ARM Star CPU up to 52MHz clock for Bluetooth
- Memory
  - Integrated SRAM for Tx frame queues/Rx data buffers
  - Support independent up to 8-Channel Direct Memory Access (DMA)
- Host Interfaces
  - Complies with SDIO2.0 for WLAN
  - UART (×2)
  - General Purpose Input Output (GPIO)
  - I2C (×1)
  - PWM (×2)
  - PCM (×1)

1.2 WLAN Features

- IEEE 802.11 Standards
  - 802.11 data rates of 1 and 2 Mbps
  - 802.11b data rates of 5.5 and 11Mbps
  - 802.11g data rates 6, 9, 12, 18, 24, 36, 48 and 54Mbps
  - 802.11g/b performance enhancements
  - 802.11n compliant with maximum data rates up to 72.2Mbps (20MHz BW channel)
  - 802.11e quality of service
  - 802.11i enhanced security
  - 802.11n block acknowledgement extension
  - Fully supports clients (stations) implementing IEEE Power Save mode
  - WiFi direct connectivity
- WLAN MAC

- Support both AP and STA mode in Infrastructure BSS.
- Support frame fragmentation and defragmentation.
- Support frame aggregation and de-aggregation (A-MPDU)
- Support Immediate block ACK and Compressed block ACK.
- Support protection mechanisms for coexistence with non-HT STAs
- Support Management Frame Protection
- Support auto rate control
- Support transmit power control
- Support Management information base (MIB)
- Support Security as 802.11i, Open/WEP/TKIP/CCMP/WAPI
- Support QoS as 802.11e and WMM
  - Support RTS/CTS as DCF and EDCA and TXOP and BlockAck
  - Support Legacy power save and APSD power save operation
- Support Low power mode
- Support Co-existence between WLAN and Bluetooth

- WLAN PHY
  - Compliment with 802.11b/g/n
  - Backward compatibility with legacy 802.11g/b technology
  - Support 2.4GHz channels
  - 20MHz bandwidth
  - DSSS/CCK Modulation
    - Support DSSS/CCK data rate of 1, 2, 5.5, 11Mbps
  - ERP Modulation
    - Support 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48 and 54 Mb/s.
  - HT
    - Support 1 spatial stream reception and transmission
    - Support HT MCS0 to MCS7 up to 72.2Mbps
    - Support PPDU non-HT/HT-mixed/HT-Greenfield format
    - Support both Short and Long Guard Interval
    - Support Rx RIFS
    - Support Rx STBC.
  - Support Power save features
- WLAN Radio
  - Integrated direct-conversion radio
  - Integrated T/R switch, PA and LNA
  - Integrated power amplifier with power control
  - Build-in gain selectable LNA with optimized noise figure and power consumption

- High dynamic range AGC function in receive mode
- On-chip ADC and DAC
- 20MHz channel bandwidth

1.3 Bluetooth Features

- Overall
  - Compliment with Bluetooth5.0 specifications
  - On-chip radio and baseband
  - Support High-speed UART: HCIOverUart(H4) and HCIOver3Wire (H5), for 3M/1.5Mbps/921600bps/etc
  - Support Simple Secure, and 192/256 bit key
  - Support 32K sleep
  - Low power consumption
  - Meet class 1 and class 2 transmitting power requirement
  - Provides +10dBm transmitting power
- Classic Bluetooth
  - Support Bluetooth Piconet and Scatternet
  - Support BR/EDR (2M/3Mbps)
  - Support 4 ACL simultaneously
  - Suport VoiceOverPCM & VoHCI
  - Support wireless broadcasting
- Bluetooth Low Energy
  - Support BLE 1Mbps/2Mbps/LR
  - Support 4 ACL simultaneously
  - Support 7 BLE Devices

2. Package Specifications

2.1 Ball Map

Figure 2-1 shows ball map from top view of the device, and Figure 2-2 shows the complete Pinout.

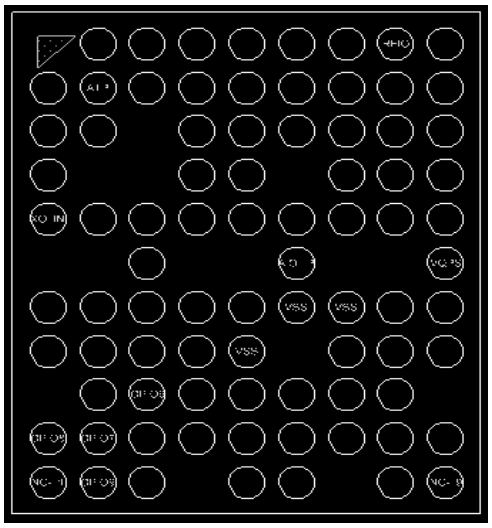


FIGURE 2-1 BALL MAP – 3.3X4.0 MM BGA PACKAGE

	1	2	3	4	5	6	7	8	9
A		VCON_PMIC	AVDD12_BLE_SYNTH	AGND_BLE_SYNTH	AVDD12_RXFE	AVDD22_PA	AGND_BALUN	RFIO	AGND_PA
B	DVDD_RF	ATP	AGND_BLE_RXBB	AGND_VCO	AGND_LO	AGND_RXFE	AVDD22_PA	AGND_PA	AGND_PA
C	AVDD12_BLE_RXBB	AGND_PSUB2		AGND_PLL	AVDD12_PLL	AGND_RXBB	AGND_PA	AGND_PA	AVDD12_BLE_PPA
D	NC			AGND_XTAL	AGND_PSUB_MIXED		AGND_PSUB1	AGND_TX	AVDD12_TX
E	CLK_IN	AVDD12_XTAL	AIO_QN	AIO_QP	AIO_IN	AGND_RXADC	VSSU_MIXED	AVDD12_RXBB	AVDD12_RXADC
F			DVSS18			AIO_IP			VQPS
G	PCM_DIN	PCM_DOUT	DVDD18	VCC_M1	VCC_M1	VSS	VSS	GPIO27	GPIO25
H	UART0_TX	PCM_CLK	PCM_SYNC	VCC_M1	VSS		GPIO29	GPIO28	XEN_OUT
J		UART0_RX	GPIO6	MODE1	MODE0	WF_LDO_EN	GPIO22	GPIO26	
K	GPIO8	GPIO7	BT_LDO_EN	HWRESET	SDIO_CMD	SDIO_DAT0	SDIO_DAT1	SDIO_DAT3	I2C_SDA
L	NC-L1	GPIO9	XIN_32K		SDIO_CLK	SDIO_DAT2		I2C_SCL	NC-L9

FIGURE 2-2 COMPLETE PINOUT 83-BALL

2.2 Pin Description

Table 2-1 Pin Types

Pin Type	Description
I/O	Digital Input/Output
I	Digital Input
O	Digital Output
A, I	Analog Input
A, O	Analog Output
DN	Pull Down
UP	Pull Up

TABLE 2-2 PIN LIST

Pin Number	Net Name	Type	Power Domain	Description
A2	VCON_PMIC	Analog I/O	1.2V	Configurable voltage to control PMIC output voltage.
A3	AVDD12_BLE_SYNTH	Power	1.2V	1.2V supply for BLE synthesizer.
A4	AGND_BLE_SYNTH	Ground	-	BLE synthesizer ground.
A5	AVDD12_RXFE	Power	1.2V	1.2V supply for WLAN front end.
A6	AVDD22_PA	Power	1.2V	2.2V supply for WLAN PA.
A7	AGND_BALUN	Ground	-	PA balun ground.
A8	RFIO	Analog I/O	1.2V	RF port for transmitter and receiver.
A9	AGND_PA	Ground	-	PA ground.
B1	DVDD_RF	Power	0.8V	0.8V core supply for RF.
B2	ATP	Analog I/O	1.2V	Analog DC test port.

Pin Number	Net Name	Type	Power Domain	Description
B3	AGND_BLE_RXBB	Ground	-	BLE baseband ground.
B4	AGND_VCO	Ground	-	WLAN VCO ground.
B5	AGND_LO	Ground	-	WLAN LO ground
B6	AGND_RXFE	Ground	-	WLAN front end ground.
B7	AVDD22_PA	Power	2.2V	2.2V supply for WLAN PA.
B8	AGND_PA	Ground	-	PA ground.
B9	AGND_PA	Ground	-	PA ground.
C1	AVDD12_BLE_RXBB	Power	1.2V	1.2V supply for BLE baseband.
C2	AGND_PSUB2	Ground	-	Ground.
C4	AGND_PLL	Ground	-	WLAN PLL ground.
C5	AVDD12_PLL	Power	1.2V	1.2V supply for WLAN pll.
C6	AGND_RXBB	Ground	-	WLAN baseband ground.
C7	AGND_PA	Ground	-	PA ground.
C8	AGND_PA	Ground	-	PA ground.
C9	AVDD12_BLE_PPA	Power	1.2V	1.2V supply for BLE pa driver.
D1	NC-D1	-	-	Leave NC on PCB. Caution: Do not connect this ball to ground.
D4	AGND_XTAL	Ground	-	XTAL buffer ground.
D5	AGND_PSUB_MIXED	Ground	-	Ground.
D7	AGND_PSUB1	Ground	-	Ground.
D8	AGND_TX	Ground	-	WLAN transmitter ground.
D9	AVDD12_TX	Power	1.2V	1.2V supply for WLAN transmitter.

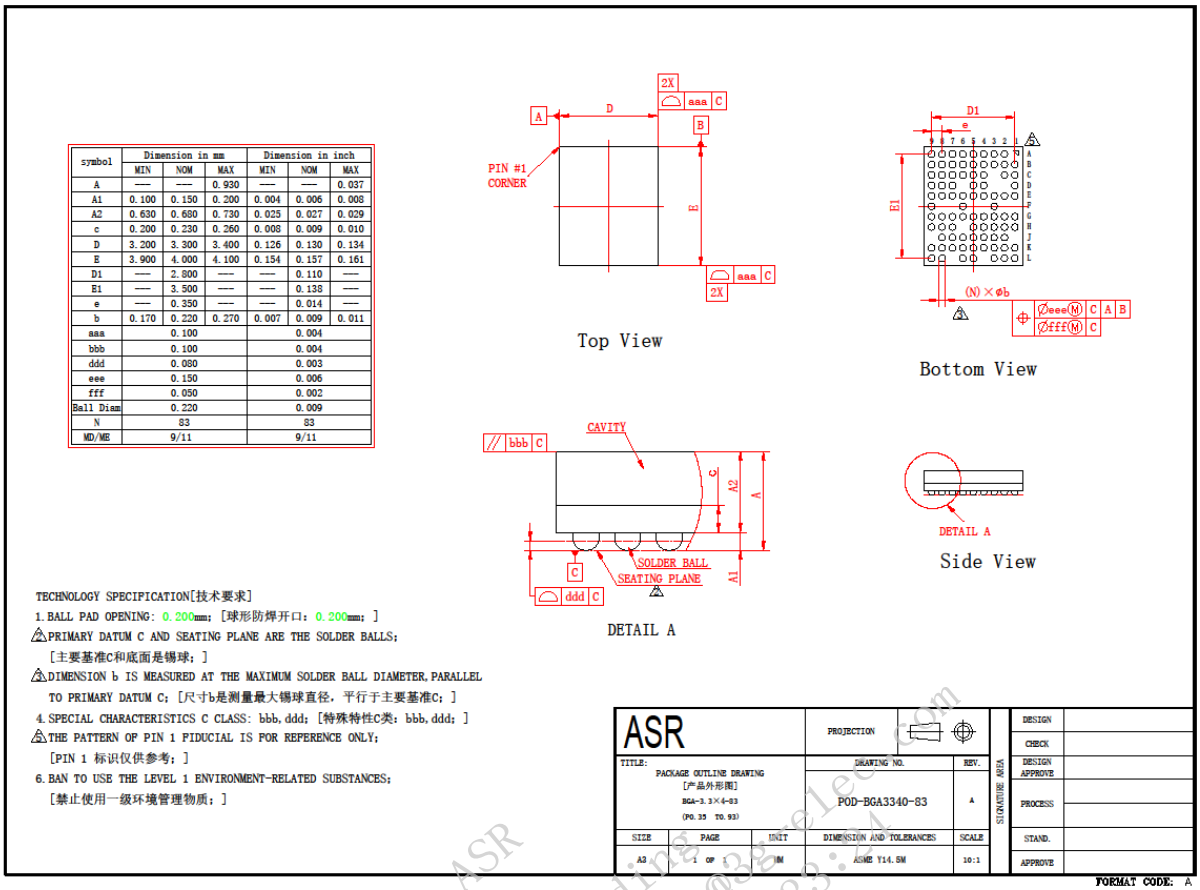
Pin Number	Net Name	Type	Power Domain	Description
E1	CLK_IN	Analog I	1.2V	Reference 26MHz clock input.
E2	AVDD12_XTAL	Power	1.2V	1.2V supply for XTAL buffer.
E3	AIO_QN	Analog I/O	1.2V	RF test port for negative Q path.
E4	AIO_QP	Analog I/O	1.2V	RF test port for positive Q path.
E5	AIO_IN	Analog I/O	1.2V	RF test port for negative I path.
E6	AGND_RXADC	Ground	-	ADC ground.
E7	VSSU_MIXED	Ground	-	ADC mixed ground.
E8	AVDD12_RXBB	Power	1.2V	1.2V supply for WLAN baseband.
E9	AVDD12_RXADC	Power	1.2V	1.2V supply for ADC.
F3	DVSS18	Ground	-	PAD ground
F6	AIO_IP	Analog I/O	1.2V	RF test port for positive I path.
F9	VQPS	Power	1.8V	1.8v supply for fuse programming power.
G1	PCM_DIN	I	1.8V	PCM data in pad
G2	PCM_DOUT	O	1.8V	PCM data out pad
G3	DVDD18	Power	1.8V	PAD power
G4	VCC_M1	Power	0.8V	digital core power
G5	VCC_M1	Power	0.8V	digital core power
G6	VSS	Ground	-	digital core ground
G7	VSS	Ground	-	digital core ground
G8	GPIO27	I/O	1.8V	General purpose I/O 27

Pin Number	Net Name	Type	Power Domain	Description
G9	GPIO25	I/O	1.8V	General purpose I/O 25
H1	UART0_TX	O	1.8V	Bluetooth UART0 TX data
H2	PCM_CLK	I/O	1.8V	PCM clock pad
H3	PCM_SYNC	I/O	1.8V	PCM sync pad
H4	VCC_M1	Power	0.8V	digital core power
H5	VSS	Ground	-	digital core ground
H7	GPIO29	I/O	1.8V	General purpose I/O 29
H8	GPIO28	I/O	1.8V	General purpose I/O 28
H9	XEN_OUT	O	1.8V	reference clock request .
J2	UART0_RX	I	1.8V	Bluetooth UART0 RX data
J3	GPIO6	I/O	1.8V	General purpose I/O 6
J4	MODE1	I	1.8V	Trap Mode select bit1
J5	MODE0	I	1.8V	Trap Mode select bit0
J6	WF_LDO_EN	I	1.8V	Wlan system power on enable
J7	GPIO22	I/O	1.8V	General purpose I/O 22
J8	GPIO26	I/O	1.8V	General purpose I/O 26
K1	GPIO8	I/O	1.8V	General purpose I/O 8
K2	GPIO7	I/O	1.8V	General purpose I/O 7
K3	BT_LDO_EN	I	1.8V	Bluetooth system power on enable
K4	HWRESET	I	1.8V	whole system reset
K5	SDIO_CMD	I/O	1.8V	SDIO command pad
K6	SDIO_DAT0	I/O	1.8V	SDIO data 0 pad
K7	SDIO_DAT1	I/O	1.8V	SDIO Data 1 pad
K8	SDIO_DAT3	I/O	1.8V	SDIO Data 3 pad

Pin Number	Net Name	Type	Power Domain	Description
K9	I2C_SDA	I/O	1.8V	I2C slave data pad
L1	NC-L1	-	-	-
L2	GPIO9	I/O	1.8V	General purpose I/O 9
L3	XIN_32K	I	1.8V	low power clock input
L5	SDIO_CLK	I	1.8V	SDIO clock pad
L6	SDIO_DAT2	I/O	1.8V	SDIO data 2 pad
L8	I2C_SCL	I	1.8V	I2C slave clock pad
L9	NC-L9	-	-	-

2.3 Mechanical Drawing

This section provides the mechanical specifications for the ASR5803 WLAN/Bluetooth combo processor.



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	——	——	0.930	——	——	0.037
A1	0.100	0.150	0.200	0.004	0.006	0.008
A2	0.630	0.680	0.730	0.025	0.027	0.029
c	0.200	0.230	0.260	0.008	0.009	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
E	3.900	4.000	4.100	0.154	0.157	0.161
D1	——	2.800	——	——	0.110	——
E1	——	3.500	——	——	0.138	——
e	——	0.350	——	——	0.014	——
b	0.170	0.220	0.270	0.007	0.009	0.011
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.220			0.009		
N	83			83		
MD/ME	9/11			9/11		

FIGURE 2-3 MECHANICAL DRAWING

TABLE 2-3 BGA PACKAGE

Unit: microns, 3 decimal places

Pin Number	X Coord	Y Coord	Net Name
A2	-1050	1750	VCON_PMIC
A3	-700	1750	AVDD12_BLE_SYNTH
A4	-350	1750	AGND_BLE_SYNTH
A5	0	1750	AVDD12_RXFE
A6	350	1750	AVDD22_PA
A7	700	1750	AGND_BALUN
A8	1050	1750	RFIO
A9	1400	1750	AGND_PA
B1	-1400	1400	DVDD_RF
B2	-1050	1400	ATP
B3	-700	1400	AGND_BLE_RXBB
B4	-350	1400	AGND_VCO
B5	0	1400	AGND_LO
B6	350	1400	AGND_RXFE
B7	700	1400	AVDD22_PA
B8	1050	1400	AGND_PA
B9	1400	1400	AGND_PA
C1	-1400	1050	AVDD12_BLE_RXBB
C2	-1050	1050	AGND_PSUB2
C4	-350	1050	AGND_PLL
C5	0	1050	AVDD12_PLL
C6	350	1050	AGND_RXBB
C7	700	1050	AGND_PA
C8	1050	1050	AGND_PA
C9	1400	1050	AVDD12_BLE_PPA

Pin Number	X Coord	Y Coord	Net Name
D1	-1400	700	NC-D1
D4	-350	700	AGND_XTAL
D5	0	700	AGND_PSUB_MIXED
D7	700	700	AGND_PSUB1
D8	1050	700	AGND_TX
D9	1400	700	AVDD12_TX
E1	-1400	350	CLK_IN
E2	-1050	350	AVDD12_XTAL
E3	-700	350	AIO_QN
E4	-350	350	AIO_QP
E5	0	350	AIO_IN
E6	350	350	AGND_RXADC
E7	700	350	VSSU_MIXED
E8	1050	350	AVDD12_RXBB
E9	1400	350	AVDD12_RXADC
F3	-700	0	DVSS18
F6	350	0	AIO_IP
F9	1400	0	VQPS
G1	-1400	-350	PCM_DIN
G2	-1050	-350	PCM_DOUT
G3	-700	-350	DVDD18
G4	-350	-350	VCC_M1
G5	0	-350	VCC_M1
G6	350	-350	VSS
G7	700	-350	VSS
G8	1050	-350	GPIO27

Pin Number	X Coord	Y Coord	Net Name
G9	1400	-350	GPIO25
H1	-1400	-700	UART0_TX
H2	-1050	-700	PCM_CLK
H3	-700	-700	PCM_SYNC
H4	-350	-700	VCC_M1
H5	0	-700	VSS
H7	700	-700	GPIO29
H8	1050	-700	GPIO28
H9	1400	-700	XEN_OUT
J2	-1050	-1050	UART0_RX
J3	-700	-1050	GPIO6
J4	-350	-1050	MODE1
J5	0	-1050	MODE0
J6	350	-1050	WF_LDO_EN
J7	700	-1050	GPIO22
J8	1050	-1050	GPIO26
K1	-1400	-1400	GPIO8
K2	-1050	-1400	GPIO7
K3	-700	-1400	Bluetooth_LDO_EN
K4	-350	-1400	HWRESET
K5	0	-1400	SDIO_CMD
K6	350	-1400	SDIO_DAT0
K7	700	-1400	SDIO_DAT1
K8	1050	-1400	SDIO_DAT3
K9	1400	-1400	I2C_SDA
L1	-1400	-1750	NC-L1

Pin Number	X Coord	Y Coord	Net Name
L2	-1050	-1750	GPIO9
L3	-700	-1750	XIN_32K
L5	0	-1750	SDIO_CLK
L6	350	-1750	SDIO_DAT2
L8	1050	-1750	I2C_SCL
L9	1400	-1750	NC-L9

3. WLAN

3.1 WLAN MAC

ASR5803 WLAN Medium Access Controller (MAC) provides all the required functions and many optional features of the IEEE 802.11 standard.

The ASR5803 WLAN MAC provides:

- Both AP and STA mode in Infrastructure BSS.
- Frame fragmentation and defragmentation.
- Frame aggregation and de-aggregation (A-MPDU)
- Immediate block ACK and Compressed block ACK.
- Protection mechanisms for coexistence with non-HT STAs
- Management Frame Protection
- Auto rate control
- Transmit power control
- Management information base (MIB)
- Security as 802.11i, Open/WEP/TKIP/CCMP/WAPI
- QoS as 802.11e and WMM
  - Support RTS/CTS as DCF and EDCA and TXOP and BlockAck
  - Support Legacy power save and APSD power save operation
- Low power mode
- Co-existence between WLAN and Bluetooth

3.2 WLAN Baseband

ASR5803 WLAN baseband supports high performance, 1x1 Single Input Single Output (SISO) applications. The key features including:

- Compliment with 802.11b/g/n
- Backward compatibility with legacy 802.11g/b technology
- Support 2.4GHz channels
- 20MHz bandwidth
- DSSS/CCK Modulation
  - Support DSSS/CCK data rate of 1, 2, 5.5, 11Mbps
- ERP Modulation
  - Support 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48 and 54 Mb/s.
- HT
  - Support 1 spatial stream reception and transmission

- Support HT MCS0~7 up to 72.2Mbps
- Support PPDU non-HT/HT-mixed/HT-Greenfield format
- Support both Short and Long Guard Interval
- Support Rx RIFS
- Support Rx STBC.

- Support Power save features

3.3 WLAN Radio

ASR5803 WLAN RF radio is a highly integrated sub-system. The direct conversion WLAN RF radio integrated all the necessary functions for transmit and receive operation. It integrates T/R switch, power amplifiers with power control and build-in gain selectable Low-noise Amplifier (LNA) with optimized noise figure and power consumption. It also integrates on-chip ADC and DAC and supports high dynamic rage AGC function in receive mode.

Table 3-1 shows the channel frequencies which supported by ASR5803. See Section 7.4 for WLAN Radio Specifications.

Table 3-1Channel Frequencies Supported

20MHz Channel	Frequency (MHz)
1	2412
2	2417
3	2422
4	2427
5	2432
6	2437
7	2442
8	2447
9	2452
10	2457
11	2462
12	2467
13	2472
14	2484

3.4 WLAN Encryption

ASR5803 WLAN Encryption unit is compliant to the 802.11i MAC Security Enhancements. The unit contains hardware support for encryption/decryption using:

- Wired Equivalent Privacy (WEP)
- Temporal Key Integrity Protocol (TKIP)
- Advanced Encryption Standard (AES) / Counter-Mode with Cipher Block Chaining Message Authentication Code Protocol (CCMP)
- Advanced Encryption Standard (AES) / Cipher-Based Message Authentication Code (CMAC)
- WLAN Authentication and Privacy Infrastructure (WAPI)

The WEP relies on the 64bit/128 bit RC4 (Rivest Cipher) algorithm used in the IEEE 802.11 standard. The algorithm is a symmetric steam cipher. The same key and algorithm are used for both encryption and decryption. Key management is performed by firmware. There are two authentication methods for WEP: Open System Authentication & Shared Key Authentication.

TKIP uses the WEP cipher algorithm with 128-bit temporal key for encryption and decryption. Based on TKIP, ASR5803 supports Wi-Fi Protected Access (WPA) encryption method.

ASR5803 also supports WiFi Protected Access 2 (WPA2). WPA2 implements the latest security standards, which is based on AES/CCMP encryption.

WAPI is Chinese National Standard. It's similar to WPA/WPA2. The WAPI Engine uses the SMS4 cipher suite for encryption and decryption.

3.5 WLAN/Bluetooth Coexistence

ASR5803 is a single-chip WLAN/Bluetooth solution with internal coexistence arbitration. In the PTA mechanism, the WLAN station and the Bluetooth device are collocated. The PTA mechanism coordinates sharing of the medium dynamically, based on the traffic load of the two wireless networks. The PTA control entity provides per-packet authorization of all transmissions. This mechanism can deny permission for transmission if it has chances of collisions. The PTA mechanism dynamically coordinates sharing of the wireless medium based on the traffic load of WLAN and Bluetooth. PTA tries to help with time domain multiplexing. What that means is that one of the radios can act as a master, the other as a slave, and the master will decide (arbitrate) access to the air medium to avoid that the radios transmit (or, to a degree, expect to receive) something at the same time. If a collision occurs, the PTA mechanism prioritizes transmission based on the priorities of different packets.

4. Bluetooth

ASR5803 includes a fully integrated Bluetooth Baseband and Radio sub-system, Link Manager Protocol (LMP) & HCI functionality in cooperation with the ARM STAR CPU. ASR5803 supports both classic Bluetooth (BT) & Bluetooth Low Energy (BLE), and compliment with Bluetooth 5.0 specifications.

4.1 Bluetooth RF and Baseband

ASR5803 key features include:

- Integrated T/R switch
- Integrated power amplifier with power control
- Shared DFE/LAN for WLAN/Bluetooth
- Meet class 1 and class 2 transmitting power requirement
- Support Bluetooth Piconet and Scatternet
- Support Adaptive Frequency Hopping (AFH), forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening
- Support Bluetooth5.0 BR and EDR packet types – 1Mbps (GFSK), 2 Mbps (π/4-DQPSK), and 3 Mbps (8DPSK)
- Up to 4 simultaneous active ACL connection support
- Standard UART and SDIO HCI transport layer
- Digital audio interfaces including PCM interface and VoHCI
- All standard SCO/eSCO voice coding
- Standard Bluetooth power saving mechanisms

4.2 Bluetooth Link Controller

ASR5803 link controller supports implementation of Standby, Connection and Sniff. The key features include:

- Paging and Page Scan
- Inquiry and inquiry Scan
- Broadcast messages
- Transparent Synchronous Data
- Asynchronous transports, both single-slot and multi-slot
- Adaptive Frequency Hopping and Channel Assessment
- Master/Slave switch
- ACL/SCO/eSCO link
- Sniff/Un-sniff/Sniff Sub-rating mode
- Wireless Broadcasting

- Enhanced power control
- Encryption
- Security mode 1~4

4.3 Bluetooth interfaces

ASR5803 provides PCM voice interface and High-Speed UART HCI interface.

ASR5803 supports a Pulse Code Modulation (PCM) interface that provides:

- Hardware support for continual PCM data transmission/reception without processor overhead
- PCM encoding/decoding support of A-law, U-law, and linear voice
- PCM bit width size of 8 bits or 16 bits
- Standard PCM clock rates from 64KHz to 2.048MHz with multi-slot handshake
- Short frame and long frames synchronization.

See Section 5.5, UART for the description of High-Speed UART interface.

4.4 Bluetooth/WLAN Coexistence

Refer to Section 3.5, WLAN/Bluetooth Coexistence.

5. Host/Peripheral Interfaces

5.1 MCU Processors

ASR5803 embedded two high performance ARM STAR CPUs. STAR is a fully featured microcontroller based on the ARMv8-M mainline architecture, supports 32-bit ARMv8-M instruction set and customizable instruction, adds coprocessor interface. STAR CPU is the most powerful and flexible secure processor which supports up to 1.50DMIPS/MHz.

ASR5803 contains an ARM STAR CPU up to 120MHz clock dedicated for WLAN and an ARM STAR CPU up to 52MHz clock dedicated for Bluetooth.

5.2 Timers & Watch-Dog

The ASR5803 has triple timers plus a Watchdog timer. The three 32-bit general-purpose timers are based on a selectable functional clock (32 kHz, 13, 6.5, 3.25, and 1 MHz).

5.2.1 Operation

The operating system timers and Watchdog timer module consist of three 32-bit Timer Clock Control Registers (TCCRn) up counters and one 16-bit WDT up counter. The module has 2 clock inputs:

- Selectable fast clock (13, 6.5, 3.25, and 1 MHz)
- Slow clock (32.768 kHz)

The fast clock is selectable through the registers. All 3 timers (Timer 0/1/2) operate at fast clock, slow clock of 32.768 kHz. When the value in the Operating System Count Register (TCRn) matches the value within any of the Match registers and the interrupt-enable bit is set, the corresponding bit in the Timer Status Register (TSR) is set. These bits are also routed to the Interrupt Controller where they are programmed to generate an interrupt. In addition, the 16-bit Watchdog timer operates using a timer module-derived clock of 256 Hz.

5.2.2 Watchdog Timer Functionality

When the value in the Watchdog timer matches the value in TWMR and the TWMER[WME] bit is set, the wdt_rst_src# signal is asserted, creating a Watchdog-timer reset event in the system.

The Watchdog Reset mode is invoked when the software fails to prevent the Watchdog time out from occurring properly. Watchdog resets are generated when the software is not executing properly and has possibly destroyed data. During Watchdog Reset mode, most internal registers in the system are reset to their defined default values. An exception to this is the real-time clock.

To avoid WDT reset, the software must restart the WDT before it matches the match value

When a WDT reset event occurs, the WDT generates a 4 msec-wide pulse on the wdt_rst_src# output. As a consequence, the system is held in a state of reset for this period of time. The system goes through a reset sequence when this reset signal is de-asserted.

5.2.3 Timer Interrupts

There is a dedicated timer in the WLAN/Bluetooth MCU, and there will be three timer interrupts 1/2/3 . There is a timer in SoC Top, which contains three timer interrupt 1/2/3, be sent to WLAN MCU/ Bluetooth MCU separately.

5.3 SDIO

5.3.1 Overview

The ASR5803 supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The ASR5803 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

5.3.2 Feature

The SDIO device interface main features include:

- On-chip memory used for CIS
- Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes at the full clock range of 0 to 50 MHz
- Special interrupt register for information exchange
- Allows card to interrupt host

5.3.3 Signal Descriptions

Table 5-1 shows the signal mapping between the ASR5803 device and the SDIO specification.

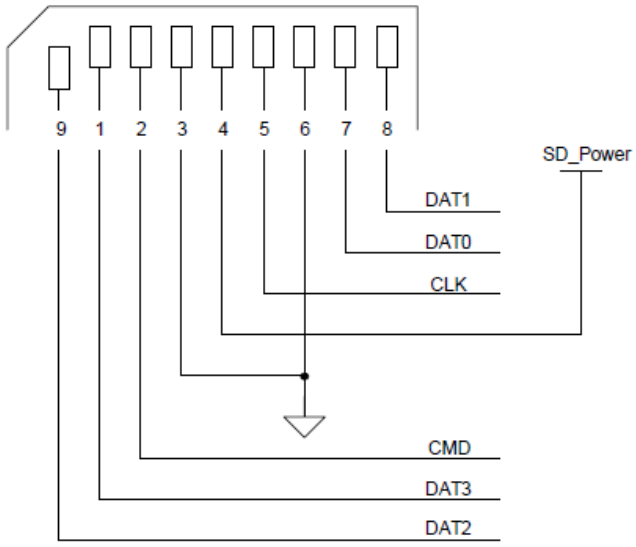
Table 5-1 SDIO Interface Singnal Description

ASR5803 Pin Name	Signal Name	Type	Description
SD_CLK	CLK	I/O	SDIO 1-bit mode: Clock SDIO SPI mode: Clock
SD_CMD	CMD	I/O	SDIO 1-bit mode: Command line SDIO SPI mode: Data input
SD_DAT[3]	DAT3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (active low)
SD_DAT[2]	DAT2	I/O	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPII mode: Reserved
SD_DAT[1]	DAT1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt
SD_DAT[0]	DAT0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data output

5.3.4 Operation

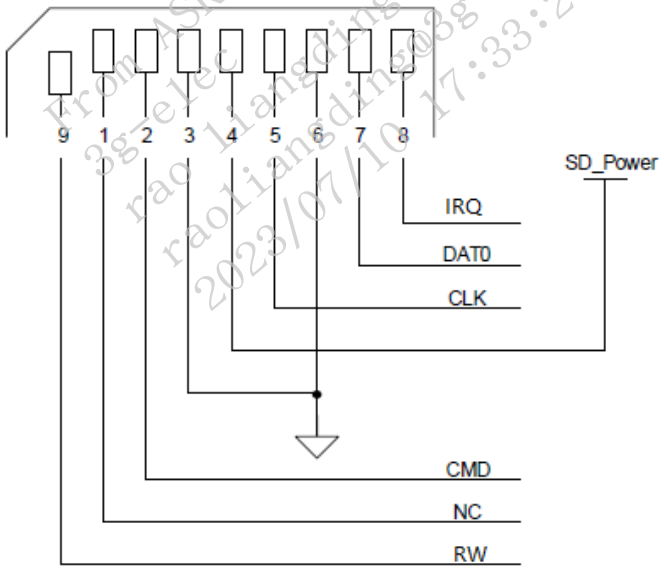
5.3.4.1 SDIO Interface Functional Description

5.3.4.1.1 SDIO Connection/Function



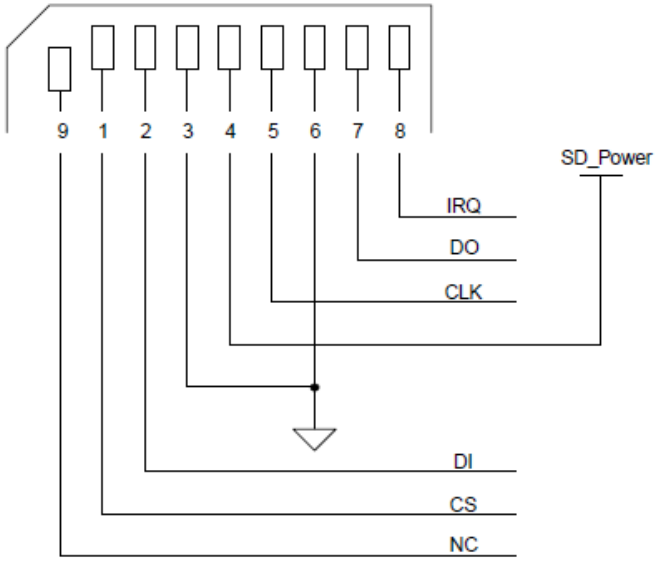
1. In 4-bit SDIO mode, data is transferred on all 4 data pins (DAT[3:0]), and the interrupt pin is not available for exclusive use as it is utilized as a data transfer line. Thus, if the interrupt function is required, a special timing is required to provide interrupts.

Figure 5-1 SDIO Physical connection - 4bit mode1



1. In 1-bit SDIO mode, data is transferred on the DAT[0] pin only. Pin 8, which is undefined for memory, is used as the interrupt pin.

Figure 5-2 SDIO physical connection - 1bit mode1



1. Pin 8, which is undefined for memory, is used as the interrupt pin in SPI mode.

Figure 5-3 SDIO Physical Connection – SPI mode1

Table 5-2 SDIO Electrical Function Definition - 1-bit

Pin	Chip Pin Name	SDIO 1-bit Mode	
1	39	N/C	Not used
2	35	CMD	Command line
3	N/A	VSS1	Ground
4	N/A	VDD	Supply voltage
5	34	CLK	Clock
6	N/A	VSS2	Ground
7	36	DATA	Data line
8	37	IRQ	Interrupt
9	38	RW	Read Wait (optional)

Table 5-3 SDIO Electrical Function Definition - SPI

Pin	Chip Pin Name	SPI Mode	
1	39	CS	Card Select
2	35	DI	Data input
3	N/A	VSS1	Ground
4	N/A	VDD	Supply voltage
5	34	SCLK	Clock
6	N/A	VSS2	Ground
7	36	DO	Data output
8	37	IRQ	Interrupt
9	38	NC	Not used

Table 5-4 SDIO Electrical Function Definition - 4-bit

Pin	Chip Pin Name	SDIO 4-bit Mode	
1	39	CD/DAT[3]	Data line 3
2	35	CMD	Command line
3	N/A	VSS1	Ground
4	N/A	VDD	Supply voltage
5	34	CLK	Clock
6	N/A	VSS2	Ground
7	36	DAT[0]	Data line 0
8	37	DAT[1]	Data line 1 or Interrupt (optional)
9	38	DAT[2]	Data line 2 or Read Wait (optional)

5.3.4.1.2 SDIO Command List

All mandatory SDIO commands are supported.

Table 5-5 SDIO Mode, SDIO Commands

Command	Command Name	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD3	SEND_RELATIVE_ADDR	SDIO Host asks for RCA
CMD5	IO_SEND_OP_COND	SDIO Host asks for and sets operation voltage
CMD7	SELECT/DESELECT_CARD	Sets SDIO target device to command state or back to standby
CMD15	GO_INACTIVE_STATE	Sets SDIO target device to inactive state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory

Table 5-6 SPI Mode, SDIO Commands

Signal Name	Type	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD5	IO_SEND_OP_COND	Used in initialization state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory
CMD58	CRC_ON_OFF	Enable/disable CRC (SPI only)

5.3.4.1.3 Power on Reset

The power-up transaction sequences for SDIO and SPI modes are as follows:

SDIO Mode Power-Up Transaction Sequence

1. CMD5 (arg=0)

2. SDIO Card response with OCR

3. CMD5 from host to set operation voltage using OCR

4. SDIO Card response with IORDY = 1 and MP = 0 (not SDIO memory, not combo card)

5. CMD3 and CMD7 to set in one active mode

6. CMD15 to put the card inactive

SPI Mode Power-Up Transaction Sequence

1. CMD0 + CS = LOW

2. CMD5 (arg =0)

3. SDIO Card response with OCR

4. CMD5 from host to set operation voltage using OCR

5. CMD15 to put the card inactive

5.3.4.1.4 Operation Sequence

Table 5-7 lists the registers used to program the operation sequence. See the SDIO Registers section of the Host Interface Registers document for register programming information.

Table 5-7 SDIO Registers

Register/Offset
Host Transfer Status (HOST_RESTART), Offset 0x128
Card to Host Event (C2H_INTEVENT), Offset 0x130

SDIO Host Reads CIS Table Sequence

1. Check Card to Host Event (C2H_INTEVENT), Offset 0x130[2]. It is set by Card after CIS table is initialized.

2. HOST reads CIS Table using Function 0 address 8030_807F and function 1 address 8080_80FF.

SDIO Host Downloads Packet

1. Card sets Card to Host Event (C2H_INTEVENT), Offset 0x130[0].

2. Host Polls Dnld_Card_Rdy and IO_Ready.

3. Host starts CMD53 block mode using function 1 with IO port address. CMD53 write clears Dnld_Card_Rdy.

4. Host sends the data in terms of predefined blocks. If BUSY, host delays the next block.

5. After CMD53 write completes, an interrupt CardInt is sent to firmware.

6. Firmware checks Host Transfer Status (HOST_RESTART), Offset 0x128[2] and Host Transfer Status (HOST_RESTART), Offset 0x128[0] registers. If Dnld_CRC_Err = 1, this packet has CRC error. If Dnld_Restart = 1, firmware ignores this packet.

7. Back to the first step.

SDIO Host Uploads Packet

1. Card sets Card to Host Event (C2H_INTEVENT), Offset 0x130[1].

2. Upld_Card_Rdy triggers an interrupt to SDIO HOST in the interrupt period.

3. SDIO Host read to clear INT or write 0 to clear the interrupt.

4. SDIO Host checks Upld_Card_Rdy and IO_Ready.

5. Host starts CMD53 read using function1 with IO address with infinite block number or defined block number. CMD53 clears Upld_Card_Rdy bit.

6. After Host receives all data, HOST writes Abort using CMD52.

7. This terminate read operation. Card gets an interrupt with abort and with packet read, is complete.

8. Firmware reads interrupt, clears interrupt.

9. Firmware reads Host Transfer Status (HOST_RESTART), Offset 0x128[1]. If it is set by Host, Firmware prepares to reissue this packet.

10. Back to the first step.

The SDIO Host checks IO_READY before starting a new CMD53. The SDIO target device can take a new SDIO host command only after the SDIO target device internal state machine is set back to IO_Ready state. Otherwise, the new CMD53 is ignored.

5.3.4.2 Multiple I/O Ports

Each I/O port is mapped to a base address (BAR). There are 16 ports per direction (Tx/Rx). The availability of each port is indicated through a bitmap register in which the firmware sets the bits (before setting Tx done or Upload ready). The hardware clears the bits upon completion of the corresponding Cmd53. Figure 5-4 Multi-port dataflow shows a sample dataflow for Tx (Rx is imilar).

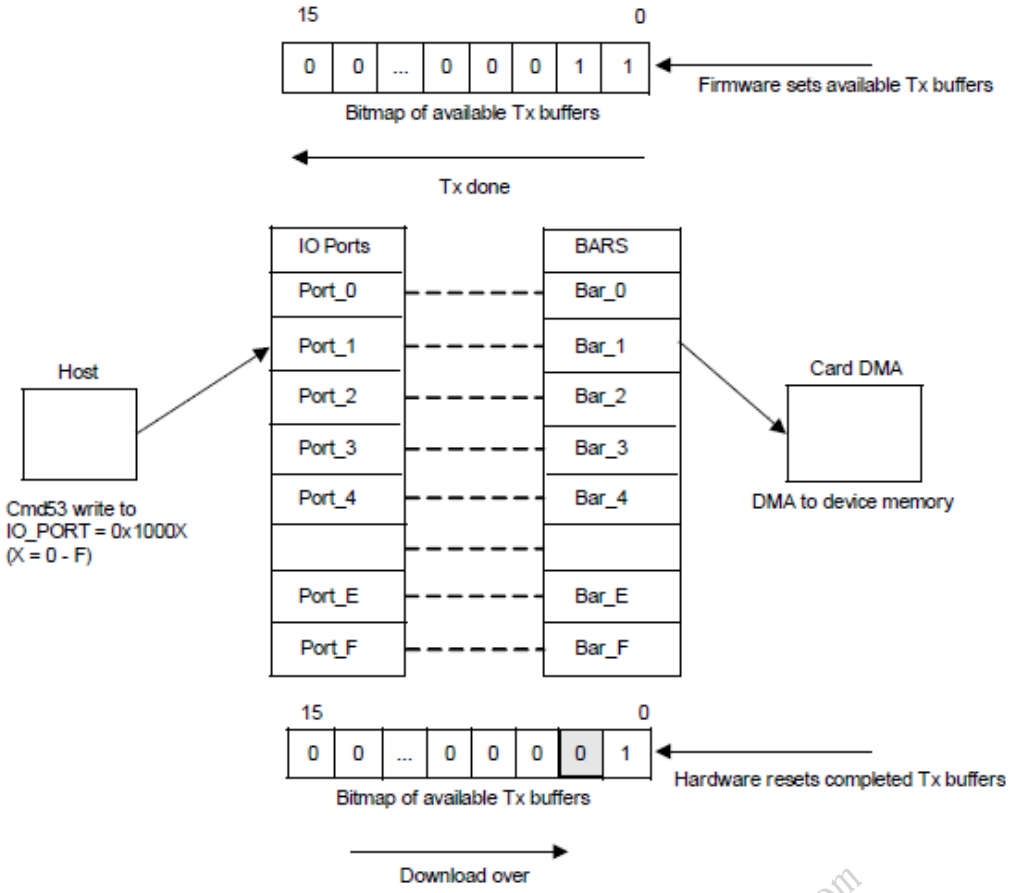


Figure 5-4 Multi-port dataflow

5.3.4.2.1 Tx Dataflow Sequence

1. Firmware programs the buffer address to the Tx BAR registers.

   Bar_0_reg = 0xC0001000

   Bar_1_reg = 0xC0001800

2. Firmware sets the corresponding IO port Tx bitmap = 0x3.

3. Firmware sets Tx download ready.

4. Driver receives Tx download ready interrupt and reads Tx bitmap (Cmd53).

5. Driver downloads a packet through Cmd53 write to Port_0.

(Driver can optionally download the second packet to Port_1).

6. Firmware receives Tx download over after completion of Cmd53 to Port_0.

7. Firmware reads Tx bitmap to get the buffer with download data.

8. Firmware sets the Tx bitmap again when the Tx buffer is free (after MAC Tx).

Setting Tx download ready is delayed until the firmware has multiple buffers free and the driver has some buffers for future downloads. This eliminates the need to interrupt the driver after each Cmd53 write.

5.3.4.2.2 Rx Dataflow Sequence

1. Firmware programs the buffer address to the Rx BAR registers.

   Bar_0_reg = 0xC0008000 Len_0_reg = 0x430

   Bar_1_reg = 0xC0008800 Len_1_reg = 0x64

2. Firmware sets the corresponding IO port Rx bitmap = 0x3.

3. Firmware sets Rx upload ready.

4. Driver receives Rx upload ready interrupt and reads Rx bitmap and length registers(Cmd53).

5. Driver uploads a packet through Cmd53 read from Port_0.

(Driver can continue to upload the second packet from Port_1).

6. Firmware receives Rx upload over after completion of Cmd53 to Port_0.

7. Firmware reads Rx bitmap to determine which buffer was uploaded.

8. Firmware sets the Rx bitmap again when the Rx packet is available.

Setting Rx upload ready is delayed until the firmware has multiple packets and the driver has some buffers pending for uploads. This eliminates the need to interrupt the driver after each Cmd53 read.

5.3.4.3 Host Interface Specifications

The ASR5803 SDIO host interface pins are powered from the VIO voltage supply.

See Section 7.3, Digital Pad Ratings, on page 57 for DC specifications.

See Section 7.3, Digital Pad Ratings, on page 57 for AC specifications.

The SDIO electrical specifications are identical for the 1-bit SDIO, 4-bit SDIO, and SPI modes

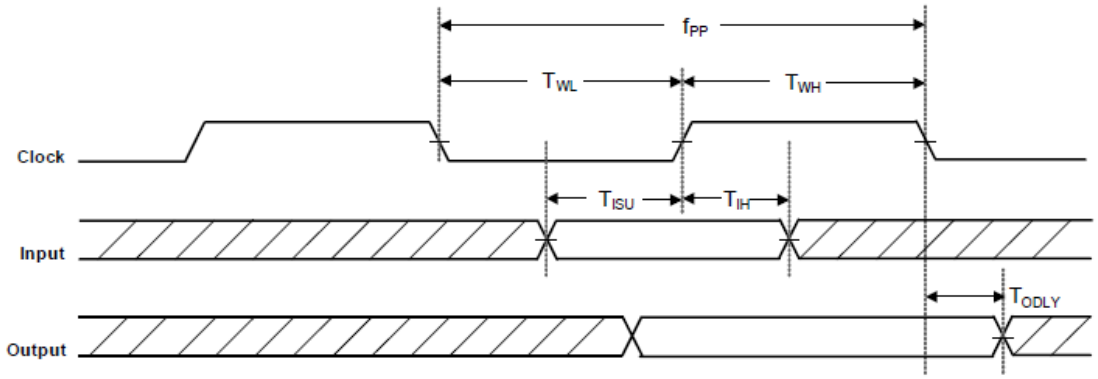


Figure 5-5 SDIO Protocol Timing Diagram - Normal Mode

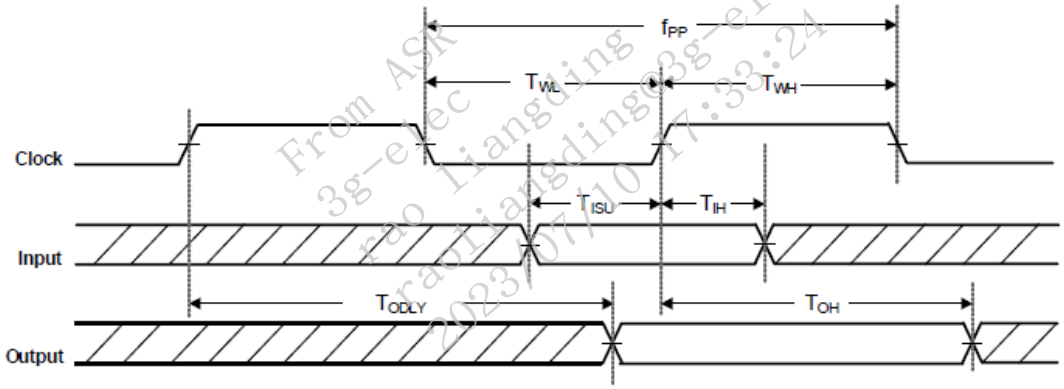


Figure 5-6 SDIO Protocol Timing Diagram – High Speed Mode

Table 5-8 SDIO Timing Data1

Symbol	Parameter	Condition	Min	Typ	Max	Units
fPP	Clock Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
TWL	Clock Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
TWH	Clock High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
TISU	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
TIH	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
TODLY TOH	Output Delay Time Output Hold Time	--	0	--	14	ns
		High Speed	2.5	--	--	ns

Note: 1. The SDIO-SPI CS signal timing is identical to all other SDIO inputs.

2. Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

5.4 GPIO

This section describes the operation of the General-Purpose Input/Output (GPIO) unit and the EINT unit of the ASR5803.

5.4.1 Overview

The ASR5803 provides GPIO ports for use in generating and capturing application-specific input and output, when GPIO ports multiplexed on the particular multi-function I/O pins. All ports are brought out of the device via the alternate function muxing. GPIO unit is in charge of GPIO ports control and status check. At the assertion of all resets, all GPIO ports are configured as inputs and remain inputs until they are configured either by the boot process or by user software.

The general features of the GPIOs include the following:

- As outputs, they can be cleared or set individually.
- As inputs, the values can be read individually.

Some multi-function I/O pins, whether the GPIO alternate function is selected or not, can be programmed to generate an interrupt via EINT unit from a rising edge, a falling edge, or both. Note that GPIO unit can be used independently or in combination with EINT unit.

5.4.2 Function Description

Figure 5-7 indicates multi-function I/O pins, GPIO unit and EINT unit connection. By virtue of GPIO unit, software is able to set and check the status of a GPIO port. By virtue of EINT unit, software is able to be awakened or interrupted from a multi-function I/O pin.

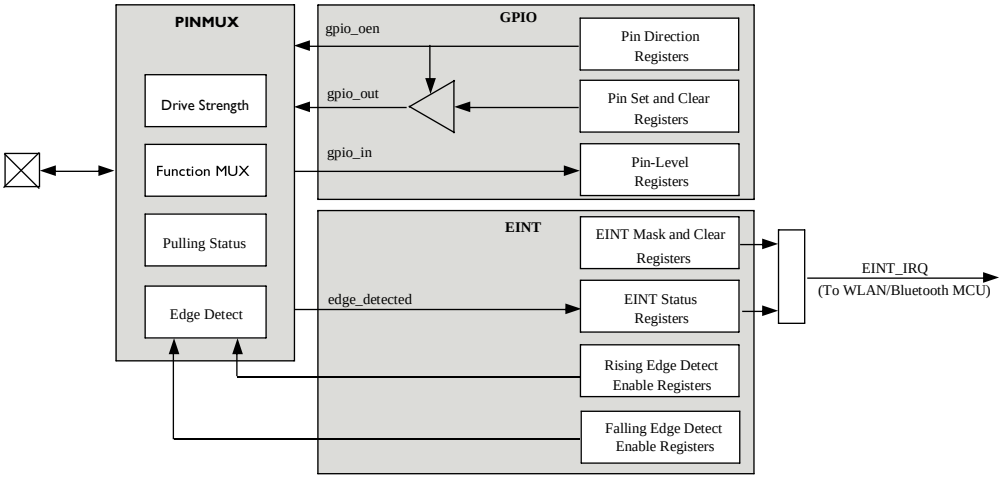


Figure 5-7 General-Purpose I/O and EINT Block Diagram

Note that there is one EINT interrupt relevant to I/O pins as shown in

IRQ Inputs	Signal Name	Notes
Int Req [6]	EINT IRQ	Generated in EINT unit. Each WLAN and Bluetooth system have one EINT interrupt.

Some multi-function I/O pins are connected to edge-detection logic. The edge-detection logic is capable of detecting a rising or falling edge on the input path of the pin. When enabled, the pins are always monitored, such that a transition triggers the edge-detection logic.

The output of the edge-detection logic is mainly used to provide a wakeup event in the WLAN or Bluetooth system sleep states. Some of these outputs are also used as interrupts assigned to WLAN or Bluetooth system interrupt controllers.

5.5 UART

This section describes the universal asynchronous receiver/transmitter (UART) serial ports.

5.5.1 Key Features

The serial ports are controlled via direct-memory access (DMA) or programmed I/O. The UARTs share the following features:

- Functionally compatible with the 16550A and 16750
- Ability to add or delete standard asynchronous communications bits (start, stop, and parity) in the serial data
- Independently controlled Transmit, Receive, line status, and data-set interrupts
- Modem control functions (CTSn and RTSn on UART0, UART1.)

- Auto-flow capability controls data I/O without generating interrupts:
  - RTSn (output) controlled by UART Receive FIFO
  - CTSn (input) from modem controls UART transmitter
- Programmable serial interface:
  - 7- or 8-bit characters
  - Even, odd, or no parity detection
  - 1 stop-bit generation
  - Baud-rate generation up to 3 Mbps for the 2 Fast UARTs
  - False start-bit detection
- 64-byte Transmit FIFO
- 64-byte Receive FIFO
- Complete status-reporting capability
- Ability to generate and detect line breaks
- Internal diagnostic capabilities that include:
  - Loopback controls for communications link fault isolation
  - Break, parity, and framing-error simulation
- Fully prioritized interrupt system controls
- Separate DMA requests for Transmit and Receive data services
- Serial infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) specification

The UARTs are functionally compatible with the 16550A and 16750 industry standards. Each UART supports most of the 16550A and 16750 functions as well as the following features:

- DMA requests for Transmit and Receive data services
- Serial infrared asynchronous interface
- Non-Return to Zero (NRZ) encoding/decoding function
- 64 byte Transmit/Receive FIFO buffers
- Programmable Receive FIFO trigger threshold
- Auto baud-rate detection
- Auto flow

5.5.2 Overview

The ASR5803 has 2 UARTs (UART 0 and UART 1). The UARTs use the same programming model.

Each port contains a UART and a slow serial infrared Transmit encoder and Receive decoder that conform to the IrDA serial infrared specification.

Each UART performs serial-to-parallel conversion on data characters received from a peripheral device or a modem and parallel-to-serial conversion on data characters received from the ASR5803.

Software can read a complete UART status for the Line Status Register. Status information includes the type and condition of transfer operations and error conditions (parity, overrun, framing, or break interrupt) associated with the UART.

Each serial port operates in either FIFO or non-FIFO mode. In FIFO mode, a 64-byte Transmit FIFO holds data from the ASR5803 until it is transmitted on the serial link; a 64-byte Receive FIFO buffers data from the serial link until it is read by the ASR5803. In non-FIFO mode, the Transmit and Receive FIFOs are bypassed, and the Transmit Holding Register and Receive Buffer Register are used instead.

Each UART includes a programmable baud-rate generator that can divide the input clock by any value from 1 to (2^{16} – 1), which produces a 16X clock that can be used to drive the internal Transmit and Receive logic. Software can program interrupts to meet its requirements, which minimizes the number of computations required to handle the communications link. Each UART operates in an environment that is either controlled by software and can be polled or is interrupt driven.

Both UARTs support the 16550A and 16750[2] functions, but support slightly different features as described in the following sections.

Note:

1. Infrared Data Association, *Serial Infrared Physical Layer Link Specification*, October 17, 1995, Version 1.1
2. The 16550A was originally produced by National Semiconductor Inc. The 16750 is produced as the TL16C750 by Texas Instruments

The supported baud rates of each UART are shown in Table 5-9

Table 5-9 Supported Baud Rates

UART	Support Baud Rates								
	9600 Hz	19.2 kHz	38.4 kHz	57.6 kHz	115.2 kHz	230.4 kHz	460.8 kHz	921.6 kHz	3.0 MHz
0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Both UARTs support the following modem control signals: CTSn, RTSn, Rx, Tx, DSRn, DTRn, RIn, and DCO.

5.5.3 Signal Descriptions

Table 5-10 lists and describes each external signal that is connected to a UART module and how these pins function as modem control lines. The pins transmit digital CMOS-level signals and are connected to the ASR5803 through GPIOs. Refer to Multi-Function pin registers for details on the alternate-function pin configuration.

Table 5-10 UART Signal Descriptions

Name	Type	Description
RXD	Input	**Serial Input** Serial data input to the Receive Shift register. In Infrared mode, it is connected to the infrared receiver input.
TXD	Output	**Serial Output** Serial data output to the communications-link peripheral, modem, or data set. The TXD signal is set to the logic 1 state upon a reset operation. It is connected to the output of the infrared transmitter in Infrared modeAuto-flow mode.
CTSn	Input	**Clear to Send** When asserted, indicates that the modem or data set is ready to exchange data. The CTSn signal is a modem status input, and its condition can be tested by reading the <CTS> field in the Modem Status Register. The <CTS> field is the complement of the CTSn signal. The <Delta Clear to Send> field in the Modem Status Register indicates whether the CTSn input has changed state since the last time the Modem Status Register was read. CTSn has no effect on the transmitter. When the <CTS> field changes state and the modem-status interrupt is enabled, an interrupt is generated. **Non-Auto-flow mode**: When not in Auto-flow mode, the <CTS> field indicates the state of CTSn. The <Delta Clear to Send> field indicates whether the CTSn input has changed state since the previous reading of MSR. CTSn has no effect on the transmitter. The user can program the UART to interrupt the ASR5803 when DCTS changes state. Software can then stall the outgoing data stream by starving the Transmit FIFO or disabling the UART with the Interrupt Enable Register. **NOTE:** If UART transmission is stalled by disabling the UART, no Modem Status Register interrupt is received when CTSn re-asserts because disabling the UART also disables interrupts. To get around this issue, use either auto-CTS in Auto-flow mode or program the CTSn GPIO pin to interrupt. **Auto-flow mode**: In this mode, the UART Transmit circuity checks the state of CTSn before transmitting each byte. No data is transmitted when CTSn is high.
Name	**Type**	**Description**
RTSn	Output	**Request To Send** When asserted, signals the modem or the data set that the UART is ready to exchange data. To assert the RTSn output (active low), set the <Request to Send> field in the Modem Control Register, which is the complement of the output signal. A reset operation de-asserts this signal (high). Loop-mode operation holds RTSn de-asserted. **Non-Auto-flow mode**: To assert the RTSn output (active low), set <Request to Send>. **Auto-flow mode**: RTSn is asserted automatically by the auto-flow circuitry when the Receive buffer exceeds its programmed trigger threshold. It is de-asserted when enough bytes are removed from the buffer to lower the data level back to the trigger threshold.

5.5.4 Operation

Figure 5-8 shows the format of a UART data frame.

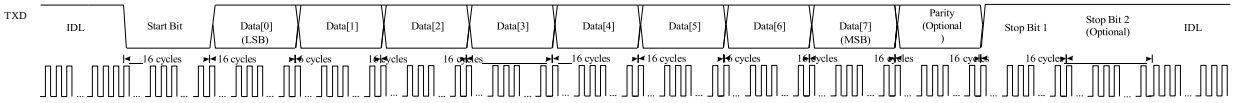


Figure 5-8 Example UART Data Frame

The Receive-data sample-counter frequency is 16 times the value of the bit frequency. The 16X clock is created by the baud-rate generator. Each bit is sampled three times in the middle. Shaded bits in Figure 5-8 are optional and can be programmed by software.

Each data frame is between 9 and 11 bits long, depending on the size of the data programmed, whether parity is enabled A data frame begins by transmitting a start bit that is represented by a high-to-low transition. The start bit is followed by 8 bits of data that begin with the Least Significant bit (LSb). The data bits are followed by an optional parity bit. The parity bit is set if: even parity is enabled and the data byte has an odd number of ones or if odd parity is enabled and the data byte has an even number of ones. The data frame ends with 1 stop bit. The stop bit represented by 1 successive bit period of logic one.

Each UART has 2 FIFOs: 1 Transmit and 1 Receive. The Transmit FIFO is 64 bytes deep and 8 bits wide. The Receive FIFO is 64 bytes deep and 11 bits wide. Three bits are used for tracking errors.

The UART can use NRZ coding to represent individual bit values. To enable NRZ coding, set the

<NRZ Coding Enable> field in the Interrupt Enable Register. A bit value of 1 is represented by a line transition, and 0 is represented by no line transition. Figure 5-9 shows the data byte 0b0100_1011 in NRZ coding. The LSb in the byte is transmitted first.

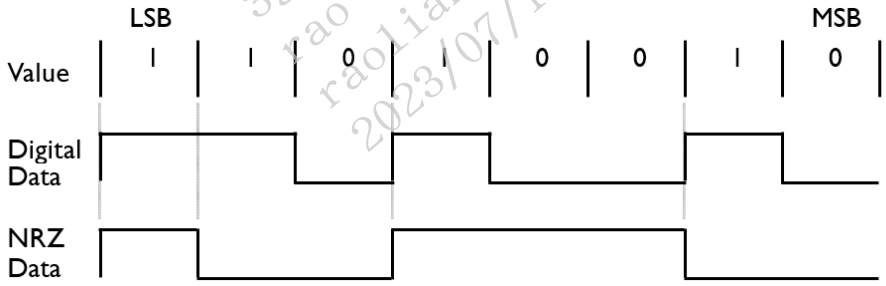


Figure 5-9 Example NRZ Bit Encoding - 0B0100_1011

5.6 I2C

The two-wire serial interface (TWSI) bus is a true multi-master bus including collision detection and arbitration. For full details of TWSI bus operation, refer to the *TWSI Bus Specification*.

A separate TWSI module, referred to as the power TWSI module, is used to interface to the power management IC.

5.6.1 Overview

The TWSI bus interface unit allows the ASR5803 to serve as a master and slave device residing on the TWSI bus, which is a serial bus (developed by Phillips Corporation) consisting of a 2-pin interface. SDA is the data pin for input and output functions, and SCL is the clock pin for reference and control of the TWSI bus.

The TWSI bus allows the TWSI unit to interface to other TWSI peripherals and microcontrollers. The serial bus requires minimal hardware for an economical system to communicate status and control information between the ASR5803 and external devices.

The TWSI bus interface unit is a peripheral device that resides on the ASR5803 peripheral bus. Data is transmitted to and received from the TWSI bus via a buffered interface. Control and status information is relayed through a set of memory-mapped registers. Refer to the *TWSI Bus Specification* for complete details on TWSI bus operation.

Note: The ASR5803 implementation of the TWSI unit does not support the hardware general call, 10-bit slave addressing, or CBUS compatibility.

5.6.2 Features

The TWSI bus interface unit features are:

- TWSI unit is compliant to TWSI *Bus Specification Version 2.1* with the exception of support for the hardware general call (see for a description of the General Call Address), 10-bit slave addressing, and CBUS compatibility.
- Multi-master and arbitration support
- Supports standard-mode operation up to 100 Kbps
- Supports fast-mode operation up to 400 Kbps
- Supports high-speed mode (HS mode) slave operation up to 3.4 Mbps (High-speed TWSI only)
- Supports high-speed mode (HS mode) master operation up to 3.3 Mbps (High-speed TWSI only)

Note: TWSI operational frequencies during Master mode decrease due to pull-up resistors on the bus. Therefore, SCL frequency is proportional to 1/R.

5.6.3 Signal Descriptions

Table 5-11 DMA Quick Reference for On-Chip Peripherals describes the TWSI bus signals, SDA and SCL. PWR_SCL and PWR_SDA are dedicated signals.

Table 5-11 DMA Quick Reference for On-Chip Peripherals

Signal Name	Input/Output	Description
Two-Wire Serial Interface Signals		
I2C_SDA	Bidirectional	TWSI serial data/address signal
I2C_SCL	Bidirectional	TWSI serial clock line signal

5.6.4 Operation

The *TWSI Bus Specification* defines a serial protocol for passing information between agents on the bus, using the 2-pin interface shown in Table 5-11: a serial data and address (SDA) line and a serial clock line (SCL). Each device on the TWSI bus is recognized by a unique 7-bit address and can operate as a transmitter or as a receiver in master or Slave mode. Table 5-12 defines the TWSI-bus terminology.

Table 5-12 TWSI Bus Definitions

TWSI Device	Definition
Transmitter	Sends data over the TWSI bus.
Receiver	Receives data over the TWSI bus.
Master	Initiates transfers, generates clock signals, and terminates transactions.
Slave	Device addressed by a master; it responds by transmitting or receiving data over the TWSI bus.
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message.
Arbitration	Ensures that only one master controls the bus when more than one master simultaneously tries to control the bus. This technique avoids message corruption.
Acknowledge	The receiver response to the master generated acknowledge clock pulse on SCL. The acknowledge can be either a positive-acknowledge (ACK) or a negative-acknowledge (NAK).
ACK	The condition on the TWSI bus where the master generates an acknowledge clock pulse and the receiver holds the SDA line low during the high period of the clock pulse.
NAK	The condition on the TWSI bus where the master generates an acknowledge clock pulse and the receiver holds the SDA line high during the high period of the clock pulse.

For example, the ASR5803 TWSI can act as a master on the bus to address an EEPROM as the slave to receive data (see Figure 5-10). When the TWSI addresses the EEPROM, it serves as a master transmitter and the EEPROM serves as a slave receiver. When the TWSI reads data, it serves as a master receiver and the EEPROM serves as a slave transmitter. Whether as a transmitter or receiver, the master generates the clock, initiates the transaction, and terminates the transaction.

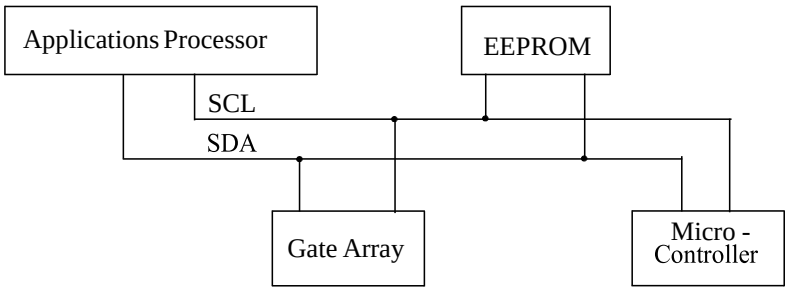


Figure 5-10 TWSI Bus Configuration Example

The TWSI bus uses an open-drain wired-AND structure, which allows multiple devices to drive the bus lines and to communicate status about events such as arbitration, wait states, and error conditions. When a master drives the clock (SCL) line during a data transfer, it transfers a bit on every instance that the clock is high. When the slave is unable to accept or drive data at the rate requested by the master, the slave can hold SCL low between the high states to insert wait intervals. The master clock can be altered only by another master during arbitration or by a slow slave peripheral that keeps the clock line low.

The TWSI bus allows multiple masters, which means that more than 1 device can initiate data transfers at the same time. Bus arbitration resolves conflicts between masters. Two masters can drive the bus simultaneously, provided they drive identical data. A master loses the arbitration if it tries to drive SDA high while another master is driving SDA low. The SCL line is a synchronized combination of clocks generated by the masters using the wired-AND connection to the SCL line.

TWSI transactions are either initiated by the TWSI as a master or received by the TWSI as a slave. Both conditions can result in Reads, Writes, or both over the TWSI bus.

5.7 PWM

The ASR5803 Pulse-Width Modulator (PWM) Controller generates 2 independent PWM signals.

Specific applications of the PWM Controller vary. Examples include:

- Controlling the brightness of an LED output by modulating the "on" time
- LCD contrast control

5.7.1 Overview

The ASR5803 contains 2 PWMs: PWM0 and PWM1. Each PWM operates independently of the others, is configured by its own set of registers, and provides a pulse-width modulated signal on a multi-function pin. Because each PWM contains identical circuitry, this section describes a generic PWMx, where x is 0 or 1.

Each PWM function enables the control of leading- and falling-edge timing of a single output channel. The edge timing can be set up to run indefinitely or adjusted on the fly to adapt to variable requirements. Power-saving modes include the ability to stop the internal clock

source · (PSCLK_PWM) used to source the PWMx and drive the PWM_OUTx signals to a steady high or low state. The frequency range supporting a 50% duty cycle varies from 198.4 Hz to 6.5 MHz. Other duty-cycle options depend on the choice of preferred frequency.

5.7.2 Features

- 4 pulse-width modulated signal channels
- Enhanced period controlled through 6-bit clock divider and 10-bit period counter
- 10-bit pulse control

5.7.3 Signal Descriptions

Output signals are the 2 single-bit output channels defined as PWM_OUT0 and PWM_OUT1(see Table 5-13). These signals are sent to multi-function pins (MFPs).

Table 5-13 Pulse Width Modulator I/O Signal Descriptions

Signal Name	Direction	Description
PWM0	Output	Pulse-width modulated signal for PWM 0
PWM1	Output	Output Pulse-width modulated signal for PWM 1

5.7.4 Operation

Figure 5-11 shows the block diagram for the PWM control logic.

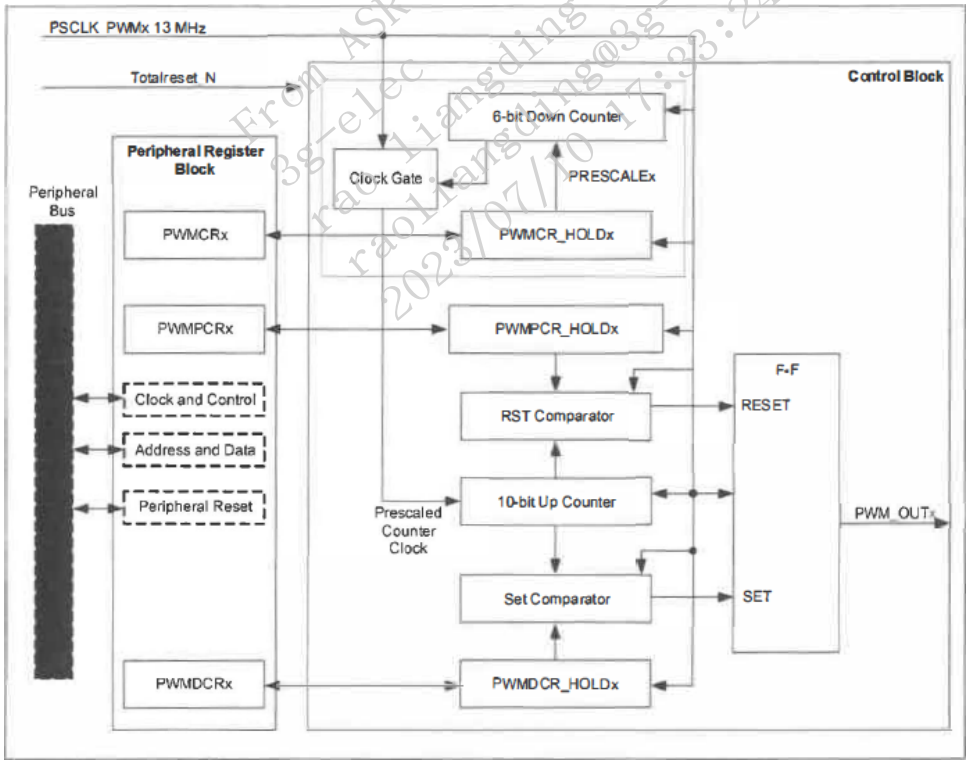


Figure 5-11 PWMx Block Diagram

5.8 PCM

5.8.1 Overview

The ASR5803 contains a general-purpose PCM interface suited to connect an ASIC to standard PCM compliant off-the-shelf devices such as audio codecs, line interfaces or TDM switches, microphone, speaker, and others. The PCM block has the following features:

- Three-wire serial bus interface:
- pcmd_in/out serial data input/output, with bidirectional output enable control
- pcmfsync_in/out frame sync input/output, with bidirectional output enable control
- pcmclk_in/out clock, with bidirectional output enable control
- PCM Interface as master or slave operation
- Programmable PCM frame rate through PLL means.
- Supports physical PCM format (single-clocking)
- Several PCM data output driver options:
    - push-pull, always driven
    - push-pull, hi-Z outside active slots
    - open-drain
- Six different frame sync pulse shapes:
    - encloses last falling pcmclk_in/out edge
    - encloses first rising pcmclk_in/out edge
    - encloses first falling pcmclk_in/out edge
    - encloses first 8 bits in the frame
    - encloses first 16 bits in the frame
    - left/right channel differentiation for Stereo support
- Transparent access to any slot in the frame (configurable first active slot)
- Support for one 8, and 16-bit linear audio codecs
- Single/Dual channel for Mono/Stereo operations
- Hardware protocol handler
- PLL smooth timing correction (depending on clock frequency)

5.8.2 Architecture

PCM is composed by 4 main blocks that are

- The EM Access interface, that perform read/write access requests to the Audio EM Access Manager, and manage left (and right) samples for the PCM interface.
- The serial/parallel interface that convert PCM interface serial sample to parallel sample (and vice-versa), according to the frame format
- The frame formatter that performs PCM frame format management (i.e. handling PCM frame synchronization signal control)

- The PLL, that is active when PCM is set as master mode only. When enabled, the PLL is in charge of generating the read/write access request indication for the EM Access Interface. It is also in charge of generating the PCM frame synchronization signal as well as the PCM interface clock according to the register settings.

Figure 5-12 details PCM block architecture.

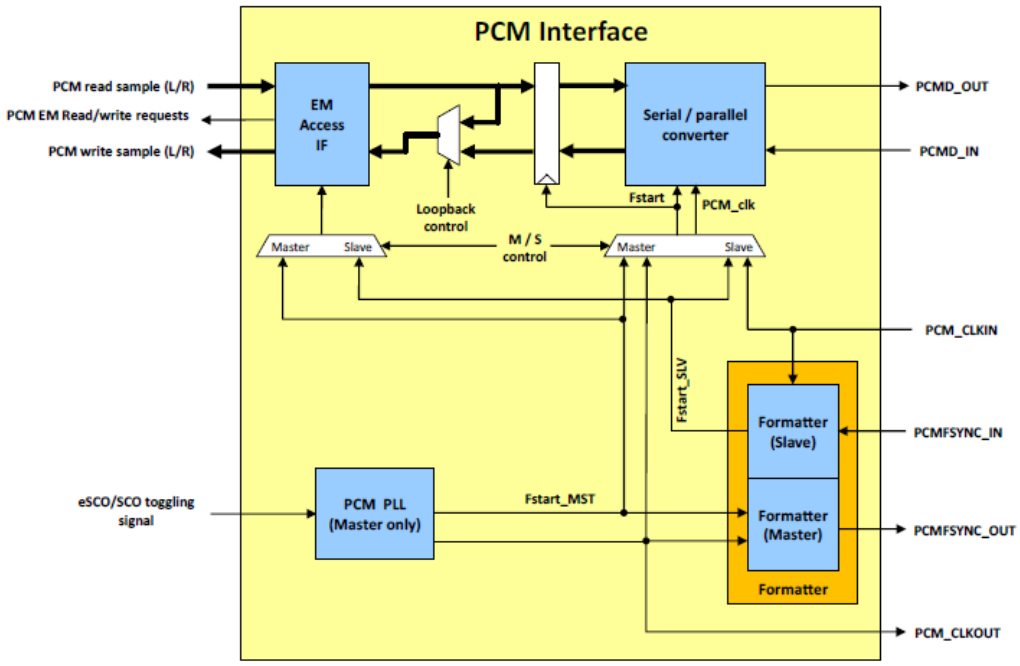


Figure 5-12 PCM Architecture

6. Power management

ASR5803 supports different power modes and might switch to each other.

- Sleep Mode: CPU running in low power mode, WLAN and Bluetooth baseband and radio system are turned off
- Active Mode: WLAN/Bluetooth RF system is active, system may transmit/receive radio and monitor iBeacon
- Power Save Mode (PSM): support legacy power save and APSD power save operation

Refer to Table 6-1 to get the ASR5803 power consumption data.

Table 6-1 Typical Power Consumption in WLAN Only mode, at 2.4GHz, BW20MHz

Mode	Power Consumption	
	Power(mW)	1.8V(uA) [a]
Sleep [b]		
Sleep [b]	0.15	1
Power Save,DTIM=1 [b,c]	1.20	1
Power Save,DTIM=2 [b,c]	0.81	1
Power Save,DTIM=3 [b,c]	0.69	1
Active		
RX, Listen [d]	40	60
RX, Continuous MCS7 [e]	44	60
TX,11b 1Mbps,17dBm@chip [f,g]	486	60
TX,11b 1Mbps,20.5dBm@chip [f,g]	625	60
TX,MCS7,13dBm@chip [f,g]	379	60
TX,MCS7,17dBm@chip [f,g]	488	60

Notes:

a. IO and VQPS works at 1.8V.The value for PS mode is sleep current.
b. PS Mode.
c. Beacon Interval = 100ms
d. Associated with AP, CCA when no carries present.
e. RX MCS7 duty rate=100%
f. Continous TX, duty rate=99%.
g. TX burst power is measured at the chip-port

ASR5803 supports BT/BLE, the typical power-current is as the following table showing:

Table 6-2 Typical Power Consumption in BT/BLE Mode

Mode	Power Consumpion	
	Power(mW)	1.8V(uA)
BT Deep Sleep	0.1	1
BT Rx	35.2	\
BT TX @14.8dBm	236.3	\
BT TX @-0.9dBm	109.8	\
BLE Deep Sleep	0.1	1
BLE Rx	21.6	\
BLE TX @ 11.3dBm	50.1	\
BLE TX @ 2.3dBm	37.0	\

7. Electrical Specifications

7.1 Absolute Maximum Ratings

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended period may affect device reliability.

Table 7-1 Absolute Maximum Ratings

Parameter	Range	Units
Input voltage	GND to VCC	V
Storage Temperature Range	-40 to +125	°C

1. Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 7-2 Recommended Operating Contitions

Parameter		Min	Typ	Max	Unit
DVDD18 (1.8V)		1.62	1.8	1.98	V
VQPS (1.8V)		1.62	1.8	1.98	V
VCC_M1 (0.8V)		0.72	0.8	0.88	V
AVDD12_BLE_SYNTH		1.14	1.2	1.26	V
AVDD12_RXFE		1.14	1.2	1.26	V
AVDD12_BLE_RXBB		1.14	1.2	1.26	V
AVDD12_PLL		1.14	1.2	1.26	V
AVDD12_BLE_PPA		1.14	1.2	1.26	V
AVDD12_TX		1.14	1.2	1.26	V
AVDD12_XTAL		1.14	1.2	1.26	V
AVDD12_RXBB		1.14	1.2	1.26	V
AVDD12_RXADC		1.14	1.2	1.26	V
DVDD_RF		0.72	0.8	0.88	V
AVDD22_PA		0.57/1.14/2.09	0.6/1.2/2.2	0.63/1.26/2.31	V
Operating temperature (T_{AMB})	ambient for Commercial Grade	-20		70	°C
	ambient for Industrial	-40		85	

Parameter		Min	Typ	Max	Unit
	Grade				

1. This device is not guaranteed to function outside the specified operating range.
2. Permissible DC droop in 2G transient state in between idle or active slots is at most 0.1V from typical voltage.
3. Ambient temperature, typical power supplies, unless otherwise noted.
4. I grade product needs special order.

7.3 Digital Pad Ratings

Table 7-3 DC Electricals - 1.8V Operation

Power Domain	Symbol	Description	Min	Typ	Max
1.8V Input	Vih	High Level input	VCC*0.7	1.8V	VCC+0.2
	Vil	Low Level input	-0.3	0V	0.3*VCC
	Rpu	Pull up resister	55K	79K	121K
	Rpd	Pull down resister	51K	87K	169K
	Iil	Input leakage current Pad in input mode			10uA
1.8V Output	Voh	High Level output	VCC-0.2V		
	Vol	Low Level output			0.2V
	Iol DCS[1:0]= 00 01 10 11	Low level output current when Vpad=0.2V	 13mA 25mA 37mA 49mA		
	Ioh DCS[1:0]= 00 01 10 11	High level output current when Vpad=VCC-0.2V	 11mA 21mA 32mA 42mA		

7.4 WLAN Radio Specifications

7.4.1 WLAN Radio General Specifications

Table 7-4 WLAN Radio General Specifications

Parameter	Min	TYP	Max	Unit
Operation band		2.4		GHz
Frequency range	2.412		2.484	GHz

7.4.2 WLAN Radio Receiver Specifications

Table 7-5 WLAN Radio Receiver Sensitivity

Parameter	Condition/Note	Min	TYP	Max	Unit
802.11b RX sensitivity (8% PER for 1024 octec PSDU, 25℃) [1]	DSSS 1Mbps		-100		dBm
	DSSS 2 Mbps		-97		dBm
	CCK 5.5 Mbps		-95		dBm
	CCK 11 Mbps		-92		dBm
802.11g RX sensitivity (10% PER for 1000 octec PSDU, 25℃) [1]	OFDM 6Mbps		-95		dBm
	OFDM 9 Mbps		-94		dBm
	OFDM 12 Mbps		-93		dBm
	OFDM 18 Mbps		-90		dBm
	OFDM 24 Mbps		-88		dBm
	OFDM 36 Mbps		-84		dBm
	OFDM 48 Mbps		-80		dBm
	OFDM 54 Mbps		-78		dBm
802.11n RX sensitivity (10% PER for 4096 octec PSDU, 25℃, GF, Long GI, no STBC) [1]	MCS 0		-95		dBm
	MCS 1		-93		dBm
	MCS 2		-90		dBm
	MCS 3		-87		dBm
	MCS 4		-84		dBm
	MCS 5		-79		dBm
	MCS 6		-78		dBm
	MCS 7		-76		dBm

Table 7-6 WLAN Radio Receiver ACR

Parameter	Condition/Note	Min	TYP	Max	Unit
802.11b RX Adjacent Channel Rejection [2]	DSSS 1Mbps		45		dB
	CCK 11 Mbps		36.5		dB

802.11g RX Adjacent Channel Rejection [2]	OFDM 6Mbps		37.5		dB
	OFDM 54 Mbps		23		dB
802.11n RX Adjacent Channel Rejection [2]	MCS 0		38.5		dB
	MCS 7		24		dB

Table 7-7 WLAN Radio Receiver Max Input Level

Parameter	Condition/Note	Min	TYP	Max	Unit
Maximum Input Level, 25℃ [3]	802.11b DSSS 1Mbps		0		dBm
	802.11g OFDM 6Mbps		0		dBm
	802.11n MM MCS0		0		dBm

Note 1: All sensitivity data are measured at the chip port unless otherwise specified

Note 2: In ACR test, desired signal level is as specified in IEEE specification.

Note 3: All maximum input level data are measured at the chip port unless otherwise specified

7.4.3 WLAN Radio Transmitter Specifications

Table 7-8 WLAN Radio Transmit Power Accuracy

Parameter	Condition/Note	Min	TYP	Max	Unit
Transmit Power Accuracy, 25℃ [1]	Open loop power control		± 3		dB
	Close loop power control [2]		± 1.5		dB

Table 7-9 WLAN Radio Maximum Transmit Power

Parameter	Condition/Note	Min	TYP	Max	Unit
802.11b Maximum Transmit Power, 25℃ [3 4]	DSSS 1Mbps		20.5		dBm
	DSSS 2 Mbps		20.5		dBm
	CCK 5.5 Mbps		20.5		dBm
	CCK 11 Mbps		20.5		dBm
802.11g Maximum Transmit Power, 25℃ [3 4]	OFDM 6Mbps		19.5		dBm
	OFDM 9 Mbps		19.5		dBm
	OFDM 12 Mbps		19.5		dBm
	OFDM 18 Mbps		19.5		dBm

	OFDM 24 Mbps		19		dBm
	OFDM 36 Mbps		19		dBm
	OFDM 48 Mbps		18		dBm
	OFDM 54 Mbps		18		dBm
802.11n Maximum Transmit Power, 25℃ [3,4]	MCS 0		19.5		dBm
	MCS 1		19.5		dBm
	MCS 2		19.5		dBm
	MCS 3		19		dBm
	MCS 4		19		dBm
	MCS 5		18		dBm
	MCS 6		18		dBm
	MCS 7		18		dBm

Note 1: In temperature range − 20°C to 0°C and 55°C to 85°C, transmit power accuracy derates by 2db.

Note 2: Close loop power control is established by enabling power detector.

Note 3: Maximum transmit power is measured at chip port, 25°C, VBAT = 4V, spectral mask and EVM compliance.

Note 4: In temperature range − 20°C to 0°C and 55°C to 85°C, maximum transmit power derates by 2db.

7.5 BT/BLE Radio Specifications

7.5.1 Classic Bluetooth

Table 7-10 BT Transmitter Character – BR

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency range		2402	-	2480	MHz
Maximum Output power			13		dBm
RF power control range			30		dB
RF power control step			4		dB
20dB occupied bandwidth			0.92		MHz
Modulation characteristic	Δf1avg		162		KHz
	Δf2avg/Δf1avg		0.86		-

Frequency tolerance	ICFT		9		KHz
	Drift rate		5		kHz/50us
	Drift(one slot)		-9		KHz
	Drift(five slot)		-11		KHz
In band spurious emissions	2MHz offset		-43		dBm
	3MHz offset		-45		dBm
	>3MHz offset		-47		dBm
Out of band spurious emission	30MHz to 1GHz		TBD		dBm
	1GHz to 12.75GHz		TBD		dBm
	1.8GHz to 1.9GHz		TBD		dBm
	5.15GHz to 5.3GHz		TBD		dBm
2nd harmonic			-25		dBm
3rd harmonic			-32		dBm

Table 7-11 BT Transmitter Character - EDR

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency range		2402	-	2480	MHz
Maximum Output power	pi/4-DQPSK		10		dBm
	8DPSK		10		dBm
Relative transmit power			-3		dB
pi/4-DQPSK modulation accuracy	RMS DEVM		6		%
	99% DEVM		13		%
	Peak DEVM		16		%
8DPSK modulation accuracy	RMS DEVM		6		%
	99% DEVM		15		%
	Peak DEVM		18		%
pi/4-DQPSK In band spurious emissions	2MHz offset		-26		dBm
	3MHz offset		-36		dBm
	>3MHz offset		-43		dBm
8DPSK	2MHz offset		-26		dBm
	3MHz offset		-36		dBm

In band spurious emissions	>3MHz offset		-42		dBm

Table 7-12 BT Receiver Character - BR

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity			-96		dBm
Maximum usable signal			0		dBm
Adjacent channel selectivity C/I	co-channel		9.5		dB
	1MHz		-14		dB
	2MHz		-36		dB
	>=3MHz		-44		dB
	Image channel		-26		dB
	Image 1MHz		-39		dB
Out-of-band blocking	30Mhz to 2000MHz	-10			dBm
	2001MHz to 2399MHz	-27			dBm
	2484MHz to 3000MHz	-27			dBm
	3001MHz to 12.75GHz	-10			dBm
Intermodulation characteristics			-29		dBm

Table 7-13 BT Receiver Character - EDR

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity	pi/4-DQPSK		-95.5		dBm
	8DPSK		-90		dBm
Maximum usable signal	pi/4-DQPSK		0		dBm
	8DPSK		0		dBm
pi/4-DQPSK	co-channel		10		dB
Adjacent channel selectivity C/I	1MHz		-7		dB
	2MHz		-35		dB
	>=3MHz		-43		dB
	Image channel		-25		dB
	Image 1MHz		-39		dB
8DPSK	co-channel		16		dB
Adjacent channel selectivity C/I	1MHz		-2		dB
	2MHz		-32		dB

	>=3MHz		-37		dB
	Image channel		-18		dB
	Image 1MHz		-35		dB

7.5.2 Bluetooth Low Energy

Table 7-14 BLE Transmitter Character – 1Mbps

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency range		2402	-	2480	MHz
Maximum Output power			10		dBm
RF power control range			30		dB
RF power control step			4		dB
Modulation characteristic	Δf1avg		255		KHz
	Δf2avg/Δf1avg		0.9		-
Frequency tolerance	ICFT		-9		KHz
	Drift rate		-3		kHz/50us
	Maximum Drift		6		kHz
In band spurious emissions	2MHz offset		-46		dBm
	3MHz offset		-48		dBm
	>3MHz offset		-50		dBm
2nd harmonic			-27		dBm
3rd harmonic			-25		dBm

Table 7-15 BLE Transmitter Character – 2Mbps

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency range		2402	-	2480	MHz
Maximum Output power			10		dBm
RF power control range			30		dB
RF power control step			4		dB
Modulation characteristic	Δf1avg		515		KHz
	Δf2avg/Δf1avg		0.9		-

Frequency tolerance	ICFT		-10		KHz
	Drift rate		2.5		Hz/us
	Drift		6		KHz
In band spurious emissions	4MHz offset		-48		dBm
	5MHz offset		-51		dBm
	>=6MHz offset		-52		dBm
2nd harmonic			-27		dBm
3rd harmonic			-25		dBm

Table 7-16 BLE Receiver Character – 1Mbps

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity			-98.5		dBm
Maximum usable signal			0		dBm
Adjacent channel selectivity C/I	co-channel		10		dB
	1MHz		-2		dB
	2MHz		-20		dB
	>=3MHz		-33		dB
	Image channel		-25		dB
	Image 1MHz		-29		dB
Out-of-band blocking	30Mhz to 2000MHz	-30			dBm
	2003MHz to 2399MHz	-35			dBm
	2484MHz to 2997MHz	-35			dBm
	3000MHz to 12.75GHz	-30			dBm
Intermodulation characteristics			-37		dBm

Table 7-17 BLE Receiver Character – 2Mbps

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity			-94.5		dBm
Maximum usable signal			0		dBm
Adjacent channel selectivity C/I	co-channel		11		dB
	2MHz		-13		dB

	4MHz		-35		dB
	>=6MHz		-40		dB
	Image channel		-12		dB
	Image 2MHz		-32		dB
Out-of-band blocking	30Mhz to 2000MHz	-30			dBm
	2003MHz to 2399MHz	-35			dBm
	2484MHz to 2997MHz	-35			dBm
	3000MHz to 12.75GHz	-30			dBm
Intermodulation characteristics			-32		dBm

Table 7-18 BLE Receiver Character – Coded S=2

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity			-102		dBm
Adjacent channel selectivity C/I	co-channel		TBD		dB
	1MHz		TBD		dB
	2MHz		TBD		dB
	>=3MHz		TBD		dB
	Image channel		TBD		dB
	Image 1MHz		TBD		dB

Table 7-19 BLE Receiver Character – Coded S=8

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity			-105		dBm
Adjacent channel selectivity C/I	co-channel		TBD		dB
	1MHz		TBD		dB
	2MHz		TBD		dB
	>=3MHz		TBD		dB
	Image channel		TBD		dB
	Image 1MHz		TBD		dB

8. Part Order Numbering/Package Marking

8.1 Part Order Numbering

The current part order numbering scheme is the same as the package marking. Details see package marking.

Table 8-1: ASR5803 Part Order Options

Package Type	Part Order Number
83-pin BGA	ASR5803

Table 8-2: ASR5803 Work Temperature

Commercial Grade

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{case}	Case Operating Temperature	Top.center of package	-20		70	℃

Industrial Grade

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{case}	Case Operating Temperature	Top.center of package	-40		85	℃

8.2 Package Marking

Figure 8-1 shows a sample Commercial package marking and pin 1 location for the ASR5803.

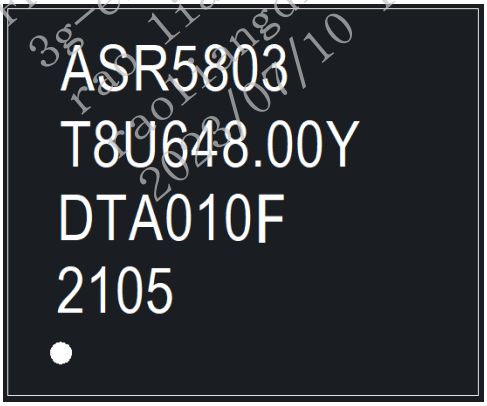


Figure 8-1 Commercial Package Marking and Pin1 Location

Marking Content		
Item	**Content**	**Description**
Line 1	ASR5803	ASR Part number
Line 2	XXXXXXXXX	Lot Number
Line 3	XXXXXXXXX	Product lot no.
Line 4	YYWW	Date code
Line 5	Pin A1 dot	Pin A1 dot

Note: The above drawing is not drawn to scale. Location of markings is approximate.

9. Revision History

Revision	Date	Description
V1.0	2021-11-30	Initial release
V1.1	2022-12-29	Update pin info.