CS 251, Spring 2023, Assignment 1

Due Friday, June 2, 10:00 PM
Late submission accepted until Monday, June 5, 10:00 PM with no penalty

You are required to read, complete and sign, and submit (as well as follow) the following statement of Academic Integrity.

Statement of Academic Integrity for CS 251 Spring 2023, **Assignment 1**
I declare the following statements to be true:

- I have not used any unauthorized aids.
- I recognize that while I can discuss the questions in this assignment on Piazza and other forums with the instructors and with other students in the class, the write up that I am submitting is my own.
- I am aware that misconduct related to course work can result in significant penalties, including failing the course and suspension (this is covered in Policy 71:)

  `https://uwaterloo.ca/secretariat/policies-procedures-guidelines/policy-71`

Student Name: George Wang

UW ID#: 20943813

Signature: 

Date: Jun. 1, 2023

The purpose of this assignment is to practice designing and implementing combinational digital logic circuits.

Coverage material for this assignment can be found on the course website as:

- Laws of Boolean Algebra Reference Sheet on the Assignment Information webpage, and
- On the Lecture Notes webpage in the
  - May 16th Lecture on Introduction to Digital Logic Design,
  - May 18th Lecture on Digital Logic Design - Combinational Logic, and
  - May 25th Lecture on Digital Logic Design - Gates, Decoders, Multiplexors and Transistors

For this assignment, make note of the following details:

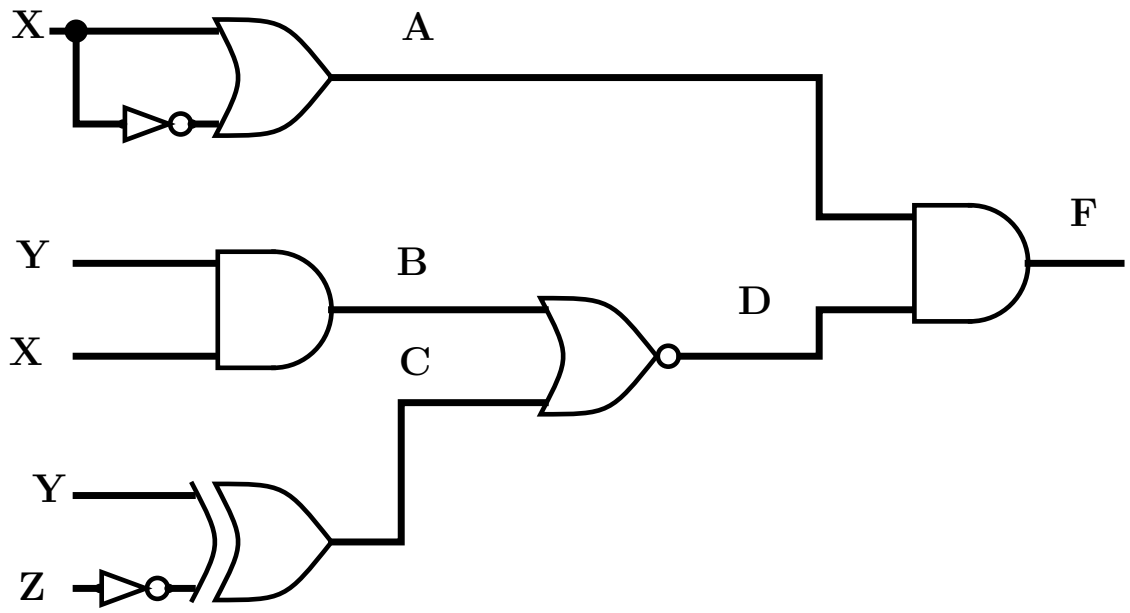
- Any diagrams that are part of your solution must be drawn neatly, using rectilinear lines and clearly labelled inputs and outputs.
- You may assume that for any valid input you also have its inverse, e.g. for input A you also have $\overline{A}$ withut using an inverter (NOT) gate explicitly.

We have an A1 Official Post on piazza. In this post, we will include all A1 assignment related information such as

- updates/corrections made to the assignment, if any
- remark request due date
- FAQs

1. (10 points)

   (a) (8 points) Complete the truth table for the combinational logic circuit given below with output F and intermediate outputs A, B, C and D.



X	Y	Z	A	B	C	D	F
0	0	0	1	0	1	0	0
0	0	1	1	0	0	1	1
0	1	0	1	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	1	0	1	0	0
1	0	1	1	0	0	1	1
1	1	0	1	1	0	0	0
1	1	1	1	1	1	0	0

   (b) (2 point) Give the **simplified** Boolean equation for F in terms of X, Y, and Z.

$F = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + XYZ$

$= (\bar{X}+X)\bar{Y}Z + \bar{X}Y\bar{Z}$

$= \bar{Y}Z + \bar{X}Y\bar{Z}$

2. (22 points) Consider the truth table given below, with inputs A, B, and C and output function F.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

(a) (5 points) Write the *unreduced* Boolean equation in **sum-of-products** form for the output function F.

$$F = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + ABC$$

(b) (3 points) Write the *unreduced* Boolean equation in **product-of-sums** form for the output function F.

$$F = (\bar{A}+\bar{B}+C)(A+\bar{B}+\bar{C})(A+\bar{B}+C)$$

$$\bar{F} = \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$$

$$F = \bar{\bar{F}} = \overline{\bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C} = \overline{\bar{A}\bar{B}C} \cdot \overline{A\bar{B}\bar{C}} \cdot \overline{A\bar{B}C}$$

$$= (A+B+\bar{C})(\bar{A}+B+C)(\bar{A}+B+\bar{C})$$

(c) (2 points) Write the **reduced** Boolean equation for the output function F. Show your steps for simplification for full points.

$$\bar{F} = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C} + ABC$$

$$= \bar{A}\bar{C}(\bar{B}+B) + (\bar{A}+A)BC + AB\bar{C}$$

$$= \bar{A}\bar{C} + BC + AB\bar{C}$$

$$= \bar{A}\bar{C} + B(C + A\bar{C})$$

$$= \bar{A}\bar{C} + B(C+A)(C+\bar{C})$$

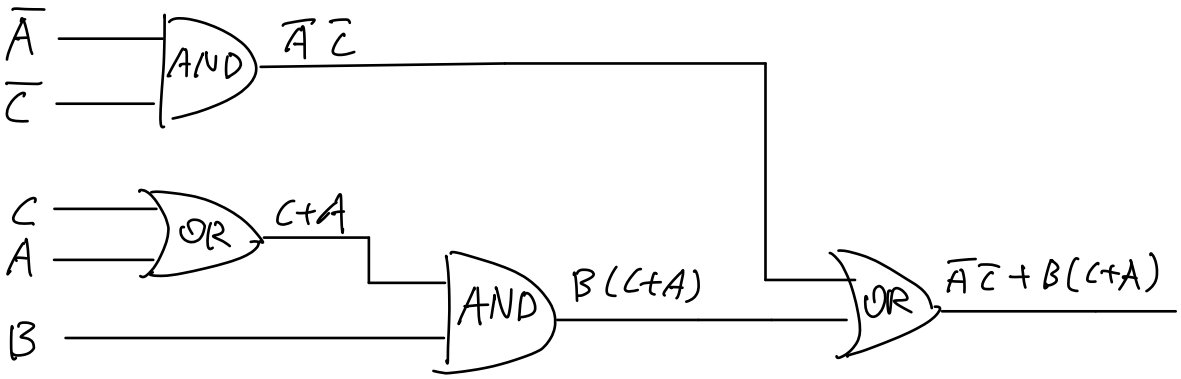
$$= \bar{A}\bar{C} + B(C+A)$$

$$= \overline{A+C} + B(A+C)$$

$$= (\overline{A+C} + B)(\overline{A+C} + A + C)$$

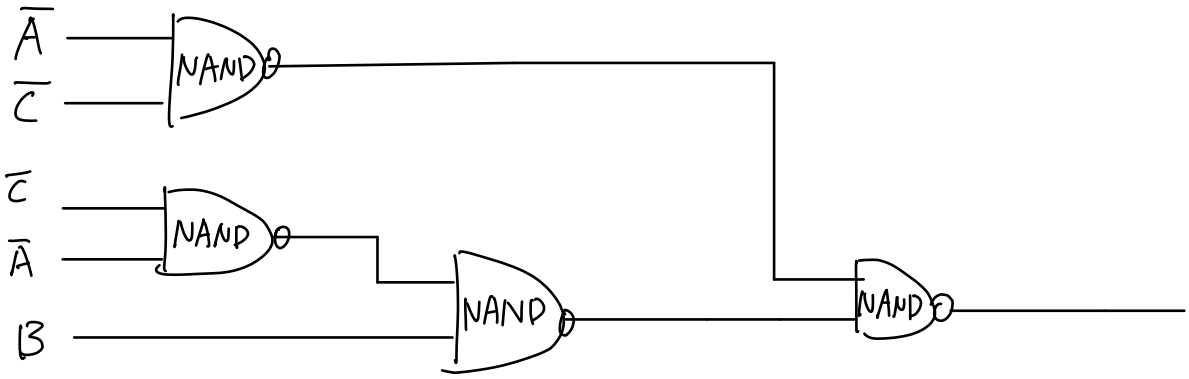
$$= \overline{A+C} + B \quad = \bar{A}\bar{C} + B$$

(d) (4 points) Implement the output function F using only AND and, or OR gate(s).

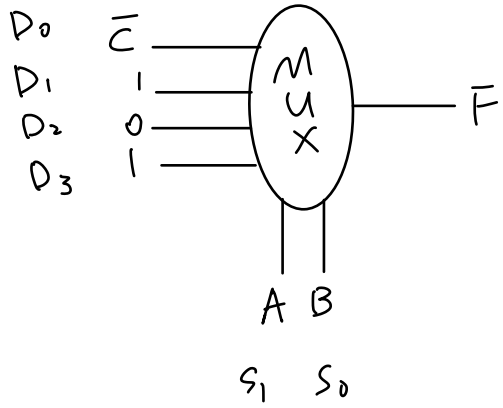


or with inverted input = NAND

(e) (3 points) Implement the output function F using a minimum number of NAND gate(s).



(f) (5 points) Implement the output function F using only a 4:1 MUX.



3. (10 points) Assume that a combinational logic circuit has two inputs S and X and an output function F. The input X consists of three bits, $X0, X1$, $X2$, where $X0$ and $X2$ are the least and most significant bits, respectively. For example, for input $X = 011$, $X0 = 1$, $X1 = 1$, and $X2 = 0$. The output function F also consists of three bits $F0, F1$, and $F2$, where $F0$ and $F2$ are the least and most significant bits, respectively.

   (a) (6 points) Construct the truth table for the output function F, which is the result of shifting the input X, left when $S = 0$. When $S = 1$, F is the result of shifting the input X right.

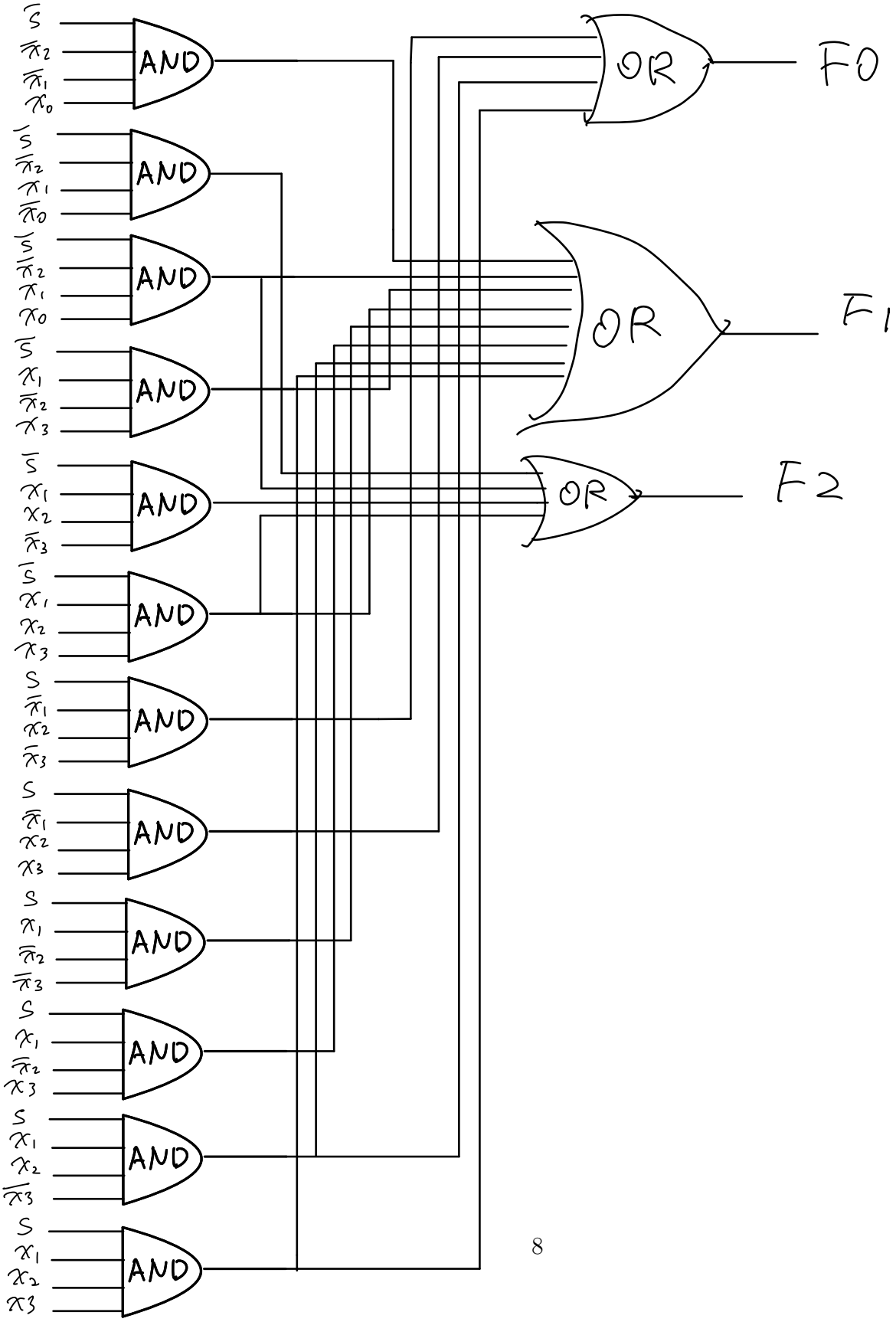
   We have provided the truth table with two entries as an example.

   When $S = 0$, the operation to perform is left shift. For input $X = 110$, the output $F = 100$. Note that the bits are shifted left by one position and the most significant bit is dropped and a zero is added in the least significant bit position.

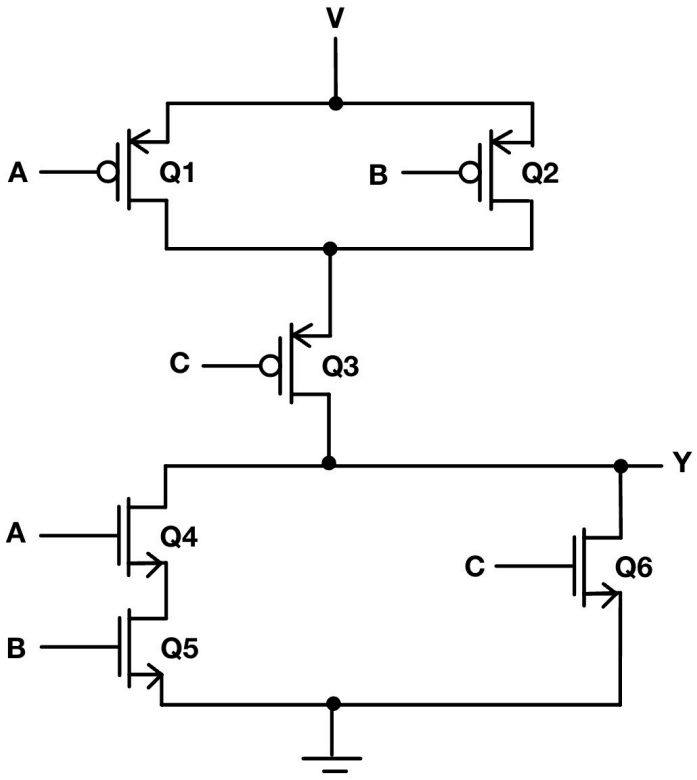
   When $S = 1$, the operation to perform is right shift for input $X = 110$, the output $F = 011$. Note that the bits are shifted right by one position and the least significant bit is dropped and a zero is added in the most significant bit position.

S	$X2$	$X1$	$X0$	$F2$	$F1$	$F0$
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0	1	0	0
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0	0	1	1
1	1	1	1			

(b) (4 points) Implement the output function F with respect to the individual output bits $F0, F1$ and $F2$ using a Programming Logic Array (PLA).



4. (8 points) Consider the transistor circuit below, where the inputs A, B and C are supplied as voltage at the gate of the transistors labelled $Q1$ to $Q6$ as illustrated in the figure. The output from the circuit is Y.



Complete the table below for the output Y and the internal resistance of each transistor $Q1$ to $Q6$ for the inputs A, B and C. The resistance of the transistors should be High or Low (or 'H' or 'L'). The output Y can be 0, 1 or high-impedance Z. You may assume all resistances are accurate when determining the final output Y.

A	B	C	$Q1$	$Q2$	$Q3$	$Q4$	$Q5$	$Q6$	Y
0	0	0	L	L	L	H	H	H	1
0	0	1	L	L	H	H	H	L	0
0	1	0	L	H	L	H	L	H	1
0	1	1	L	H	H	H	L	L	0
1	0	0	H	L	L	L	H	H	1
1	0	1	H	L	H	L	H	L	0
1	1	0	H	H	L	L	L	H	0
1	1	1	H	H	H	L	L	L	0