Homework #8b

Build a circuit to read in an 16-bit KEY using a two-line handshake; the circuit is a passive consumer. The circuit should search an 18kx16 RAM, counting the number of words that match KEY. Assume the RAM is preloaded with data and it can respond to a read request with valid data within one clock. Here is the mini-C to implement:

```
1. while(1) {
2.     while(REQ == 0);
3.     KEY = data;
4.     ACK = 1;
5.     while(REQ == 1);
6.     ACK = 0;
7.     match = 0;
8.     for(i=0; i<1024; i++) {
9.         MBR = RAM[i];
10.        if (MBR == KEY) {
11.            match=match+1;
12.        } // end if
13.    } // end for
14. } // end while
```

Turn in:

- Block diagram of your datapath design.
- State diagram for your control unit design
- The output control word table for your design.
- A testbench and partial datapath VHDL code are provided. The datapath has a partial BRAM instantiation with 1024 16-bit initial data values preloaded. Turn in the final version of the testbench, control unit, and datapath VHDL code you use
- Digital Images of your testbench output simulation plot showing at least the following signals - remove all other signals. One plot should be zoomed in showing all the states of the statemachine executing for the 1st MBR value fetched from memory and another plot showing the entire run for the 1024 values, with the final value for “match”
  - clk
  - reset
  - REQ
  - ACK
  - Data
  - Match
  - MBR
  - i (or address into BRAM)
  - control unit state
  - Status word
  - Control word
- With the testbench providing an initial data value of 0x7FFF, how many matches did you get?