6 Chapter 6 – Basic Sequential Logic Building Blocks

6.1 Helpfull Stuff

Here are the devices introduced in this chapter.

Nomenclature:	N-bit register
Data Input:	N-bits vector $D = d_{N-1} \dots d_1 d_0$.
Data Output:	N-bit vector $Q = q_{N-1} \dots q_1 q_0$
Control:	1-bit c
Status:	none
Others:	1-bit edge-sensitive clock. 1-bit asynchronous active low reset.
Behavior:	

reset	clk	C	D	Q^+	comment
0	x	x	x	0	reset
1	0,1,falling	x	x	Q	hold
1	rising	0	x	Q	hold
1	rising	1	D	D	load

Nomenclature:	N-bit shift register with parallel load
Data Input:	N-bits vector $D = d_{N-1} \dots d_1 d_0$.
Data Output:	N-bit vector $Q = q_{N-1} \dots q_1 q_0$
Control:	2-bits $c = c_1 c_0$
Status:	none
Others:	1-bit edge-sensitive clock. 1-bit asynchronous active low reset.
Behavior:	

reset	clk	C	D	Q^+	comment
0	x	xx	x	0	reset
1	0,1,falling	xx	x	Q	hold
1	rising	00	x	Q	hold
1	rising	01	x	$Q >> 1$	shift right
1	rising	10	x	$Q << 1$	shift left
1	rising	11	x	D	load

Nomenclature:	N-bit counter with parallel load
Data Input:	N-bits vector $D = d_{N-1} \dots d_1 d_0$.
Data Output:	N-bit vector $Q = q_{N-1} \dots q_1 q_0$
Control:	2-bits $c = c_1 c_0$
Status:	none
Others:	1-bit edge-sensitive clock. 1-bit asynchronous active low reset.

Behavior:

reset	clk	C	D	Q^+	comment
0	x	xx	x	0	reset
1	0,1,falling	xx	x	Q	hold
1	rising	00	x	Q	hold
1	rising	01	x	D	count up
1	rising	10	D	D	count up
1	rising	11	x	D	load

Nomenclature:	three state buffer
Data Input:	1-bit X.
Data Output:	1-bit Y
Control:	1-bit c
Status:	none
Others:	none
Behavior:	Output equals input when $C = 1$ otherwise output disconnected from input.

Nomenclature:	NxM RAM (random access memory)
Data Input:	M-bit vector $D = d_{M-1} \dots d_1 d_0$ $log_2(N)$-bit address $A = a_{log_2(N)-1} \dots a_1 a_0$
Data Output:	M-bit vector $D = d_{M-1} \dots d_1 d_0$
Control:	1-bit CS (chip select), RE (Read enable), WE (write enable)
Status:	none
Others:	none

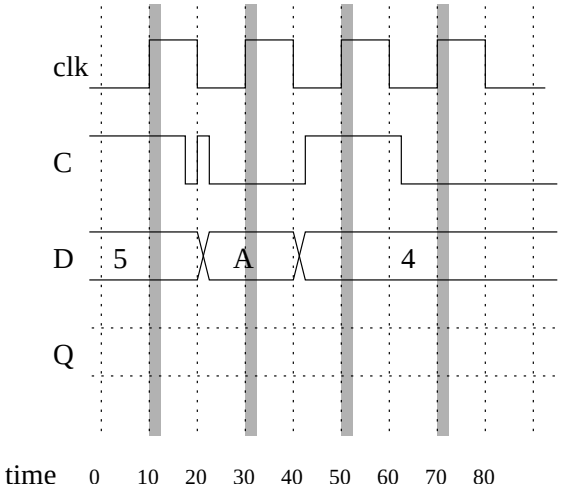
Behavior:

A	CS	RE	WE	D	Note
x	0	x	x	Z	RAM deactivated
x	1	0	0	Z	RAM deactivated
A	1	0	1	D	RAM[A] = D (write)
A	1	1	0	RAM[A]	D = RAM[A] (read)

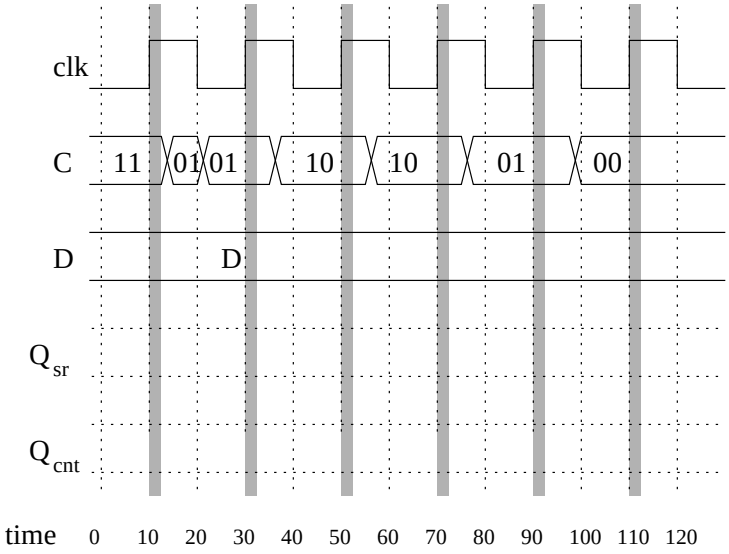
	Left	Right
Arithmetic	$x_2x_1x_00$	$x_3x_3x_2x_1$
Circular	$x_2x_1x_0x_3$	$x_0x_3x_2x_1$
Logical	$x_2x_1x_00$	$0x_3x_2x_1$

6.2 Problems

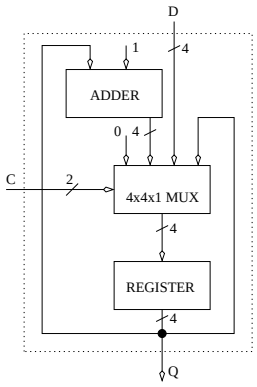
Plot Complete the timing diagram for the register. You may assume that Q is initially 0.



Plot Let Q_{sr} is the output of a logical shift register (assume that 0 is shifted into the vacated bit position. Let Q_{cnt} is the output of a counter.

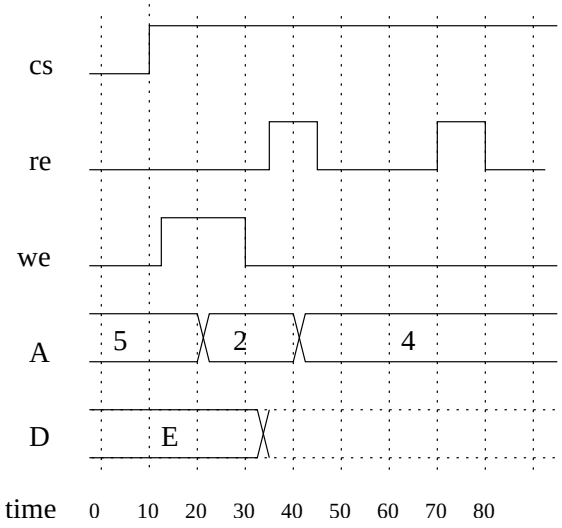


Label the mux inputs. Make the resulting circuit operate according to the truth table shows at left.



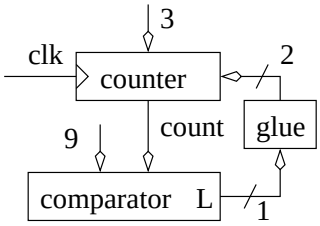
reset	clk	C	D	Q^+	comment
0	x	xx	x	0	reset
1	0,1,falling	xx	x	Q	hold
1	rising	00	x	Q	hold
1	rising	01	x	0	clear
1	rising	10	D	$Q+1$	count up
1	rising	11	x	D	load

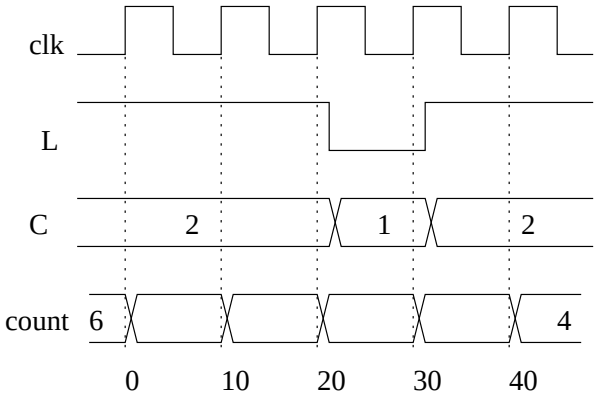
Complete the timing diagram. Note any changes in the RAMs content.



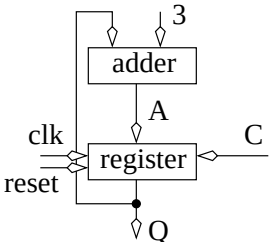
0	0110
1	1010
2	1101
3	0010
4	1000
5	0001
6	1101
7	1111

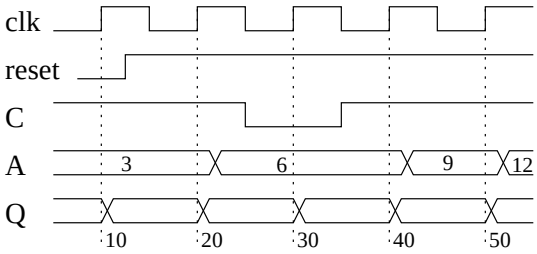
Complete the timing diagram. Use the counter control table from page 128. Assume that c1=L and c0=L'.



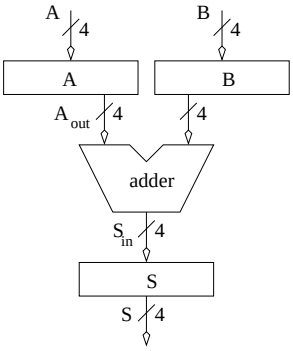


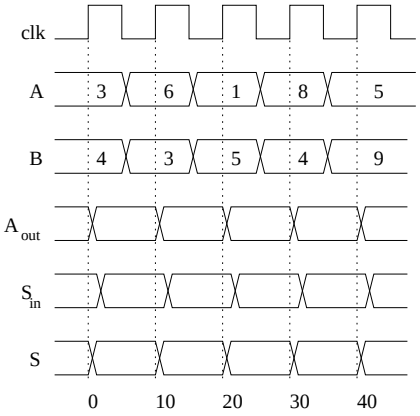
Complete the timing diagram. Put "u" in spaces where the output is undefined.



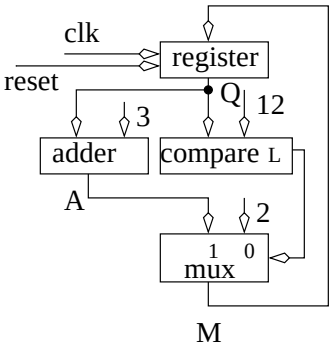


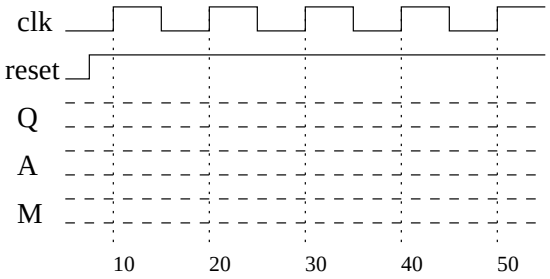
Complete the timing diagram. Put "u' in spaces where the output is undefined.





Complete the timing diagram for the following circuit. Note the labels of the signals.





Complete the timing diagram for the following circuit. Note the labels of the signals.