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-- Date: Jan 15, 2015

-- File: lec05.vhdl

-- HW: Lecture 5

-- Crs: ECE 383

-- Purp: Demo the difference between gates and non-gated outputs

-- Documentation: I pulled some information from chapter 8.

-- Academic Integrity Statement: I certify that, while others may have

-- assisted me in brain storming, debugging and validating this program,

-- the program itself is my own work. I understand that submitting code

-- which is the work of other individuals is a violation of the honor

-- code. I also understand that if I knowingly give my original work to

-- another individual is also a violation of the honor code.

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

entity lec5 is

Port( clk: in STD\_LOGIC;

reset : in STD\_LOGIC;

btn: in STD\_LOGIC\_VECTOR(4 downto 0);

JB: out STD\_LOGIC\_VECTOR(7 downto 0));

end lec5;

architecture behavior of lec5 is

signal processQ: unsigned (7 downto 0);

constant L0: unsigned(7 downto 0) := "00101111";

constant L1: unsigned(7 downto 0) := "01011111";

constant L2: unsigned(7 downto 0) := "10111111";

begin

process(clk)

begin

if (rising\_edge(clk)) then

if (reset = '0') then

processQ <= (others => '0');

elsif (btn(4) = '0') then

processQ <= processQ + 1;

end if;

end if;

end process;

process(clk)

begin

if (rising\_edge(clk)) then

if (reset = '0') then

JB(6 downto 4) <= "000";

elsif ((processQ >= 0) and (processQ < L0)) then

JB(6 downto 4) <= "001";

elsif ((processQ >= L0) and (processQ < L1)) then

JB(6 downto 4) <= "010";

elsif ((processQ >= L1) and (processQ < L2)) then

JB(6 downto 4) <= "100";

elsif (processQ >= L2) then

JB(6 downto 4) <= "111";

end if;

end if;

end process;

JB(7) <= clk;

JB(3 downto 0) <= "0001" when ((processQ >= 0) and (processQ < L0)) else

"0010" when ((processQ >= L0) and (processQ < L1)) else

"0100" when ((processQ >= L1) and (processQ < L2)) else

"1000";

end behavior;