# Name: Section:

# Homework Assignment: submit via gradescope

1. [3.5] Assume that a is a 10-bit signal with the std\_logic\_vector(9 downto 0) data type. List the 10 bits assigned to the a signal following each operation below.
   1. a <= (others => ‘1’);
   2. a <= (1|3|5|7|9 => ‘1’, others => ‘0’);
   3. a <= (9|7|2 => ‘1’, 6 => ‘0’, 0 => ‘1’, 1|5|8 => ‘0’, 3|4 => ‘0’);
2. [3.6] Assume that a and y are 8-bit signals with the std\_logic\_vector(7 downto 0) data type. If the signals are interpreted as unsigned numbers, the following assignment statement performs a / 8. Explain.

y <= “000” & a(7 downto 3);

1. [3.7] Assume the same a as in Problem above. We want to perform a mod 8 and assign the result to y. Rewrite the previous signal assignment statement using only the & operator.
2. Draw a hardware schematic, similar to the one at the end of lecture 3, for the following circuits. You are given comparators, muxes and adders; do NOT show the internal organization of these devices. Whenever possible reduce the number of devices required to realize the design. You should assume that X, Y, and Z are unsigned(7 downto 0).
3. if (X==0) then Z = X else Z = Y
4. if (X==Y) then Z = Y else Z = X+Y
5. if (X < Y) then Z = X+4 else Z = Y+6
6. if (X > Y) then Z = X+5 else Z = X+6
7. In VHDL, create a digital circuit that takes as input a 8-bit unsigned value (provided by the DIP switches) and illuminates an LED if the input is a multiple of 17. Do NOT use the remainder or division operations. This can easily be accomplished using a single conditional signal assignment statement.
   1. Upload your VHDL file (include a proper header) to bitbucket.
   2. Upload a testbench and simulation timing diagram testing several inputs and showing the output. [do not need to test all possibilities]
   3. Upload your UCF file to Bitbucket.
   4. Demo your circuit either with a video (uploaded to Streams) or in class on LSN 4.