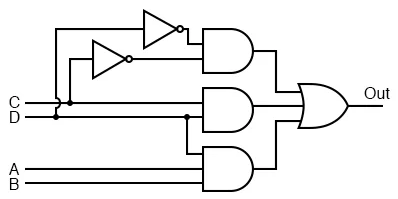
# Name: Section:

# Homework Assignment: submit via gradescope

1. Crusty the engineer is a well-intentioned employee in your organization who, unfortunately, is caught in some kind of 70's time warp. Crusty is convinced that a FSM built using discrete logic gates will outperform your shiny new 100Mhz FPGA design. Arguing with Crusty has come to nothing and its time to put an end to this once and for all. You are going to do the calculations to see how fast a discrete logic gate realization can run.

You are to build the FSM using the architecture given in Lecture 9. Use the positive edge triggered flip flops inside the SN74LS273N chip, and the AND, OR and NOT gates inside the SN74LS08N, SN74LS32N, and SN74LS04N chips respectively. You are to assume that the logic inside the MIE and OE boxes are 2-level combinational logic such as the example circuit below (note: 2-level logic actually needs a 3rd level for the inverters).



To save you time from looking up the chips timing specs from sites like Digi-Key, use these values:

SN74LS273N D flip flop setup time = 20nS

hold time = 5nS

propagation delay = 27nS

SN74LS08N AND propagation delay = 27nS

SN74LS32N OR propagation delay = 22nS

SN74LS04N NOT propagation delay = 22nS

Show your work for partial credit.

* 1. Calculate the minimum clock period and the maximum clocking frequency designing the FSM with these digital logic chips:
  2. What is the minimum clock period and the maximum clocking frequency designing the FSM with a 100Mhz FPGA?
  3. Which can run faster, the discrete logic realization or the 100Mhz FPGA realization? How much faster?
  4. Check out the [Logic Families](http://en.wikipedia.org/wiki/Logic_family) entry on Wikipedia (<https://en.wikipedia.org/wiki/Logic_family>). Excluding the G series, what TTL family type should have the highest clocking rate?
  5. Provide a rough estimate of the clocking frequency of a FSM built from this type of logic (the logic family you choose in part d). Making sure to show your calculation.
  6. List How does the speed of the FSM in part e compare to using a 100MHz FPGA?

1. Complete the timing diagram below assuming that the register is positive edge trigger and has an asynchronous active low reset.

