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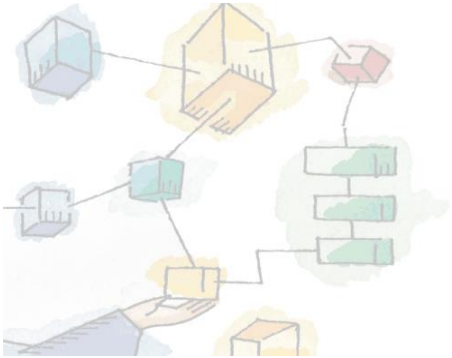
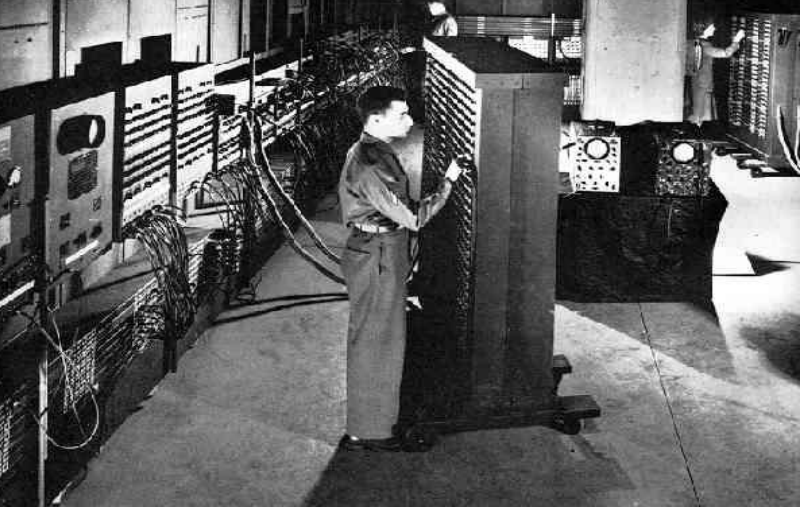
Chapter 1
Computer System Overview

Operating Systems:
Internals and Design Principles, 9/E
William Stallings



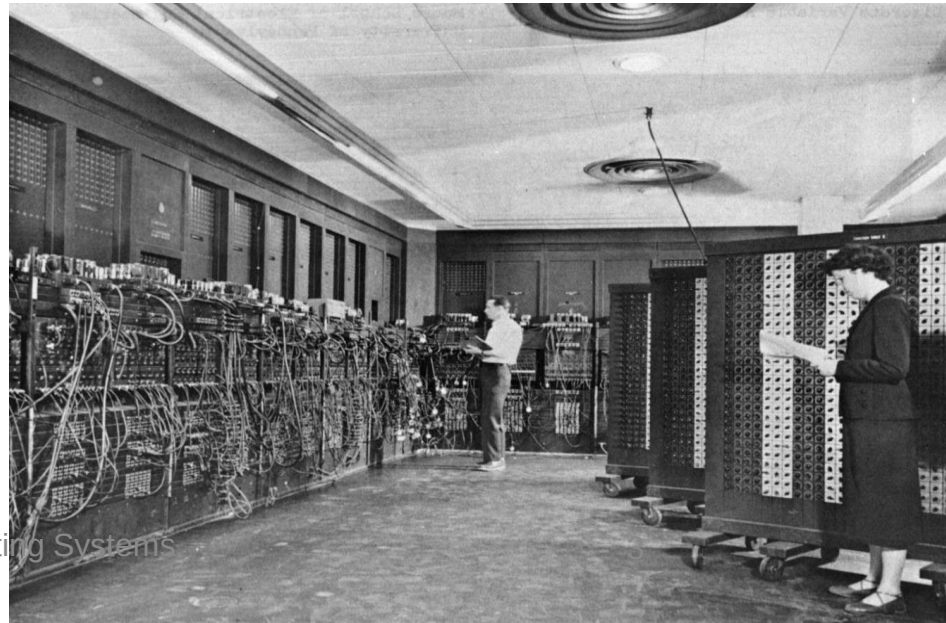
Roadmap

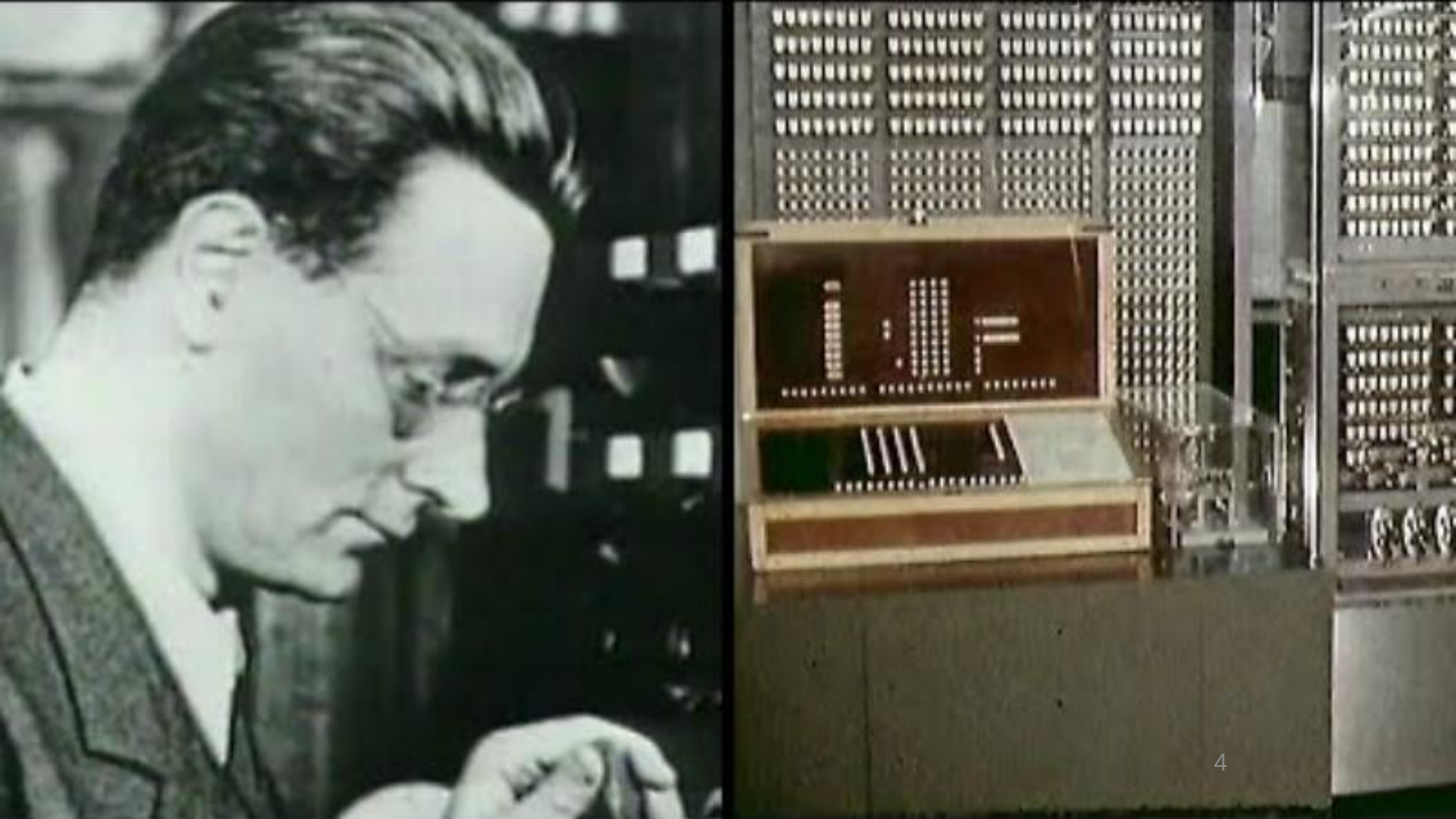
- **History**
- Basic Elements
- Processor Registers
- Instruction Execution
- Interrupts
- The Memory Hierarchy
- Cache Memory
- I/O Communication Techniques



Eniac (1946-1955)

- **Specs**
- 30 short tons (27,000 kg)
- 2.6 m × 0.9 m × 24 m
- 150 kW of power
- 5KHz clock: 5000 adds / mul per sec
- 36 vacuum tubes / decimal digit
- several tubes burned out almost every day
- programming: 6 women (no men)





Konrad Zuse's z23 (1960)

Flex-O-writer (1965)

http://www.cs.utexas.edu/users/EWD/transcriptions/EWD01xx/EWD139.html

Punch tapes or punch cards, Dijkstra goes for punch tapes +/- 1965

Time sharing – Teletype (1970)

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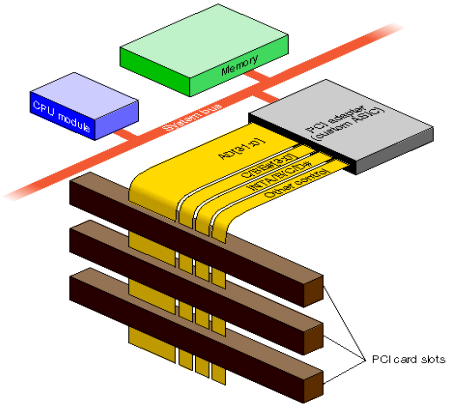
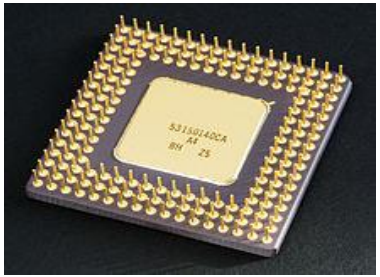
Operating System

- Exploits the hardware resources of one or more processors
- Provides a set of services to system users
- Manages secondary memory and I/O devices

A Computer's basic Elements

- Processor
- Main Memory
- I/O Modules
- System Bus






Lets see this video for
better
understanding...

Top-Level View

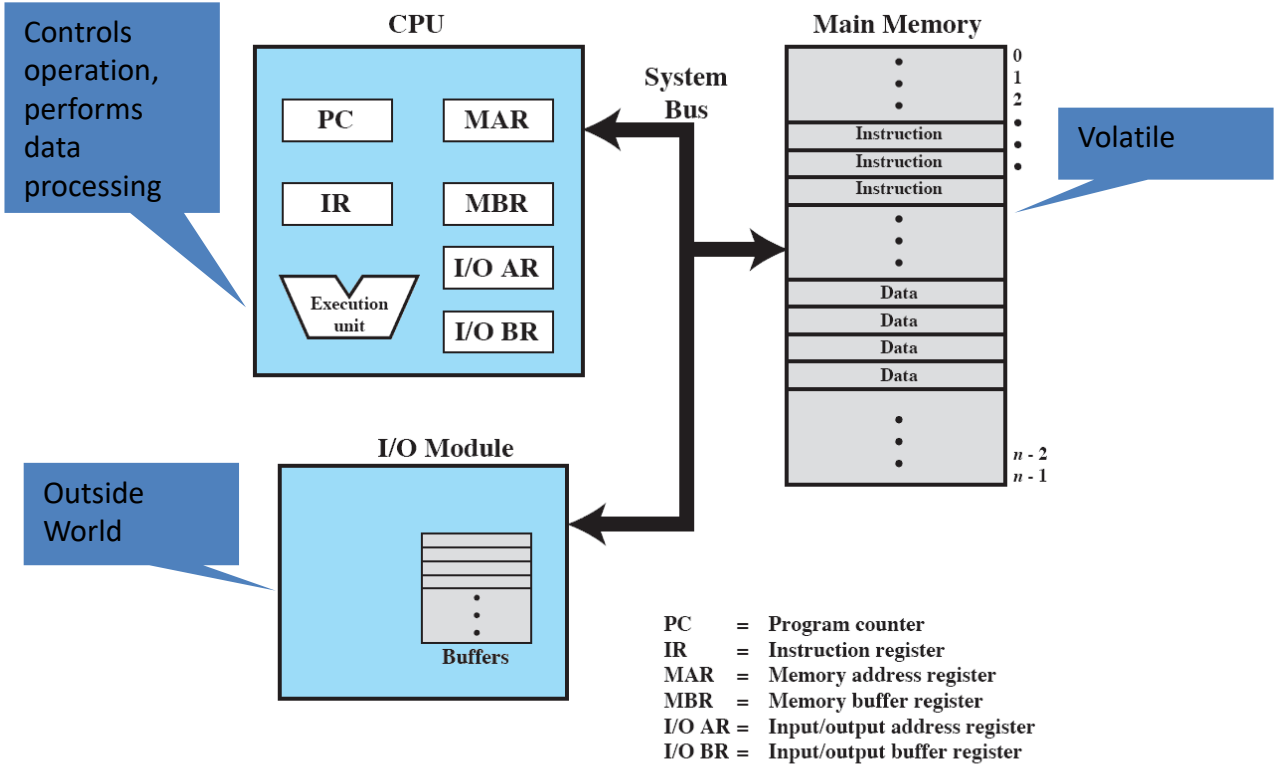


Figure 1.1 Computer Components: Top-Level View

Roadmap

- History
- Basic Elements
- **Processor Registers**
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Registers

- PC
- IR
- PSW

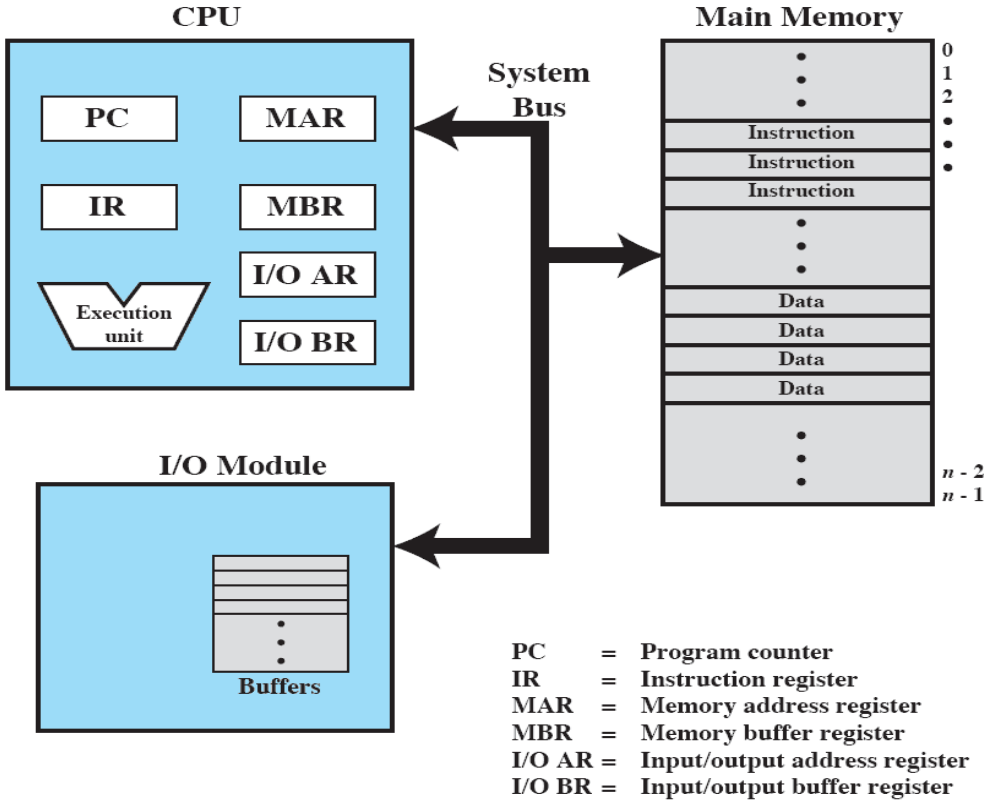

Figure 1.1 Computer Components: Top-Level View

Roadmap

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Basic Instruction Cycle

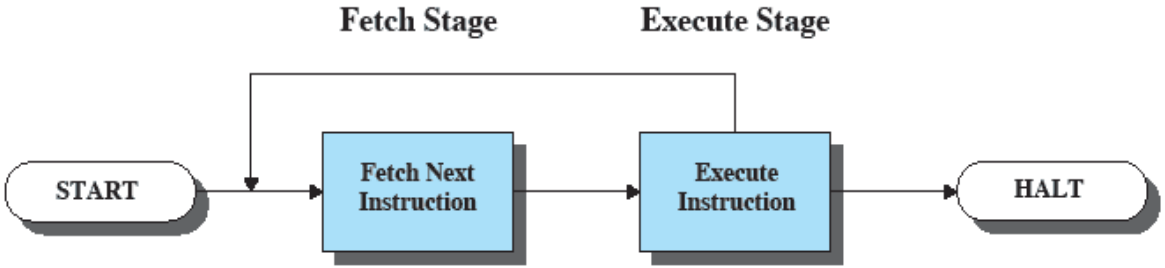
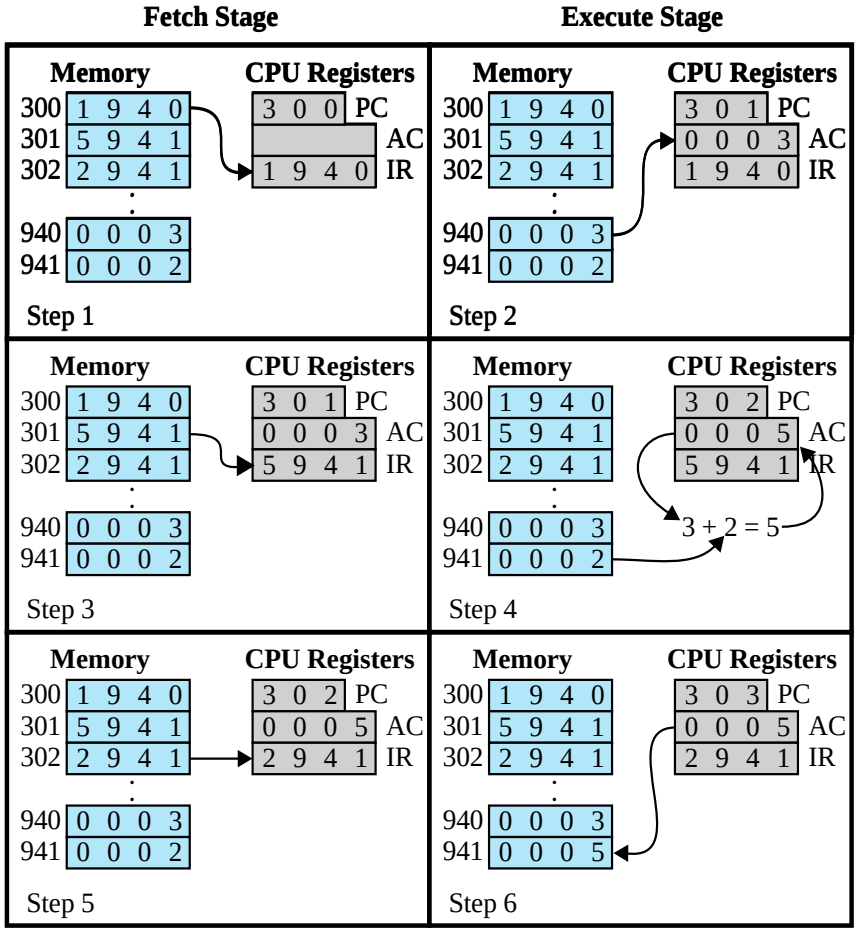


Figure 1.2 Basic Instruction Cycle

Program Execution

1. PC 300 → Load in IR
2. Load 940 in AC
3. PC 301 → Load in IR
4. Add 941 and AC → Put in AC
5. PC 302 → Load in IR
6. Put AC in 941



Roadmap

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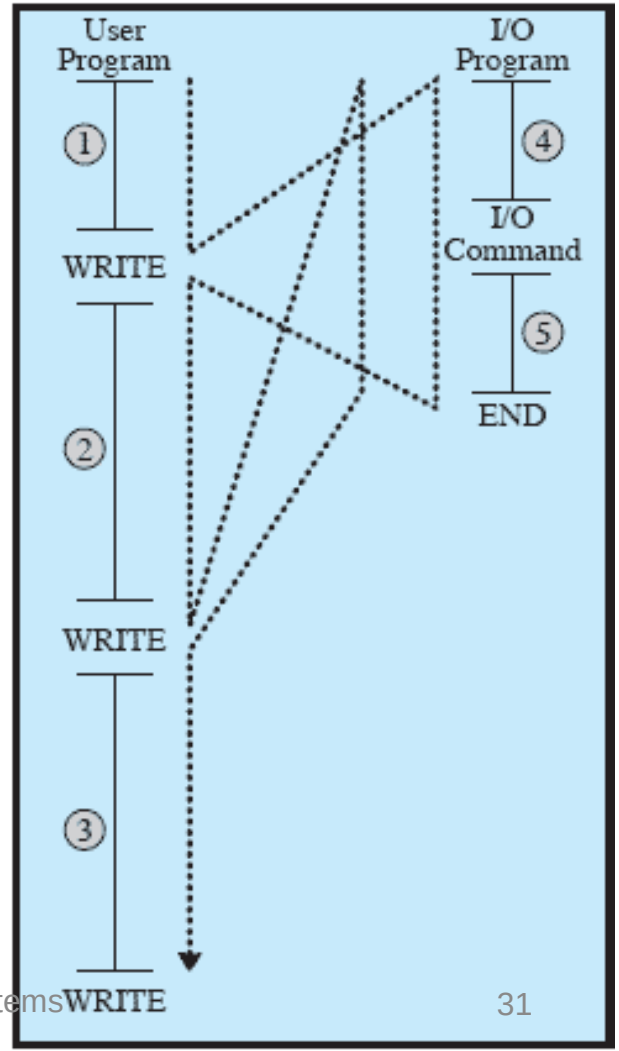
Interrupts

Table 1.1 Classes of Interrupts

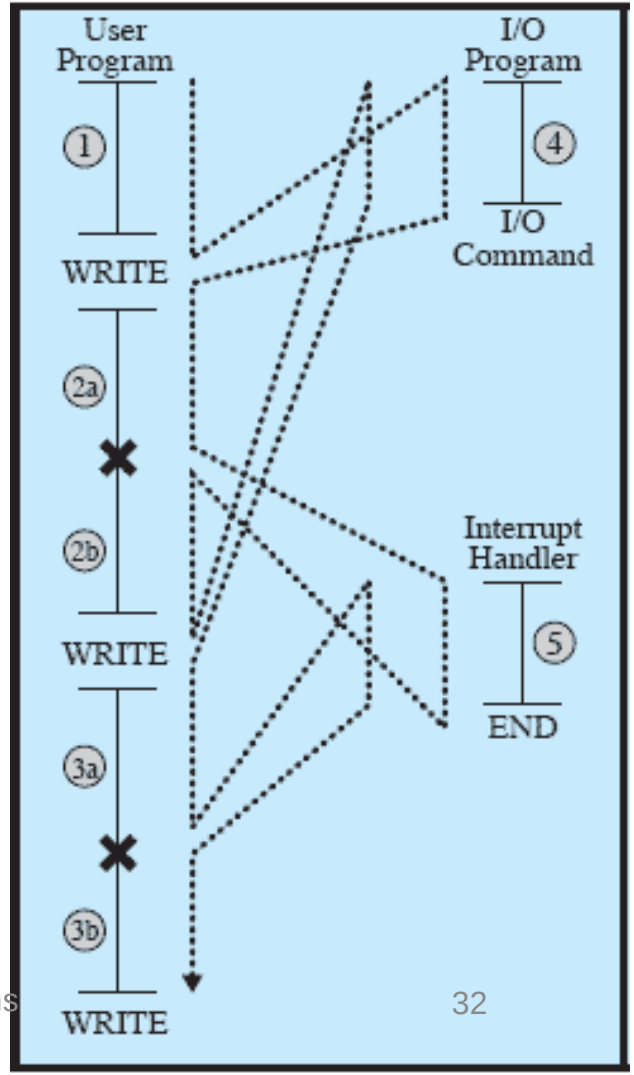
Program	Generated by some condition that occurs as a result of an instruction execution, such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction, and reference outside a user's allowed memory space.
Timer	Generated by a timer within the processor. This allows the operating system to perform certain functions on a regular basis.
I/O	Generated by an I/O controller, to signal normal completion of an operation or to signal a variety of error conditions.
Hardware failure	Generated by a failure, such as power failure or memory parity error.

Flow of Control without Interrupts



(a) No interrupts

Interrupts and the instruction Cycle



Transfer of Control via Interrupts

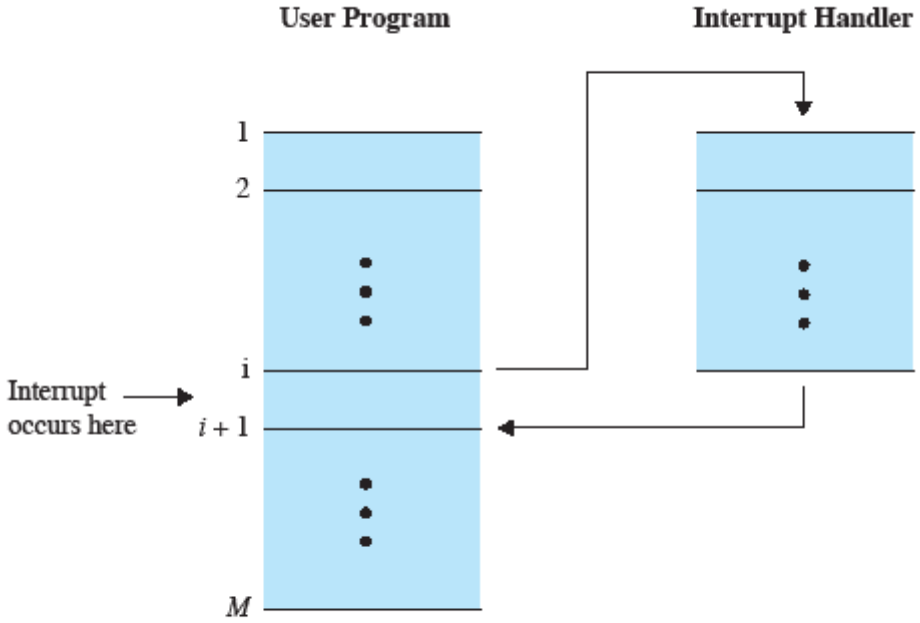
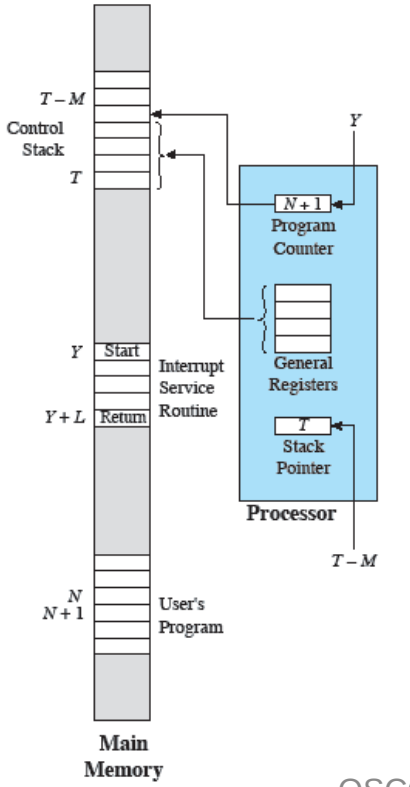
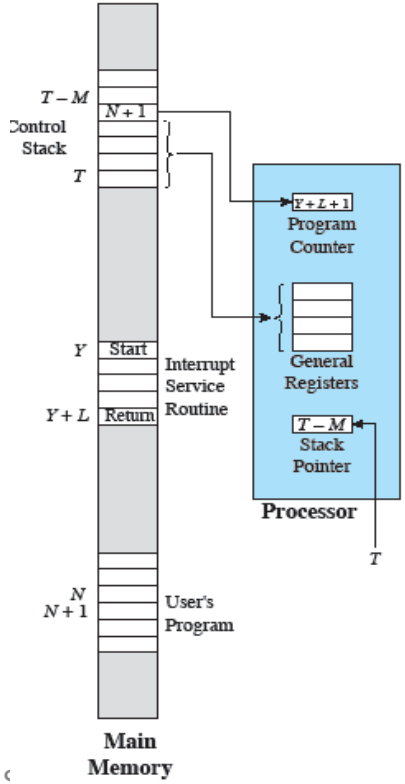


Figure 1.6 Transfer of Control via Interrupts

Changes in Memory and Registers for an Interrupt



(a) Interrupt occurs after instruction at location N

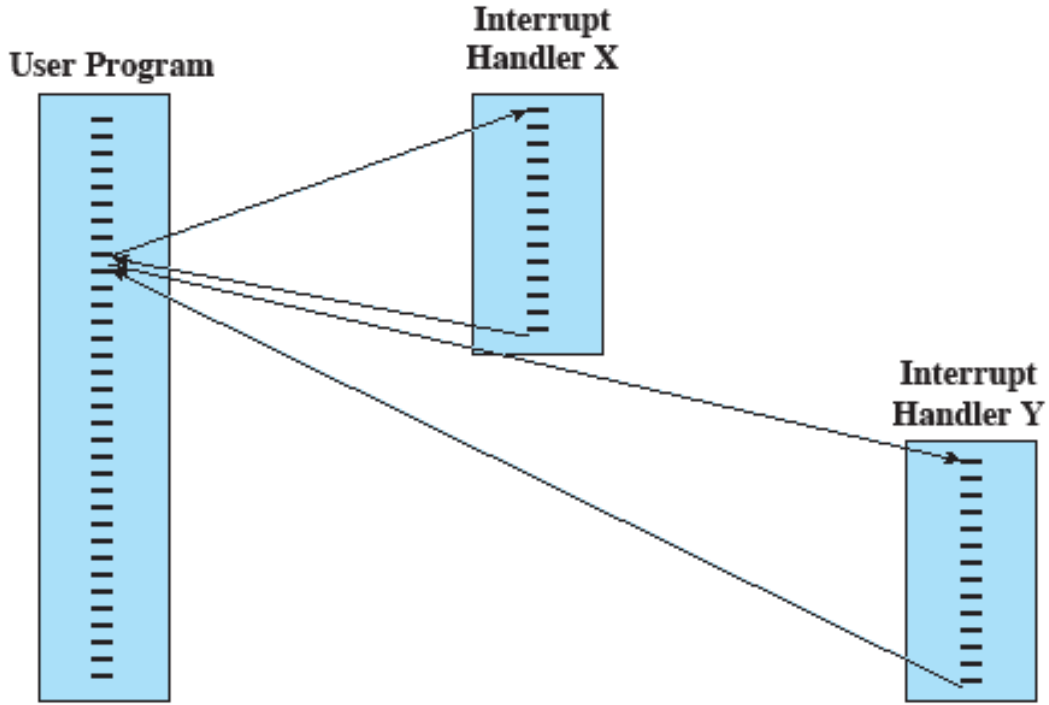


(b) Return from interrupt

Multiple interrupts

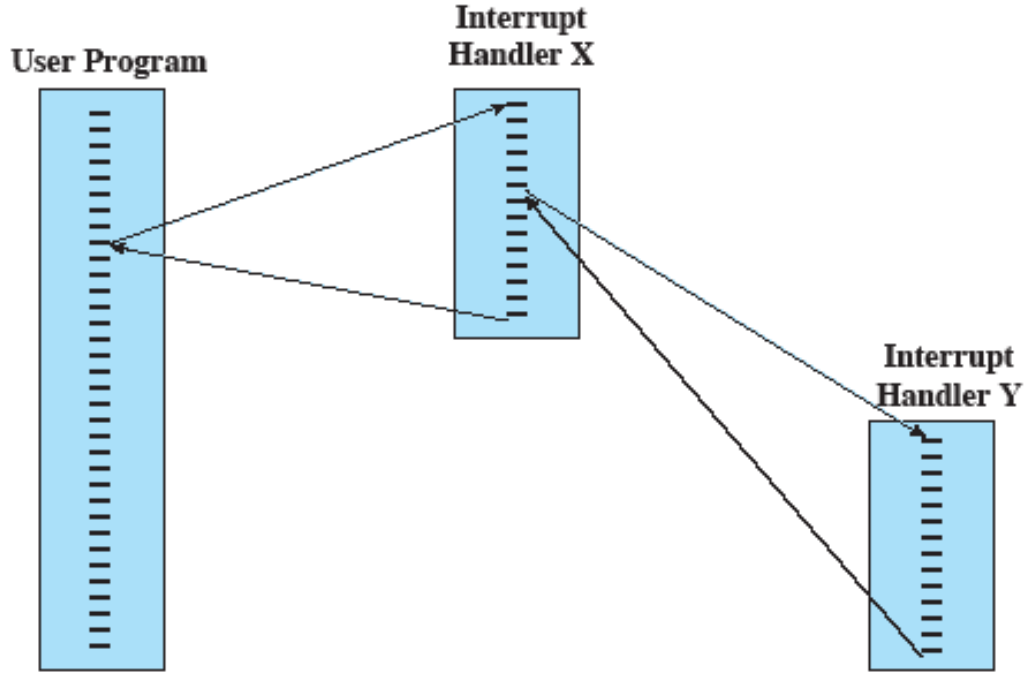
- When can that happen?
- How can we handle them?

Sequential Interrupt Processing



(a) Sequential interrupt processing

Nested interrupt Processing



(b) Nested interrupt processing

Roadmap

- History
- Basic Elements
- Processor Registers
- Instruction Execution
- Interrupts
- **The Memory Hierarchy**
- Cache Memory
- I/O Communication Techniques

The Memory Hierarchy

- Going down the hierarchy
  - Decreasing cost per bit
  - Increasing capacity
  - Increasing access time
  - Decreasing frequency of access to the memory by the processor

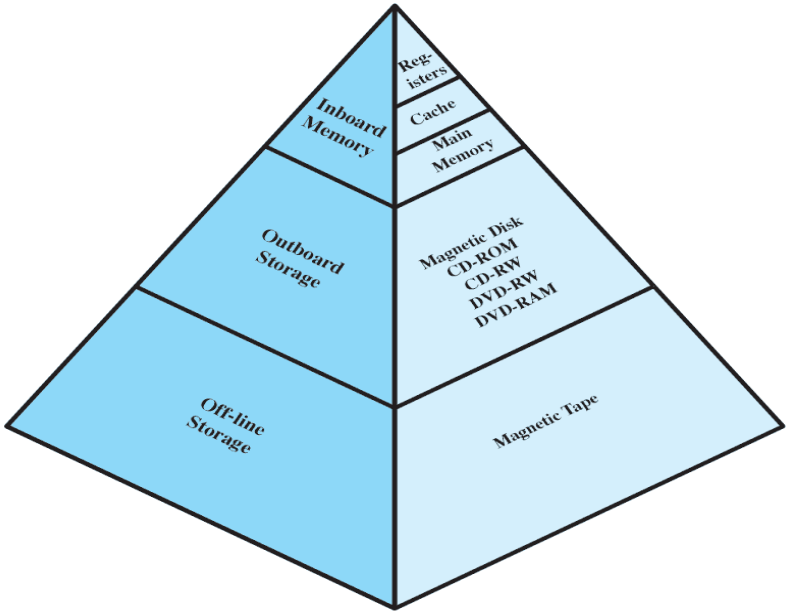


Figure 1.14 The Memory Hierarchy

Roadmap

- History
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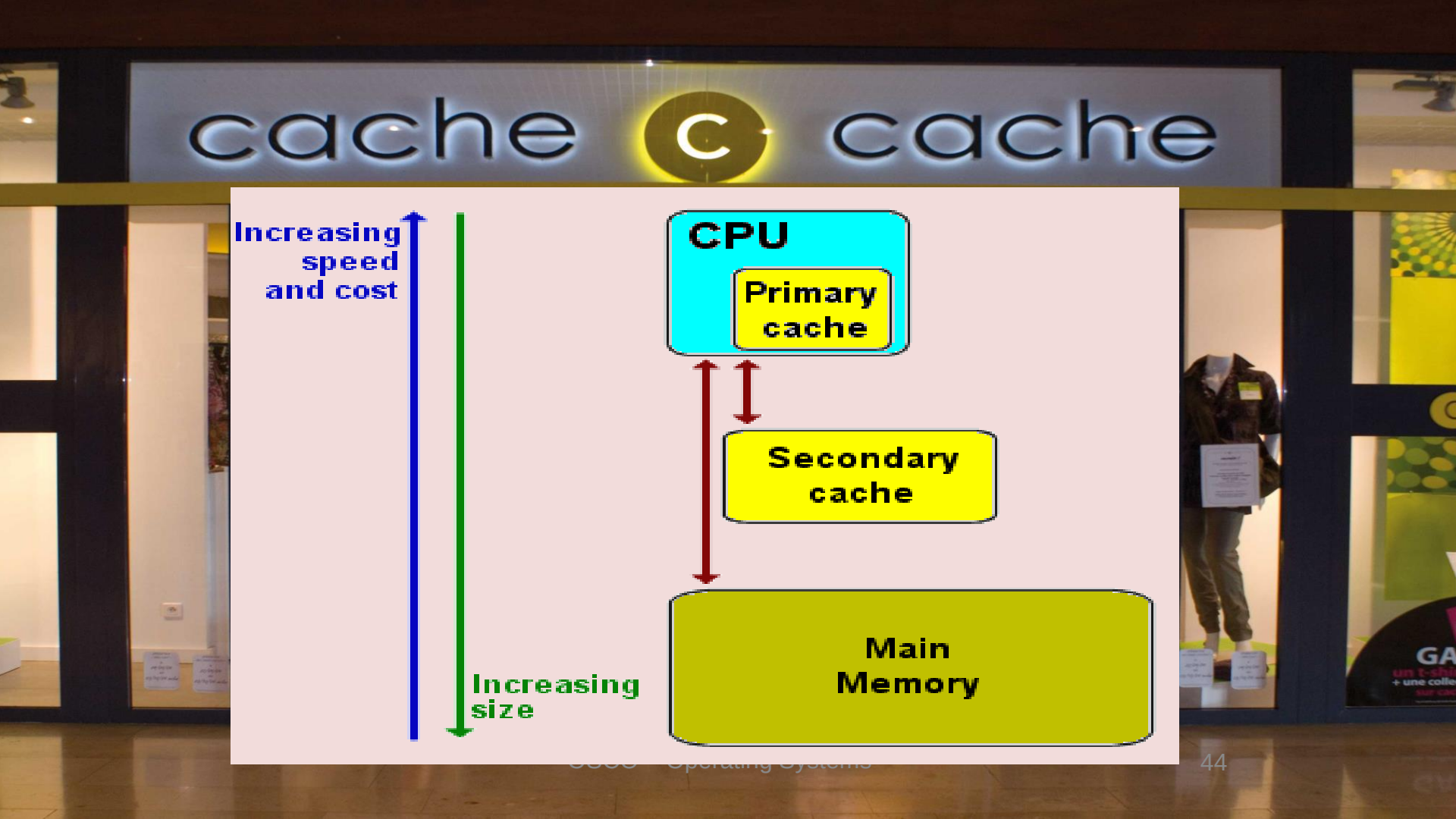
- **Cache Memory**
- I/O Communication Techniques


cache
cache
Increasing speed and cost
Increasing size
CPU
Primary cache
Secondary cache
Main Memory

Principal of Locality

More details later but in short …

Data which is required soon is often close to the current data

- If data is referenced, then it's neighbour might be needed soon.

Cache and Main Memory

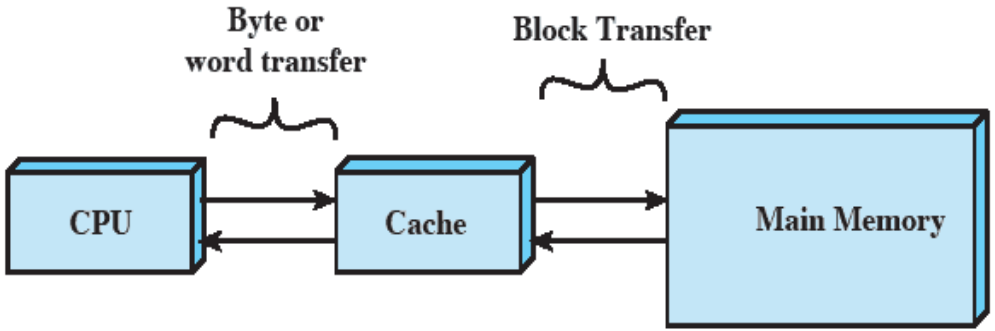
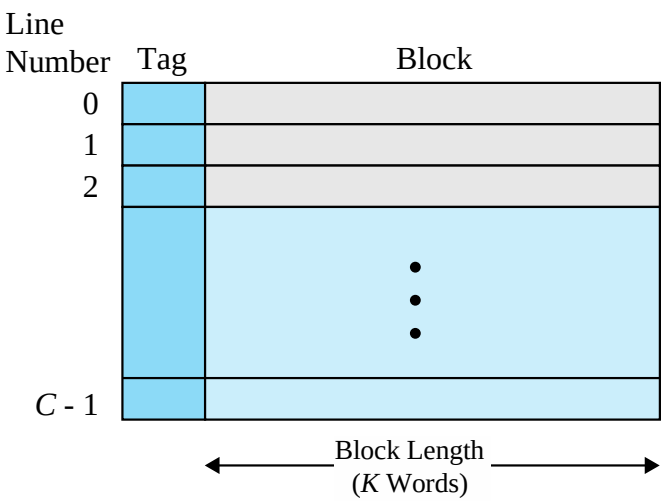
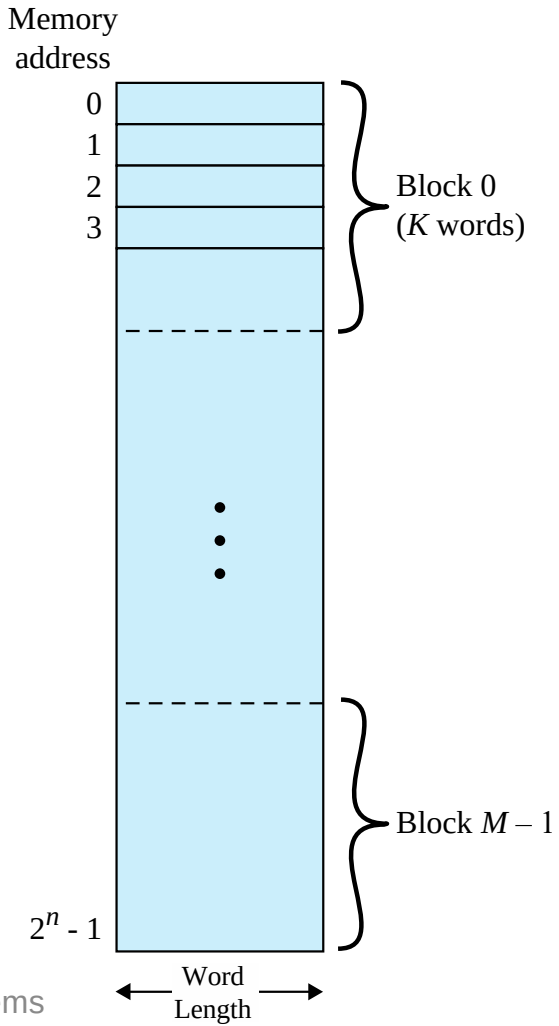


Figure 1.16 Cache and Main Memory

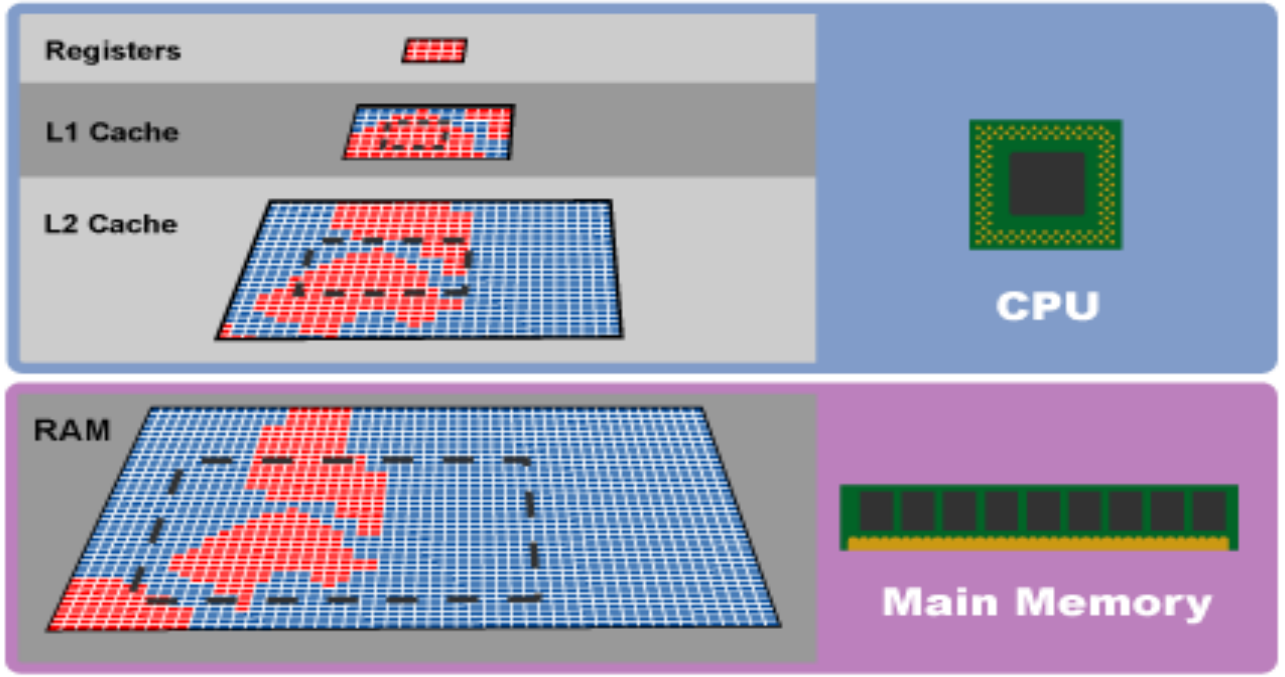


(a) Cache



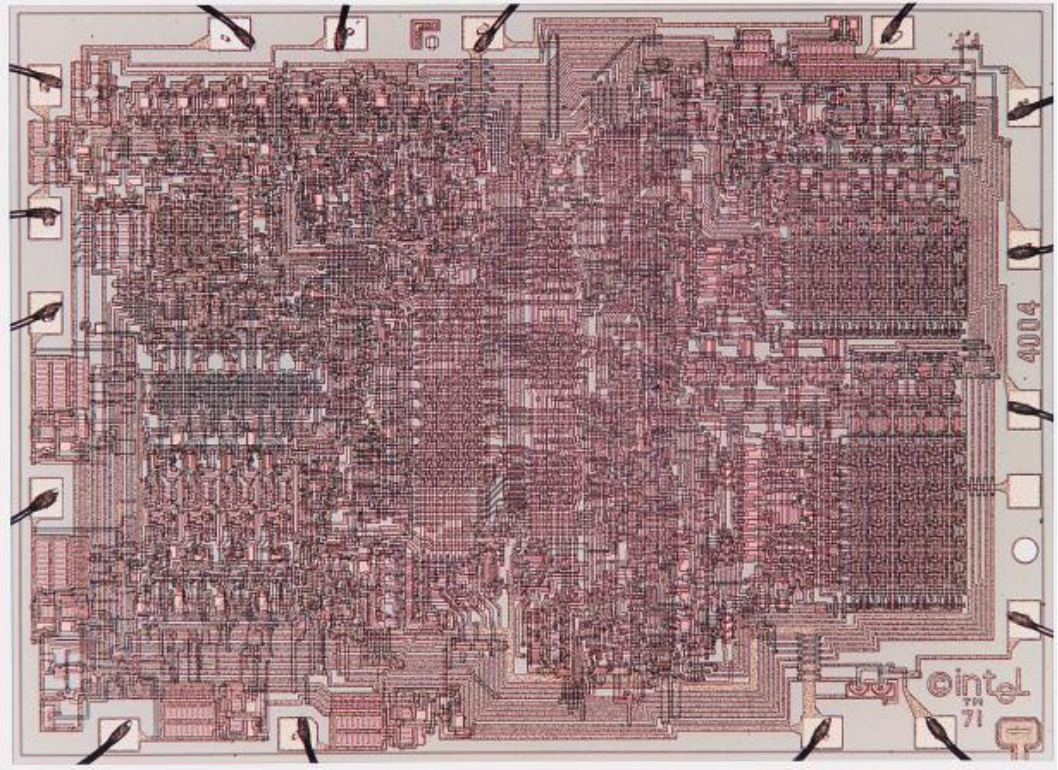
(b) Main memory

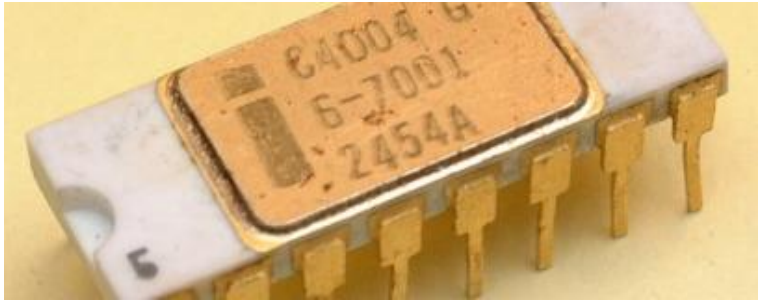
Caches and main memory

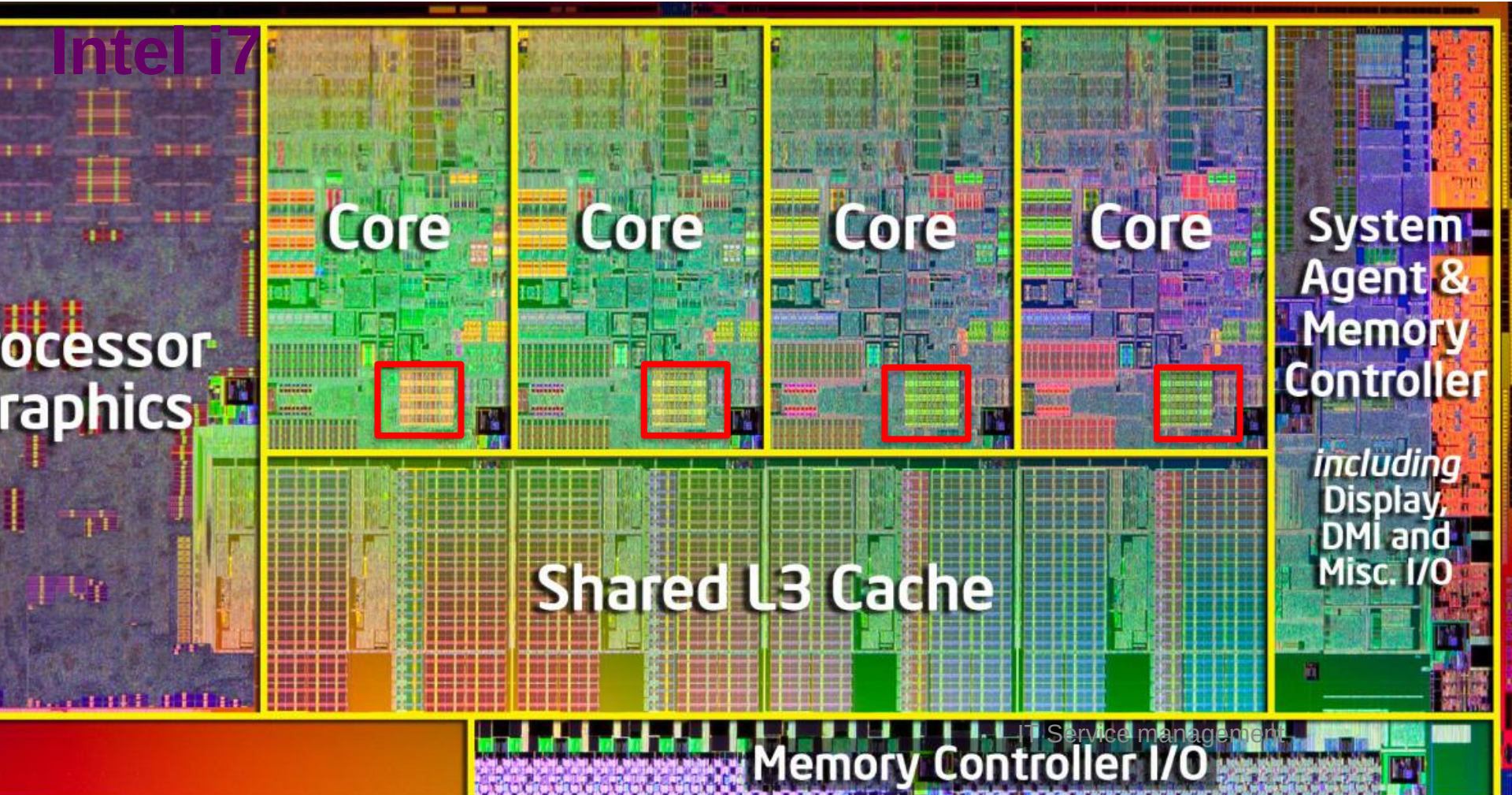


What are design issues?

Intel 4004






Intel i7
ocessor
raphics
Core
Core
Core
Core
System Agent & Memory Controller
including Display, DMI and Misc. I/O
Shared L3 Cache
Memory Controller I/O

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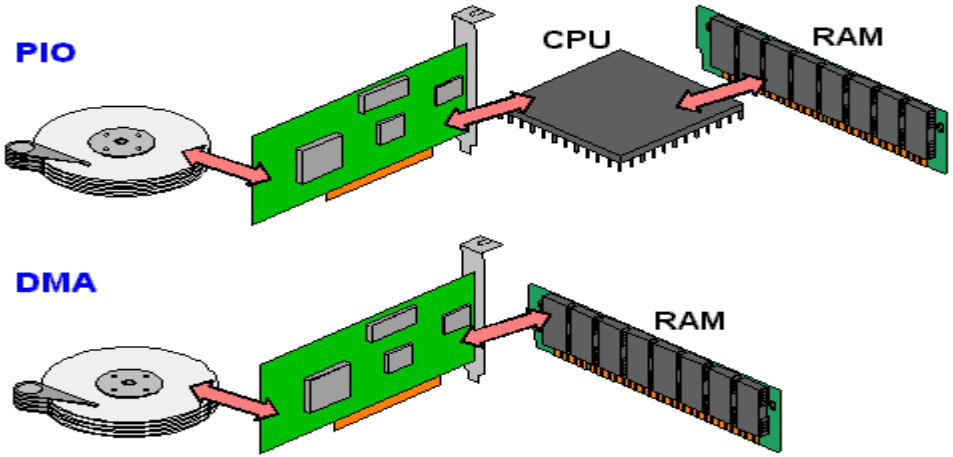
I/O Techniques

- Programmed I/O
- Interrupt-driven I/O
- Direct memory access (DMA)



Questions?