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Computer Interfacing and Peripheral Equipment
Laboratory Exercise 03b
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Lab Objective:

Interfacing with Schmitt trigger, Open-Collector and Tri-State Gates

Material:

- **TTL logic gates: 74LS14 (Schmitt Trigger Inverter). 74LS05 – 06 (Open Collector Inverter), 74LS125 – 126 (Tri-State Buffers)**
- **CMOS logic gates: CD4069 (Totem-Pole Inverter). CD40106 (Schmitt Trigger Inverter)**
- **ULN2003 as an High Powered Open-Collector device**
- **Function Generator, Power supply, Multimeter**
- **12V Relay and Light Bulb**
- **1 Breadboard**

Part 1 (Schmitt trigger): Most CMOS, BiCMOS and TTL devices require fairly fast edges on the high and low transitions on their inputs. If the edges are too slow they can cause excessive current, oscillation and even damage the device. Slow edges are sometimes hard to avoid at power up or when using push button or manual type switches with the large capacitors needed for filtering. Heavily loaded outputs can also cause input rise and fall time to be out of spec for the next part down the line.

The solution to these problems is to use a Schmitt trigger type device to translate the slow or noisy edges into something faster that will meet the input rise and fall specs of the following device. A true Schmitt trigger input will not have rise and fall time limitations.

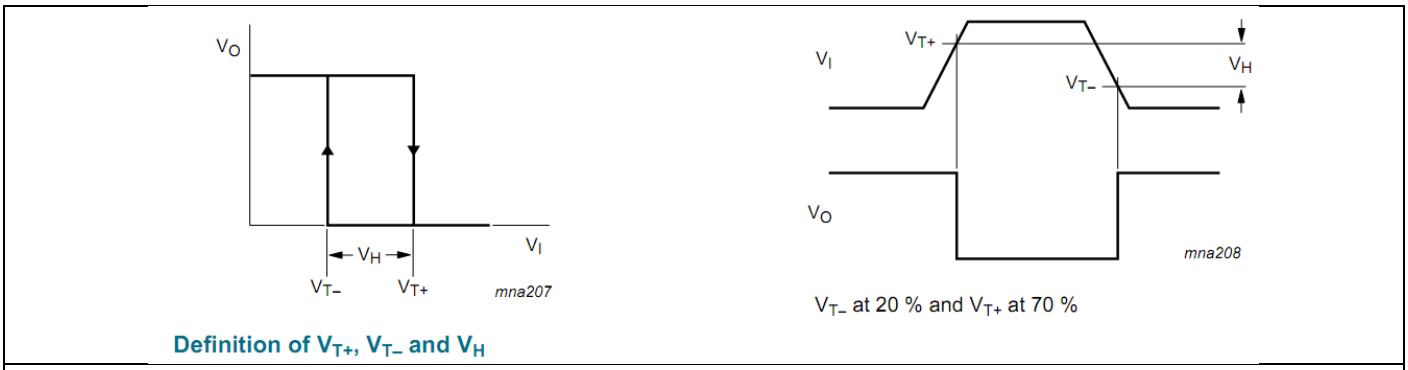
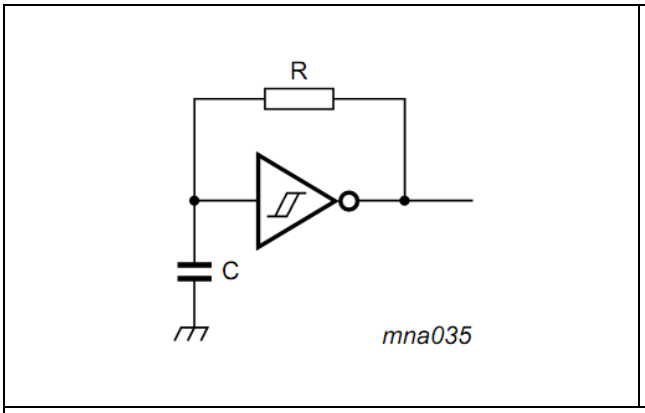


Fig 1: Waveforms for a Schmitt Trigger Inverter. V_{T+} (Positive Voltage Threshold), V_{T-} (Negative Voltage Threshold), V_H (Voltage Hysteresis)

Assemble and try the following applications:



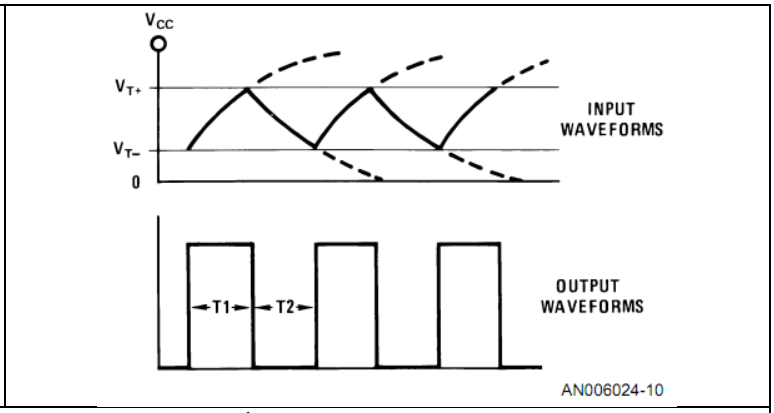


Fig 2: Relaxation Oscillator. $Fout \approx {}^{1}/_{0.7RC}$

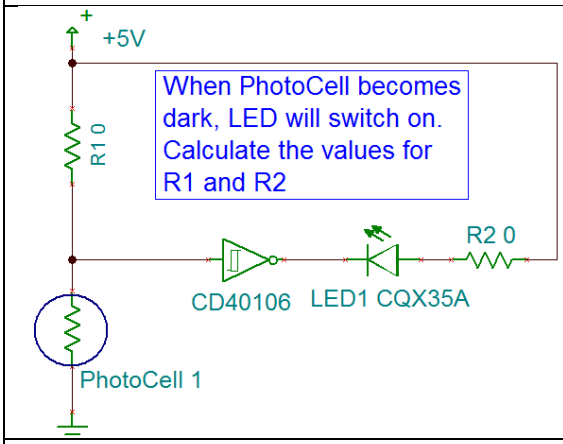


Fig 3: Light Sensor

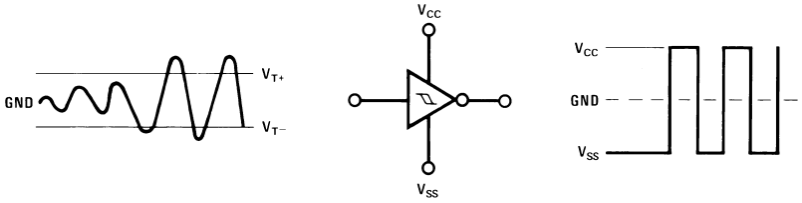


Fig 4: Convert any Waveform to a Square Wave

Part 2 (Open-Collector or Open-Drain): Open-collector devices are totem pole outputs where the upper output (usually a Darlington transistor) is left out of the circuit. As such, these devices have no active logic high drive and cannot be used to drive a line high. The advantage to open-collector devices is that a number of outputs can be directly tied together.

When dealing with open-collector devices, it must be noted that each output requires a resistive pull-up, usually tied to V_{CC}. (By using high voltage outputs, one can tie the resistor pull-up to a voltage higher than V_{CC}.) Designers often try to get away with tying the output to an input and relying on the I_{IL} current to pull up the output. This is unwise, as it is just like leaving inputs floating: the input is very susceptible to noise and can easily give false signals. Shown below are two equations that can be used to determine the min/max range of the pull-up resistor.

$$R_{MAX} = \frac{(V_{CC(MIN)} - V_{OH})}{(N1 \bullet I_{OH} + N2 \bullet I_{IH})}$$

$$R_{MIN} = \frac{(V_{CC(MIN)} - V_{OL})}{(I_{OL} - N2 \bullet I_{IL})}$$

where: N1 = the number of open-collector devices tied together,

N2 = the number of inputs being driven on the line.

$$Vc = Vcc\left(1 - e^{-\frac{t}{\tau}}\right) \therefore -\frac{t}{\tau} = \ln\left(1 - \frac{Vc}{Vcc}\right) \therefore t = -\tau * \ln\left(\frac{Vc}{Vcc}\right)$$

For the Fig 2:

The circuit have a resistor of $R = 1K\Omega$ and a capacitor of $C = 0.01\mu F$. The frequency is equal to $f = \frac{1}{\tau}$. Also, by the datasheets, we can have the following values:

	CMOS	TTL
V_{OH}	5V	3.4V
V_{OL}	0V	0.35V
V_{T+}	3.6V	1.6V
V_{T-}	1.4V	0.8V

Considering the capacitor time (rise and fall) varying with supply voltage and considering that is t_1 and t_2, after clearing, we got the next equations to solved; also, considering the values from the previous table. (Curd, 2015)

$$f = \frac{1}{T}$$

$$T = t_1 + t_2$$

$$\tau = time\ constant\ RC$$

To get the rise time, the formula will be:

For the CD40106: $T_r = t_1 = \tau \ln\left(\frac{V_{OH}-V_{T-}}{V_{OH}-V_{T+}}\right) = (1K\Omega)(0.01\mu F) * \ln\left(\frac{5V-1.4V}{5V-3.6V}\right) = 9.44\mu s$

For the 74LS14: $T_r = t_1 = \tau \ln\left(\frac{V_{OH}-V_{T-}}{V_{OH}-V_{T+}}\right) = (1K\Omega)(0.01\mu F) * \ln\left(\frac{3.4V-0.8V}{3.4V-1.6V}\right) = 3.67\mu s$

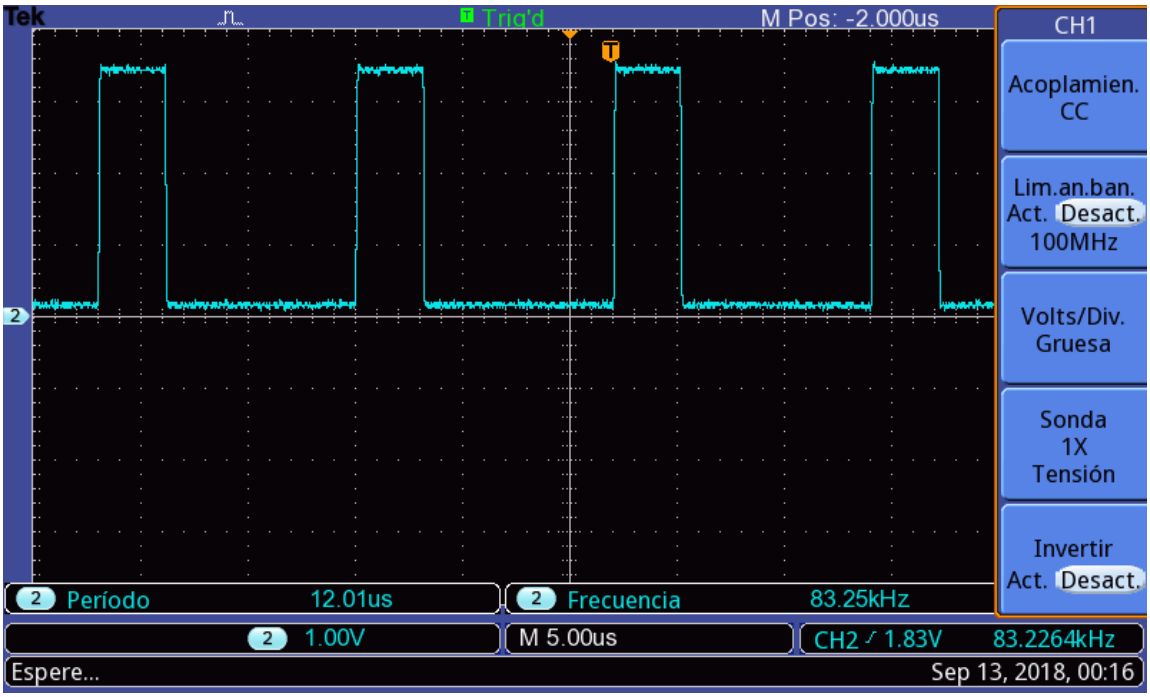
To obtain the fall:

For the CMOS: $T_f = t_2 = \tau \ln\left(\frac{V_{T+}-V_{OL}}{V_{T-}-V_{OL}}\right) = (1K\Omega)(0.01\mu F) * \ln\left(\frac{3.6V-0}{1.4V-0}\right) = 9.44\mu s$

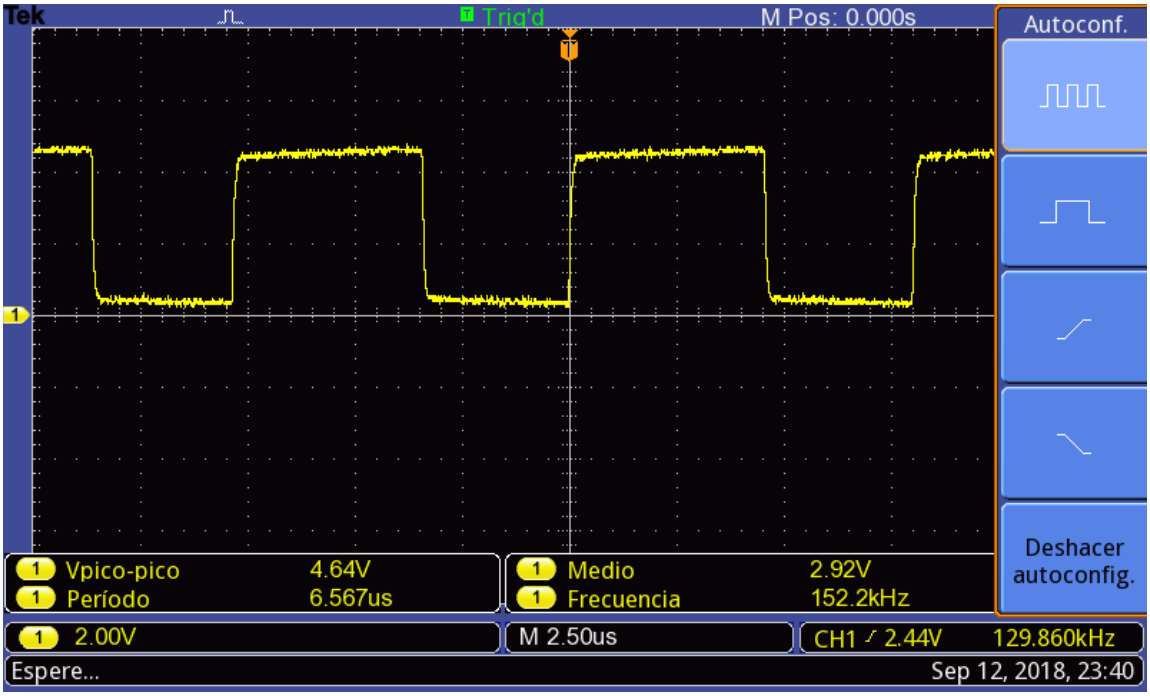
For the TTL: $T_f = t_2 = \tau \ln\left(\frac{V_{T+}-V_{OL}}{V_{T-}-V_{OL}}\right) = (1K\Omega)(0.01\mu F) * \ln\left(\frac{1.6V-0.35V}{0.8V-0.35V}\right) = 10{,}22\mu s$

Rise plus fall will give us the t_1 and t_2, corresponding to the output waveform. The output waveform would be as the following picture of the oscilloscope.

For the TTL (74LS14):



And for the CMOS (CD40106):



For Fig 3:

First, we calculate the value for R2 and would be $R2 = \frac{5V-2.2V-0.35V}{8mA} \approx 330\Omega$.

To get the photocell resistor, we have a certain light intensity and we measure the output resistor at that point for the photocell, which is $R = 104K\Omega$.

For V_{T+}: $R_1 = \frac{R(V)-R(Va)}{Va} = \frac{(104K\Omega)(5V)-(104K\Omega)(3V)}{3V} = 69{,}333.33K\Omega \approx 69K\Omega$

For V_{T-}: $R_1 = \frac{R(V)-R(Va)}{Va} = \frac{(104K\Omega)(5V)-(104K\Omega)(3.6V-1.4V)}{(3.6V-1.4V)} = 132{,}363.63K\Omega \approx 132K\Omega$

Assemble and try the following applications. A good alternative to an open collector inverter is the ULN2003 capable of draining up to 500 mA if properly heat sunk.

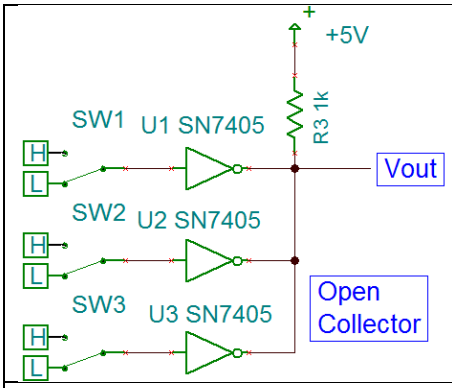


Fig 5: Obtain the voltage table for the circuit

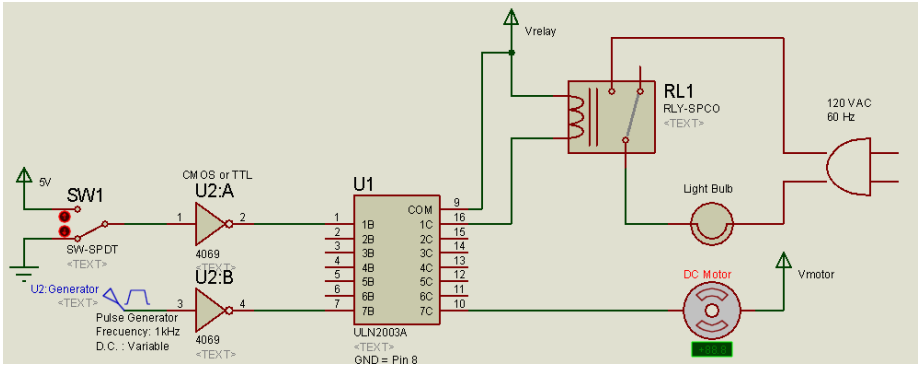


Fig 6: ULN2003 as an open collector driver

After the circuit was assembly, at $Vout$ you can see a behavior of a 3 inputs logic NAND gate. Therefore, the truth table will be the following:

SW1	SW2	SW3	Vout
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Part 3 (Hi-Z): Tri-State challenge. Connect an TTL 74LS125 or 74LS126 to a breadboard. Describe a method using a multimeter to determine whether the output of the gates is V_{OL}, V_{OH} or Hi-Z.

We have attached a video to explain this exercise.

Referencias

Curd. (30 de jun de 2015). *help related to frequency of schmitt oscillator*. Obtenido de Electrical Enginnering: https://electronics.stackexchange.com/questions/177997/help-related-to-frequency-of-schmitt-oscillator