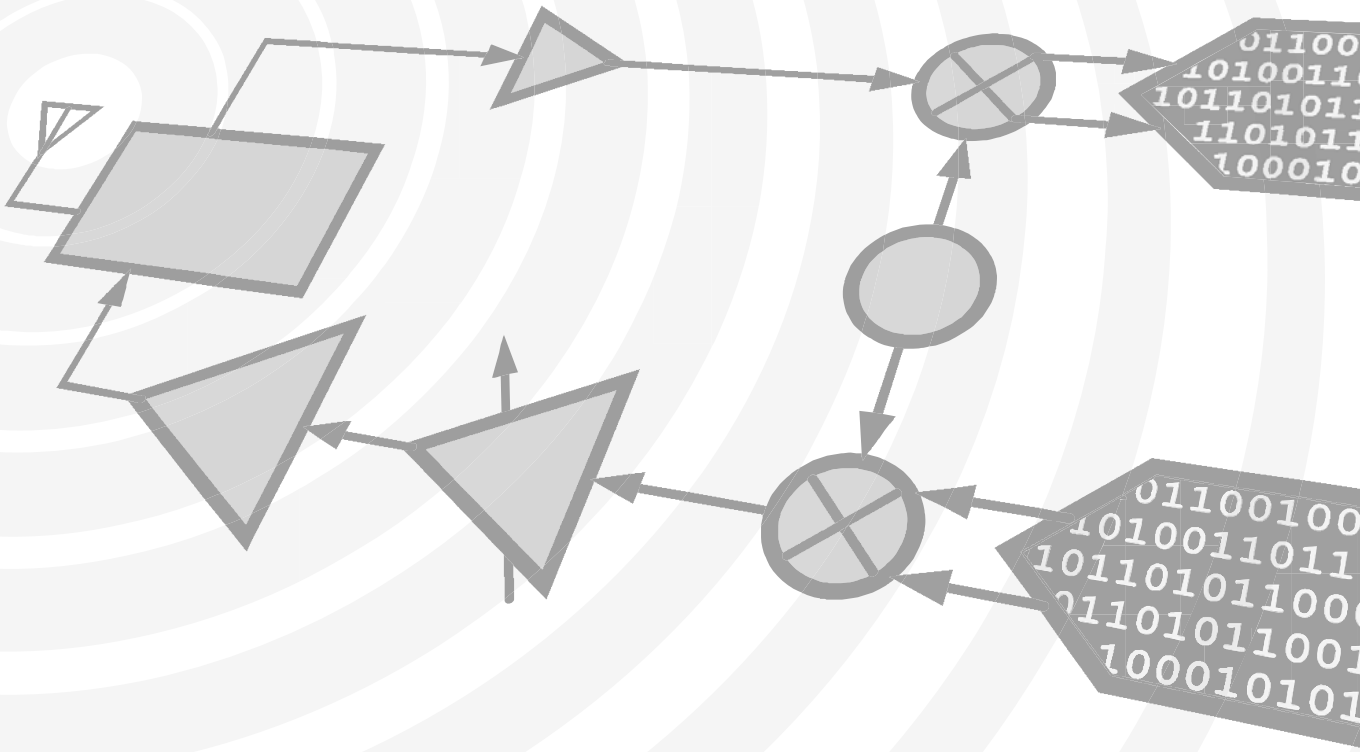
ANALOG DEVICES

Hittite MICROWAVE PRODUCTS FROM ANALOG DEVICES

Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



www.analog.com

www.hittite.com

THIS PAGE INTENTIONALLY LEFT BLANK

HMC830LP6GE

v03.0512

FRACTIONAL-N PLL WITH INTEGRATED VCO 25 - 3000 MHz

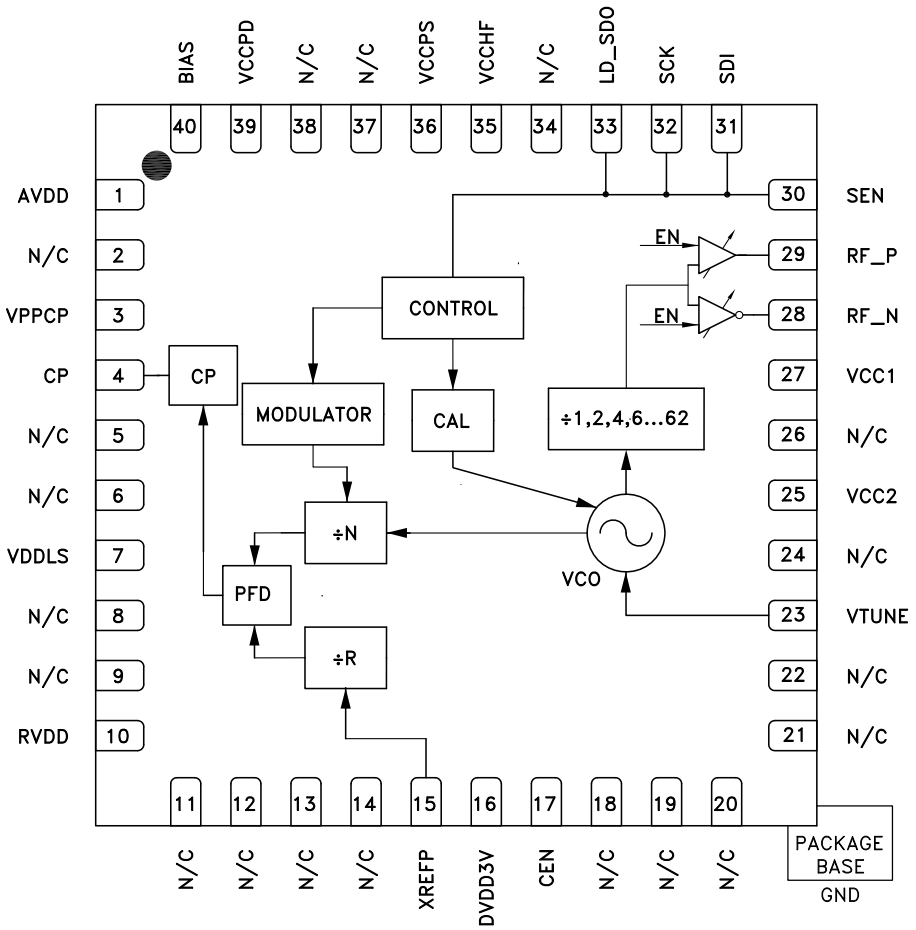
Features

- RF Bandwidth: 25 - 3000 MHz
- Maximum Phase Detector Rate 100 MHz
- Ultra Low Phase Noise -110 dBc/Hz in Band Typ.
- Figure of Merit (FOM) -227 dBc/Hz
- <180 fs RMS Jitter
- 24-bit Step Size, Resolution 3 Hz typ
- Exact Frequency Mode
- Built in Digital Self Test
- 40 Lead 6x6 mm SMT Package: 36 mm^2

Typical Applications

- Cellular/4G Infrastructure
- Repeaters and Femtocells
- Communications Test Equipment
- CATV Equipment
- Phased Array Applications
- DDS Replacement
- Very High Data Rate Radios
- Tunable Reference Source for Spurious-Free Performance

Functional Diagram



FRACTIONAL-N PLL WITH INTEGRATED VCO 25 - 3000 MHz

General Description

The HMC830LP6GE is a low noise, wide band, Fractional-N Phase-Locked-Loop (PLL) that features an integrated Voltage Controlled Oscillator (VCO) with a fundamental frequency of 1500 MHz - 3000 MHz, and an integrated VCO Output Divider (divide by 1/2/4/6.../60/62), that together allow the HMC830LP6GE to generate frequencies from 25 MHz to 3000 MHz. The integrated Phase Detector (PD) and delta-sigma modulator, capable of operating at up to 100 MHz, permit wider loop-bandwidths with excellent spectral performance.

The HMC830LP6GE features industry leading phase noise and spurious performance, across all frequencies, that enable it to minimize blocker effects, and improve receiver sensitivity and transmitter spectral purity. The superior noise floor (< -170 dBc/Hz) makes the HMC830LP6GE an ideal source for a variety of applications - such as; LO for RF mixers, a clock source for high-frequency data-converters, or a tunable reference source for ultra-low spurious applications.

Additional features of the HMC830LP6GE include RF output power control from 0 to 9 dB (3 dB steps), output Mute function, and a delta-sigma modulator Exact Frequency Mode which enables users to generate output frequencies with 0 Hz frequency error.

For theory of operation and register map refer to the "PLLs with Integrated VCOs - RF VCOs Operating Guide". To view the Operating Guide, please visit www.hittite.com and choose HMC830LP6GE from the "Search by Part Number" pull down menu.

Electrical Specifications

VPPCP, VDDLS, VCC1, VCC2 = 5 V; RVDD, AVDD, DVDD3V, VCCPD, VCCHF, VCCPS = 3.3 V Min and Max Specified across Temp -40 °C to 85 °C

Parameter	Condition	Min.	Typ.	Max.	Units
RF Output Characteristics					
Output Frequency		25		3000	MHz
VCO Frequency at PLL Input		1500		3000	MHz
RF Output Frequency at f_{VCO}		1500		3000	MHz
Output Power					
RF Output Power at f_{VCO} = 2000 MHz Across All Frequencies see Figure 10	Broadband Matched Internally [1]	4.5	6	7.5	dBm
Output Power Control	3 dB Steps	7		9	dB
Harmonics					
fo Mode at 2 GHz	2nd / 3rd / 4th		-20/-29/-45		dBc
fo/2 Mode at 2GHz/2 = 1 GHz	2nd / 3rd / 4th		-23/-15/-35		dBc
fo/30 Mode at 3 GHz/30 = 100 MHz	2nd / 3rd / 4th		-25/-10/-33		dBc
fo/62 Mode at 1550 MHz/62 = 25 MHz	2nd / 3rd / 4th		-17/-8/-21		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynamically max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled [2]	1	2	3.3	Vp-p
Ref Input Capacitance				5	pF

[1] Measured single-ended. Additional 3 dB possible with differential outputs.
[2] Measured with 100 Ω external termination. See Hittite PLL w/ Integraged VCOs Operating Guide Reference Input Stage section for more details.

Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
14-Bit R-Divider Range		1		16,383	
Phase Detector (PD) [3]					
PD Frequency Fractional Mode B	[4]	DC		100	MHz
PD Frequency Fractional Mode A (and Register 6 [17:16] = 11)		DC		80	MHz
PD Frequency Integer Mode		DC		125	MHz
Charge Pump					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		µA
PD/Charge Pump SSB Phase Noise	50 MHz Ref, Input Referred				
1 kHz			-143		dBc/Hz
10 kHz	Add 1 dB for Fractional		-150		dBc/Hz
100 kHz	Add 3 dB for Fractional		-153		dBc/Hz
Logic Inputs					
Vsw		40	50	60	% DVDD
Logic Outputs					
VOH Output High Voltage			DVDD		V
VOL Output Low Voltage			0		V
Output Impedance		100		200	Ω
Maximum Load Current				1.5	mA
Power Supply Voltages					
3.3 V Supplies	AVDD, VCCHF, VCCPS, VCCPD, RVDD,DVDD	3.0	3.3	3.5	V
5 V Supplies	VPPCP, VDDLS, VCC1, VCC2	4.8	5	5.2	V
Power Supply Currents					
+5V Analog Charge Pump	VPPCP, VDDLS		8		mA
+5V VCO Core and VCO Buffer	fo/1 Mode VCC2		105		mA
	fo/N Mode VCC2		80		mA
+5V VCO Divider and RF/PLL Buffer	fo/1 Mode VCC1		25		mA
	fo/N Mode VCC1	80		100	mA
+3.3V	AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD3V		52		mA
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked		10		µA
Power Down - Crystal On, 100 MHz	Reg 01h=0, Crystal Clocked 100 MHz		10	30	mA
Power on Reset					
Typical Reset Voltage on DVDD			700		mV
Min DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		µs
VCO Open Loop Phase Noise at fo @ 2 GHz					
10 kHz Offset			-86		dBc/Hz

[3] Slew rate of greater or equal to 0.5 ns/V is recommended, see PLL with Integrated RF VCOs Operating Guide for more details. Frequency is guaranteed across process voltage and temperature from -40 °C to 85 °C.
[4] This maximum phase detector frequency can only be achieved if the minimum N value is respected. eg. In the case of fractional feedback mode, the maximum PFD rate = fvco/20 or 100 MHz, whichever is less.

Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
100 kHz Offset			-116		dBc/Hz
1 MHz Offset			-141		dBc/Hz
10 MHz Offset			-162		dBc/Hz
100 MHz Offset			-171		dBc/Hz
VCO Open Loop Phase Noise at fo @ 2 GHz/2 = 1 GHz					
10 kHz Offset			-92		dBc/Hz
100 kHz Offset			-122		dBc/Hz
1 MHz Offset			-147		dBc/Hz
10 MHz Offset			-165		dBc/Hz
100 MHz Offset			-165		dBc/Hz
VCO Open Loop Phase Noise at fo @3 GHz/30 = 100 MHz					
10 kHz Offset			-112		dBc/Hz
100 kHz Offset			-142		dBc/Hz
1 MHz Offset			-165		dBc/Hz
10 MHz Offset			-168		dBc/Hz
100 MHz Offset			-171		dBc/Hz
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
VCO Characteristics					
VCO Tuning Sensitivity at 2800 MHz	Measured at 2.5 V		13.3		MHz/V
VCO Tuning Sensitivity at 2400 MHz	Measured at 2.5 V		13.8		MHz/V
VCO Tuning Sensitivity at 2000 MHz	Measured at 2.5 V		13.6		MHz/V
VCO Tuning Sensitivity at 1600 MHz	Measured at 2.5 V		12.1		MHz/V
VCO Supply Pushing	Measured at 2.5 V		2		MHz/V

FRACTIONAL-N PLL WITH INTEGRATED VCO 25 - 3000 MHz

Figure 1. Typical Closed Loop Integer Phase Noise ["Loop Filter Configuration Table"]

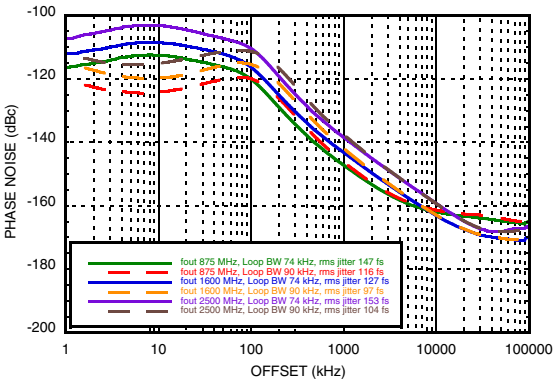


Figure 2. Typical Closed Loop Fractional Phase Noise ["Loop Filter Configuration Table"]

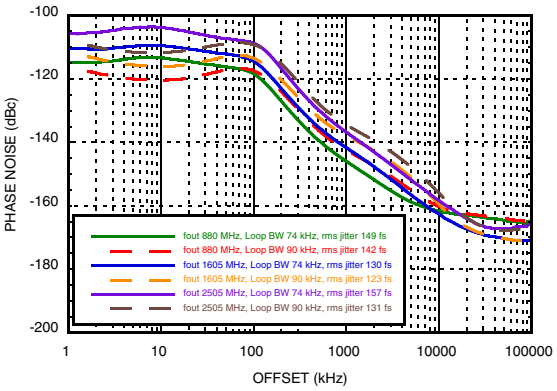


Figure 3. Free Running Phase Noise

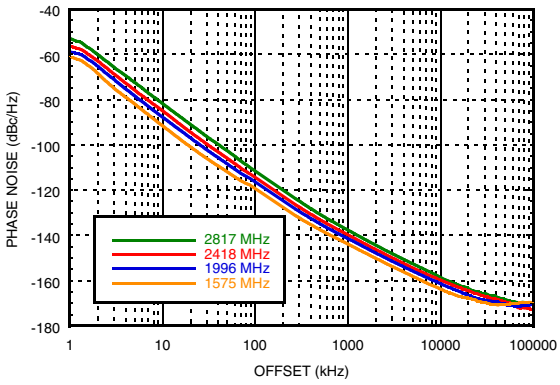


Figure 4. Free Running VCO Phase Noise vs. Temperature

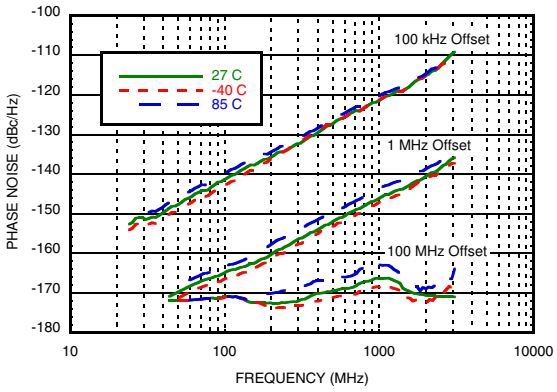


Figure 5. Typical VCO Sensitivity

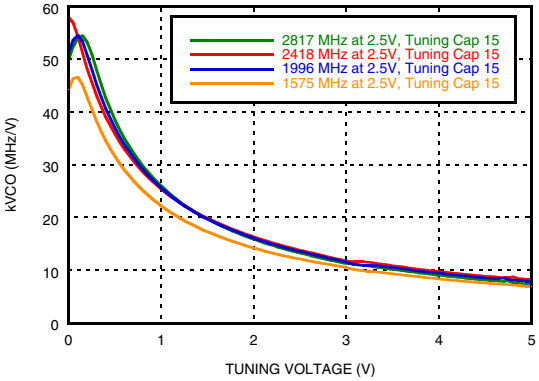


Figure 6. Typical Tuning Voltage After Calibration

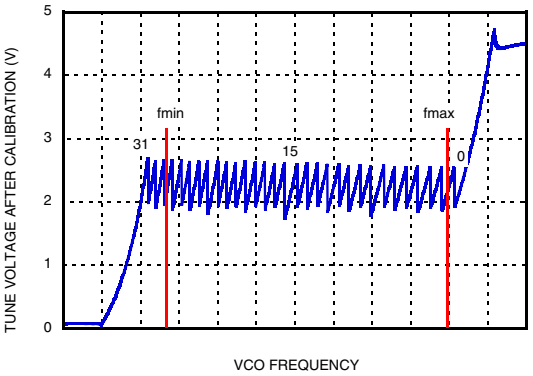


Figure 7. Integrated RMS Jitter[1]

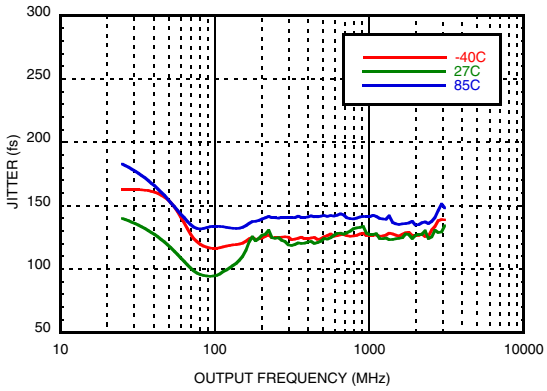


Figure 8. Figure of Merit

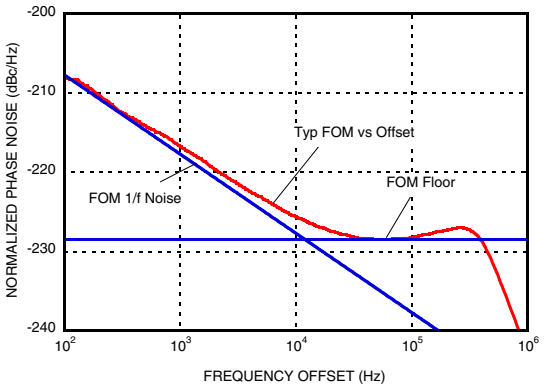


Figure 9. Typical Output Power

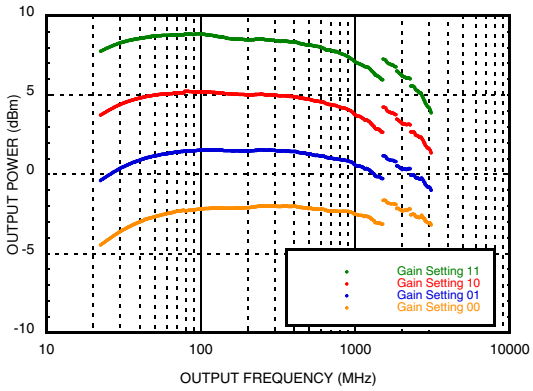


Figure 10. Typical Output Power vs. Temperature, Maximum Gain

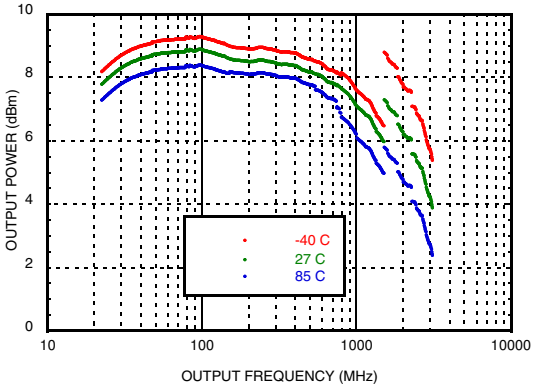


Figure 11. RF Output Return Loss

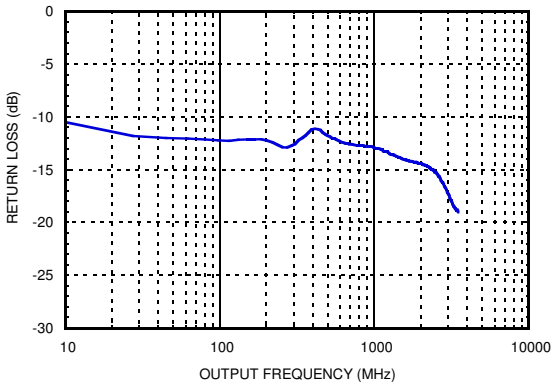
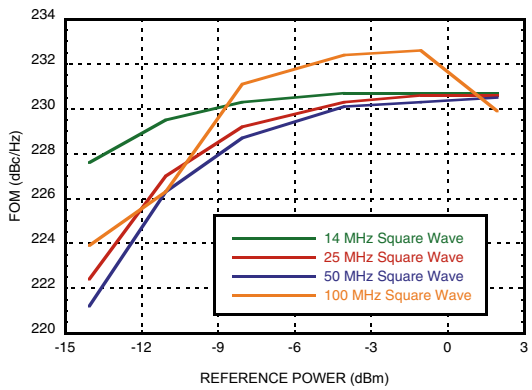


Figure 12. Reference Input Sensitivity, Square Wave, 50 Ω [2]



[1] RMS Jitter data is measured in fractional mode with 100 kHz Loop bandwidth using 50 MHz reference frequency from 1 kHz to 20 MHz integration bandwidth.

[2] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

Figure 13. Reference Input Sensitivity Sinusoid Wave, 50 Ω[3]

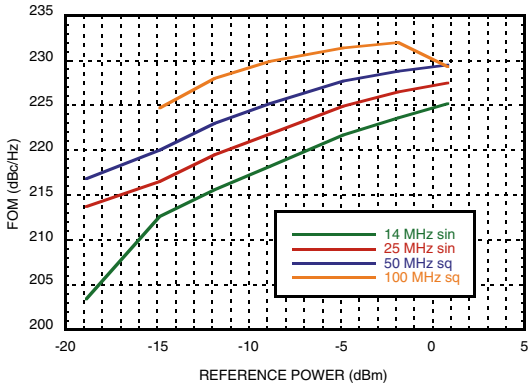


Figure 14. Integer Boundary Spur at 2500.2 MHz[4]

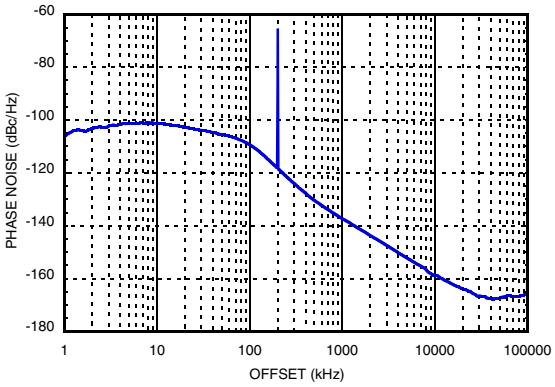


Figure 15. Integer-N Exact Frequency Mode ON Performance at 704 MHz[5]

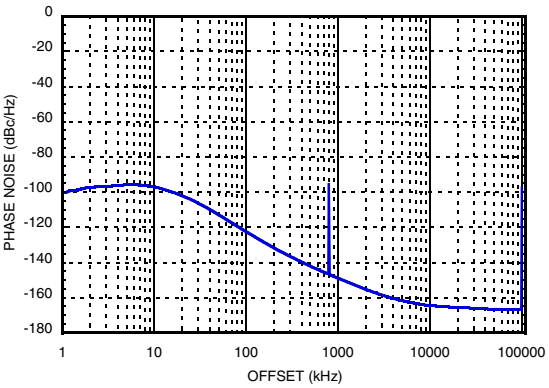


Figure 16. Fractional-N Exact Frequency Mode ON Performance at 2113.5 MHz[6]

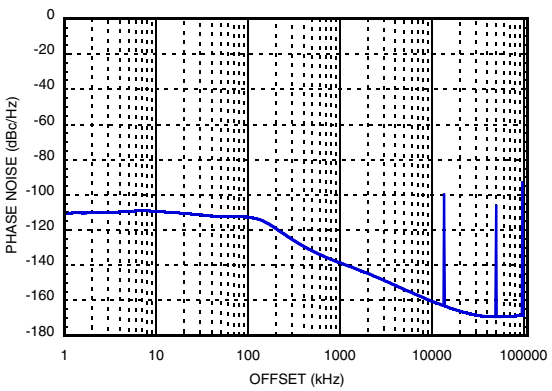


Figure 17. Fractional-N Exact Frequency Mode ON Performance at 2591 MHz[7]

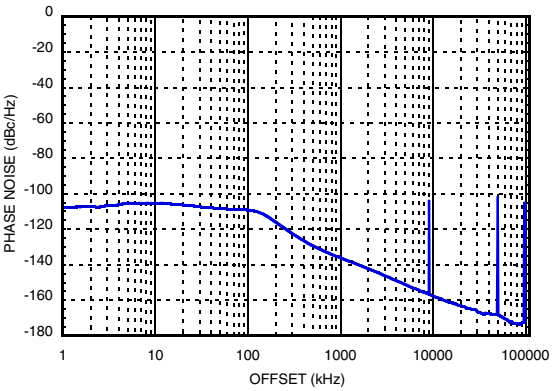
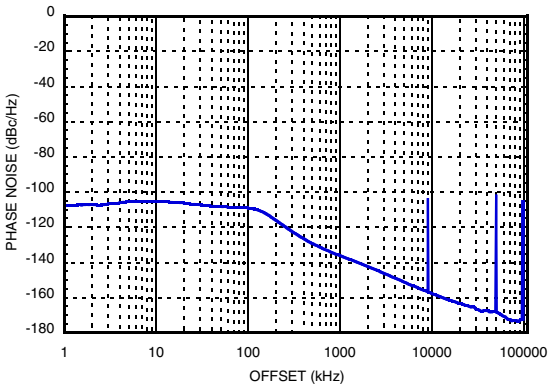


Figure 18. Fractional-N Exact Frequency Mode OFF Performance at 2591 MHz[8]



[3] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

[4] Fractional Mode in Mode B, Integer Boundary at 2500 MHz

[5] REF in = 100 MHz, PD = 800 kHz, Output Divider 4 Selected, Loop Filter bandwidth = 16 kHz, Channel Spacing 200 kHz

[6] Exact Frequency Mode, REF in = 100 MHz, PD = 50 MHz, Output Divider 1 Selected, Loop Filter bandwidth = 100 kHz, Channel Spacing = 100 kHz

[7] Exact Frequency Mode, Channel Spacing = 100 kHz, Fractional Mode B RF out = 2591 MHz, REF in = 100 MHz, PD frequency = 50 MHz, Output Divider 1 selected, Loop Filter bandwidth = 120 kHz,

[8] Fractional Mode B RF out = 2591 MHz, REF in = 100 MHz, PD frequency = 50 MHz, Output Divider 1 selected, Loop Filter bandwidth = 120 kHz.

Figure 19. Worst Spur, Fixed 50 MHz Reference, Output Freq. = 2000.1 MHz[9]

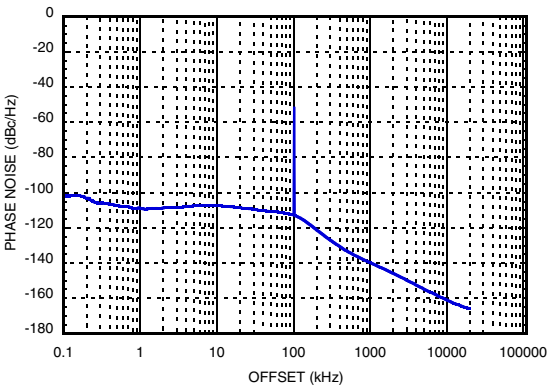


Figure 20. Worst Spur, Tunable Reference, Output Frequency = 2000.1 MHz [9]

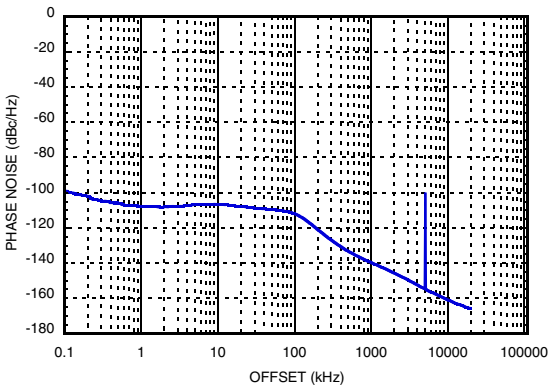


Figure 21. Worst Spur, Fixed vs. Tunable Reference [10]

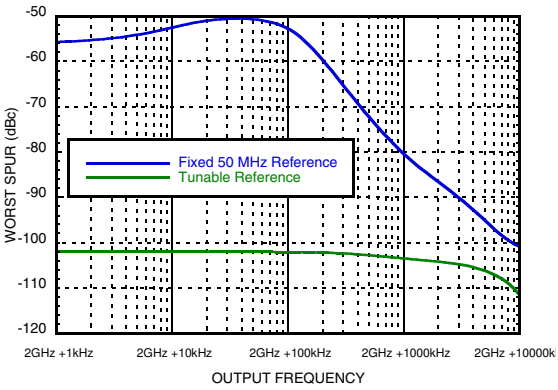
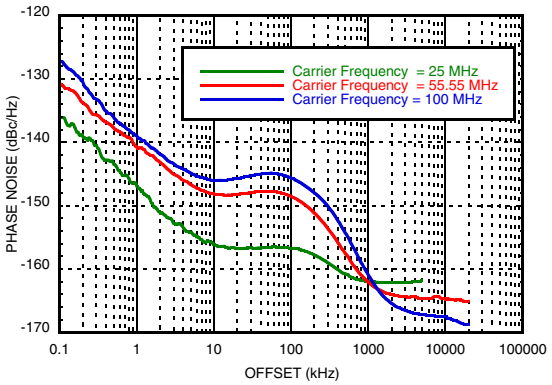
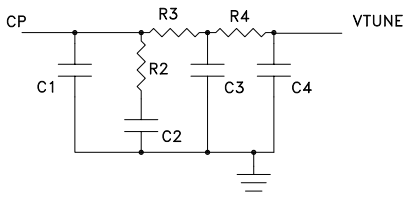


Figure 22. Low Frequency Performance [11]



Loop Filter Configuration Table

Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
74	150	27	220	220	0.82	1	1	
90	270	3.9	56	56	1.2	1	1	

[9] Capability of HMC830LP6GE to generate low frequencies (as low as 25 MHz), enables the HMC830LP6GE to be used as a tunable reference source into another HMC830LP6GE, which maximizes spur performance of the second HMC830LP6GE. Please see "HMC830LP6GE Application Information" for more information.

[10] The graph is generated by observing, and plotting, the magnitude of only the worst spur (largest magnitude), at any offset, at each output frequency, while using a fixed 50 MHz reference and a tunable reference tuned to 47.5 MHz. See "HMC830LP6GE Application Information" for more details.

[11] Phase noise performance of the HMC830LP6GE when used as a tunable reference source. HMC830LP6GE is operating at 3 GHz/30, 3 GHz/54, and 1.55 GHz/62 for the 100 MHz, 55.55 MHz, and 25 MHz curves respectively. 25 MHz output is 50 MHz low pass filtered prior to input to second PLL. 100 MHz and 55.55 MHz curves were not filtered.

Pin Descriptions

Pin Number	Function	Description
1	AVDD	DC Power Supply for analog circuitry.
2, 5, 6, 8, 9, 11 - 14, 18 - 22, 24, 26, 34, 37, 38	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
3	VPPCP	Power Supply for charge pump analog section
4	CP	Charge Pump Output
7	VDDLS	Power Supply for the charge pump digital section
10	RVDD	Reference Supply
15	XREFP	Reference Oscillator Input
16	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry
17	CEN	Chip Enable. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning Port Input.
25	VCC2	VCO Analog Supply 2
27	VCC1	VCO Analog Supply 1
28	RF_N	RF Negative Output (On in differential configuration, On in single-ended configuration)
29	RF_P	RF Positive Output (On in differential configuration, Off in single-ended configuration)
30	SEN	PLL Serial Port Enable (CMOS) Logic Input
31	SDI	PLL Serial Port Data (CMOS) Logic Input
32	SCK	PLL Serial Port Clock (CMOS) Logic Input
33	LD_SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)
35	VCCHF	DC Power Supply for Analog Circuitry
36	VCCPS	DC Power Supply for Analog Prescaler
39	VCCPD	DC Power Supply for Phase Detector
40	BIAS	External bypass decoupling for precision bias circuits. Note: 1.920V ±20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10GΩ meter such as Agilent 34410A, normal 10MΩ DVM will read erroneously.

Absolute Maximum Ratings

AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS	-0.3 V to +3.6 V
VPPCP, VDDLS, VCC1	-0.3 V to +5.5 V
VCC2	-0.3 V to +5.5 V
Operating Temperature	-40 °C to +85 °C
Storage Temperature	-65 °C to 150 °C
Maximum Junction Temperature	150 °C
Thermal Resistance (Θ_{JC}) (junction to case (ground paddle))	9 °C/W
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

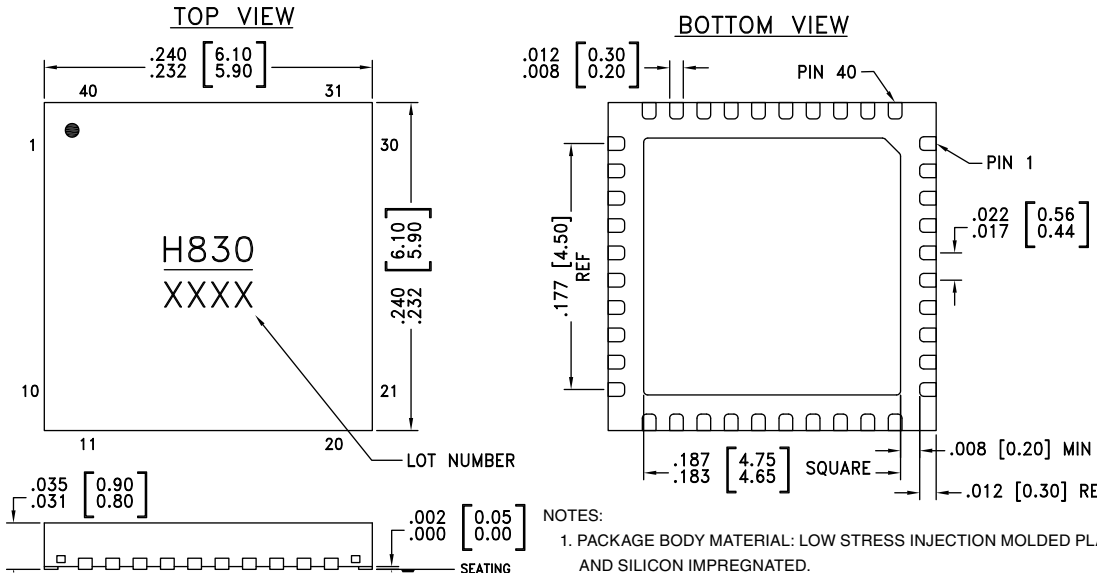
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Condition	Min.	Typ.	Max.	Units
Temperature					
Junction Temperature				125	°C
Ambient Temperature		-40		85	°C
Supply Voltage					
AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS		3.0	3.3	3.5	V
VPPCP, VDDLS, VCC1, VCC2		4.8	5	5.2	V

[1] Layout design guidelines set out in Qualification Test Report are strongly recommended.

Outline Drawing



NOTES:

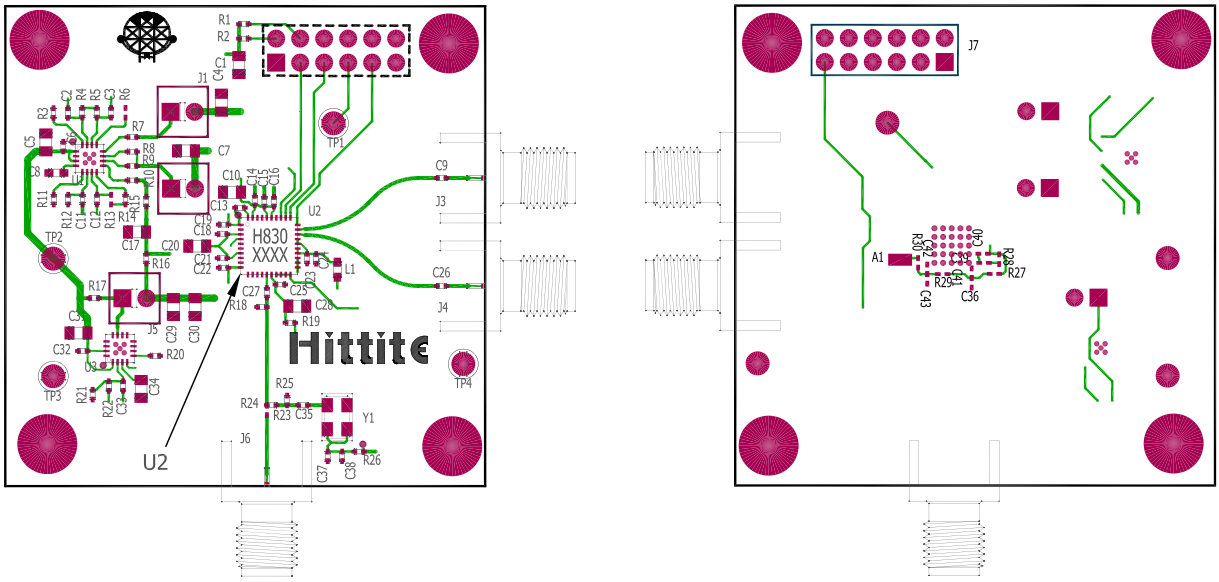
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC830LP6GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H830 XXXX

[1] 4-Digit lot number XXXX

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC830LP6GE from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC830LP6GE Evaluation PCB	EVAL01-HMC830LP6GE
Evaluation Kit	HMC830LP6GE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC830LP6GE

HMC830LP6GE Application Information

Large bandwidth (25 MHz to 3000 MHz), industry leading phase noise and spurious performance, excellent noise floor (<-170 dBc/Hz), coupled with a high level of integration make the HMC830LP6GE ideal for a variety of applications; as an RF or IF stage LO, a clock source for high-frequency data-converters, or a tunable reference source for extremely low spurious applications (< -100 dBc/Hz spurs).

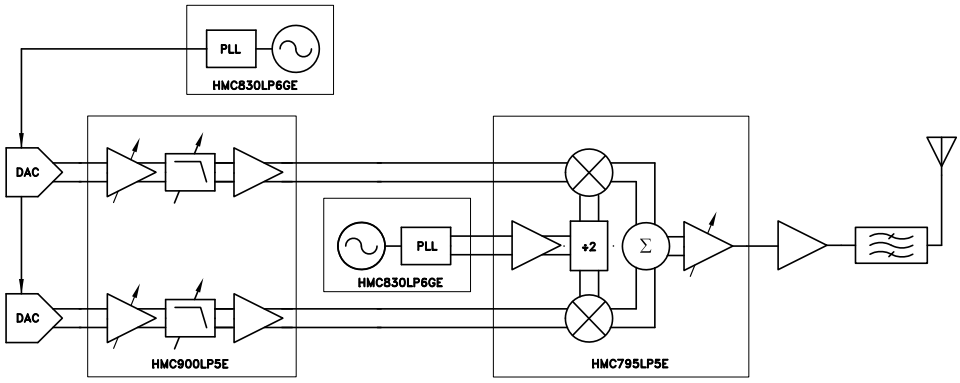


Figure 23. HMC830LP6GE in a typical transmit chain

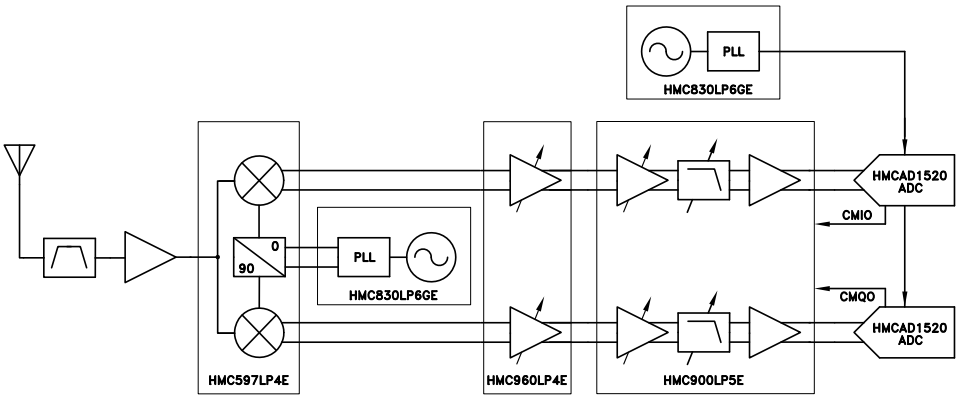


Figure 24. HMC830LP6GE in a typical receive chain

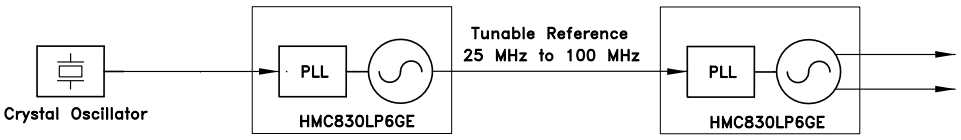


Figure 25. HMC830LP6GE used as a tunable reference for second HMC830LP6GE

Using the HMC830LP6GE with a tunable reference as shown in Figure 25, it is possible to drastically improve spurious emissions performance across all frequencies. Example shown in Figure 21 graph shows that it is possible to have spurious emissions < -100 dBc/Hz across all frequencies. For more information about spurious emissions, how they are related to the reference frequency, and how to tune the reference frequency for optimal spurious performance please see the "Spurious Performance" section of Hittite PLL w/ Integraged VCOs Operating Guide. Note that at very low output frequencies < 100 MHz, harmonics increase due to small internal AC coupling. Applications which are sensitive to harmonics may require external low pass filtering.

Notes: