Serial Communication Circuit with Optimized Skew Characteristics

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***Abstract*—This letter highlights features of an optimized serial communication system, including an oversampling technique of data recovery, issues related to off-board communications and a modified Universal Asynchronous Receiver Transmitter (UART) implemented in programmable logic device (PLD). The resulting system provides high skew tolerance at 44 Mb/s data rate and has achieved a transmission distance of 130 m, at this rate, with the aid of an enhanced differential transceiver circuit. The principal application is for embedded systems with medium distance communication requirements. This UART can be integrated with other communication functions, such as packet routing switches, in a PLD device.**

***Index Terms*—Data communication, DC coupled transmission lines, LAN, UART.**

I. Introduction

THE ADVANTAGES of Universal Asynchronous Receiver Transmitter (UART) systems are the simplicity of interconnection wiring and character transmission protocol/formats. Standard 16 550 UART devices can provide transmission rates of up to 115.2 kb/s. However through recent developments, some high performance UART devices exist that can achieve a maximum speed of 10 Mb/s [1]. The UART technology uses an over-sampling technique for data recovery and is totally asynchronous with independent transmit and receive clocks. This technique requires a higher operating frequency than the actual data transmission rate. However, oversampling (OS) methods are easier and more economical to implement when compared to designs using a clock recovery method, especially in programmable logic device (PLD) implementations. Clock recovery methods normally require special data encoding to carry clock information and a phase lock loop (PLL) to synchronize the receiver clock for data recovery. Most serial communication standards utilize clock recovery methods; however, this letter is directed solely at performance improvement for a basic OS UART circuit.

For UART systems that require extended distance differential transmission, interfaces like RS-422/485 are desirable. As the signal propagates, signal quality deteriorates: the maximum data transmission rate is dependent on the maximum transmission distance and the interface circuit configuration. Signal attenuation and skew/jitter increase as a function of distance and signal speed. With the straightforward framing method of the UART formats, some characters produce an unbalanced 1 and 0 bit pattern. This unbalanced bit stream has proved to be the main contributing factor of the signal skew as the distance increases.

This letter describes an enhanced transmission-line interface and a modified UART, which have been implemented using discrete components and a complex programmable logic device (CPLD). This combination of interface and UART circuits allow transmission rates of 44 Mb/s at distances of up to 130 m with standard category 5 unshielded twisted pair (UTP) cables without the use of additional line balance encoding.

II. Description of the Modified UART

The skew tolerance is an important measurement to account for all the signal distortions within a system. For example any distortion of the signal due to line transmission characteristics will reduce the circuit tolerance measurement to distortion due to noise and visa versa. UART devices use a 16-times OS technique to provide optimum skew tolerance for data recovery; consequently it requires a high operating clock frequency which effectively limits the data transmission rate. Therefore, at a similar maximum operating clock frequency, reducing the sampling rate offers the potential of higher data transmission rates, with a trade-off of against skew tolerance. Although higher sampling rates provide better skew tolerance, the "odd" sampling rates are actually superior to the adjacent higher "even" sampling rates. For example; 5 times OS (skew tolerance of 2/5 bit period) is better than 6 times OS (skew tolerance of 2/6 bit period). However, the minimum sampling requirement is 3 times OS which provides a theoretical maximum skew tolerance of 1/3 of the bit period compared to 7/16 for 16 times OS.

The implementation of the serial communication device for this project utilizes 3 times OS and samples with both edges of the clock. Thus, it only requires a sampling clock of 1.5 times of the transmission rate, i.e., initially operating with 30-MHz sampling frequency to achieve 20-Mb/s data transmission. Hence, over an order of magnitude reduction in clock speed is traded against a 24% degradation in theoretical maximum skew tolerance. Such a significant reduction in clock speed could lead to problems with recovery from metastability but this is not a major issue for the technology used, e.g., Altera CPLD devices offer recovery times of less than 2 ns [2].

III. Test Setup

The OS serial communication design and most of the test circuit were combined into an Altera F10KA device

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(EPF10K10ATC100-2). The design when optimized achieved a maximum operating frequency of 66 MHz. This results in a data transmission rate of 44 Mb/s. The OS Link device was interfaced to the high performance RS-422 transceiver, from Analog Devices (ADM1485), to provide differential transmission along large lengths of twisted pair cable. The twisted pair cable chosen was the CAT 5 UTP cable from Belden (SM1720A), of which separate line pairs were used to provide a full duplex connection. All tests were carried out with continuous bi-directional data transfer.

The basic tests were executed by transmitting pseudo-random data bytes, and verifying the data bytes at the receiving end for correct data recovery. A counter kept track of the number of correctly recovered data bytes. If a mismatch was found, an error was flagged and the count recorded. The tests were repeated for a number of different cable lengths to a maximum length of 130 m.

To measure the quality of the signal received, eye patterns were formed at the receiving end. These were obtained by using the infinite persistence display mode of the oscilloscope, triggered from the transmitting clock. The amplitude attenuation was measured at the input side of the receiver and the signal skew was measured at the output of the receiver.

The first test configuration consists of the recommended set of requirements for differential transmission, that is, termination of both ends of the transmission line with 100 ohms resistors. Tests with random data were carried out to determine the maximum cable length over the range of data rates. The final tests and analysis were carried out at these maximum cable lengths so that the greatest effect on the signal quality was seen when modifications were made. The major modifications were aimed toward line balance improvement and transient spike protection. The combined enhanced circuit diagram is shown in Fig. 1 [3].

IV. Line Balance Improvements

As the transmission line is DC coupled at both ends, there is a charging of the line as one value is maintained over several bit intervals. To show how the unbalanced data pattern can affect the skew at the receiving end, a series of tests were run with different unbalanced data patterns. Each selected data pattern was transmitted repetitively and the jitter measurement was recorded. The results indicate that for the basic circuit, minimum skew is recorded for the best data balance. As the imbalance of the data pattern increases the skew increases.

To improve the line balance effect, a parallel *RC* circuit was added to each output terminal as shown in Fig. 1. The coupling capacitor $C_{\rm tx}$ allows rapid rate of change in the signal while the resistor $R_{\rm tx}$ provides a lower voltage level to maintain the charge line at a constant value. With the enhanced interface circuit, the unbalance data pattern tests show that the skew is independent of data pattern. The magnitude of skew is also reduced to a value comparable with the minimum skew achieved in the basic circuit tests. However, the values of $R_{\rm tx}$ and $C_{\rm tx}$ have to be carefully chosen. Larger values of R tend to attenuate the signal too much, while larger values of C incur increased skew. Transmission line impedance matching must be considered also, to ensure optimum transmission characteristics.

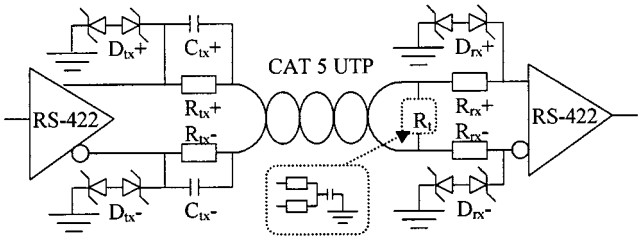

Fig. 1. Enhanced RS-422 circuit diagram (for one direction).

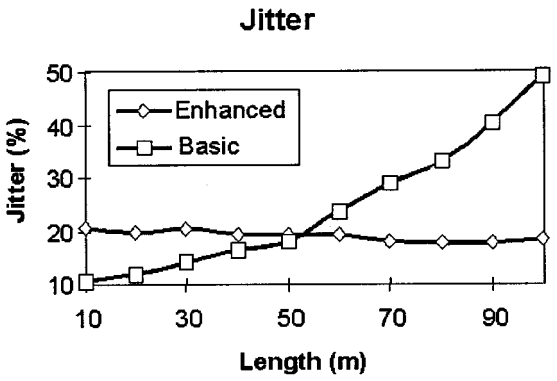

Fig. 2. Overall jitter results.

V. Diode Protection

Transient voltages induced on a transmission medium can destroy unprotected digital circuits and it is therefore important to test the modified circuit for protection. A number of economical solutions were analyzed for signal degradation and protection capability. Good galvanic isolation can be obtained by using transformers but this requires a.c. coupling of the circuit. Transient voltage suppresser (TVS) diodes are more commonly used, though they provide a lower level of protection.

High power TVS diodes are available on the market that can sustain peak pulse powers of several hundred watts. However, these protection diodes possess a fairly large capacitance, which will effectively distort the signal quality, especially at high speed with long distance transmission. A test was undertaken with TVS diodes from Fairchild (P6KE13CA). The result showed a totally closed eye pattern.

The use of lower power zener diodes (lower capacitance) in conjunction with a current limit resistor $R_{\rm rx}$ was used as an alternative solution, as shown in Fig. 1. The BZX79xx series was used in this test. The effect of adding this protection only incurred an extra skew of 0.7 ns. Surge tests indicated that this circuit provides protection against pulses in excess of 100 V for 100 μs.

VI. Applications

Although the application of this serial communication system is general, it is particularly advantageous in complex multilink networks: for example in a parallel processing system with packet routing switches with multiple serial links [4]. The simplicity of this design significantly reduces the logic requirements of the UART interface. When these UART's are inte-

grated directly to a packet routing device, the replication of the UART logic gives a significant saving.

VII. Results and Conclusions

Fig. 2 shows the overall jitter/skew comparison of random data test results for the basic configuration and the full-enhanced configuration. For the basic circuit, the jitter increases as the length of cable increases. It reaches the receiver capability limit (33%) at 70 m. For the enhanced circuit, the jitter remains constant for the lengths of cable up to 100 m. Although, the jitter is worse than the basic circuit at short distances, there is a increasing improvement at lengths greater then 50 m. At the length of 100 m, the jitter is only 19% and therefore provides a 13% skew tolerance for noise. The level of noise immunity of this circuit under controlled background conditions is yet to be determined. The performance limit of 130 m at 44 Mbit/s was due to signal attenuation rather than jitter.

As the last phase, the enhanced circuit was tested for reliability. The test was run for 20 h without any errors, which gives an extrapolated maximum experimental bit error rate value of 3.16E-13.

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