TI Designs

Automotive Resistive Bridge Pressure Sensor Reference Design

TI Designs

The TIDA-00793 design provides a simple, robust, and accurate sensor signal conditioning solution using the PGA400-Q1 for resistive bridge type pressure sensors. The protection strategies implemented in this design protect the pressure sensor against wiring harness faults, EMI, and automotive electrical transients. Additionally, this design guide systematically explains the theory, operation, and challenges involved in this TI Design.

Design Resources

TIDA-00793	Design Folder
PGA400-Q1	Product Folder
PGA400EVM	Product Folder

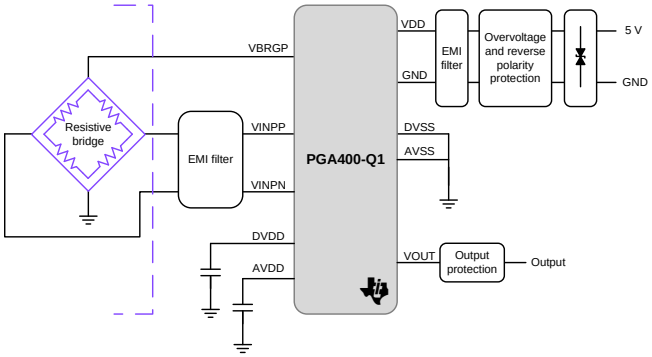
TI E2E™ Community — ASK Our E2E Experts

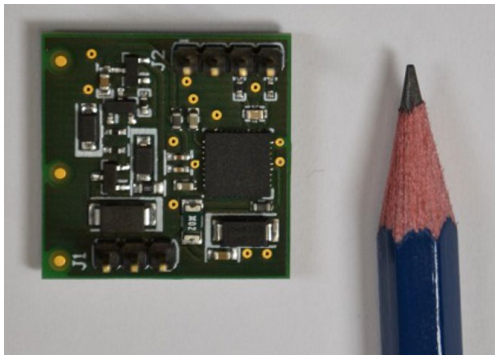
Design Features

- Accuracy of 0.17% Over Temperature (–40°C to 125°C)
- Second Order Temperature and Linearity Compensation Algorithm
- Form Factor Design of 23 × 23 mm
- Protection Against Harness Faults (Overvoltage and Reverse Polarity Protection), Broken Wire Detection
- Meets ISO 7637-3 Requirements for Transient Pulses
- Tested for Bulk Current Injection (BCI) ISO 11452-4

Featured Applications

- Manifold Absolute Pressure
- Engine Oil Pressure
- Transmission Oil Pressure
- Occupant Weight
- In-Cylinder Pressure
- EGR Pressure
- HVAC Compressor Pressure
- Pedal Force





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1 Key System Specifications

Table 1. Design Requirements

PARAMETER	DESCRIPTION
Sensor type	Resistive
Pressure range	Custom ranges: • 15 Kpa to 102 Kpa • 12.5 Kpa to 115 Kpa • 20 Kpa to 250 Kpa • 10 Kpa to 350 Kpa • and so on
Power supply operating voltage	5 V
Overvoltage protection	Yes, up to 30 V
Reverse polarity protection	Yes
Calibration	Based on the sense element specifications
Transient immunity	Designed to meet ISO 7637-3 standards
Nominal output voltage	0.5 to 4.5 V
Output V_{OUT} protection	Yes
Temperature range	–40°C to 125°C
EMI protection	Tested for BCI
Harness faults protection	Yes
Form factor	23 × 23 mm
Number of layers	Two-layer, single side populated
Interface connectors	One 4-pin connector for sensor interface One 3-pin connector for sensor output and power supply

2 Introduction

This design guide details how to design a simple, robust, and accurate pressure sensor signal condition circuit for resistive based sense elements. This reference design also explains the theory, operation, and complications involved.

This TI Design emphasizes topics such as harness faults, protection strategies (reverse polarity protection, overvoltage protection), EMI filter, PGA400-Q1 calibration procedure, and the design challenges of printed circuit boards. Furthermore, the external protection circuitry complies with regulatory ISO 7637-3 and ISO 11452-4 standards: Capacitive coupling clamp (CCC) and BCI methods. This guide provides all the relevant design files such as schematics, Bill of Materials (BOM), Altium files, and Gerber files.

3 System Description

A typical pressure sensor has two building blocks as shown in Figure 1: a sense element and a signal conditioner.

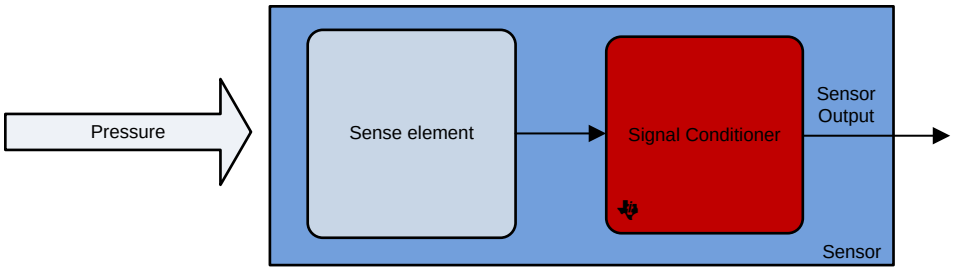

Figure 1. Block Diagram of a Typical Pressure Sensor

The primary purpose of the signal conditioner (SC) is to process the output of the sense element for its non-idealities and provide the processed output to the ECU. The conceptual block diagram in Figure 2 represents a pressure sensor signal conditioner for resistive bridge type sense elements. The heart of this reference design is the PGA400-Q1, which consists of an integrated analog front end (AFE), a digital compensation algorithm, and a DAC. This device converts pressure signals directly into desired voltage levels.

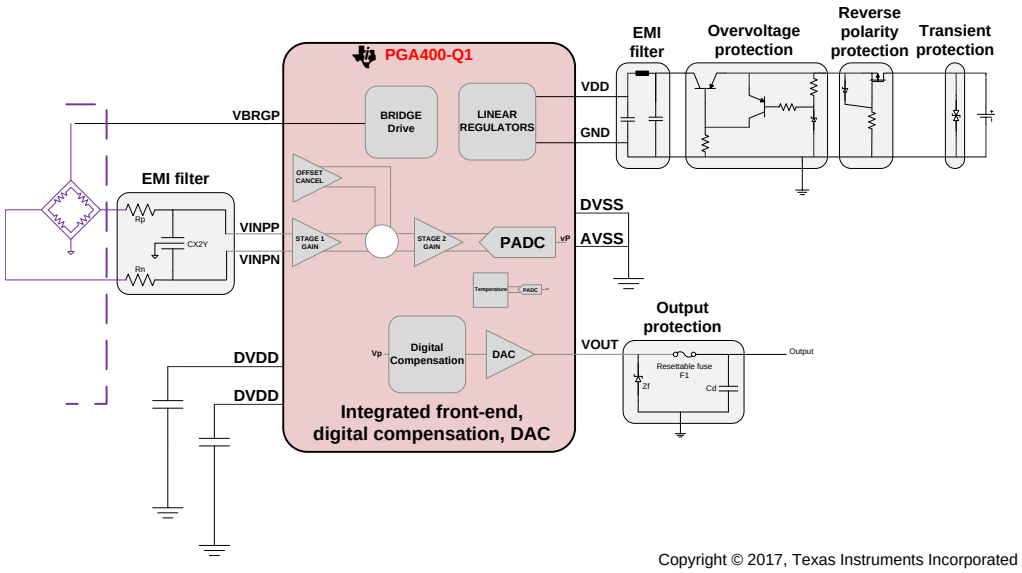

Figure 2. Conceptual Block Diagram

Figure 2 describes the conceptual block diagram of the system. Sense element (resistive bridge) output is given to the PGA400-Q1 through the EMI filter (serves the purpose of removing electromagnetic noise). Normally, the output of the bridge is in millivolts. In order to amplify and remove the offset, gain and offset adjustment is provided in the AFE stage of the PGA400-Q1. Based on the provided gain and offset, the ADC interprets digital values and sends information to the built-in compensation algorithm. The algorithm is designed to compensate for linearity and temperature effects on the sense element (non-idealities of the bridge). The DAC translates output into analog values. A simple discrete circuit around the PGA400-Q1 protects the chip from overvoltages and transients. More than 20 harness faults conditions in automotive environment are analyzed, and it is designed to withstand all the conditions.

In a real application scenario, the device is powered up with the 5-V supply from ECU. To protect the lines from coupling effects, the power supply is shunted with a TVS diode to clamp the wiring harness pulses (capacitive and inductive coupled surges). To account for the reverse battery connections, a discrete reverse voltage circuit is provided for –20 to 20 V. Although the absolute maximum rating of the PGA400-Q1 is 16 V, to provide the overvoltage protection for >16 V, a discrete overvoltage protection circuit is implemented in the design. The bridge drive supply inside the PGA400-Q1 biases the resistive bridge. The output DAC delivers a 0.5- to 4.5-V signal across the output pin. During normal operation, the signal travels through a resettable fuse (PTC, which offers a very low resistance of 2 Ω) and outputs the sensor signal. Whenever overvoltage appears across the sensor output pin, the resettable fuse along with the Zener limits the overvoltage and fuse opens, thereby the PGA400-Q1 survives.

Making all three external connections fully protected, this reference design protects the sensor against all wiring harness faults. Figure 2 shows the components of this design in a conceptual schematic diagram.

4 Block Diagram

Figure 3 describes the blocks involved in the pressure sensor design. Figure 4 shows the pin description of the TIDA-00793 design.

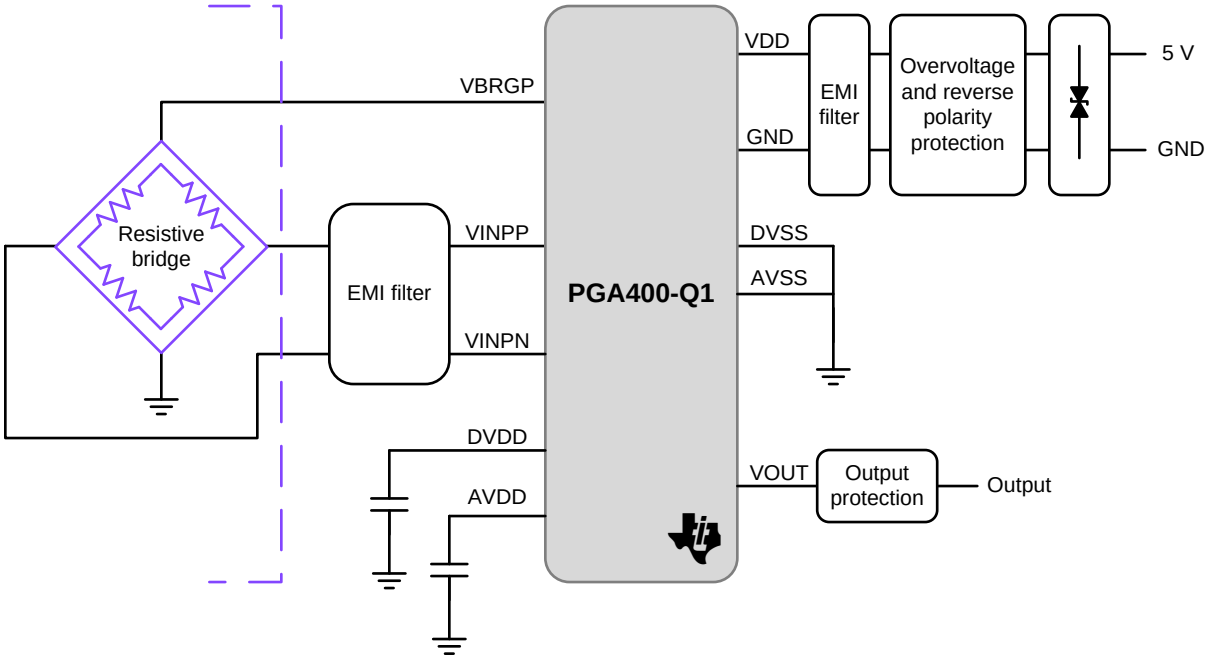

Figure 3. Pressure Sensor Block Diagram

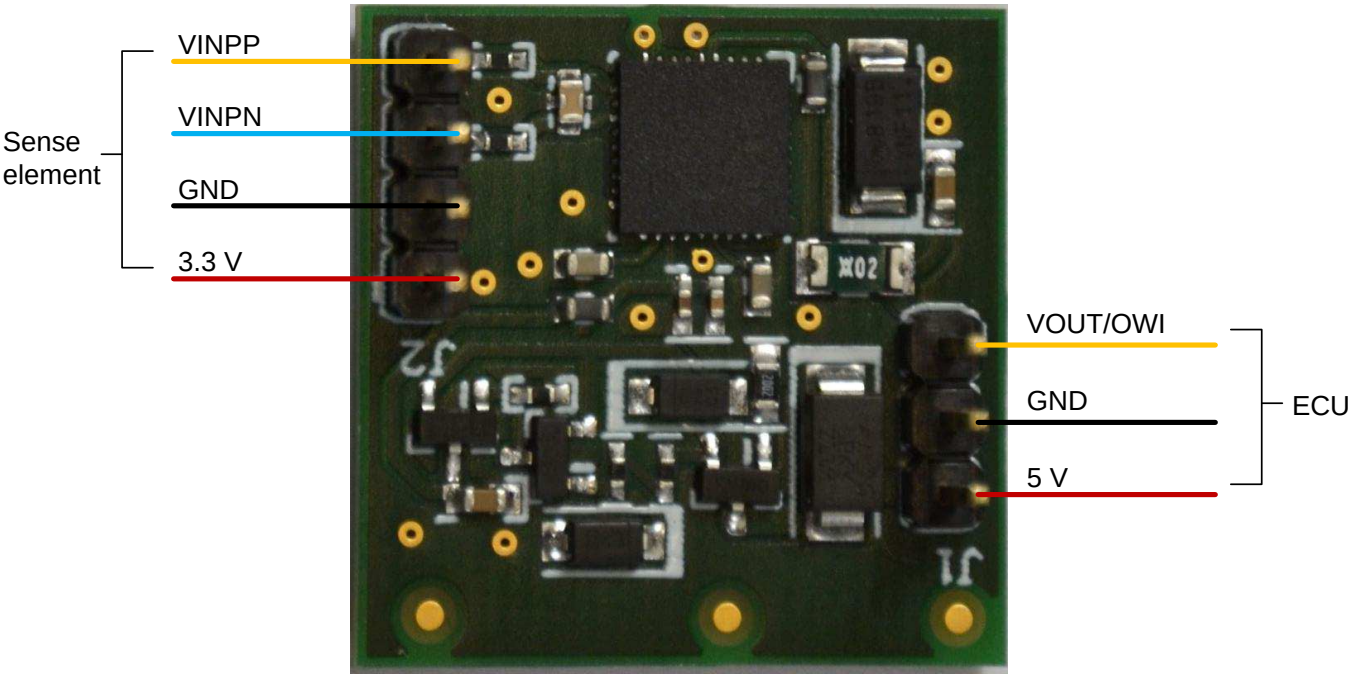

Figure 4. TIDA-00793 Pin Description

4.1 Highlighted Product

The PGA400-Q1 is a pressure sensor signal conditioner with built-in linearity and compensation algorithm. The accuracy and robustness of the device make it a perfect choice for choosing signal conditioning elements for pressure sensor applications.

- Suited for AFE resistive bridge sensors. Directly accepts the bridge output without any need of external conditioning amplifiers. A two-stage adjustable gain and offset feature enables different combinations of gain and offset adjustments based on the sense element input range
- Second order compensation and EEPROM memory (accuracy improvement for temperature variations and sense element linearity variations)
- Also includes one ratiometric voltage output
- On-chip temperature sensor enables full accuracy over grade 1 temperature range
- 16-bit, 1-MHz sigma-delta analog-to-digital converter (ADC) for signal channel
- Digital features include:
  - Compensation equation
    - Second order temperature: Two clocks per instruction cycle
    - On-chip oscillator
- One-wire interface (OWI)
- Analog low-voltage detect
- Power supply: 4.5- to 5.5-V operational, –5.5- to 16-V absolute maximum
- Qualified in accordance with AEC-Q100

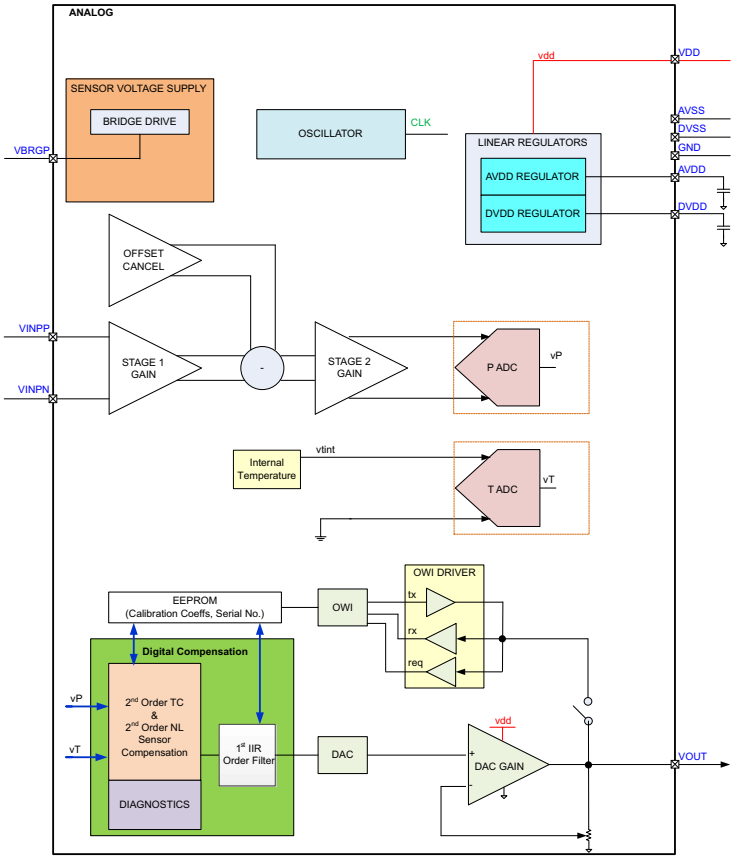

Figure 5. PGA400-Q1 Functional Block Diagram

5 System Design Theory

5.1 Sensor Interface

Pressure sensors are usually connected to the electronic control unit (ECU). Figure 6 shows the normal connection of pressure sensors with the ECU. The output of the sensor has mainly three wires, namely 5 V, signal, and ground. The supply is provided by the ECU. The signal wire is connected to the pullup resistor on the ECU side for diagnostic purposes. The ECU interprets the signal from the pressure sensor and sends the information to the respective unit to make a necessary controlling action. Figure 6 shows the connection between the sensor and the ECU.

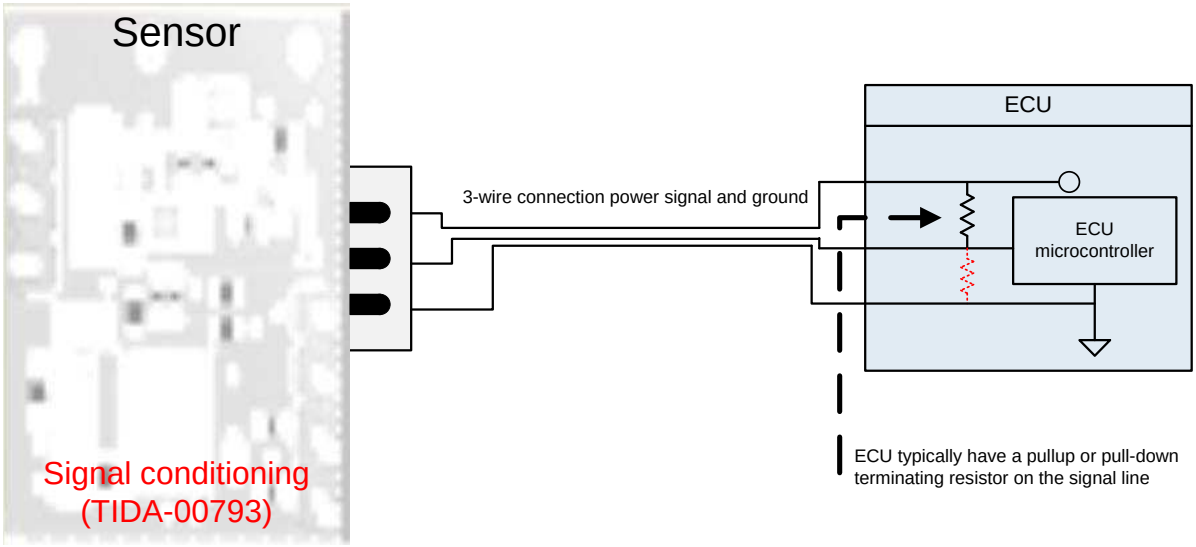

Figure 6. Pressure Sensor Connection to ECU

5.2 Sense Element

With regards to pressure sensors based on the resistive type, resistors are typically arranged in bridge configuration. Figure 7 shows a full Wheatstone bridge arrangement of the resistors. As the pressure changes, the value of resistance in each bridge leg changes as well. This in turn causes the output voltage of the Wheatstone bridge to change.

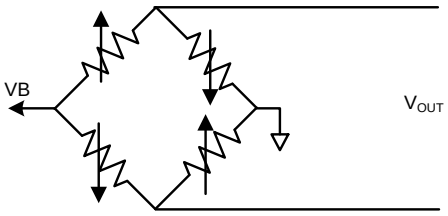

Figure 7. Resistors Arranged in Wheatstone Bridge Configuration to Form Pressure Sensor

5.3 Signal Conditioning

The main purpose of signal conditioning is to process the sensor signal for its non-idealities and make the fully protected and accurate signal available to the ECU. The conceptual schematic diagram in Figure 8 describes the signal condition circuit for Wheatstone bridge using the PGA400-Q1 single-chip solution.

The signal conditioning is mainly divided into three stages:

1. Front end (EMI filter)
2. Power supply protection
3. Output protection

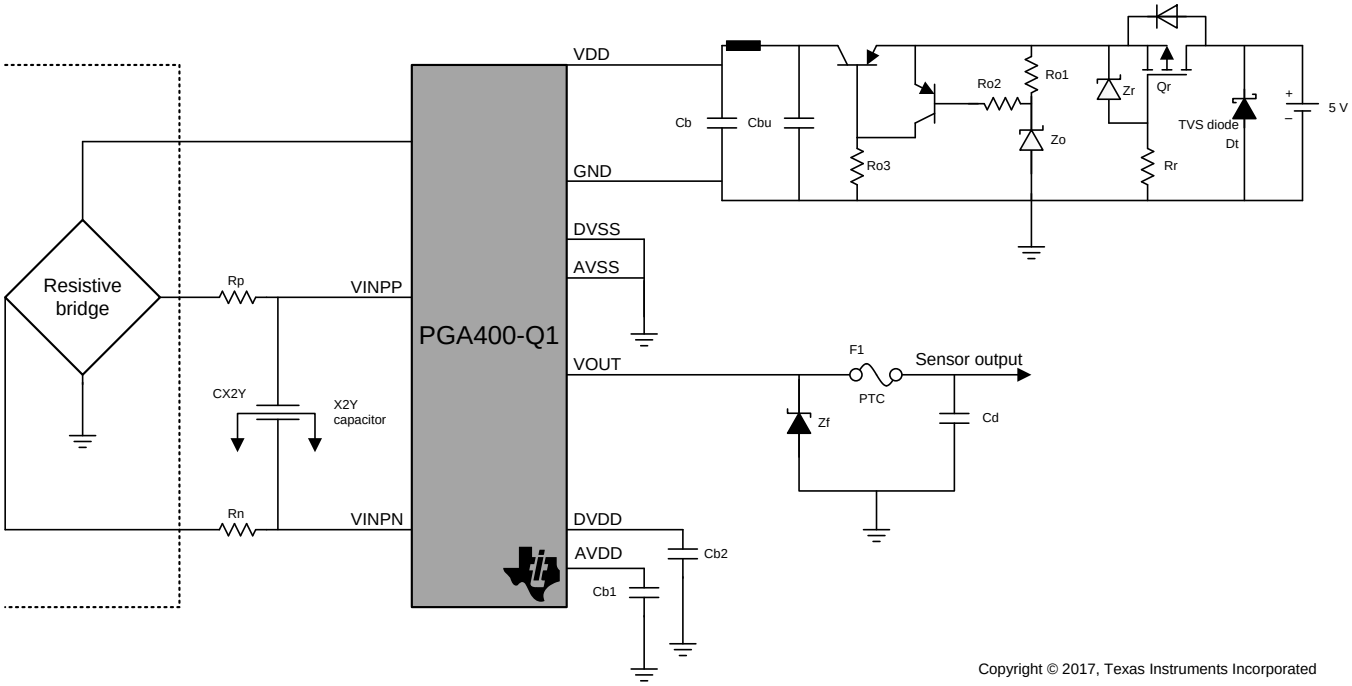

Figure 8. Conceptual Schematic Diagram

5.3.1 Frond End

Figure 9 shows the AFE module. Resistive sense elements in a Wheatstone bridge configuration are given to the EMI filters in order to remove radiative and conductive electromagnetic noise. Due to issues such as small output voltage and different types of non-idealities, achieving overall system accuracy is critical but very important in automotive pressure sensor applications. The front end pressure sensor signal chain consists of a resistive sense element in the front, an EMI filter, gain stage, offset correction stage, second gain stage, ADC (sigma delta), and a decimation filter.

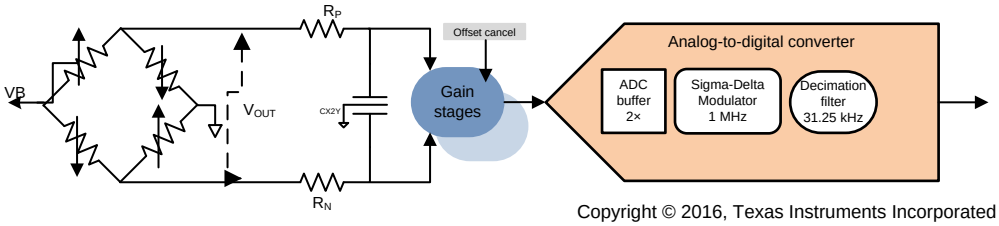

Figure 9. AFE

The ADC in the PGA400-Q1 has three main stages: the ADC buffer, sigma-delta modulator, and decimation filter. To ensure the input signal is as free of noise as possible, a low-pass filter network is placed between the bridge output and the PGA400-Q1 input pins. The input filter is designed in such a way to remove both common-mode and differential-mode noise components. As shown in Figure 10, a single pole RC filter is designed. Only the first-order filter is used because of the placement of the resistive bridge (which is very near to the sense element), so it is less prone to EMI noise.

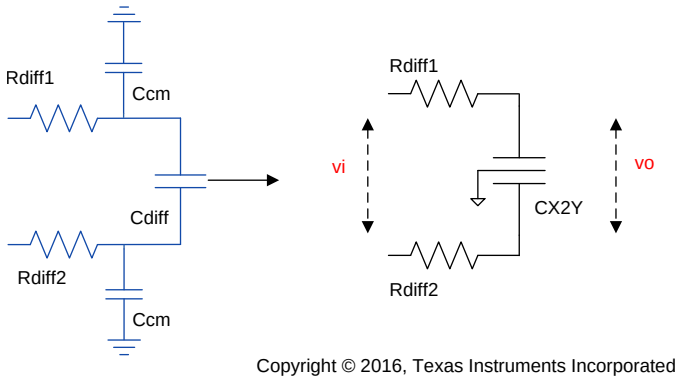

Figure 10. Sensor Voltage Input Filter

5.3.1.1 Filter Cutoff Frequency

The current design proposes a band of frequencies based on interference from the sigma-delta modulator frequency, decimation filter output data rate, and sense element configuration the user can select exact sensor cutoff frequency.

The PGA400-Q1 front end (ADC) cannot digitally reject noises of higher frequencies. Analog input filtering is required to reject noises of higher frequencies, as shown in Figure 11, Figure 12, and Figure 13. Sigma-delta ADCs (which the PGA400-Q1 has) specify the sampling frequency of the modulator to allow external filters to be designed accordingly. The PGA400-Q1 has a modulator sampling frequency of 1 MHz. As shown in Figure 11, the actual sensor signal is at low frequencies compared to the modulator frequency and output data rate. The unwanted signal components are rejected by the decimation filter; the external analog filter removes the harmonics that are left by decimation filter. In order to remove the harmonics, the cutoff frequency can be chosen to be less than the Nyquist rate (< 0.5 MHz). Additionally, between 0 to 0.5 MHz the cutoff frequency can be chosen depending on the sense element configuration.

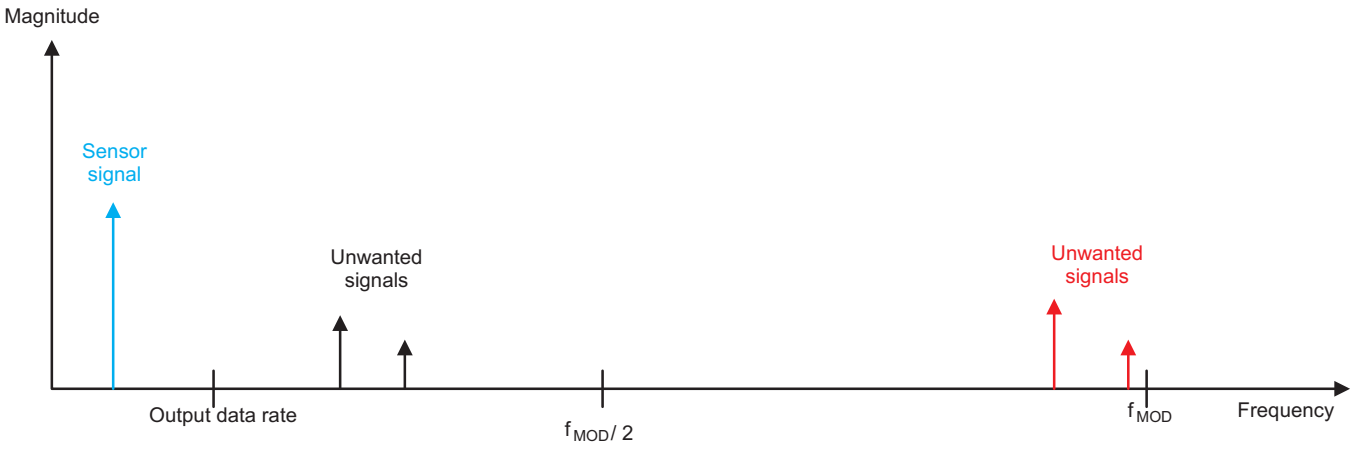

Figure 11. Unwanted Signal in Frequency Domain

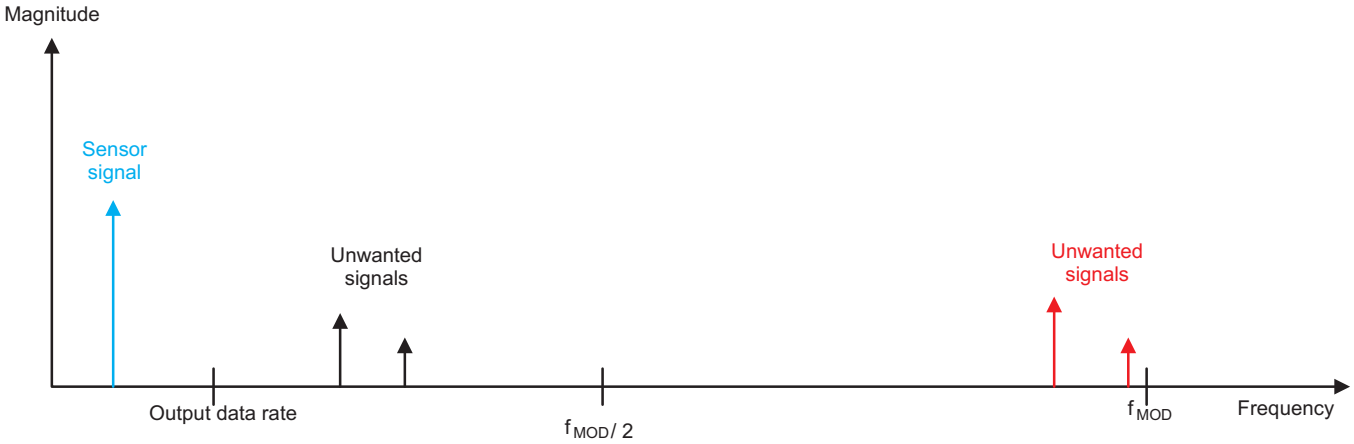

Figure 12. Aliasing After Sampling

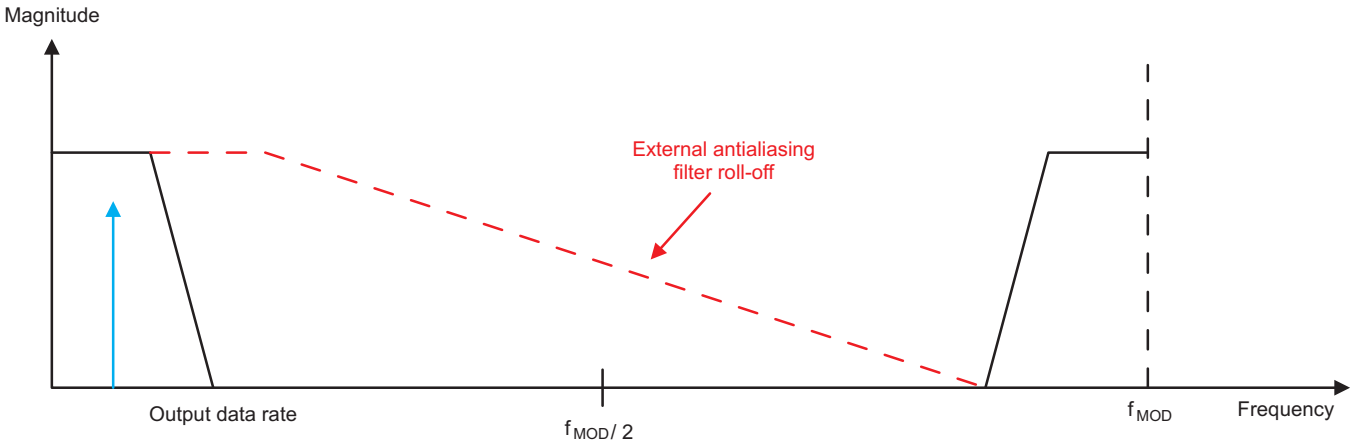

Figure 13. Antialiasing Filter

5.3.1.2 Resistors and Capacitors Selection

The left filter shown in Figure 14 is an example of a structure commonly used for differential signals. There are a few important points to consider when selecting components. To avoid differential noise caused by mismatches in the common-mode capacitors, an X2Y capacitor is selected to perfectly match the common mode capacitive values without having any tolerances between capacitors. In addition, the X2Y structure includes an effective auto-transformer or common-mode choke. As a result, when these devices are used for common-mode filters, they provide greater attenuation of common-mode signals above the filter's corner frequency than a comparable RC filter. As shown in the right of Figure 14, this usually allows the omission of the differential capacitor, with subsequent savings in cost and board space.

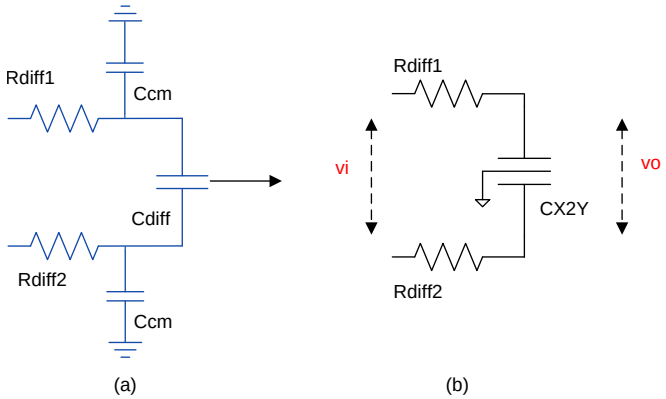

Figure 14. RC Low-Pass Filter

The chosen capacitor and resistor values are $R_{DIFF1} = R_{DIFF2} = 49.9\ \Omega$ and CX2Y = 0.01 µF.

$$f = \frac{1}{2 \times \pi \times R_{DIFF} \times C_{CM}} = \frac{1}{2 \times \pi \times 49.9 \times 100\ nF} = 318.95\ kHz \quad (1)$$

Figure 15 and Figure 16 show the design simulation of RC low-pass filter with the above derived component values. An X2Y capacitor with two matching common mode capacitors (C1, C2) introduces no noise in the differential output signal.

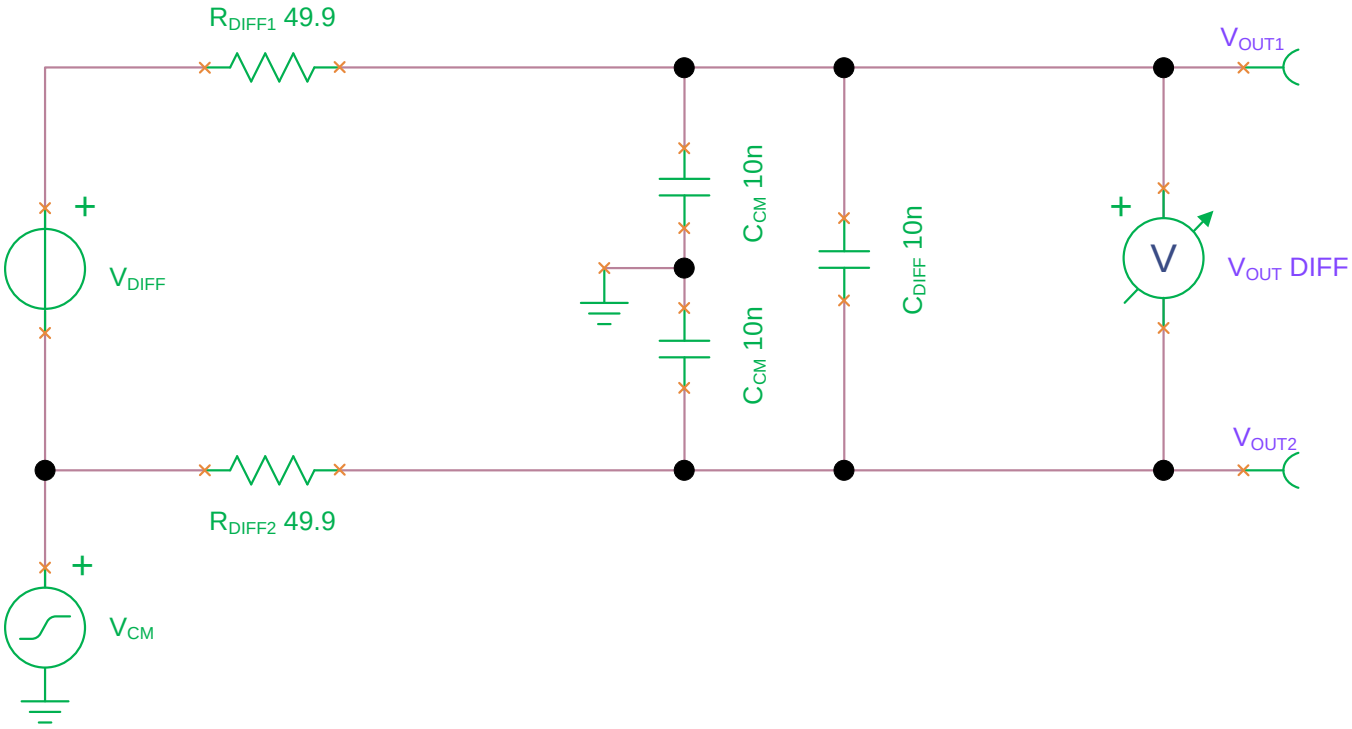

Figure 15. Low-Pass Filter Simulation

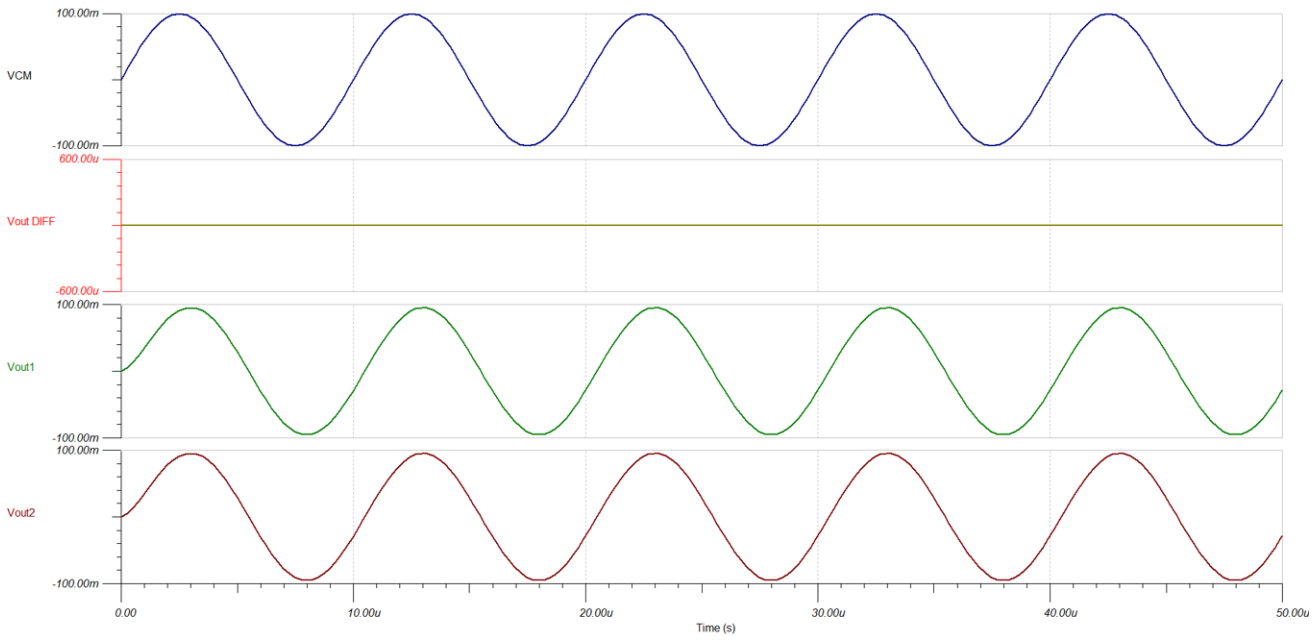

Figure 16. Matched Common-Mode Filter

5.4 Power Supply Stage

The main purpose of the external power supply stage is to protect the PGA400-Q1 from transients, overvoltages, and reverse polarities. Figure 17 divided into three stages:

1. Transient pulse suppression
2. Reverse polarity protection
3. Overvoltage protection

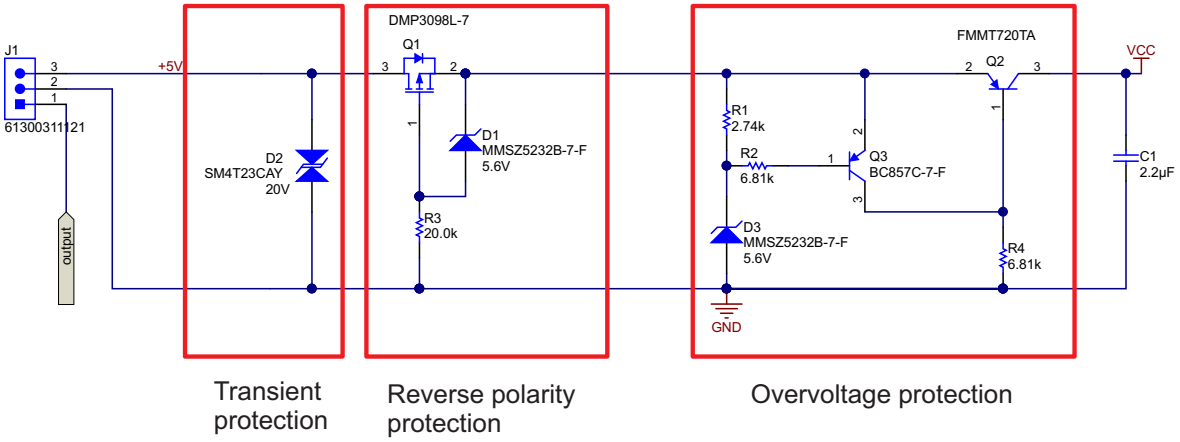

Figure 17. Power Supply Stage

5.4.1 Transient Pulse Suppression

To provide immunity for transients at a system level, external transient protection is installed. The effect of transients on the pressure sensor is mainly due to the wiring harness faults (coupling transients). The circuit was made according to ISO 7637-3 standards and as per the standard, there are two main types of coupling effects (capacitive or inductive) on supply lines. The strength of pulses according to level IV would be in magnitudes of –60 V and 40 V and with varying times. These coupling effects are not from the supply lines, but supply lines itself could also affect coupling transients because of other wiring harness coupling mechanisms. The diode breakdown voltages must be chosen such that transients are clamped at voltages that will protect the MOSFET and the rest of the system. In the present case, there is a need to protect a continuous 20-V signal, so the breakdown voltage of the TVS should be more than 20 V (typical 23.4-V breakdown voltage diode selected). A TVS diode with a breakdown voltage of 24 V and a clamping voltage of 33 V is selected to serve this purpose. The reverse clamping device will clamp all negative voltages greater than the battery voltage so it does not short out during a reverse-battery condition.

The other parameter to choose for the TVS diodes is the peak power rating. This is important because it is proportional to the package size of the diodes. Measure the amount of peak power that the diode can see to size the package properly. The important features are its clamping voltage, the voltage of the pulse it is clamping, and the source impedance of the pulse. The rise time and duration of the pulse also play a role, although not an immediate one.

The following is an example of calculating for Pulse B from ISO 7637-3, which ends up being the worst case (test level IV):

- V_{PULSE} = 40 V
- R_{SOURCE} = 50 Ω
- V_{CLAMP} = 32.4 V (for 10/1000 µs)

The worst case assumption is that the load draws very little current, so the majority will go through the TVS diodes. If V_{PULSE} = 32.4 V and pulse generator generates a 40-V pulse, this implies that there is a 7-V drop across R1 (the source impedance of the pulse as defined in ISO 7637-3), 7.6 V / 50 Ω = 0.152 A, coming out of the pulse generator. Most of this passes through the TVS diode, and so one can estimate the peak power seen by the device as P = I × V = 32.4 V × 0.152 A = 4.9248 W. Based on the specifications listed, a 400-W, 32.4-V clamping voltage TVS diode is selected.

5.4.2 Reverse Polarity Protect

The circuit in Figure 17 withstands reverse power-supply voltages. The power supply circuit provides a –20-V reverse voltage protection capability. Three simple additions (components) to the circuit in Figure 17 will provide the necessary reverse-voltage protection. The circuit employs a P-channel MOSFET. By configuring the MOSFET as shown, the device's body diode will automatically conduct when a power supply voltage of greater than about 0.5 V is present. The body diode of this transistor is a necessary feature because without it the circuit will not start up. The addition of this component provides a disconnect function under reverse-voltage conditions. The requirements for the reverse protection MOSFET is that the ON resistance (R_{ON}) should be a low to have less forward voltage drop. A DMP3098L serves this purpose and it has 120-mΩ ON resistance. A Zener diode and resistor configuration is used to protect the MOSFET.

5.4.3 Overvoltage Protection

The main pass element in the protection circuit shown in Figure 17 is the PNP transistor Q2. Take care when selecting this part because any drops in the power supply voltage will be determined by the characteristics of this transistor. The FMMT720T device has been used for this duty. The FMMT720T is one of a family of devices that exhibit very low VCE saturation voltage values. This minimizes the voltage drop induced by the presence of the protection circuit. The transistor Q3 acts as the control element for Q2 and will turn on (turning Q2 off) when the voltage at the power supply input is equal to the sum of the Zener voltage due to diode D3 and Q3's own VBE voltage at a collector current of about 650 µA. Q3 and D3 together produce a typical trip voltage of 5.85 V at 25°C. Approximately 0.53 V of this is due to the VBE voltage of Q3. The remaining 5.32 V is produced across D3. Note that the Zener diode D3, although a nominal 5.6-V device, is being operated at a very low reverse current, about 200 µA, as defined by the VBE of Q3 together with the 2.7-kΩ resistor. At this current, the Zener voltage is below the characteristic "knee" and is therefore less than the rated value. The 6.8-kΩ resistor connected to the base of Q3 provides the current necessary to keep Q2 turned on under normal circumstances.

5.5 Output Stage

The output protection is achieved with the combination of a Zener diode and resettable fuse. This circuit consists of a series element, a resettable fuse, and a parallel element Zener diode. The series element limits the current and the parallel element clamps the voltage level. The resettable fuse disconnects or breaks when the there is a large current passing through the fuse.

When an input voltage exceeds the Zener diode breakdown voltage parameter, there is a sudden surge in current through the Zener diode and in the resettable fuse. The temperature increase in the fuse causes the fuse to break the circuit. The resistance of the fuse will increase many folds, which is equivalent to the circuit being open. When the overvoltage condition is removed, the current stops flowing through the fuse and the temperature of the fuse reduces, thus closing the circuit again after some time.

5.5.1 Reverse Voltage Protection on Output Pin

When a reverse voltage is applied at the input, the Zener diode will be forward biased. There will a large surge of current through the PTC fuse leading to an increase in temperature of the fuse, and hence the circuit breaks.

The main advantage of this circuit is that it can protect the devices and systems from all EOS scenarios—overvoltage, reverse voltage, short circuit, and overcurrent. Only two components are added to the BOM. The two main parameters of a resettable fuse are the "I_{HOLD}" current and the series resistor. The I_{HOLD} current is the current up to which the fuse will not break. This current value must be equal to or slightly more than the systems maximum current consumption. To keep the series voltage drop across the fuse minimum, use a fuse with the least series resistance. A Zener diode must be chosen such that the breakdown voltage of the Zener diode is equal to or slightly more than the working voltage of the system being protected. However, the breakdown voltage must not exceed the maximum voltage limit of the system being protected.

In resettable fuses as the resistance is decreasing, I_{HOLD} current is increasing. To have an optimum value between the I_{HOLD} current and series resistance, a resettable fuse with an I_{HOLD} current of 200 mA and a series resistance of ~1 Ω is chosen. In normal operation, the fuse will not break, and with a very small voltage drop, the output signal follows the path to ECU. Whenever an overvoltage event occurs, the resettable fuse forms a loop with the 7.5-V, 1.5-W Zener and fuse breaks. Figure 18 shows the output overvoltage protection circuit.

NOTE: To facilitate OWI communication, a Zener diode with a 7.5-V rating is selected.

The maximum power that the Zener diode handles in an overvoltage condition is:

$$P = V \times I = 7.5\ V \times 200\ mA = 1.5\ W \quad (2)$$

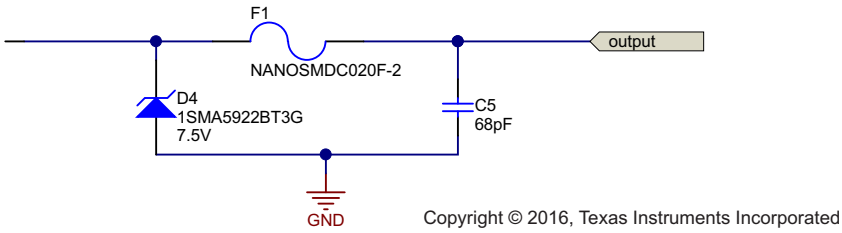

Figure 18. Output Overvoltage Protection

6 PCB and Form Factor

The only goal of the design with regards to the PCB is to make as compact a solution as possible while still providing a reasonable way to mount the components to remove EMI noise. Figure 19 compares a PCB size to a pencil tip.

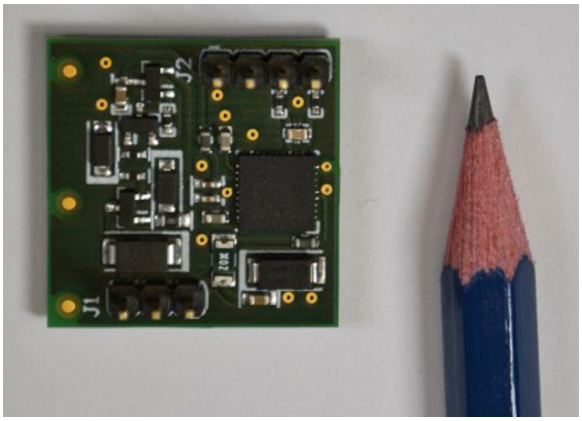

Figure 19. TIDA-00793 Board Form Factor

7 Harness Fault Conditions and Solutions

Table 2 describes the possible combinations of harness faults for the pressure sensor mechanism. The circuit is designed to meet all these harness faults. Each case describes the way these fault conditions are handled.

Table 2. Harness Fault Conditions

FAULT NO	DEVICE VDD	DEVICE GND	DEVICE V_{OUT}	REMARK	DEVICE STATUS AFTER REMOVAL OF FAILURE
1	5 V	0 V	Pull up to VDD	Normal connection with V_{OUT} to be pulled to VDD	Safe
2	5 V	0 V	Pull down to GND	Normal Connection with V_{OUT} to be pulled to GND	Safe
3	20 V	0 V	GND to VDD	Overvoltage	Safe
4	Open	0 V	Pull up to VDD	Open VDD with V_{OUT} to be pulled to VDD	Safe
5	Open	0 V	Pull down to GND	Open VDD with V_{OUT} to be pulled to GND	Safe
6	5 V	Open	Pull up to VDD	Open GND with V_{OUT} to be pulled to VDD	Safe
7	5 V	Open	Pull down to GND	Open GND with V_{OUT} to be pulled to GND	Safe
8	0 V	20 V	Pull up to VDD	Reverse voltage with V_{OUT} to be pulled to VDD	Safe
9	0 V	20 V	Pull down to GND	Reverse voltage with V_{OUT} to be pulled to GND	Safe
10	0 V	0 V	Pull up to VDD	VDD shorted to GND with V_{OUT} to be pulled to VDD	Safe
11	0 V	0 V	Pull down to GND	VDD shorted to GND with V_{OUT} to be pulled to GND	Safe
12	20 V	20 V	Pull up to VDD	GND shorted to VDD with V_{OUT} to be pulled to VDD	Safe
13	20 V	20 V	Pull down to GND	GND shorted to VDD with V_{OUT} to be pulled to GND	Safe
14	20 V	0 V	20 V	V_{OUT} shorted to VDD	Safe
15	20 V	0 V	Pull down to GND	V_{OUT} shorted to GND	Safe

Set up the hardware as shown in Figure 20. Apply different combinations of voltages at J1 connector as described in Table 2.

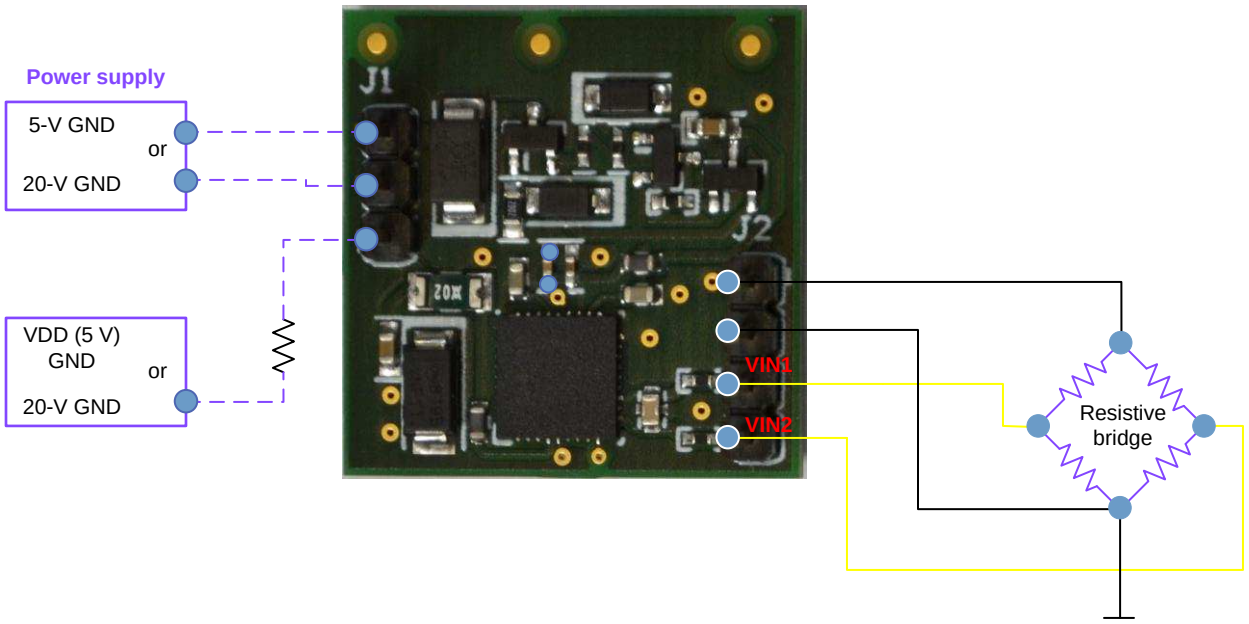

Figure 20. Power Supply Connections for Harness Faults

7.1 Case 1: VDD = 5 V, GND = 0 V, V_{OUT} = 5 V (VDD)

Apply a voltage (5 V) to output pin through a 1-kΩ pullup resistor.

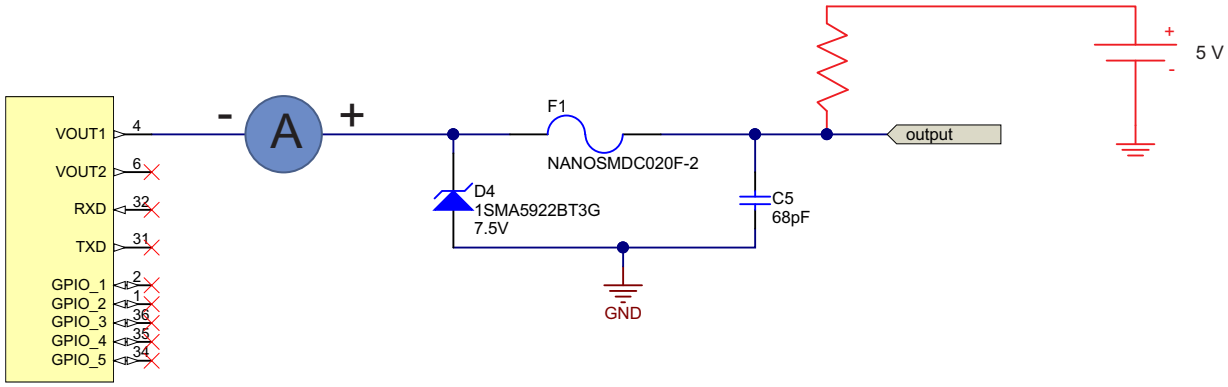

Figure 21. 5-V Across Output Pin

Internal current limit protection is available when the output is at 5 V (30-mA short to battery). No external protection circuitry is required. This is a safe case and the signal follows the normal path.

7.2 Case 2: VDD = 5 V, GND = 0 V, V_{OUT} = 0 V (GND)

Output to ground and the power supply is at 5 V. A dead short to ground can allow as much as 30 mA of current to flow. This is a safe case.

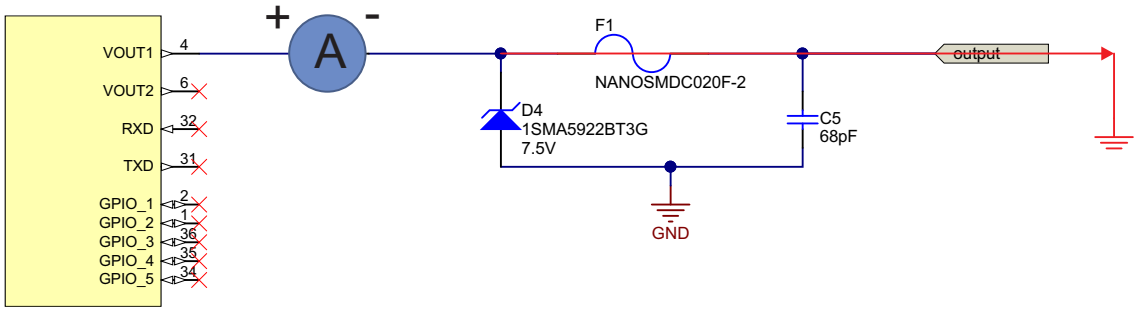

Figure 22. Output Connected to Ground

7.3 Case 3: VDD = 20 V, GND = 0 V, V_{OUT} = 5 V (VDD)

Same as Section 7.14 (see Section 7.14 for details), the power supply section opens (overvoltage condition). When the output is at 5 V with VDD open, all circuits inside the PGA400-Q1 try to power up, but nothing happens to the device as it cannot pass much current inside.

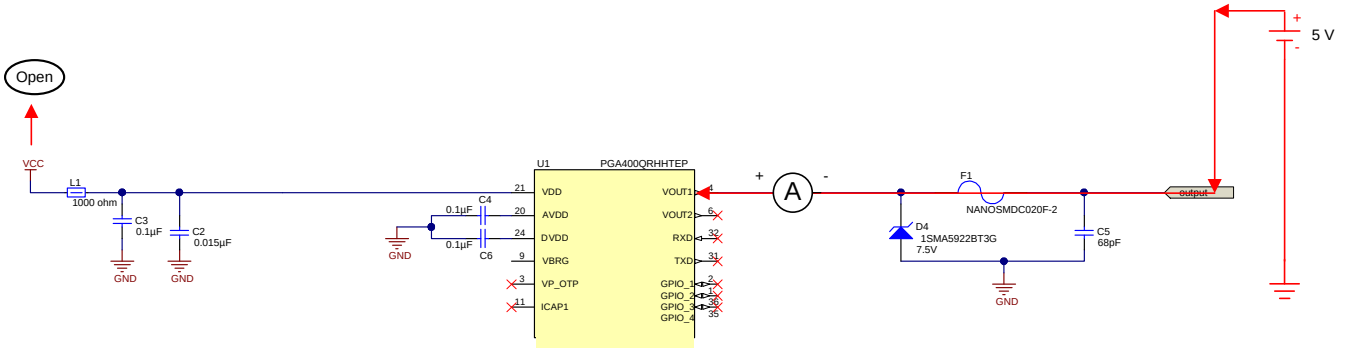

Figure 23. VDD Opens and Output is at 5 V

This is a safe case.

7.4 Case 4: VDD = OPEN, GND = 0 V, V_{OUT} = 5 V (VDD)

As described in Section 7.3, the power supply section opens. When the output is at 5 V with VDD open, all circuits inside the PGA400-Q1 try to power up, but nothing happens to the device as it will not pass much current inside. This is a safe case.

7.5 CASE 5: VDD = OPEN, GND = 0 V, V_{OUT} = 0 V (GND)

In this case, there is no possibility of excess current to flow because no potential exists and the device is safe. This is a safe case.

7.6 CASE 6: VDD = 5 V, GND = OPEN, V_{OUT} = 5 V (VDD)

The two ends of the internal pullup diode are at same voltage. There is no path for the excess current to flow as the diode is not conducting. The device is safe. This is a safe case.

7.7 CASE 7: VDD = 5 V, GND = OPEN, V_{OUT} = 0 V (GND)

All the internal circuits of the PGA get power and try to discharge through the V_{OUT} pull-down diode.

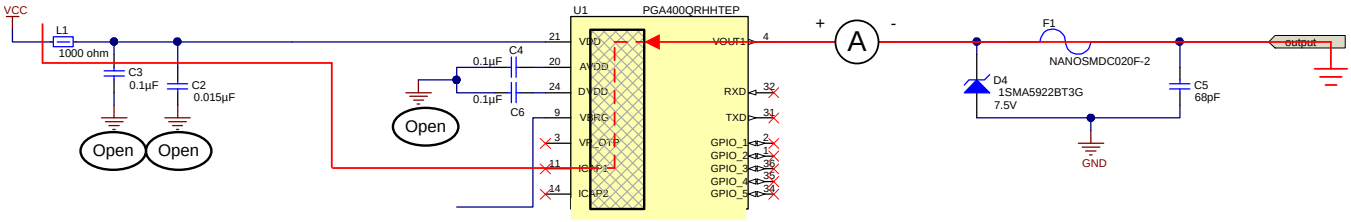

Figure 24. Original Ground Open and Ground Connected to Output

The device is safe.

7.8 CASE 8: VDD = 0 V, GND = 20 V, V_{OUT} = 5 V (VDD)

In the power supply section, reverse voltage protection is achieved using PMOS and Zener diode configuration. As shown in Figure 25, when the reverse voltage is applied across the terminals, gate source voltage (VGS) is not sufficient for the PMOS to switch ON, meaning PMOS is in OFF condition. This implies that the other part of the circuit is floating. VDD of the PGA400-Q1 is open because of the reverse polarity protection implemented. The device is safe. The Zener diode protects the PMOS from higher voltages.

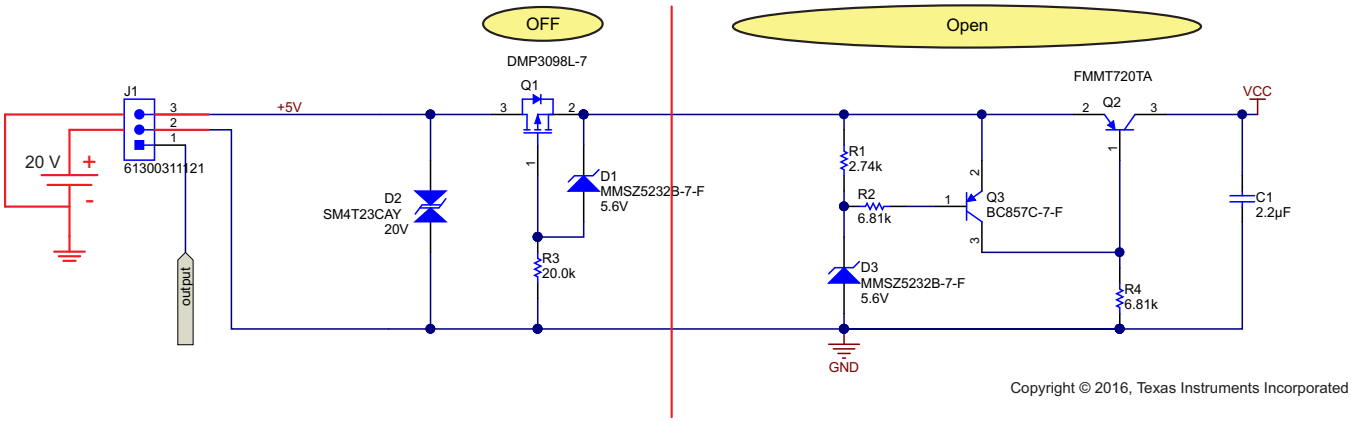

Figure 25. Reverse Polarity Protection

Now the condition evolves into an open VDD with GND 20 V, and output is at 5 V. As described in Figure 26, there exists a high current path in between the 5- and 20-V supply. The output fuse opens as high current flows, implying the output is floating. As a result, output and VDD are open. The device is safe.

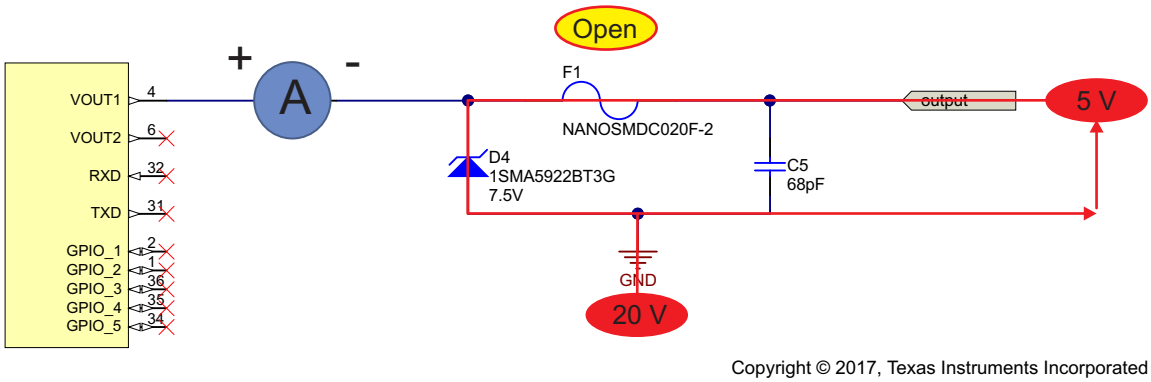

Figure 26. Output Protection When Ground is at 20 V and Output is at 5 V

This is a safe case.

7.9 CASE 9: VDD = 0 V, GND = 20 V, V_{OUT} = 0 V (GND)

Reverse voltage protection is applied and circuit behaves according to Section 7.8 (VDD opens). Output is grounded with VDD open and ground at 20 V. There is no path for the current to flow through the PGA400-Q1 because supply is open and no closed loop exists. The only possibility for the current to flow is through a Zener diode to fuse to the output. The Zener diode forward current is 200 mA; when the current is more than 200 mA, the fuse opens and the circuits survive.

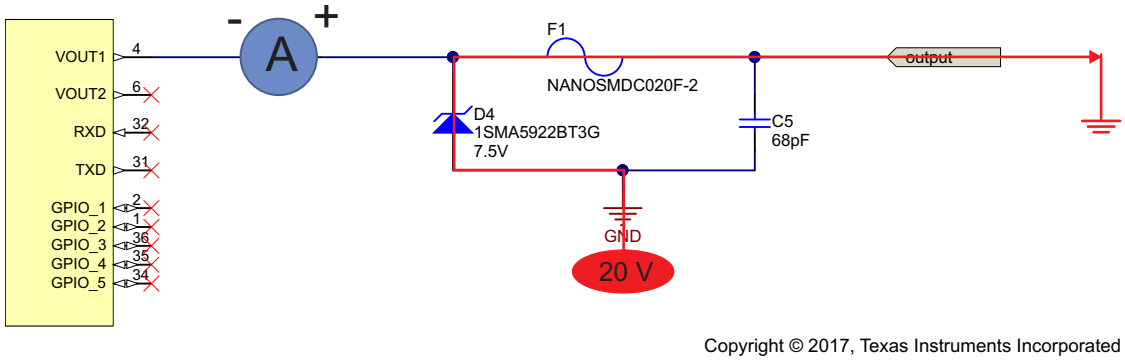

Figure 27. Ground is at 20 V and Output is Grounded

7.10 CASE 10: VDD = 0 V, GND = 0 V, V_{OUT} = 5 V (VDD)

There is no effect on the circuit (see Section 7.4). This is a safe case.

7.11 CASE 11: VDD = 0 V, GND = 0 V, V_{OUT} = 0 V (GND)

There is no effect on the circuit as everything is grounded, and no potential exists in the circuit (see Section 7.5). This is a safe case.

7.12 CASE 12: VDD = 20 V, GND = 20 V, V_{OUT} = 20 V

The initial PMOS does not have enough voltage (threshold voltage) to turn ON; both positive and negative supplies are in 20 V. VCC opens.

On the output section, applying 20 V with respect to 20 V (GND) means nothing applied (GND) across the output. The output shorted to 0 V, same as Section 7.5. This is a safe case.

7.13 CASE 13: VDD = 20 V, GND = 20 V, V_{OUT} = 0 V (GND)

VDD is open and output is grounded (Section 7.5). This is a safe case.

7.14 Case 14: VDD = 20 V, GND = 0 V, V_{OUT} = 20 V

Once the voltage at the output pin is greater than the supply voltage (5 V) by about 0.5 V, the internal top diode (pullup diode) starts to conduct and it cannot tolerate high voltages, resulting in a high voltage across the output pin and the chip might damage. Output protection needs to be implemented in this case.

Also according to absolute maximum ratings of PGA400-Q1, it can only survive until 16 V. Applying 20 V might damage the chip. Overvoltage protection is needed in this case for 20 V.

7.14.1 Power Supply Protection

The transistor Q3 acts as the control element for Q2 and will turn on (turning Q2 off) when the voltage at the power supply input is equal to the sum of the Zener voltage due to diode D3 and Q3's own VBE saturation voltage. Q3 and D3 together produce a typical trip voltage of 5.85 V. This path exists only when the Zener diode has a sufficient voltage to breakdown (in overvoltage situations); in normal cases, the 6.8k resistor connected to the base of Q2 provides the current necessary to keep Q2 turned on. As shown in Figure 28, the circuit operates to disconnect the load during overvoltage conditions, meaning Q2 switches off when an overvoltage condition is detected, removing power from the load. Q2 will turn on again when the overvoltage condition is removed.

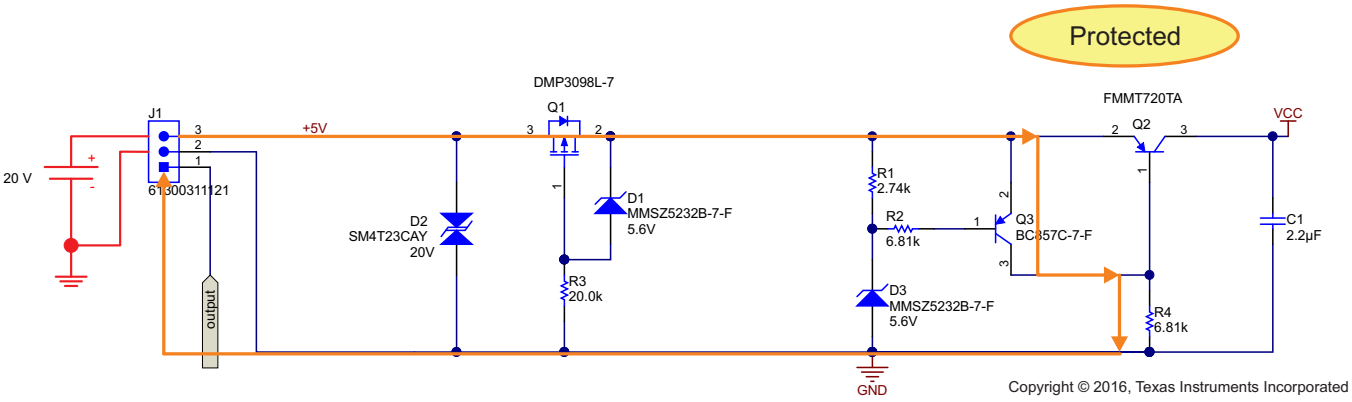

Figure 28. Power Supply Protection

7.14.2 Output PIN Protection

As shown in Figure 29, consider the case when the output is at 20 V. Then the voltage across the fuse becomes high thereby current and fuse opens. Consider its resistance is 650 mΩ with a 20-V output, then most of the current flows through the fuse and it opens, the fuse takes almost 100 ms to blow, in this time Zener should tolerate this current; therefore, Zener has to be selected in such a way that, it should handle a high pulse current.

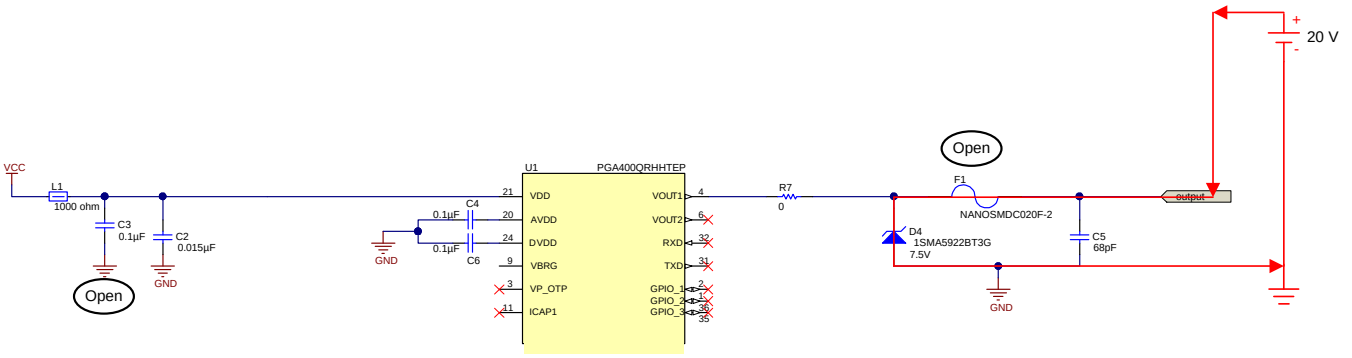

Figure 29. Output Pin Protection

This is a safe case.

7.15 Case 15: VDD = 20 V, GND = 0 V, V_{OUT} = 0 V (GND)

The output is short to ground and power supply is at 20 V (overvoltage), implying VDD opens. With the VDD open and output grounded, there is no potential existing in the network. The device is safe.

8 Sensor Connectivity and Gain Input Faults (Diagnostic Resistors Active)

Behavior is analyzed when resistive sense elements have wrong connections with the input pins of the PGA400-Q1. Connect the hardware as shown in Figure 30.

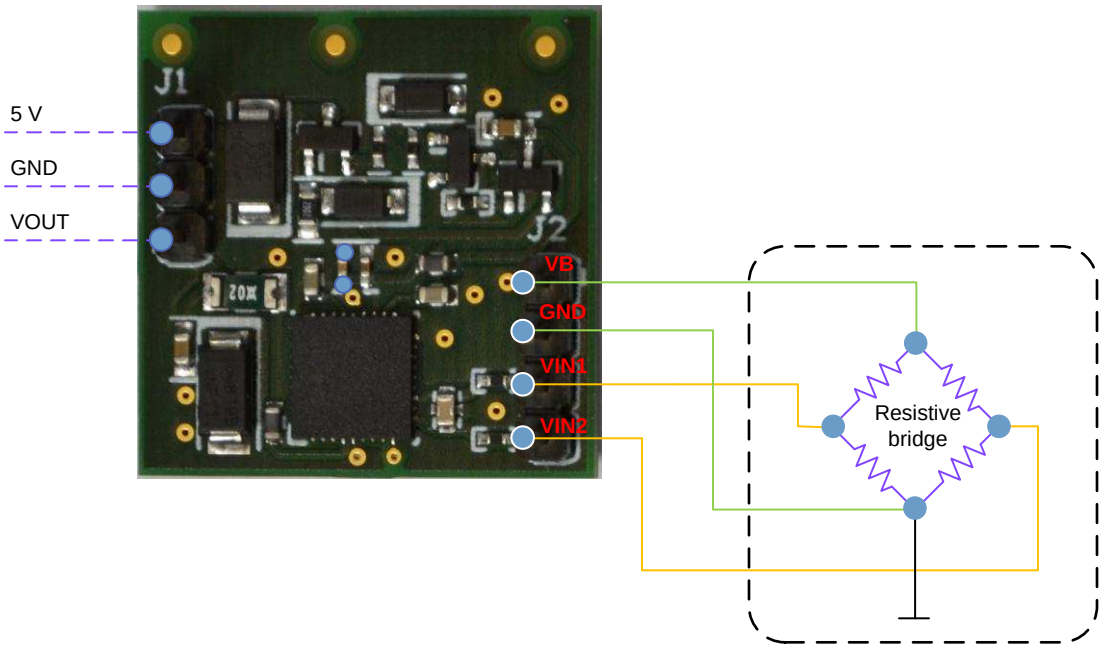

Figure 30. Sensor Connectivity and Gain Input Faults Connections

Apply the different combinations as shown in Table 3.

Table 3. Sensor Connectivity and Gain Input Fault Combinations

FAULT NO	FAULT MODE	PGA400-Q1 BEHAVIOR (OUTPUT BEHAVIOR)
16	VBRGP open (VB)	Stable
17	VBRGN open (GND)	Stable
18	VINPP open (VIN1)	Stable
19	VINPN open (VIN2)	Stable
20	VBRGP (VB) shorted to VBRGN (GND)	Stable
21	VBRGP (VB)shorted to VINPP (VIN1)	Stable
22	VBRGP (VB) shorted to VINPN (VIN1)	Stable
23	VINPP (VIN1)shorted to VINPN (VIN2)	Stable
24	VINPP (VIN1) shorted to VBRGN (GND)	Stable

9 Hardware

For the initial board setup, the following equipment is required:

- TIDA-00793 PCB with the PGA400-Q1 preprogrammed on it
- PGA400-Q1 EVM with TI-GER USB board
- PC (PGA400-Q1 GUI installed)
- 5-V battery or power supply
- 12-V battery or power supply
- External bridge (sense element)
- HP 3458A 8½ digit multimeter (preferably)
- Keithley 2001 6½ digit multimeter (preferably)

To calibrate the PGA400-Q1 for a particular sense element, connect the hardware as shown in Figure 31.

9.1 Hardware Setup for Calibration

1. Connect the 5-V power supply or battery to connector J1:1-2 (40-mA current limitation).
2. Connect J1:3 to the HP 3458A 8½ digit multimeter.
3. Connect the external bridge to connector J2 as shown in Figure 31.
4. Connect the Keysight 6½ digit multimeter to connector J2: 3-4.
5. Connect the 12-V power supply to the PGA400-Q1 EVM (100-mA current limitation).
6. Connect the output terminal of the TIDA-00793 (J1:3) to the GPIO: VOUT1 pin of PGA400-Q1 EVM (to establish OWI), as shown in Figure 31.
7. Connect the EVM and TIDA-00793 grounds (J1:2 to GPIO: GND) as shown in Figure 31.
8. Connect the PGA400-Q1 EVM to the PC through TI-GER USB board as shown in Figure 31.

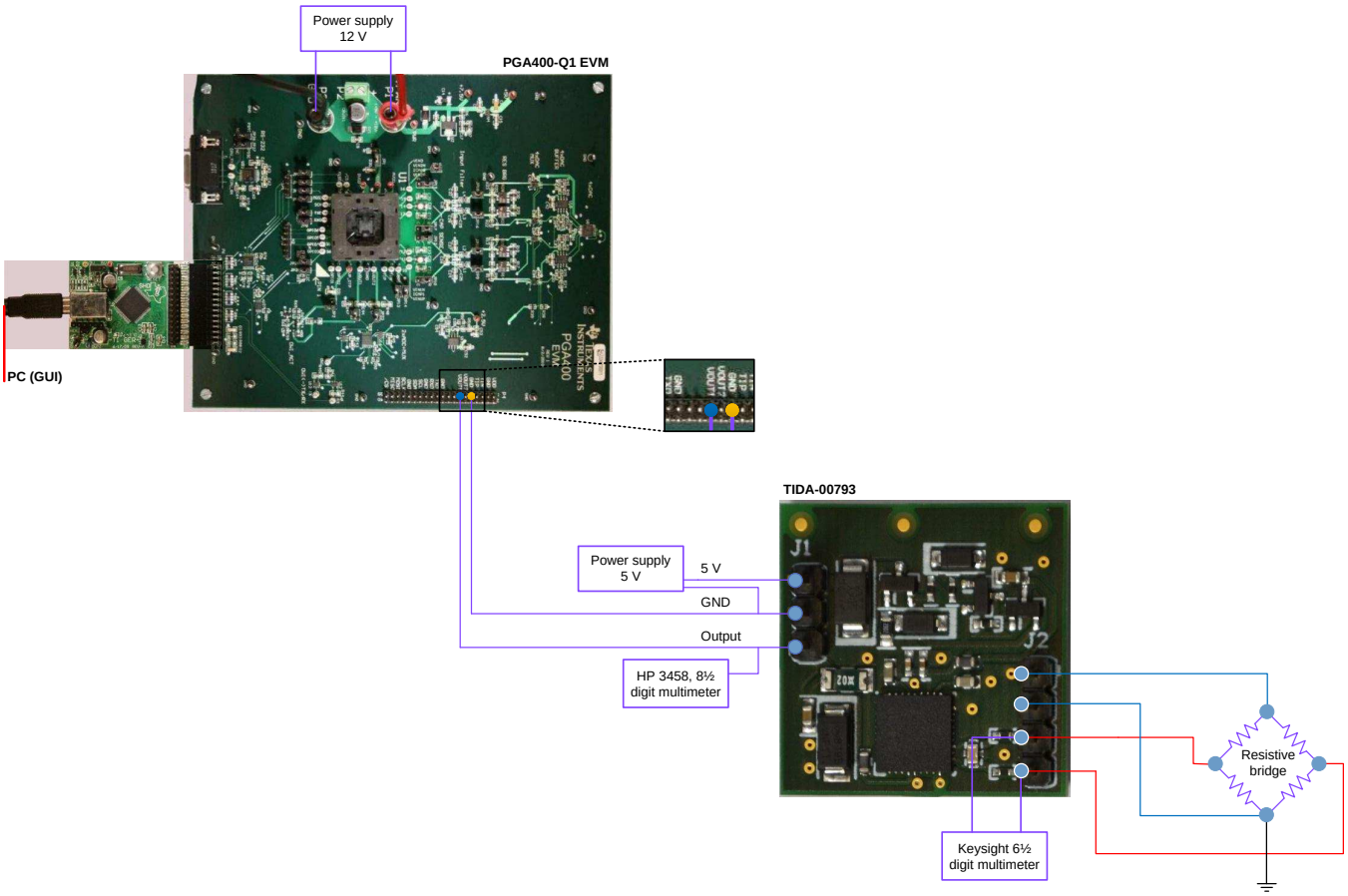

Figure 31. TIDA-00793 Connection to PGA400-Q1 EVM

9. Connect the jumpers on the PGA400-Q1 EVM as shown in Figure 32 (Although the jumpers are installed to default settings in the factory, TI recommends the user verify that the shunts are installed to the default settings before powering on the EVM).

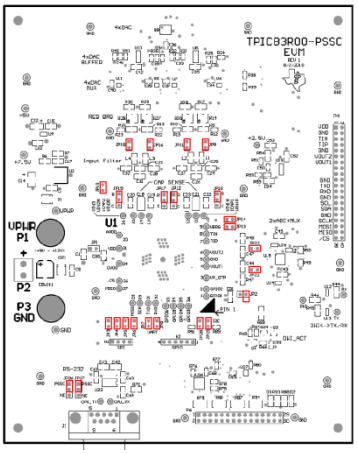

Figure 32. Default Jumper Settings

9.2 Final Hardware Connection to ECU (After Calibration)

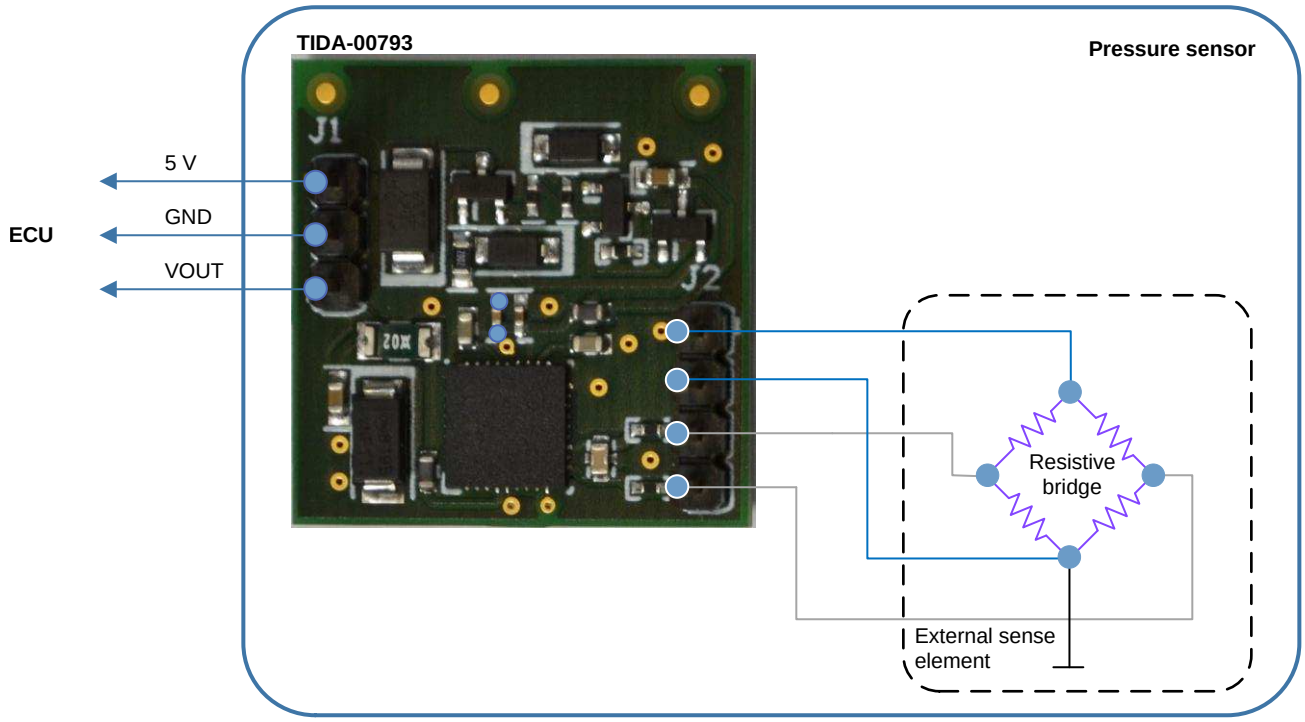

Figure 33. Sensor to ECU Connection

10 Calibration Procedure

The PGA400-Q1 comes with built-in programming for the pressure sensors applications. But there are different pressure sensors with different voltage levels. To calibrate the PGA400-Q1 for a particular sense element the user needs to calibrate the PGA400-Q1. The device can be calibrated using the OWI pin of the PGA400-Q1. The VOUT pin on the PGA400-Q1 is responsible for the OWI communication. OWI driver circuitry and PC interface (TI-GER USB board) circuitry is available on the PGA400-Q1 EVM, so PGA400-Q1 EVM needs to be interfaced with the TIDA-00793 in order to do the calibration. Connect the PGA400-Q1 EVM to the TIDA-00793 board as shown in Figure 31.

The following steps describe the calibration procedure in detail. For easy understanding and to avoid confusion, a step-by-step procedure is described by taking an example sensor bridge.

10.1 Step 1: Hardware

Connect the hardware as described in Section 9.1 (and as shown in Figure 31).

10.2 Step 2: Software

Verify all the listed required files are available before starting the procedure:

- PGA400-Q1 GUI
- PGA400-Q1 coefficient calculations spreadsheet
- PGA400-Q1 signal chain spreadsheet
- PGA400-Q1 EEPROM memory MAP

10.3 Step 3: OWI Starting

1. Power up EVM power supply and the TIDA-00793 power supply.
2. Start the PGA400-Q1 GUI.
3. Click on OWI in the right half of the GUI → *1. Activate OWI with Over-Voltage Drive* → *2. Activate TI-GER UART*.
4. Click on the *TEST* tab in the left half of the GUI and click on *IFSEL/uc_RST* to reset the microcontroller. "03" should appear under the register *OE Micro CTL*. This verifies that the hardware is connected properly and the sensor is ready for calibration.

10.4 Step 4: Gain and Offset Setting

1. To calibrate, implant a resistive bridge with normal resistors. For example, assume the sensor voltage range (bridge output voltage) is from –22.5 to 213.5 mV (at 25°C).
2. Configure Gain 1 and Gain 2 using the PGA400-Q1 signal chain spreadsheet in such a way to get the ADC input in between –1.65 to 1.65 V.
3. Enter the Gain 1 and Gain 2 values in the *EEPROM → BANK5 → SEN1GAIN* section. Here in the present case, Gain 1 = 4.43 and Gain 2 = 1.67 are selected (which gives ADC input in between –1.65 to 1.65 V). Enter "25(HEX)" in the *SEN1GAIN* section in *EEPROM BANK5* [see *7.3.4 Sensor 1 Gain Register (SEN1GAIN)* of the PGA400-EP datasheet (SLDS195)].
4. Go to *EEPROM BANK5 → SEN1OFF1* = 00, *SEN1OFF2* = A0.
5. Click *WRITE ALL*.
6. Click *Program EEPROM*.
7. Click *Reload Cache* to verify whether it is written in EEPROM registers or not. The GUI should look like Figure 34.

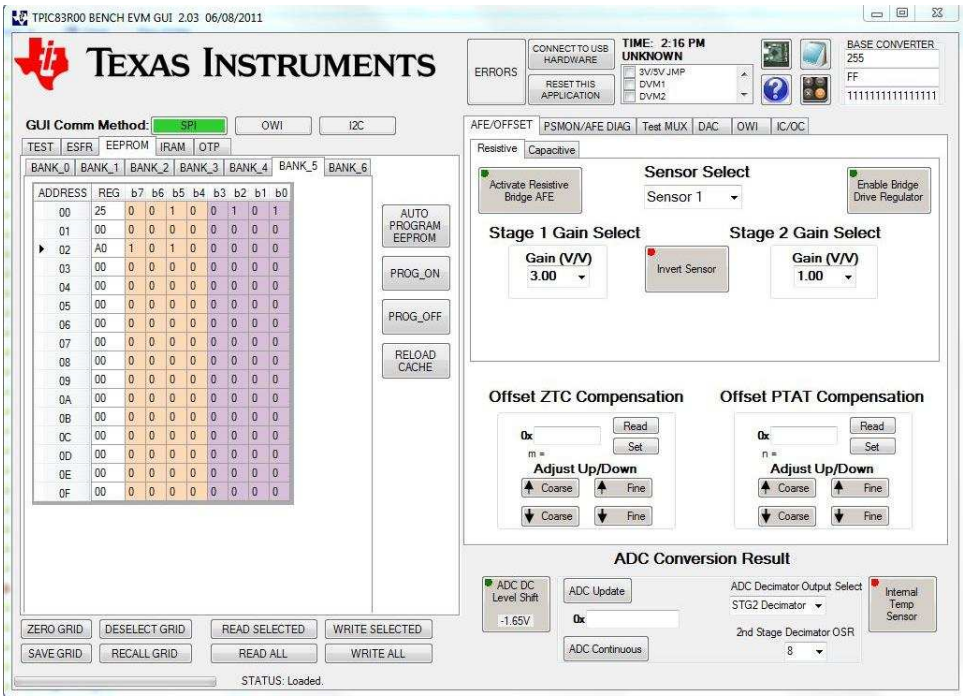

Figure 34. EEPROM BANK_5 Registers in PGA400-Q1 GUI

10.5 Step 5: ADC Calibration

NOTE: First, complete the 3P-1T measurements. Then, follow with 3P-3T measurements.

For 3P-1T (25°C):

1. Unreset the micro.
2. Place the sensor at its minimum pressure (22.5 mV in the present case).
3. Start OWI and reset the micro.
4. Go to the *ADC Conversion Result* tab in the right half of the GUI.
5. Click *PADC Continuous*.
6. In 1 to 2 minutes, it generates a .csv file in the folder where the GUI is located. Take the average of 500 generated values and enter the value in the PGA400-Q1 coefficient calculations spreadsheet under *PRESSURE ADC* → P_{MIN}.
7. Repeat the previous steps for sensor maximum and mid voltages (213.5 mV and 118.2 mV in the present case) and enter the *PADC Continuous* averaged value under P_{MAX} and P_{MID} (PGA400-Q1 coefficient calculations spreadsheet under *PRESSURE ADC*), respectively.

	User Input Data			Values in Decimal			Values in Hex		
ADC DATA	PRESSURE ADC			PRESSURE ADC			PRESSURE ADC		
	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax
	-13862	637	15147	-13862	637	15147	FFFFFFC9DA	027D	3B2B
DAC DATA	DAC CODE			DAC CODE			DAC CODE		
	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax
	403	2000	3597	403	2000	3597	0193	07D0	0E0D

Figure 35. Representation of ADC and DAC Data in 3P-1T Measurements Spreadsheet

3P-3T (–30°C, 45°C, 120°C):

1. Place the TIDA-00793 in the temperature chamber and set the temperature to –30°C.
2. Unreset the micro.
3. Place the sensor at its minimum pressure (22.5 mV in the present case).
4. Start OWI and reset the micro.
5. Go to the *ADC Conversion Result* tab in the right half of the GUI.
6. Click *PADC Continuous.*
7. In 1 to 2 minutes, it generates a PADC.csv file in the folder where the GUI is located. Take the average of 500 generated values and enter the value in the PGA400-Q1 coefficient calculations spreadsheet under PRESSURE ADC → Pmin → Tmin.
8. Repeat Steps 2 through 6 for sensor maximum and mid voltages (213.5 mV and 118.2 mV in the present case) and enter the *PADC Continuous* averaged value under Pmax and Pmid (PGA400-Q1 coefficient calculations spreadsheet under *PRESSURE ADC* → Pmin → Tmin and → Pmid → Tmin), respectively.
9. Click *TADC Continuous.*
10. In 1 to 2 minutes, it generates a TADC.csv file in the folder where the GUI is located. Take the average of 500 generated values and enter the value in the PGA400-Q1 coefficient calculations spreadsheet under the following locations:
    - TEMPERATURE ADC → Pmin → Tmin
    - TEMPERATURE ADC → Pmid → Tmin
    - TEMPERATURE ADC → Pmax → Tmin
11. Set the chamber temperature to 45°C.
12. Repeat Steps 2 through 6.
13. In 1 to 2 minutes, it generates a PADC.csv file in the folder where the GUI is located. Take the average of 500 generated values and enter the value in the PGA400-Q1 coefficient calculations spreadsheet under PRESSURE ADC → Pmin → Tmid.

14. Repeat Steps 2 through 6 for the sensor maximum and mid voltages (213.5 mV and 118.2 mV in the present case) and enter the *PADC Continuous* averaged value under Pmax and Pmid (PGA400-Q1 coefficient calculations spreadsheet under PRESSURE ADC → Pmin → Tmid and → Pmid → Tmid), respectively.
15. Click *TADC Continuous.*
16. In 1 to 2 minutes, it generates a TADC.csv file in the folder where the GUI is located. Take the average of 500 generated values and enter the value in the PGA400-Q1 coefficient calculations spreadsheet under the following locations:
    - TEMPERATURE ADC → Pmin → Tmid
    - TEMPERATURE ADC → Pmid → Tmid
    - TEMPERATURE ADC → Pmax → Tmid
17. Set the temperature to 120°C.
18. Repeat Steps 2 through 6.
19. In 1 to 2 minutes, it generates a PADC.csv file in the folder where the GUI is located. Take the average of 500 generated values and enter the value in the PGA400-Q1 coefficient calculations spreadsheet under PRESSURE ADC → Pmin → Tmax.
20. Repeat Steps 2 through 6 for sensor maximum and mid voltages (213.5 mV and 118.2 mV in the present case) and enter *PADC Continuous* averaged value under Pmax and Pmid (PGA400-Q1 coefficient calculations spreadsheet under PRESSURE ADC → Pmin → Tmax and → Pmid → Tmax), respectively.
21. Click *TADC Continuous*.
22. In 1 to 2 minutes, it generates a TADC.csv file in the folder where the GUI is located. Take the average of 500 generated values and enter the value in the PGA400-Q1 coefficient calculations spreadsheet under the following locations:
    - TEMPERATURE ADC → Pmin → Tmax
    - TEMPERATURE ADC → Pmid → Tmax
    - TEMPERATURE ADC → Pmax → Tmax

	User Input Data			Values in Decimal			Values in Hex		
ADC DATA	PRESSURE ADC			PRESSURE ADC			PRESSURE ADC		
TEMPERATURE	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax
Tmin	-13920	610	15160	-13920	610	15160	FFFFFFC9A0	0262	3B38
Tmid	-13821	644	15108	-13821	644	15108	FFFFFFCA03	0284	3B04
Tmax	-13739	661	15038	-13739	661	15038	FFFFFFCA55	0295	3ABE
ADC DATA	TEMPERATURE ADC			TEMPERATURE ADC			TEMPERATURE ADC		
TEMPERATURE	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax
Tmin	-73	-73	-73	-73	-73	-73	FFFFFFFFB7	FFFFFFFFB7	FFFFFFFFB7
Tmid	72	72	72	72	72	72	0048	0048	0048
Tmax	210	210	210	210	210	210	00D2	00D2	00D2
DAC DATA	DAC CODE			DAC CODE			DAC CODE		
TEMPERATURE	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax
Tmin	410	2034	3659	410	2034	3659	019A	07F2	0E4B
Tmid	411	2039	3668	411	2039	3668	019B	07F7	0E54
Tmax	409	2034	3659	409	2034	3659	0199	07F2	0E4B

Figure 36. Representation of ADC and DAC Data in 3P-3T Measurement Spreadsheet

10.6 Step 6: DAC Calibration

NOTE: First complete the 3P-1T measurements. Then, follow with 3P-3T measurements.

For 3P-1T (25°C):

1. Go to *EEPROM BANK4* → *DAC CAL ENABLE* = 01.
2. Go to *EEPROM BANK4* → *DACCALMSB* = 01, *DACCALLSB* = 9C.
3. Unreset the micro by placing "00" in *0E MICRO CTL* (under the *TEST* tab).
4. Measure the output voltage of DAC using the multimeter (HP 3458 8 ½ digit multimeter) and enter the measured value in the PGA400-Q1 coefficient calculations spread sheet under Pmin Measured VOUT.
5. Start OWI and reset the micro.
6. Go to *EEPROM BANK4* → *DACCALMSB* = 07, *DACCALLSB* = FD.
7. Unreset the micro by placing "00" in *0E MICRO CTL* (under the *TEST* tab).
8. Measure the output voltage of DAC using the multimeter (HP 3458 8 ½ digit multimeter) and enter the measured value in the PGA400-Q1 coefficient calculations spreadsheet under Pmid Measured VOUT.
9. Start OWI and reset MICRO.
10. Go to *EEPROM BANK4* → *DACCALMSB* = 0E, *DACCALLSB* = 60.
11. Unreset the micro by placing "00" in *0E MICRO CTL* (under the *TEST* tab).
12. Measure the output voltage of DAC using the multimeter (HP 3458 8 ½ digit multimeter) and enter the measured value in the PGA400-Q1 coefficient calculations spreadsheet under Pmax Measured VOUT. The spreadsheet should be visible as shown in Figure 38.
13. Measure the exact supply value as shown in Figure 37 and enter in the coefficients spreadsheet under VDD.

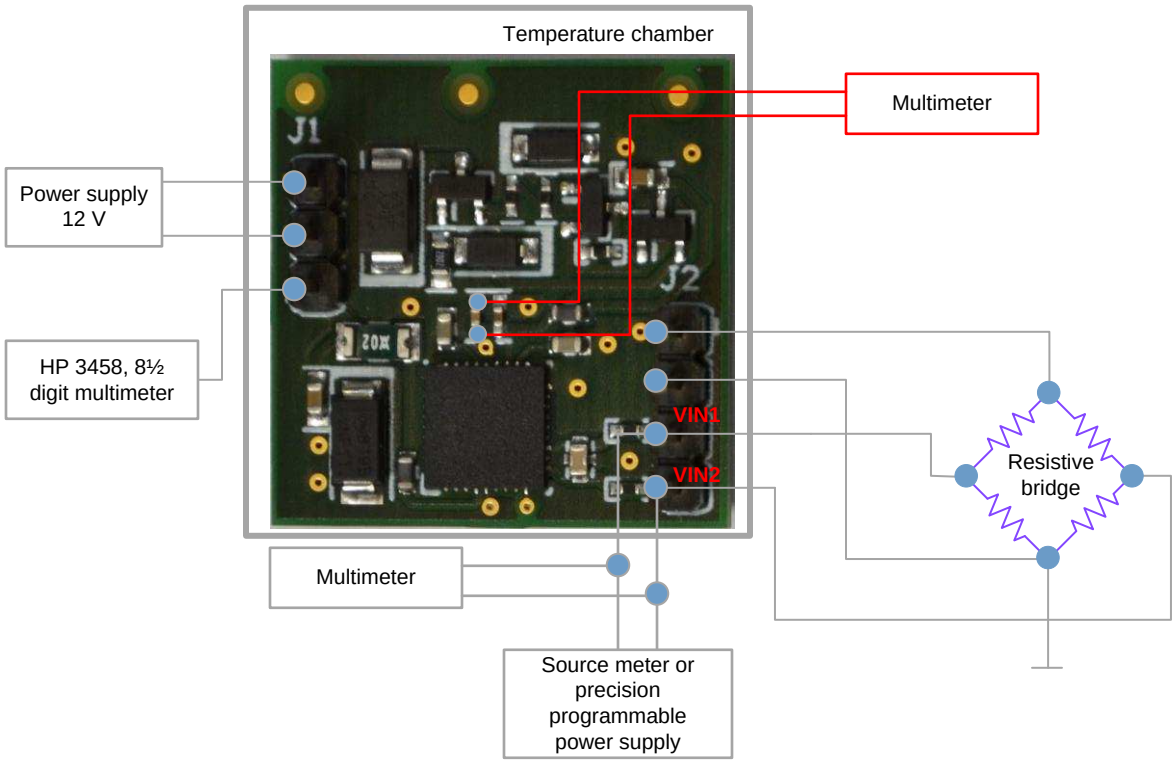

Figure 37. VDD Measurement Across PGA400-Q1

14. Enter the given DAC codes in spreadsheet. Finally, the spreadsheet should look like Figure 38.

User Input Data				Values in Decimal			Values in Hex		
VDD VOLTAGE									
VDD (V)	4.89	V							
DAC DATA	DAC CODE			DAC CODE			DAC CODE		
	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax
DAC CODE	19C	7FD	E60	412	2045	3680	019C	07FD	0E60
Measured VOUT (V)	0.49649	2.4827	4.4707	0.49649	2.4827	4.4707			
Desired VOUT (V)	0.49692	2.482425	4.468365						
DESIRED DAC				403	2000	3597	193	7D0	E0D

Figure 38. DAC Codes for 3P-1T Measurements

For 3P-3T (–30°C, 45°C, 120°C):

1. Place the TIDA-00793 in the temperature chamber and set the temperature to –30°C.
2. Start OWI and reset MICRO.
3. Go to *EEPROM BANK4* → *DAC CAL ENABLE* = 01.
4. Go to *EEPROM BANK4* → *DACCALMSB* = 01, *DACCALLSB* = 9C.
5. Unreset the micro by placing "00" in *0E MICRO CTL* (under the *TEST* tab).
6. Measure the output voltage of DAC using the multimeter (HP 3458 8 ½ digit multimeter) and enter the measured value in the PGA400-Q1 coefficient calculations spreadsheet (3P-3T DAC) under Pmin → Tmin Measured VOUT.
7. Start OWI and reset MICRO.
8. Go to *EEPROM BANK4* → *DACCALMSB* = 07, *DACCALLSB* = FD
9. Unreset the micro by placing "00" in *0E MICRO CTL* (under the *TEST* tab).
10. Measure the output voltage of DAC using the multimeter (HP 3458 8 ½ digit multimeter) and enter the measured value in the PGA400-Q1 coefficient calculations spreadsheet (3P-3T DAC) under Pmid → Tmin Measured VOUT.
11. Start OWI and reset MICRO.
12. Go to *EEPROM BANK4* → *DACCALMSB* = 0E, *DACCALLSB* = 60.
13. Unreset the micro by placing "00" in *0E MICRO CTL* (under the *TEST* tab).
14. Measure the output voltage of DAC using the multimeter (HP 3458 8 ½ digit multimeter) and enter the measured value in the PGA400-Q1 coefficient calculations spreadsheet (3P-3T DAC) under Pmax → Tmin Measured VOUT.
15. Measure the VDD voltage as shown in Figure 37 and enter in the spreadsheet under Tmin VDD.
16. Place the TIDA-00793 in the temperature chamber and set the temperature to 45°C.
17. Repeat Steps 2 through 14 but enter the respective values in
    - Pmin → Tmid Measured VOUT
    - Pmid → Tmid Measured VOUT
    - Pmax → Tmid Measured VOUT
18. Measure the VDD voltage as shown in Figure 37 and enter in the spreadsheet under Tmid VDD
19. Place TIDA-00793 in the temperature chamber and set the temperature to 125°C
20. Repeat Steps 2 through 14 but enter the respective values in
    - Pmin → Tmax Measured VOUT
    - Pmid → Tmax Measured VOUT
    - Pmax → Tmax Measured VOUT

21. Measure the VDD voltage as shown in Figure 37 and enter in the spreadsheet under Tmax VDD. Finally, the spreadsheet should look like Figure 39:

	User Input Data			Values in Decimal			Values in Hex		
VDD VOLTAGE									
Tmin VDD (V)	4.971	V		4.971					
Tmid VDD (V)	4.9699	V		4.9699					
Tmax VDD (V)	4.9638	V		4.9638					
DAC DATA	DAC CODE			DAC CODE			DAC CODE		
	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax	Pmin	Pmid	Pmax
DAC CODE	019C	07FD	E60	412	2045	3680	019C	07FD	0E60
Tmin MEASURED V	0.49769	2.4871	4.4787	0.49769	2.4871	4.4787			
Tmid MEASURED V	0.49595	2.480635	4.467	0.49595	2.480635	4.467			
Tmax MEASURED V	0.49697	2.47767	4.4595	0.49697	2.47767	4.4595			
Desired V	0.5	2.5	4.5						
Tmin DESIRED DAC				412	2044	3676	19C	7FC	E5C
Tmid DESIRED DAC				413	2049	3685	19D	801	E65
Tmax DESIRED DAC				412	2044	3676	19C	7FC	E5C

Figure 39. DAC Codes for 3P-3T Measurements

10.7 Step 7: Coefficients Calculation

For 3P-1T (25°C):

1. In the coefficient calculations spreadsheet under 3P-1T ADC, note the N0, G0, H0 values that are generated based on ADC and DAC measurements as described in Steps 4 and 5.
2. Go to the PGA400-Q1 GUI.
3. Start OWI and reset MICRO.
4. Click *EEPROM* → *BANK_1* and enter N0, G0, H0 values as per the EEPROM memory MAP spreadsheet.
5. Click *WRITE ALL.*
6. Click *Program EEPROM.*
7. Click *Reload Cache* to verify whether it is written in EEPROM registers or not.

Coefficients				
	PADC			
Software Offset	0			
Software Gain	1			
RESULT	**n0**	**g0**	**h0**	
COEFFS (DEC)	-3	7379	7893	
COEFFS (HEX)	FFFFFFFFFD	1CD3	1ED5	

Figure 40. 3P-1T Measurement Coefficients

The GUI should look like Figure 41:

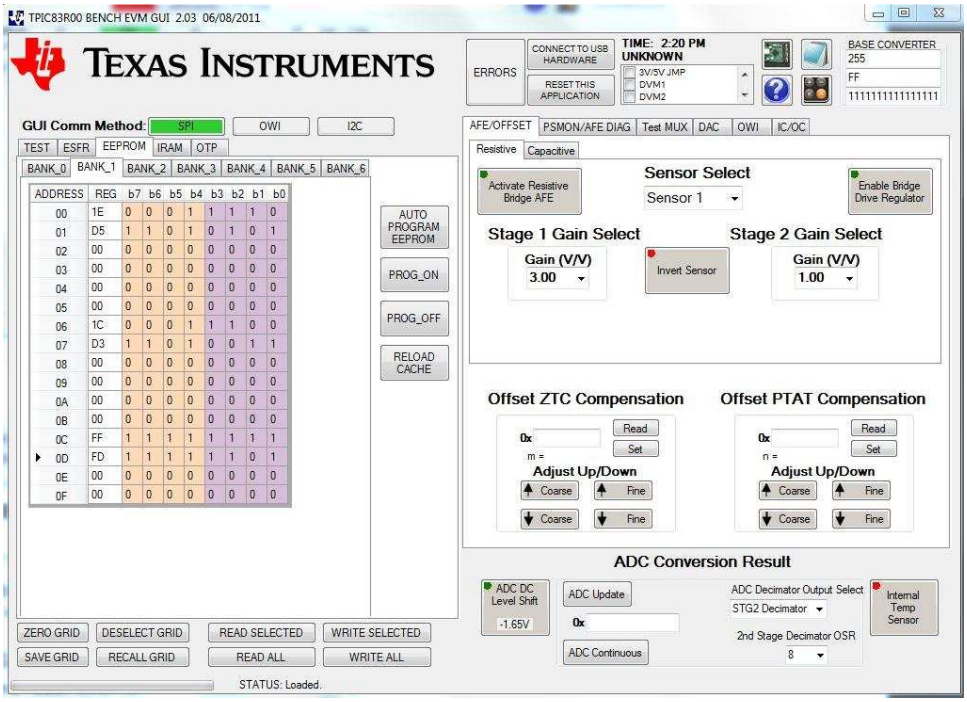

Figure 41. EEPROM BANK_1 Registers When 3P-1T Coefficients Entered in PGA400-Q1 GUI

For 3P-3T (–30°C, 45°C, 120°C):

1. In the coefficient calculations spread sheet under 3P-3T ADC, note the N0, G0, H0, N1, G1, H1, N2, G2, and H2 values that are generated based on ADC and DAC measurements as described in Steps 4 and 5.
2. Go to the PGA400-Q1 GUI.
3. Start OWI and reset MICRO.
4. Click *EEPROM → BANK_1* and enter the N0, G0, H0, N1, G1, H1, G2, and H2 values as per the EEPROM memory MAP spreadsheet.
5. Click *WRITE ALL.*
6. Click *Program EEPROM.*
7. Click *Reload Cache* to verify whether it is written in EEPROM registers or not.
8. Click *EEPROM → BANK_2* and enter the N2 value as per the EEPROM memory MAP spreadsheet.
9. Click *WRITE ALL.*
10. Click *Program EEPROM.*
11. Click *Reload Cache* to verify if it is written in EEPROM registers or not. The coefficients in the spreadsheet should look like Figure 42:

	Coefficients									
	PADC	TADC								
Software Offset	0	0								
Software Gain	1	1								
RESULT	n2	n1	n0	g2	g1	g0	h2	h1	h0	
COEFFS (DEC)	5	21	-3	-221	198	7389	-208	9	7908	
COEFFS (HEX)	0005	0015	FFFFFFFFD	FFFFFFF23	00C6	1CDD	FFFFFFF30	0009	1EE4	

Figure 42. 3P-3T Measurement Coefficients

The GUI should look like Figure 43:

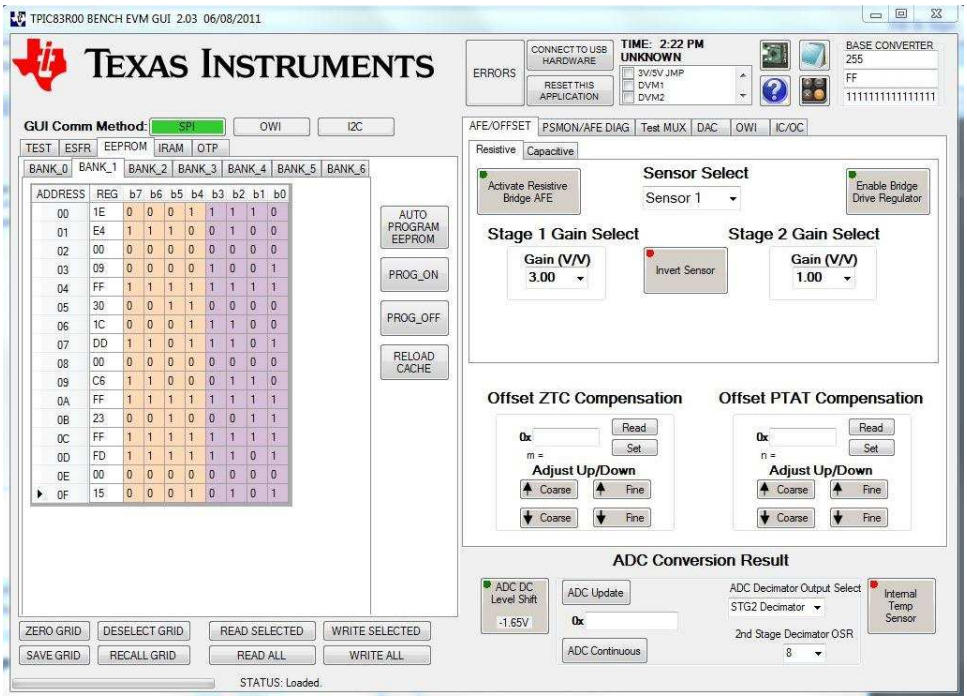

Figure 43. EEPROM BANK_1 Registers When 3P-3T Coefficients Entered in PGA400-Q1 GUI

10.8 Step 8: PGA400-EEPROM Bank 2 Registers

1. Click *EEPROM → BANK_2.*
2. Enter the values as shown in Figure 44:

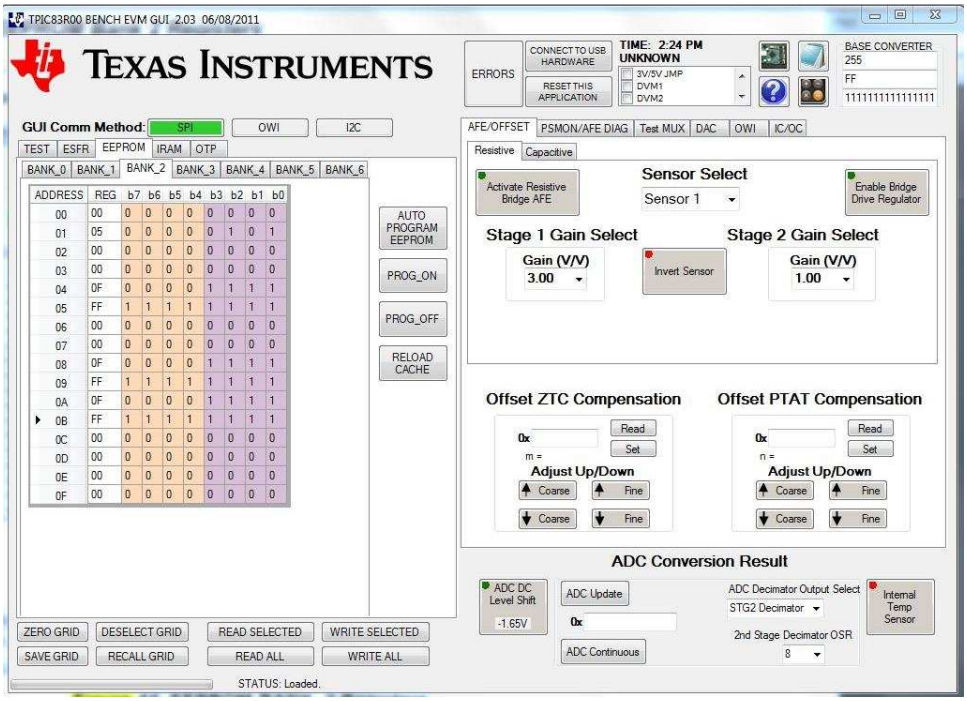

Figure 44. EEPROM BANK_2 Registers

3. Click *WRITE ALL.*
4. Click *Program EEPROM.*
5. Click *Reload Cache* to verify whether it is written in EEPROM registers or not.

10.9 Step 9: PGA400-EEPROM Bank 3 Registers

1. Click *EEPROM → BANK_3.*
2. Enter the values as shown in Figure 45:

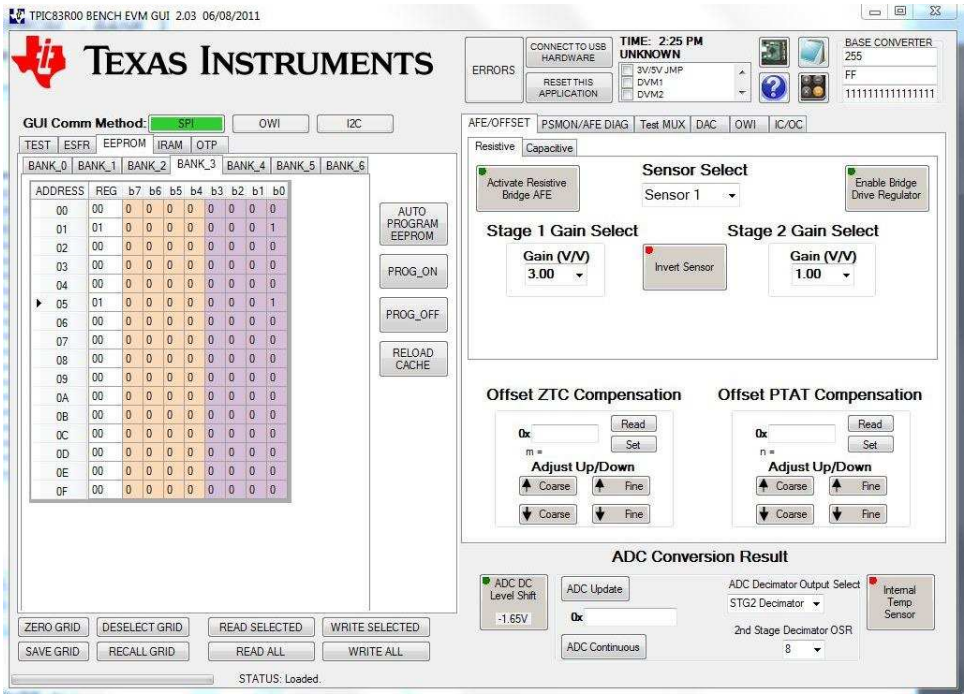

Figure 45. EEPROM BANK_3 Registers in PGA400-Q1 GUI

3. Click *WRITE ALL.*
4. Click *Program EEPROM.*
5. Click *Reload Cache* to verify whether it is written in EEPROM registers or not.

10.10 Step 10: PGA400-EEPROM Bank 4 Registers

1. Click *EEPROM → BANK_4.*
2. Enter the values as shown in Figure 46:

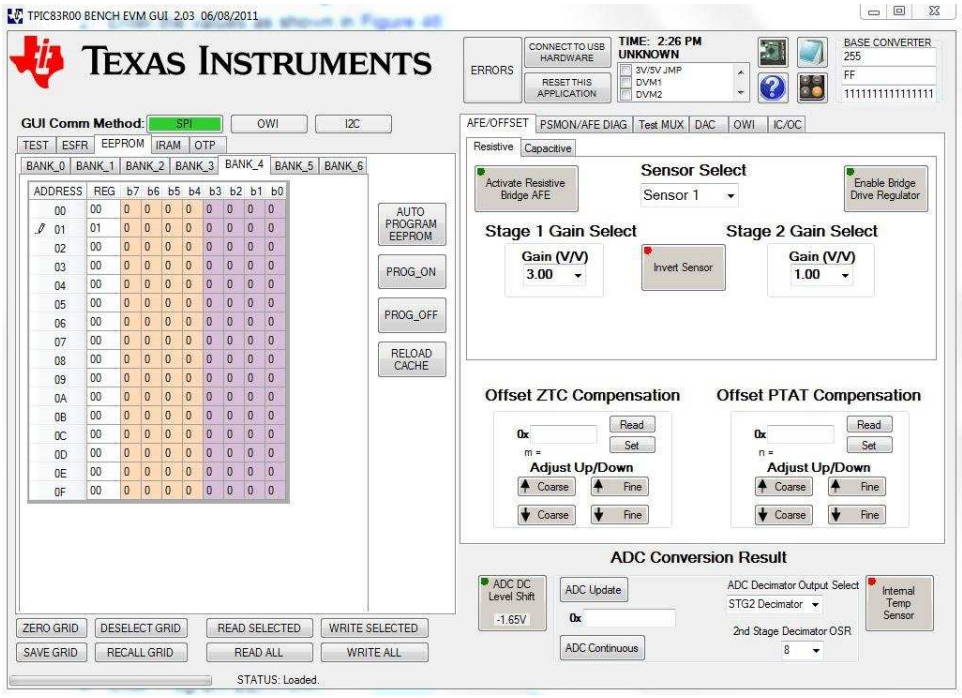

Figure 46. EEPROM BANK_4 Registers in PGA400-Q1 GUI

3. Click *WRITE ALL.*
4. Click *Program EEPROM.*
5. Click *Reload Cache* to verify whether it is written in EEPROM registers or not.

10.11 Step 11: Microcontroller Unreset

Unreset the microcontroller by placing "00" in *0E MICRO CTL* (under the *TEST* tab).

11 Test Setup

The testing procedures outlined in this document are designed to ensure proper functionality and to analyze the effects of harness faults, EMI, and ISO 7637-3 pulses on the pressure sensor system.

11.1 Basic Functionality

Using the real sense element in bridge configuration, apply voltages across VIN1 and VIN2 to generate differential voltage across the VIN1N and VIN1P terminals of the PGA400-Q1, as shown in Figure 47. In the present case, voltages are applied using the SMD resistors in bridge configuration.

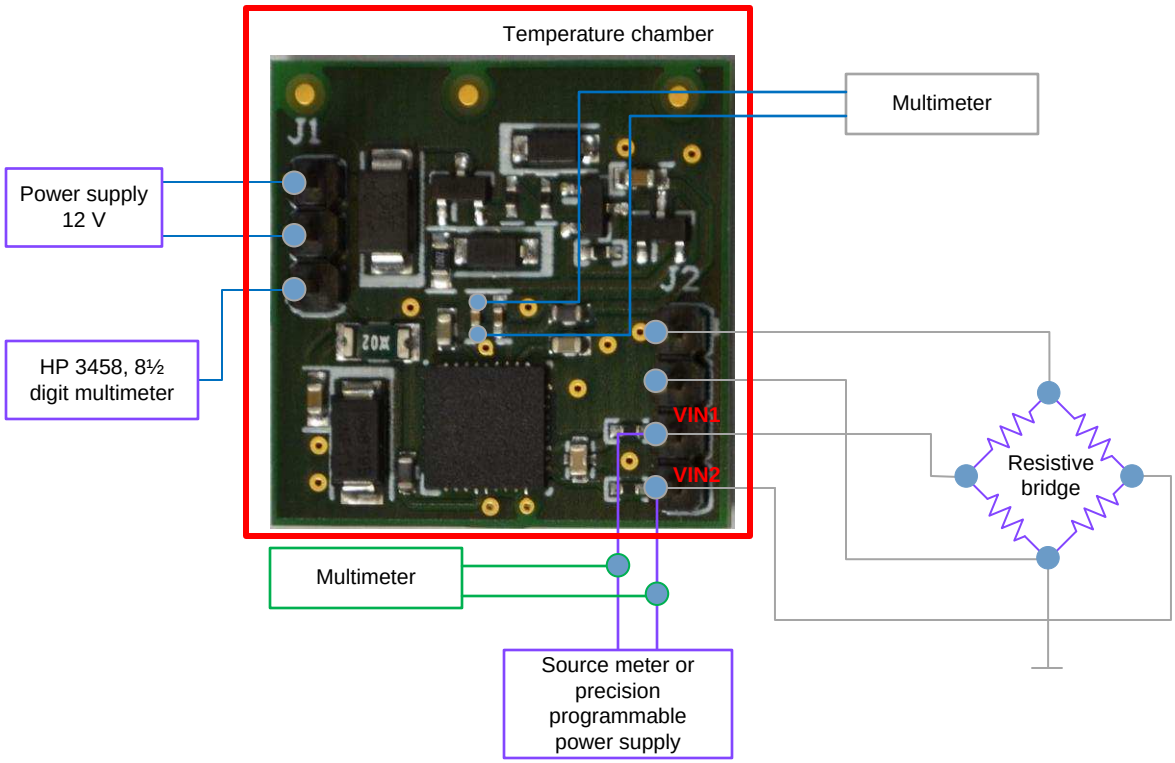

Figure 47. Test Setup to Measure Basic Functionality

Set the chamber temperature to 25°C and apply voltages in even steps from 22.5 to 213.5 mV (exact applied voltage can be seen in the multimeter). Note the output voltage corresponding to the particular input. Table 4 and Figure 48 show the applied input voltages and corresponding output voltages.

The expected voltage can be calculated using Equation 3. Assume sensor output voltage range is 22.53 to 213.5 mV and output span is 0.5 to 4.5 V.

The expected voltage for minimum sensor voltage should be 0.5 but the output of the PGA400-Q1 is ratiometric, so the output depends on the supply voltage variations.

$$\text{Output expected}(\text{V}) = \frac{\text{Supply voltage}(\text{V}) \times 0.5}{5} = \frac{4.9722 \times 0.5}{5} = 0.49722\ \text{V} \quad (3)$$

Full-scale accuracy can be calculated using Equation 4.

$$\%\text{FS accuracy} = \text{Output expected}(\text{V}) - \text{Output measured}(\text{V}) \times \frac{100}{\text{Output span}(4)}$$

$$= 0.49722\ \text{V} - 0.492\ \text{V} \times \frac{100}{4} = 0.1305\% \quad (4)$$

Table 4. Pressure Sensor Output Voltage, %FS Accuracy versus Input Voltage

S/N	V_{DIFF} (VINP – VINN) (mV)	SUPPLY (V)	OUTPUT EXPECTED (V)	OUTPUT MEASURED (V)	FS ACCURACY (%)
1	22.530	4.9722	0.497220	0.4920	0.1305
2	41.610	4.9722	0.894996	0.8894	0.1399
3	60.710	4.9722	1.292772	1.2874	0.1343
4	79.800	4.9722	1.690548	1.6846	0.1487
5	98.902	4.9722	2.088324	2.0831	0.1306
6	118.000	4.9722	2.486100	2.4810	0.1275
7	137.102	4.9722	2.883876	2.8802	0.0919
8	156.202	4.9722	3.281652	3.2788	0.0713
9	175.290	4.9722	3.679428	3.6747	0.1182
10	194.420	4.9722	4.077204	4.0733	0.0976
11	213.500	4.9722	4.474980	4.4706	0.1095

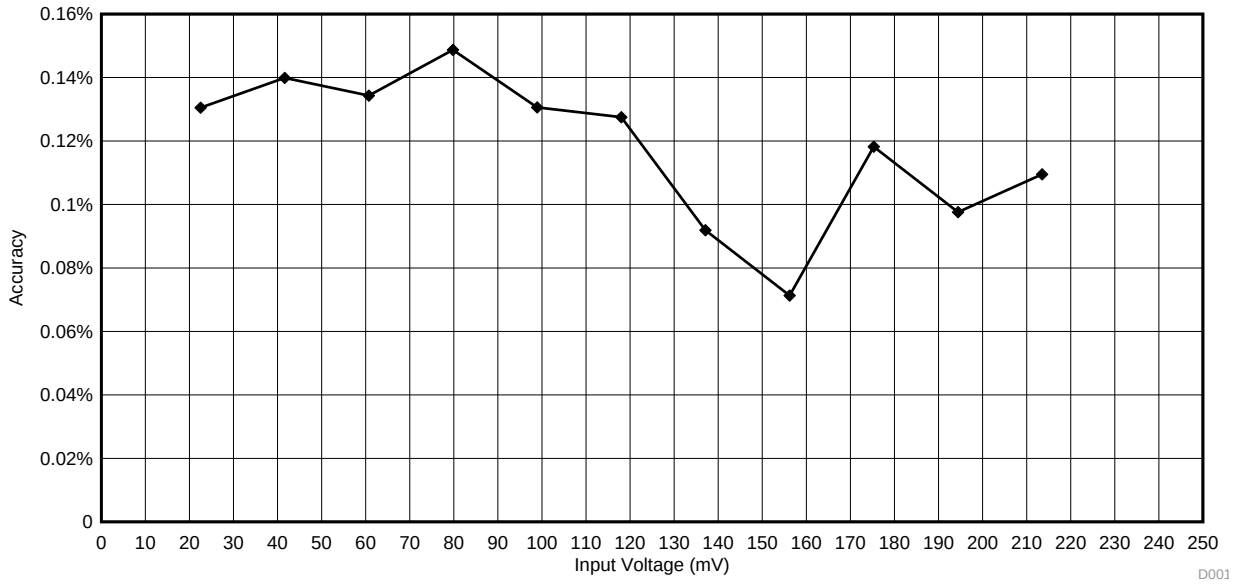

Figure 48. %FS Accuracy versus Input Voltage

From Table 4 and Figure 48, the accuracy of the system at 25°C is less than 0.1487%.

11.1.1 Response Time

Response time is the time from power up to a valid output.

To measure response time, set the input to P_{MID}, power up the device, and measure the time from power up to when V_{OUT} settles to an expected output value. This value can be measured using an oscilloscope. From Figure 49, the response time measured is 23.67 ms.

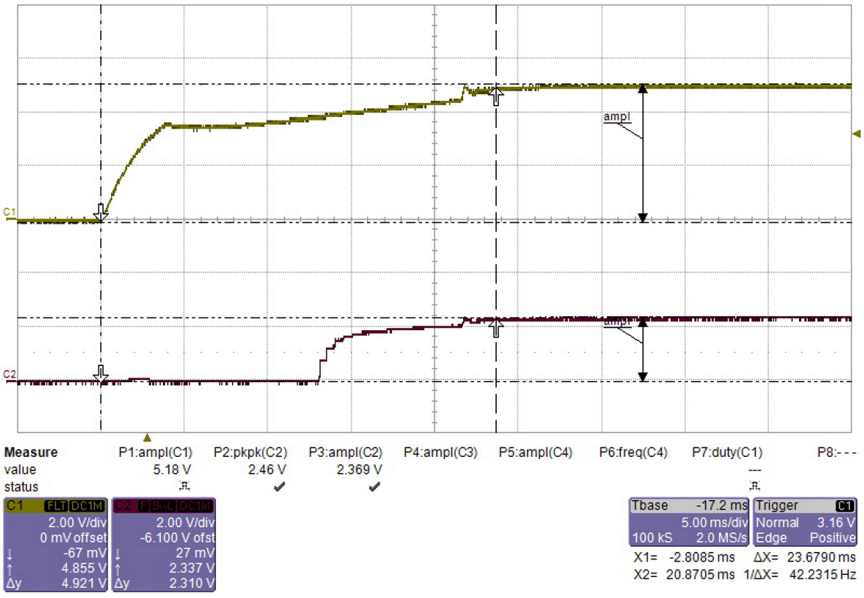

Figure 49. Response Time

11.2 Temperature Dependence

Normally, pressure-based measurements vary with respect to temperature. But in the present case, using PGA400-Q1 the accuracy of the device can be improved over the grade 1 temperature range. Second order linearity compensation algorithms have imported inside the chip to compensate the temperature changes and to give more accurate result. Section 11.2.1 describes %FS accuracy calculations over the grade 1 temperature range.

11.2.1 Temperature versus Output Pressure Variations

The following tables show the variation of output voltage with respect to temperature variations. As shown in Figure 47, set up the experiment and change the temperatures in steps of 20°C.

The PGA400-Q1 has a built-in temperature compensation algorithm. Using the internal temperature sensor and compensation algorithm, the output voltage changes are minimized with respect to temperature changes. Table 5 shows the effect on output voltage accuracy over the grade 1 temperature range (–40°C to 125°C). For calculations of expected output and accuracy, see Equation 3 and Equation 4.

Table 5. Output Voltage Change With Respect to Temperature (at P_{MIN} Input)

TEMPERATURE (°C)	INPUT (P_{MID}) (mV)	SUPPLY (V)	EXPECTED OUTPUT (V)	MEASURED OUTPUT (V)	ACCURACY (%)
–40	22.52	4.9960	0.49960	0.5007	–0.02750
–20	22.49	4.9940	0.49940	0.5001	–0.01750
0	22.49	4.9922	0.49922	0.4999	–0.01700
20	22.48	4.9896	0.49896	0.4987	0.00650
40	22.46	4.9897	0.49897	0.4980	0.02425
60	22.46	4.9868	0.49868	0.4972	0.03700
80	22.46	4.9857	0.49857	0.4967	0.04675
100	22.45	4.9844	0.49844	0.4963	0.05350(1)
120	22.45	4.9845	0.49845	0.4968	0.04125
125	22.40	4.9829	0.49829	0.4966	0.04225

(1) The maximum deviation of accuracy observed among all measurements.

From Table 5, the variation of output voltage over the defined temperature range is very low (accuracy of 0.0535%) when the input is at its minimum value.

Table 6 shows the effect on output voltage accuracy over the grade 1 temperature range (–40°C to 125°C). When the input is locked at a medium value and changes from –40°C to 125°C, the output voltage variation can be seen in Table 6.

Table 6. Output Voltage Change With Respect to Temperature (at Pmid Input)

TEMPERATURE (°C)	INPUT (P_{MID}) (mV)	SUPPLY (V)	EXPECTED OUTPUT (V)	MEASURED OUTPUT (V)	ACCURACY (%)
–40	118.460	4.9925	2.4960	2.4923	0.09875
–20	118.230	4.9920	2.4960	2.4949	0.02750
0	118.200	4.9905	2.4950	2.4958	–0.01375
20	118.020	4.9900	2.4950	2.4953	–0.00750
40	118.023	4.9894	2.4947	2.4961	–0.03500
60	118.000	4.9872	2.4936	2.4939	–0.00750
80	117.960	4.9858	2.4929	2.4924	0.01250
100	117.950	4.9850	2.4925	2.4934	–0.02250
120	117.890	4.9833	2.4916	2.4913	0.00875
125	117.819	4.9835	2.4917	2.4916	0.00375

From Table 6, the variation of output voltage over the defined temperature range is very low when the input is at its medium value.

Table 7 shows the effect on output voltage accuracy over the grade 1 temperature range (–40°C to 125°C). When the input is locked at the maximum value and changes the temperatures from –40°C to 125°C, the output voltage variation can be seen in Table 7.

Table 7. Output Voltage Change With Respect to Temperature (at P_{MAX} Input)

TEMPERATURE (°C)	INPUT (P_{MID}) (mV)	SUPPLY (V)	EXPECTED OUTPUT (V)	MEASURED OUTPUT (V)	ACCURACY (%)
–40	214.44	4.9932	4.49388	4.5006	–0.16800[(1)]
–20	214.12	4.9921	4.49289	4.4989	–0.15025
0	214.02	4.9906	4.49154	4.4971	–0.13900
20	213.96	4.9906	4.49154	4.4968	–0.13150
40	213.85	4.9891	4.49019	4.4935	–0.08275
60	213.59	4.9872	4.48848	4.4912	–0.06800
80	213.66	4.9859	4.48731	4.4884	–0.02725
100	213.26	4.9850	4.48650	4.4886	–0.05250
120	213.25	4.9836	4.48524	4.4867	–0.03650
125	213.27	4.9832	4.48488	4.4865	–0.04050

(1) The maximum deviation of accuracy observed among all measurements.

From Table 7, the variation of output voltage over the defined temperature range is low (accuracy of –0.168%) when the input is at its maximum value.

12 EMC Tests

One of the goals of this design is to qualify the design according to automotive EMC standards. In order to prove that the TIDA-00793 is immune to conductive and radiative disturbances, the current design mainly focuses on immunity standards in automotive. In general, sensors in the vehicle are connected to the ECU through a wiring harness, and the wiring harness may introduce many coupling effects. The current design tested for these types of coupling effects using ISO 7637-3 simulated pulses. Also one of the toughest tests for common automotive systems regarding immunity against continuously applied RF energy is the BCI test. Radiative frequencies disturb the sensor signals and the output signal varies. To qualify that the sensor is prone to radiative disturbances, the ISO 11452-4 BCI test is performed.

12.1 ISO 7637-3

ISO 7637 is titled *Road vehicles – Electrical disturbances from conduction and coupling*, and part 3 is specifically for "Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines". The current design relates to sensors and sensor to ECU lines are a part of wiring harness. According to the standard, the coupling effects might occur on all input and output lines and also on the supply line. So the sensor three wires (supply, GND, and output) are needed to be tested for coupling effects.

The standard defines a test procedure, including the description of test pulses, to test the susceptibility of an electrical subsystem to transients, which could potentially be harmful to its operation. Each pulse is modeled to simulate a transient that could be created by a real event in the car. The following subsections go into the pulses tested for in this design.

The standard specifies two types of transients: Fast transient pulses and slow transient pulses. The fast transient test uses bursts composed of a number of fast transients, which are coupled into lines of electronic equipment, in particular input/output (I/O) lines. The fast rise time, the repetition rate, and the low energy of the fast transient bursts are significant to the test. The slow transient test uses a single pulse similar to that used for conducted transient, and is applied a number of times to the device under test (DUT).

During the design phase, the production wiring harness is not available and the vehicle's electrical noises are not known. The test must therefore be performed with the worst case situation, which is represented by the capacitive and inductive coupling described in this part of ISO 7637. The current design is tested for fast transients according to capacitive coupling clamp method.

12.1.1 CCC Method

According to this method, sensor wiring harness should be placed in between two metal plates (forms capacitor), a capacitive clamp forms using these two plates setup. One end of the plates is connected to the pulse generator (pulse description is given in Section 12.1.1.1) and other end is connected to oscilloscope. Pulses travel from one end to other end via the capacitive clamp. It implies the pulse is coupled to the sensor lines which are in between the capacitive clamp (in between two metal plates). The result of the test and the pass fail criteria depends on the design requirement specifications.

This method is applicable for fast transient pulses and pulse description is given in Section 12.1.1.1.

12.1.1.1 EFT Pulses a and b

The fast transient test pulses are a simulation of transients that occur as a result of the switching processes. The characteristics of these transients are influenced by distributed capacitance and inductance of the wiring harness. The pulse shapes and parameters are:

- t — time
- U — tension in volts

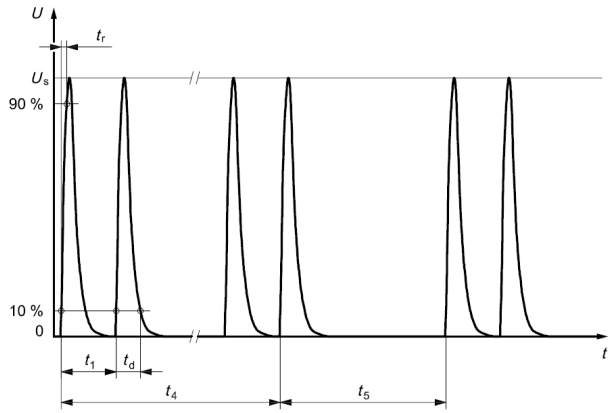

Figure 50. Pulse a

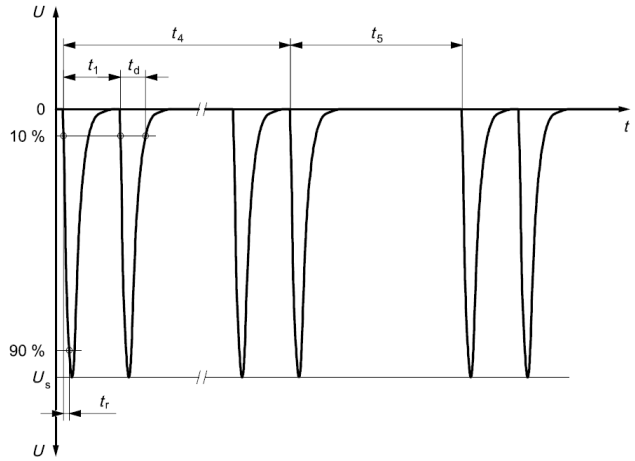

Figure 51. Pulse b

PARAMETERS	12-V SYSTEM
U_s in V	
t_r in ns	5
t_d in µs	0,1
t_1 in µs	100
t_4 in ms	10
t_5 in ms	90
R_i in Ω	50

TEST PULSE	SELECTED TEST LEVEL	TEST LEVELS U_s				TEST TIME (ms)
		I	II	III	IV (max)	
Fast a (DCC and CCC)		–10	–20	–40	–60	10
Fast b (DCC and CCC)		10	20	30	40	10

Figure 52. Pulse Specifications

12.2 BCI (ISO 11452-4)

BCI is a method of carrying out immunity tests by inducing disturbance signals directly into the wiring harness by means of a current injection probe. The injection probe is a current transformer through which the wiring harnesses of the DUT are passed. Immunity tests are carried out by varying the test severity level and frequency of the induced disturbance. Typically, the frequency range tested is 100 kHz to 400 MHz. The test simulates worst case conditions for RF cross-coupling in a harness for a different electric subsystem's wires assembled inside a car. Because of the small distance between the RF source (emitting harness or wire) and the RF sink (harness of the sensor module), the induced energy can be very high and is measured in "mA" or "dBµA" during the BCI test. To ensure the induced energy can influence only the sensor module during the test, the ECU is replaced by a standardized artificial network.

13 EMC Test Results

Table 8. General Summary

TEST	RESULT
Capacitive coupling clamp (ISO 7637-3)	Passed (meets requirement)
BCI (ISO 11452-4)	Passed (meets requirement)

The power line of PCB is connected to the 5-V supply. The device status is turned on.

NOTE: During both tests, the device status is always ON.

13.1 CCC Test Results

Table 9. Test Requirements

PARAMETER	DESCRIPTION
Test level	IV
Mode	Fast transient pulses
Device status	ON
Temperature	25°C
Test time	10 min

Table 10. Acceptance Criteria

OPERATION MODE	MONITORING PARAMETERS	ACCEPTANCE	TEST LEVEL
ON Status	Device survival	Class B (Device should survive for the pulses)	IV

As per the design acceptance level stated in Table 10, the device survives after the application of pulses and passes the test.

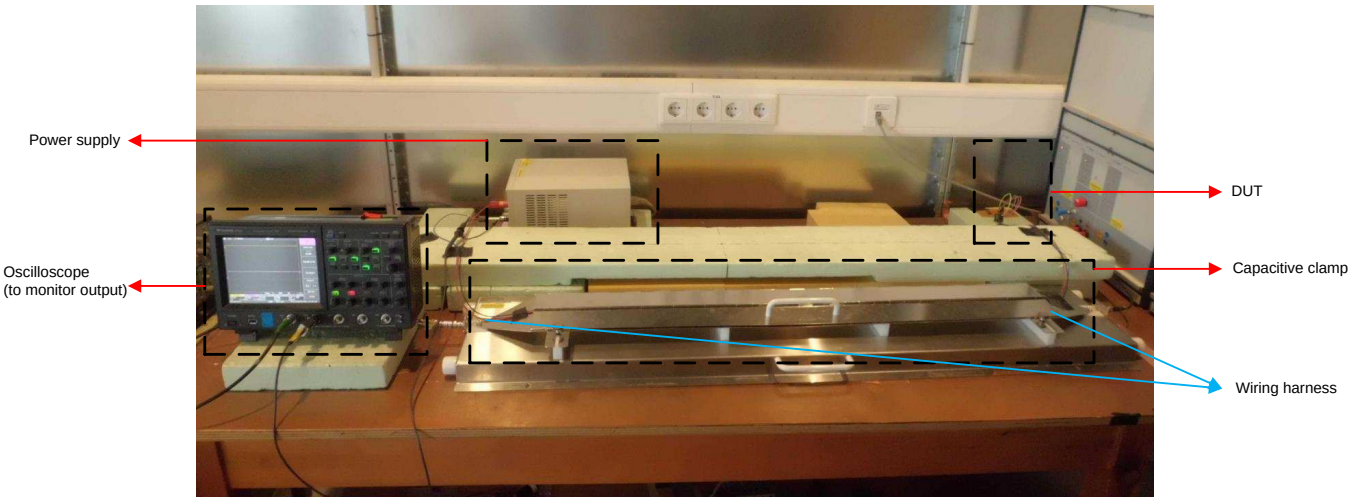

Figure 53. CCC Test Method Setup

13.2 BCI Method

Table 11. Test Requirements

PARAMETER	DESCRIPTION	
Test modulation	0.1 to 400 MHZ	CW, AM
Test method	Open loop method; CBCI	
Clamp position	150 cm to DUT	
Test level	IV	
Temperature	25°C	

Table 12. Monitoring Parameters and Acceptance Criteria

OPERATION MODE	MONITORING PARAMETERS	ACCEPTANCE	TEST LEVEL
Device status ON	Output voltage deviation	A deviation more that 10% considered as fault	IV

Table 13. Test Results

FREQUENCY (MHz)	INJECTION MODE	POSITION (mm)	MODULATION	DUT MODE	TEST LEVEL	TEST LEVEL DESCRIPTION
0.1 to 400	CBCI	150	CW	ON mode	IV	Meets Class A
0.1 to 400	CBCI	150	AM	ON mode	IV	Meets Class A

13.3 Results Graph

As shown in Figure 54, current is injected into the wiring harness at frequencies of 100 kHz to 400 MHz. During this, the output voltage deviation is monitored and the resulting graph is shown in Figure 55. From Figure 55, the deviation is very small and the maximum deviation is only around the frequencies from 24 to 32 MHz. This deviation is because the sensor element construction is not proper; with a real customer's perfect placement of sense element, the deviation could be minimized. To prove that the device is prone to BCI, instead of just ISO 11452-4, the device is also tested for OEM current profiles according to the following standards:

- MBN_10284-2_2011
- GS95002-2 - 2013-07
- TL 81000_2013

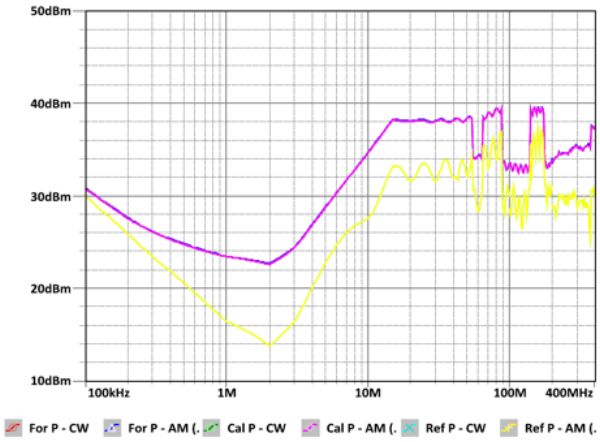

Figure 54. Input Current Profile Through Current Probe

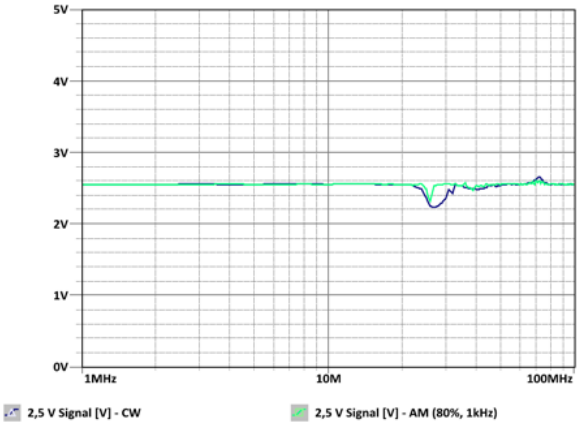

Figure 55. Output Voltage Deviation With Respect to Frequency

Figure 56 describes the test setup.

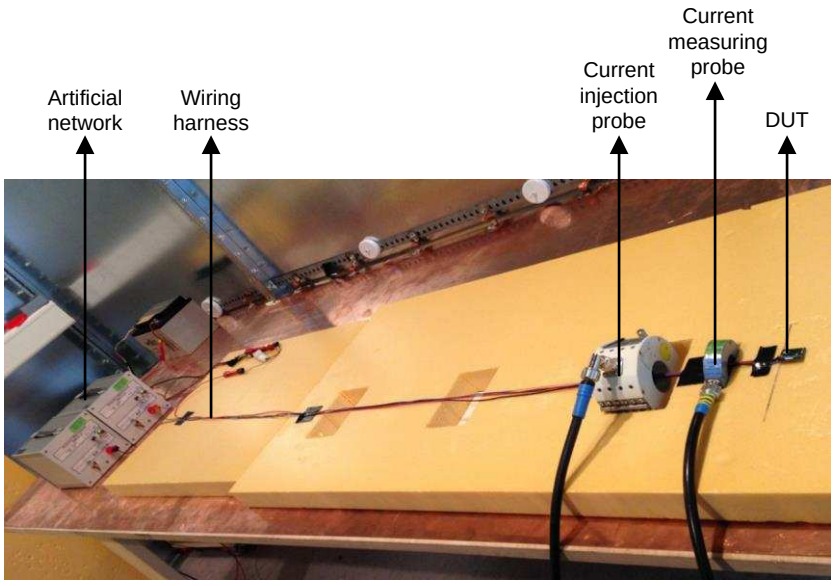

Figure 56. BCI Test Setup

Test results meet the requirement and the test is passed.

14 Design Files

14.1 Schematics

To download the schematics, see the design files at TIDA-00793.

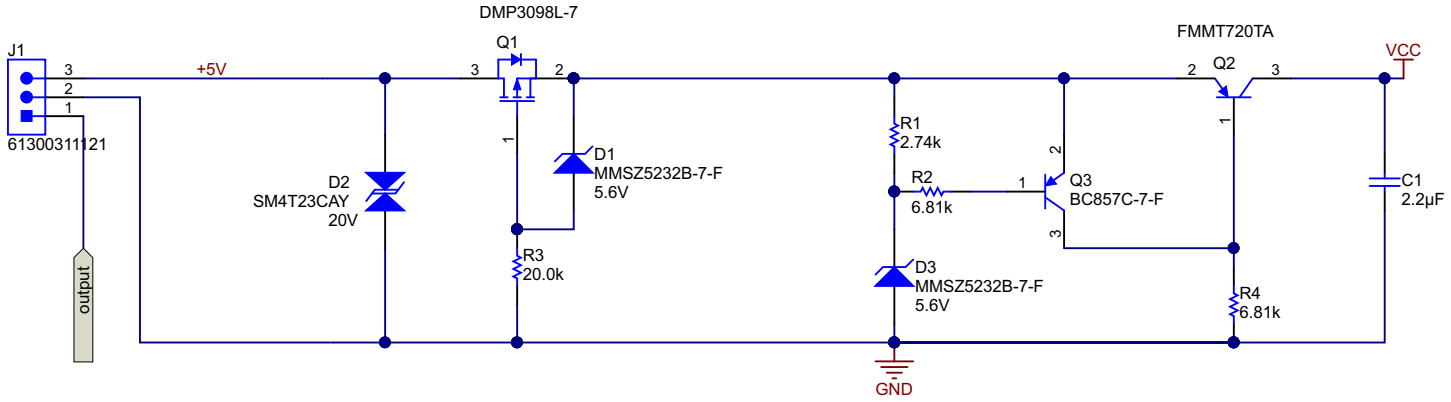

Figure 57. Power Supply Schematic

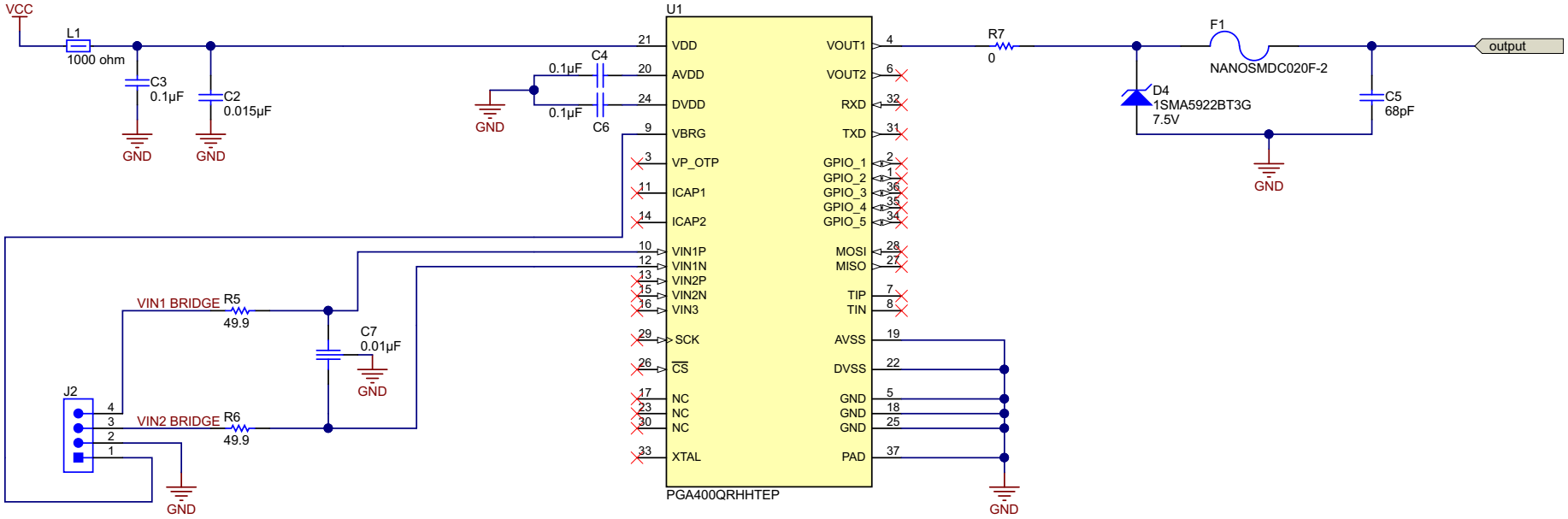

Figure 58. Signal Conditioning Circuit Schematic

14.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00793.

Table 14. BOM

DESIGNATOR	DESCRIPTION	PARTNUMBER	FOOTPRINT	QTY
C1	CAP, CERM, 2.2 µF, 50 V, +/- 10%, X7R, 0603	06035C104KAT2A	603	1
C2	CAP, CERM,15nF, 16 V, +/- 10%, X7R, 0402	C0402C392K4RACTU	402	1
C3	CAP, CERM, 100nF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B1X7R1E333K050BC	402	1
C4	CAP, CERM, 0.1 µF, 16 V, +/- 5%, X7R, 0603	0603YC104JAT2A	603	1
C5	CAP, CERM, 68 pF, 50 V, +/- 5%, C0G/NP0, 0603	C0603C680J5GACTU	603	1
C6	CAP, CERM, 0.1 µF, 16 V, +/- 5%, X7R, 0603	0603YC104JAT2A	603	1
C7	CAP, CERM, 0.01 µF, 50 V, +/- 20%, X7R, 0603	500X14W103MV4T	603	1
D1	Diode, Zener, 5.6 V, 500 mW, SOD-123	MMSZ5232B-7-F	SOD-123	1
D2	Diode, TVS, Bi, 24 V, 600 W, AEC-Q101, SMA	SM4T23CAY	SMA	1
D3	Diode, Zener, 5.6 V, 500 mW, SOD-123	MMSZ5232B-7-F	SOD-123	1
D4	Diode, Zener, 7.5 V, 1.5 W, AEC-Q101, SMA	1SMA5922BT3G	SMA	1
F1	Fuse, Resettable, 0.2 A, 24 V, SMD	NANOSMDC020F-2	SMD	1
J1	Header, 2.54 mm, 3x1, Gold, TH	61300311121	3x1,TH	1
J2	Header, 2.54 mm, 4x1, Gold, TH	61300411121	4x1,TH	1
L1	Ferrite Bead, 1000 ohm @ 100 MHz, 0.2 A, 0603	74279266	603	1
Q1	MOSFET, P-CH, -30 V, -3.8 A, AEC-Q101, SOT-23	DMP3098L-7	SOT-23	1
Q2	Transistor, PNP, 40 V, 1.5 A, AEC-Q101, SOT-23	FMMT720TA	SOT-23	1
Q3	Transistor, PNP, 45 V, 0.1 A, SOT-23	BC857C-7-F	SOT-23	1
R1	RES, 2.74 k, 1%, 0.063 W, 0402	CRCW04022K74FKED	402	1
R2	RES, 6.81 k, 1%, 0.063 W, 0402	CRCW04026K81FKED	402	1
R3	RES, 20.0 k, 1%, 0.1 W, 0603	CRCW060320K0FKEA	603	1
R4	RES, 6.81 k, 1%, 0.063 W, 0402	CRCW04026K81FKED	402	1
R5	RES, 511, 1%, 0.063 W, 0402	CRCW0402511RFKED	402	1
R6	RES, 511, 1%, 0.063 W, 0402	CRCW0402511RFKED	402	1
U1	Resistive Bridge Sensor Signal Conditioner for Automotive application, RHH0036C	PGA400RHHQ1	QFN-36	1

14.3 PCB Layout Recommendations

To download the layer plots, see the design files at TIDA-00793.

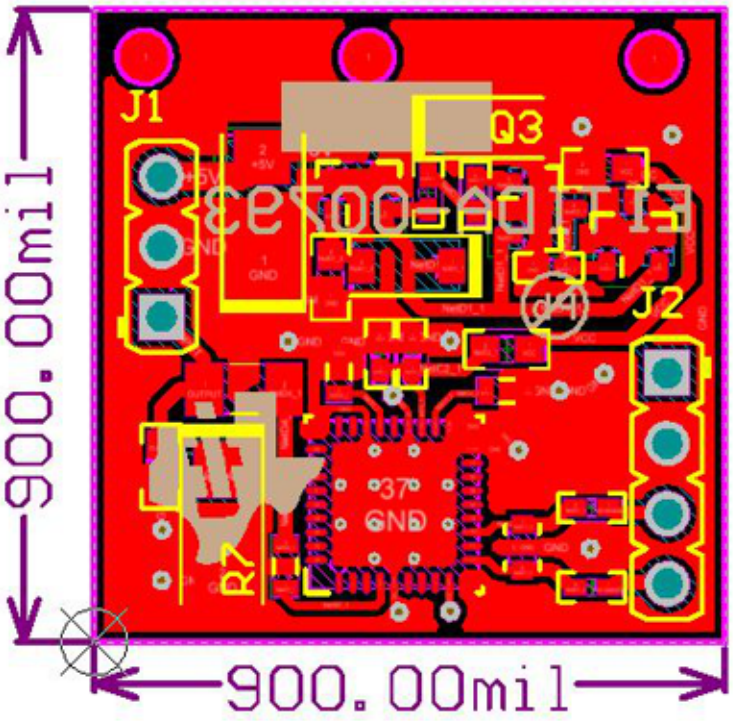

Figure 59. Input Symmetry and Ground Planes Representation

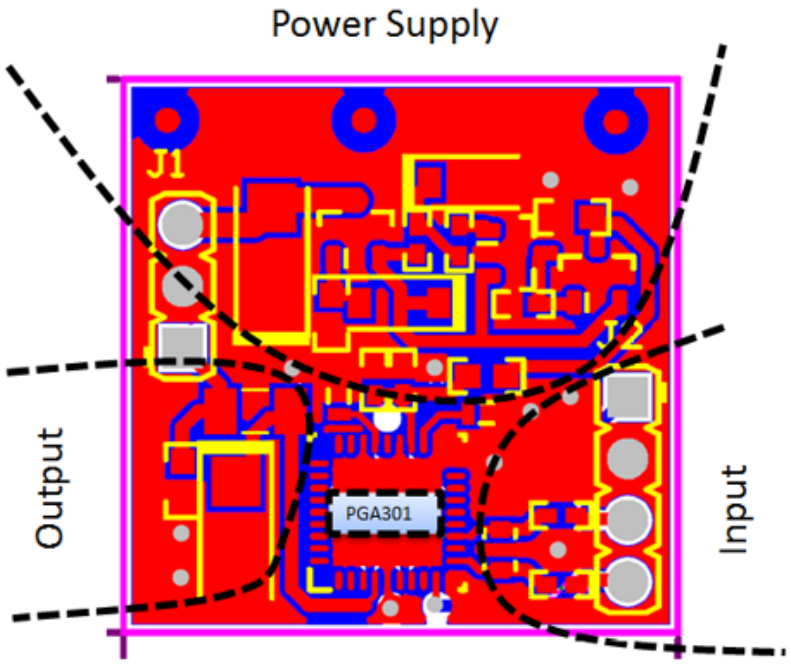

Figure 60. PCB Partitioning Power Supply, Input, and Output

- Place a solid ground "island" underneath the PGA400-Q1.
- Place sensor input circuitry (or filter structure) as close to the I/O connector as possible. Treat every trace carrying sensitive signals (PGA400-Q1 input circuitry) as a receiving antenna when considering its routing (consideration implies shortest paths).
- Maintain symmetry between two lines of a differential signal routing (Wheatstone's bridge outputs).
- Separate input, output, and power circuitry (as shown in Figure 60).
- Pour solid ground planes on both the top and bottom layers.
- Place the TVS diode as close as possible to the power connector.
- Place input capacitors as close to the IC as possible to reduce the parasitic series inductance.

14.4 Altium Project

To download the Altium project files, see the design files at TIDA-00793.

14.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00793.

14.6 Calibration Documents

To download the supportive documents for calibration, see the design files at TIDA-00793.

14.7 Software Files

To download the software files, see the design files at TIDA-00793.

- PGA400.exe
- TINA-SPICE simulation program

15 Related Documentation

1. Texas Instruments, *PRESSURE SENSOR SIGNAL CONDITIONER*, PGA400-Q1 Datasheet (SLDS186)
2. Texas Instruments, *Power Supply Requirements and Connections*, PGA400-Q1 EVM User Guide (SLDU010)
3. ISO 7637-3, *Road vehicles — Electrical disturbances from conduction and coupling — Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines* (http://www.iso.org/iso/iso_catalogue/catalogue_tc/catalogue_detail.htm?csnumber=59603)
4. CISPR 25, Edition 3.0 2008-03, *Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers* (https://webstore.iec.ch/publication/78)
5. Texas Instruments, *Bridge Measurements Systems*, Precision Analog Applications Seminar (SLYP163)
6. Texas Instruments, *Two-step calibration of sensor signal conditioners*, Analog Applications Journal: Automotive (SLYT625)

15.1 Trademarks

16 About the Author

SANDEEP TALLADA is a systems engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, Sandeep focuses on powertrain end-equipment and creating subsystem reference designs. He brings to this role experience in sensor systems technology. Sandeep earned his master of science in sensor systems technology from the University of Applied Sciences Karlsruhe, Germany.

Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (June 2016) to B Revision	Page
• Changed all instances of PGA301-Q1 to PGA400-Q1	1

Revision A History

Changes from Original (March 2016) to A Revision	Page
• Changed from D2	21
• Changed from Q2	21
• Changed from Q2	21
• Changed from D2	21
• Changed from Q1	21
• Changed from Q1	21
• Changed circuit path on Figure 28	21
• Added "VB" and GND" to Figure 30	23
• Added "(VB)" to Fault 16 in Table 3	23
• Added "(VIN1)" to Fault 18 in Table 3	23
• Added "(VIN2)" to Fault 19 in Table 3	23
• Added "(VB)" to Fault 20 in Table 3	23
• Added "(VB)" to Fault 20 in Table 3	23
• Added "(VIN1)" to Fault 21 in Table 3	23
• Added "(VB)" to Fault 22 in Table 3	23
• Added "(VIN1)" to Fault 22 in Table 3	23
• Added "(VIN1)" to Fault 23 in Table 3	23
• Added "(VIN2)" to Fault 23 in Table 3	23
• Added "(VIN1)" to Fault 24 in Table 3	23
• Added "(GND)" to Fault 24 in Table 3	23
• Changed cross reference from Section 1 to Section 9.1	27
• Deleted "source meter and precision programmable power supply or"	39
• Added "in bridge configuration"	39
• Changed "source meter" to "SMD resistors in bridge configuration"	39

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