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A Security Analysis of Interrupts in Embedded Enclaved Execution

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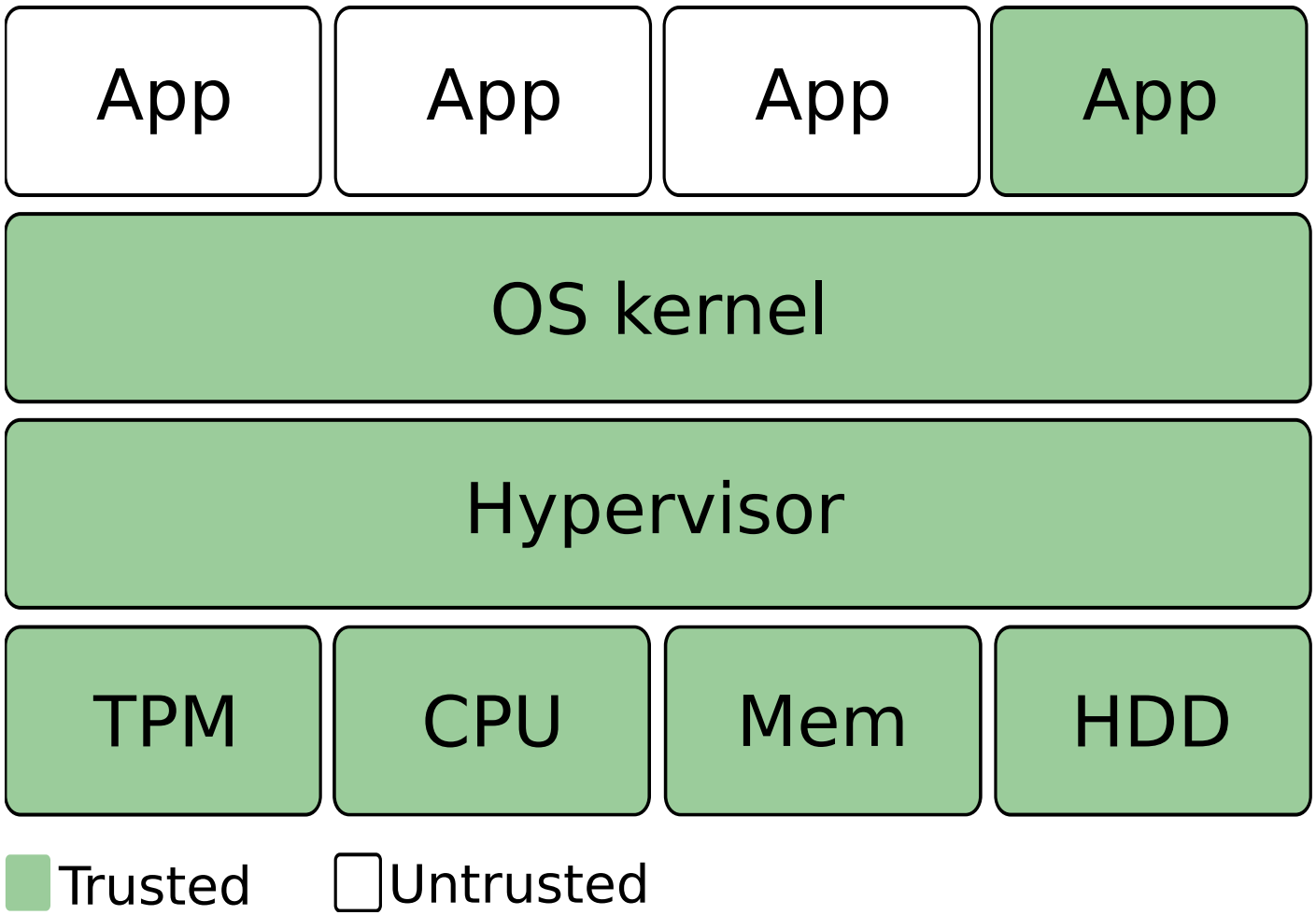
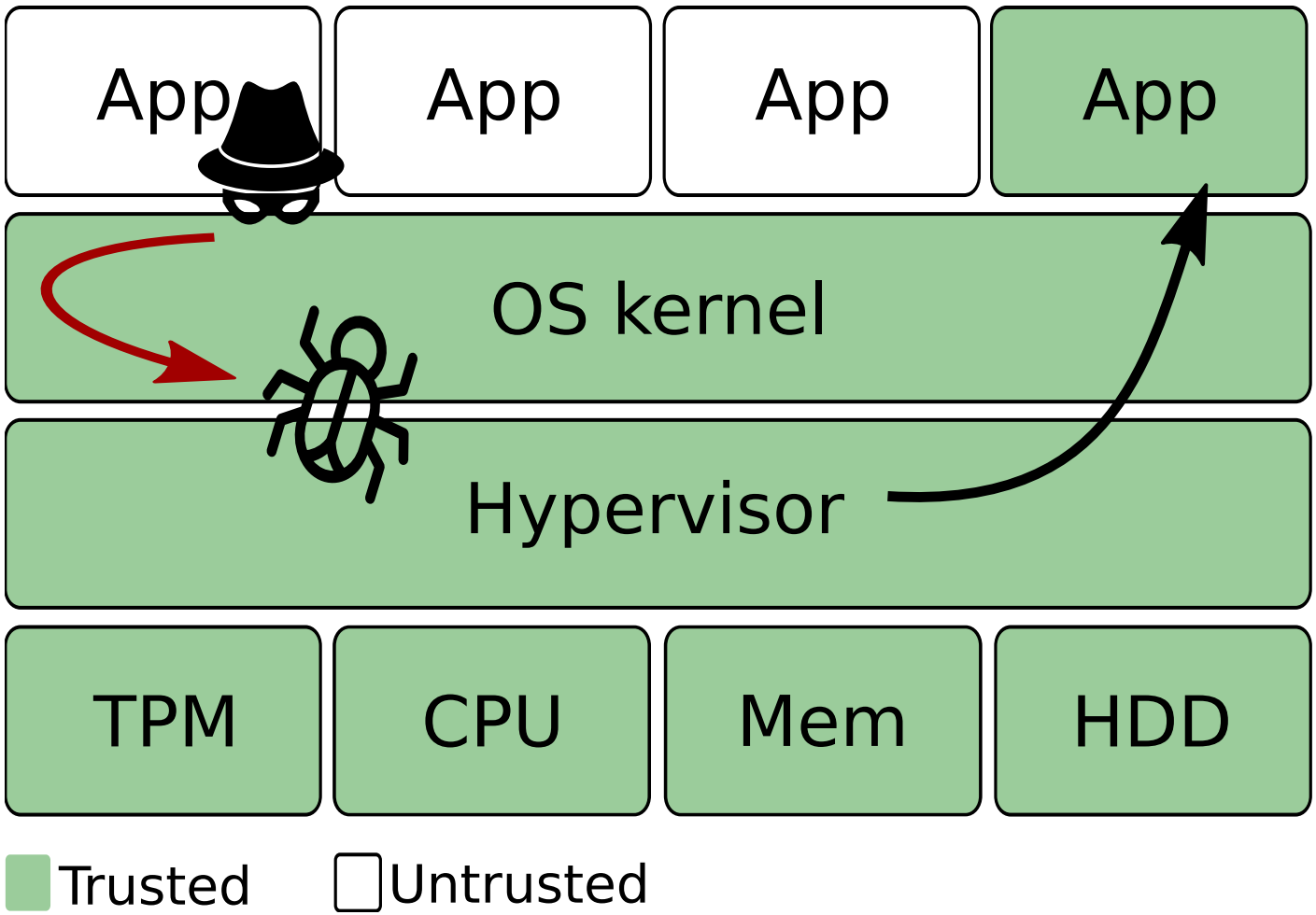
Conventional Software Isolation



based on: https://distrinet.cs.kuleuven.be/software/sancus/publications/ccs18-slides.pdf

TCB: Security Risk



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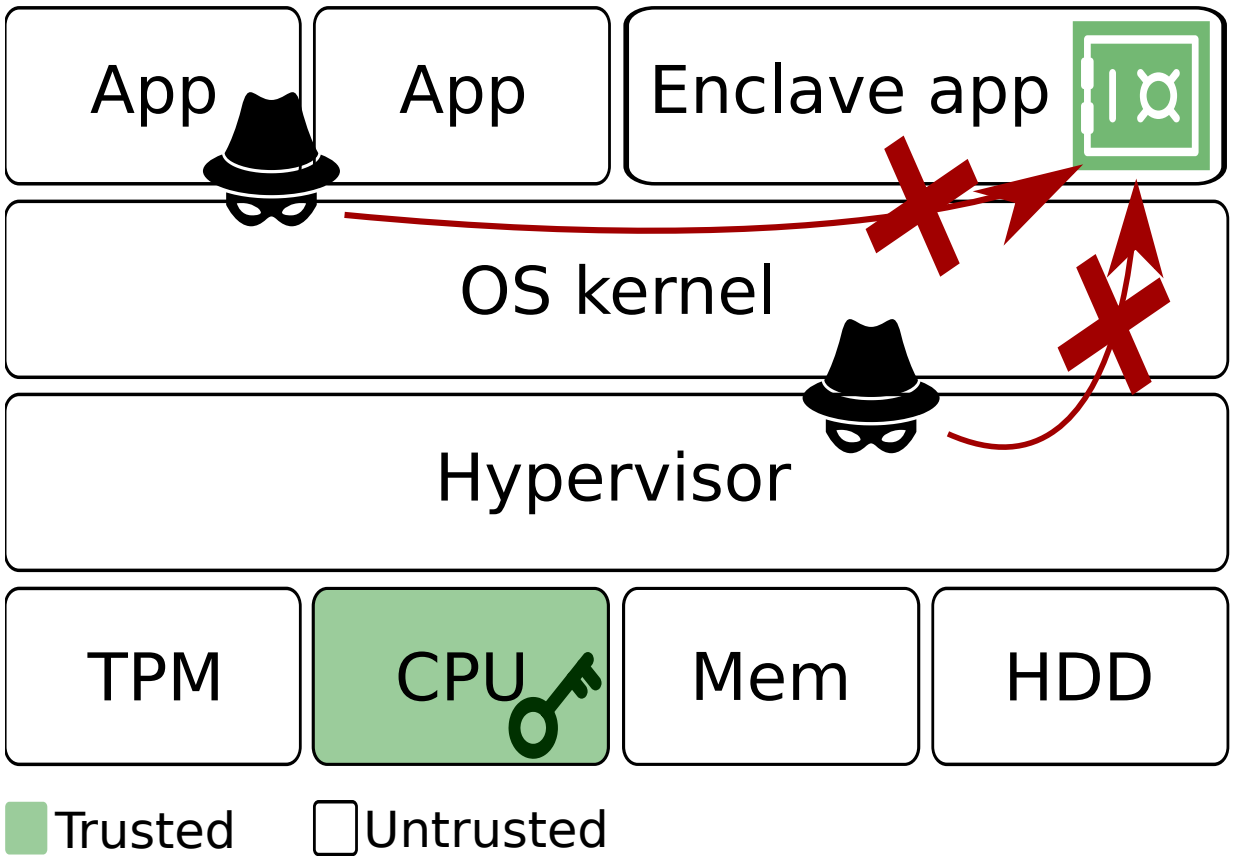
Enclaved Execution



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Key feature: **Isolation** and **Attestation**

Sancus

Sancus

- Embedded PMA

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- Hardware TCB only

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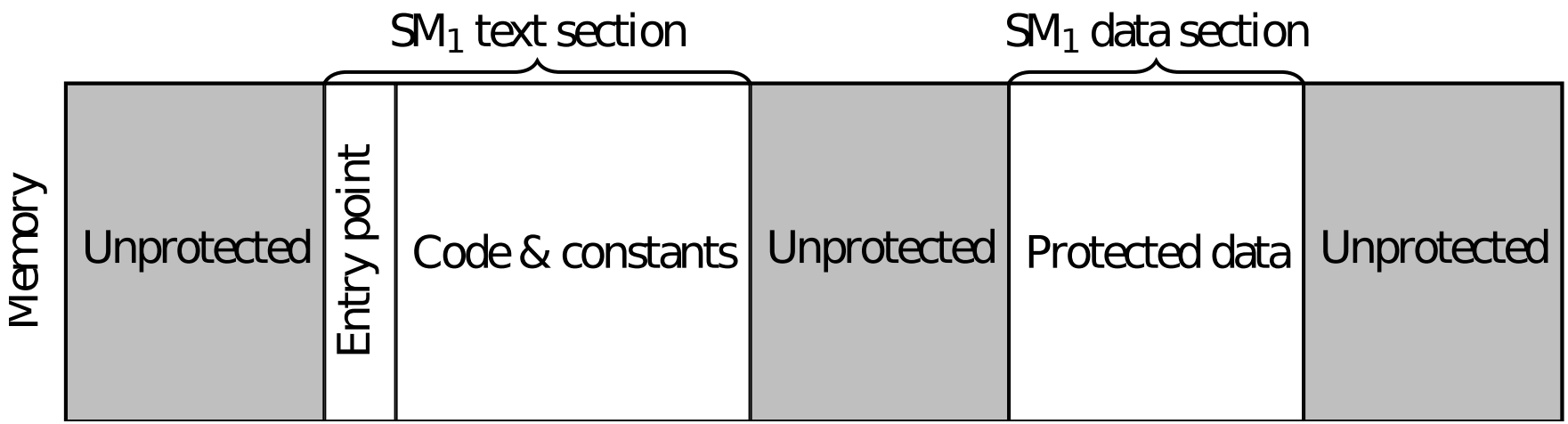
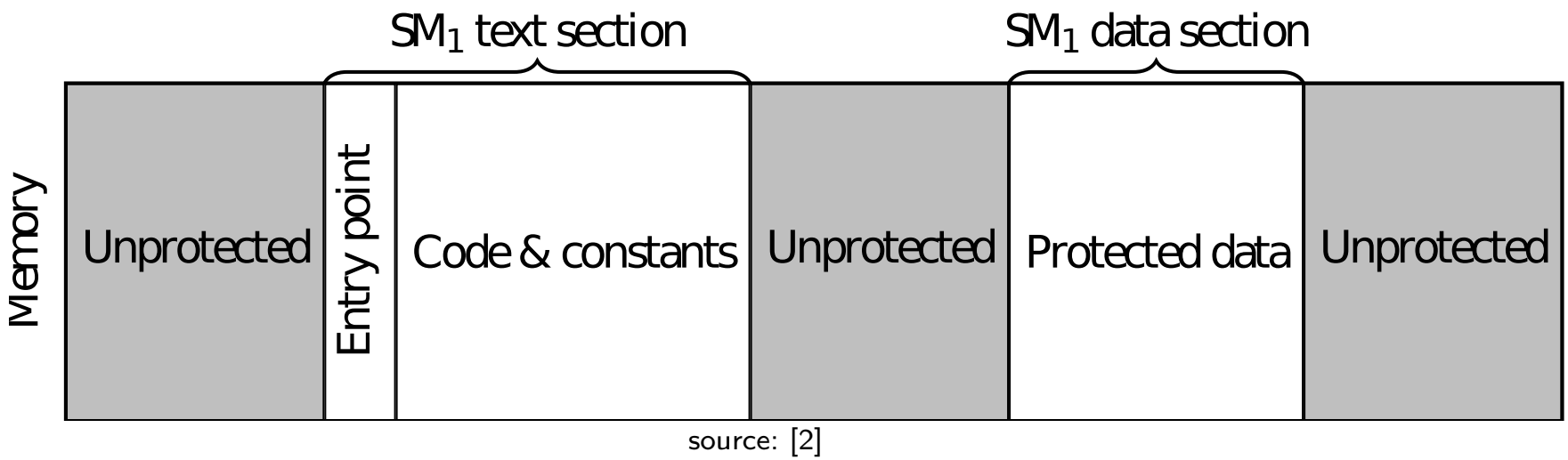
- Hardware TCB only
- Enclave layout



source: [2]

Sancus

- Embedded PMA
- Hardware TCB only
- Enclave layout



source: [2]

- Fully abstract compilation [1]

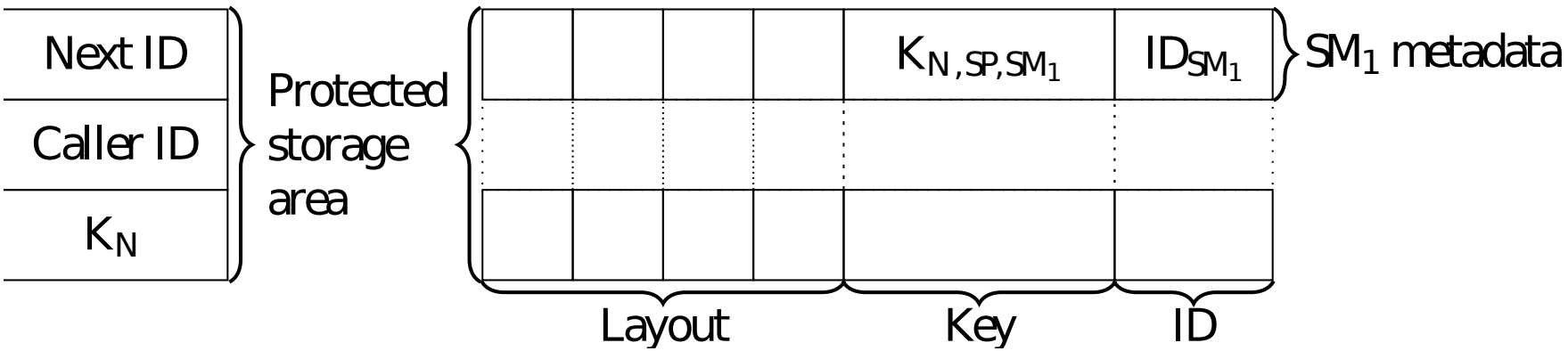
Sancus: Isolation

Program counter based access control policy

From\To	Entry	Text	Data	Unprotected
Entry	r-x	r-x	rw-	rwx
Text	r-x	r-x	rw-	rwx
Other	--x	---	---	rwx

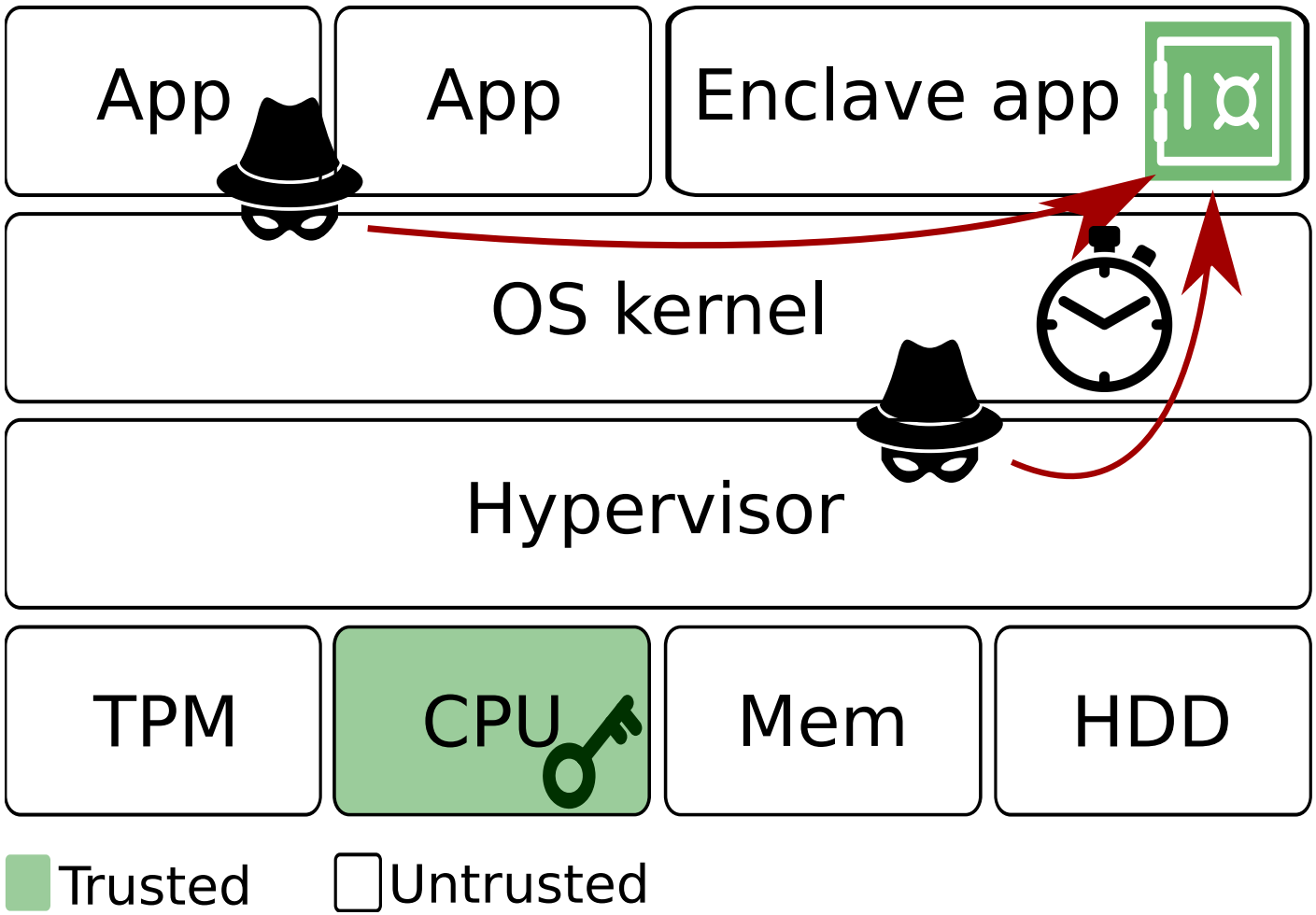
source: [2]

Sancus: Attestation



source: [2]

Side-Channel Attacks



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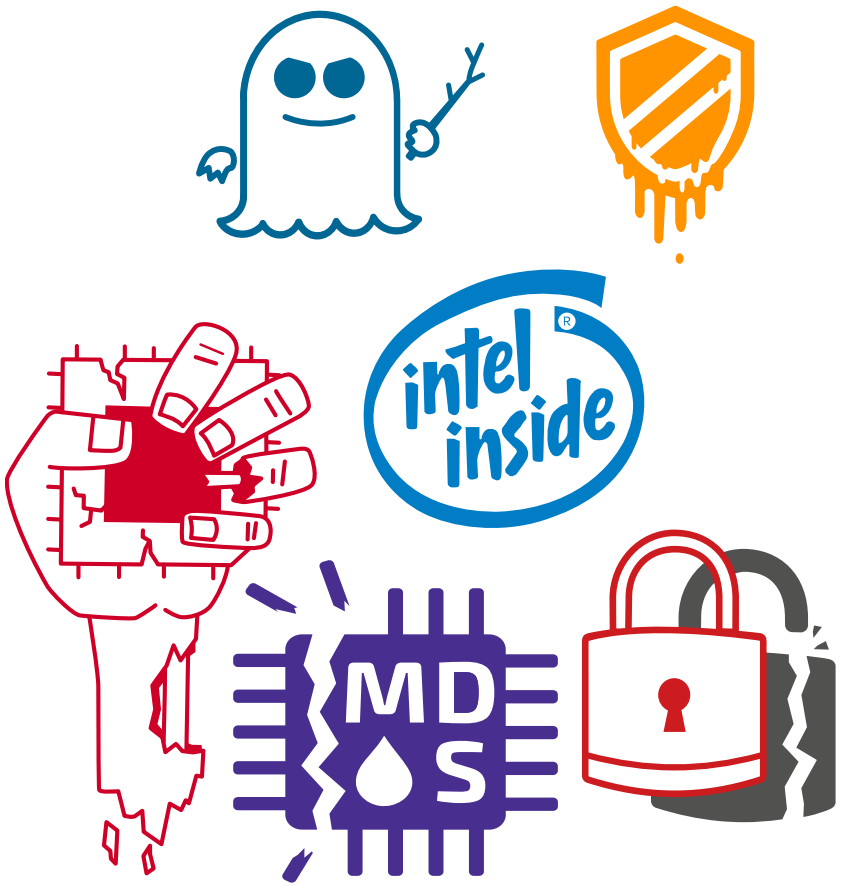
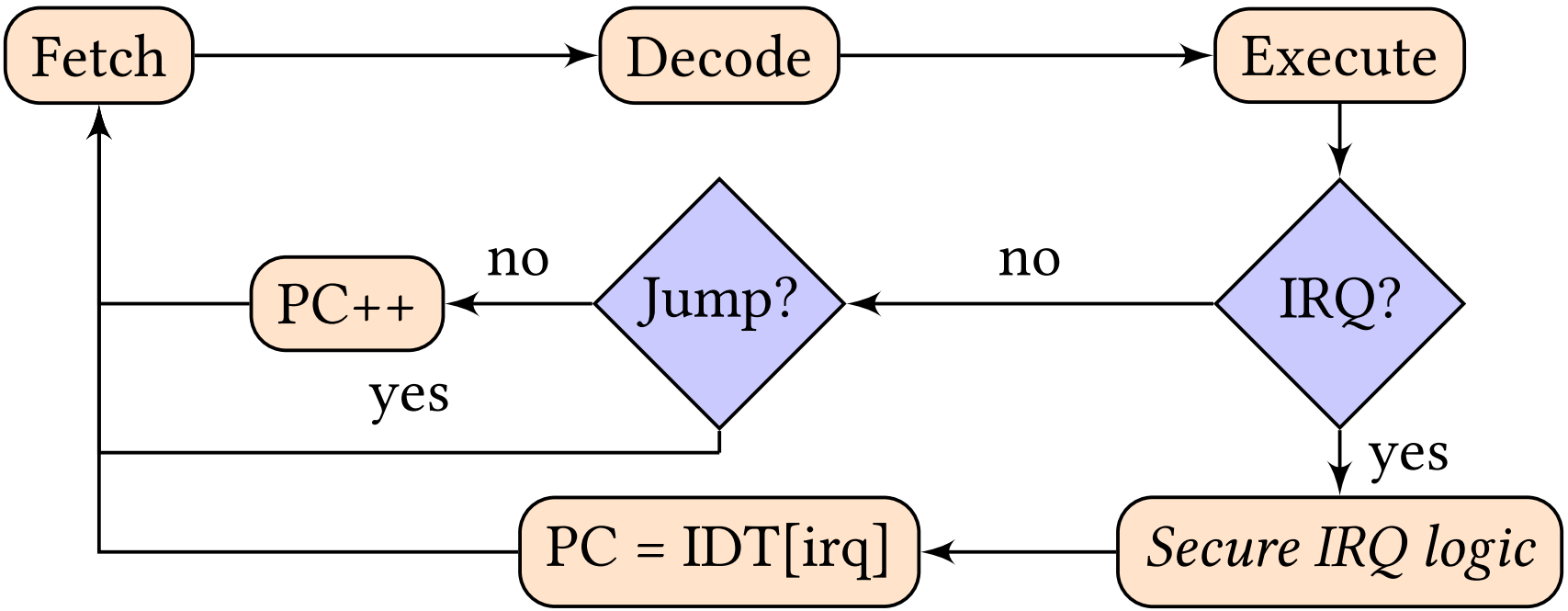
Side-Channels inside Intel



Abusing microarchitectural optimizations

$\rightarrow$ Not present in embedded

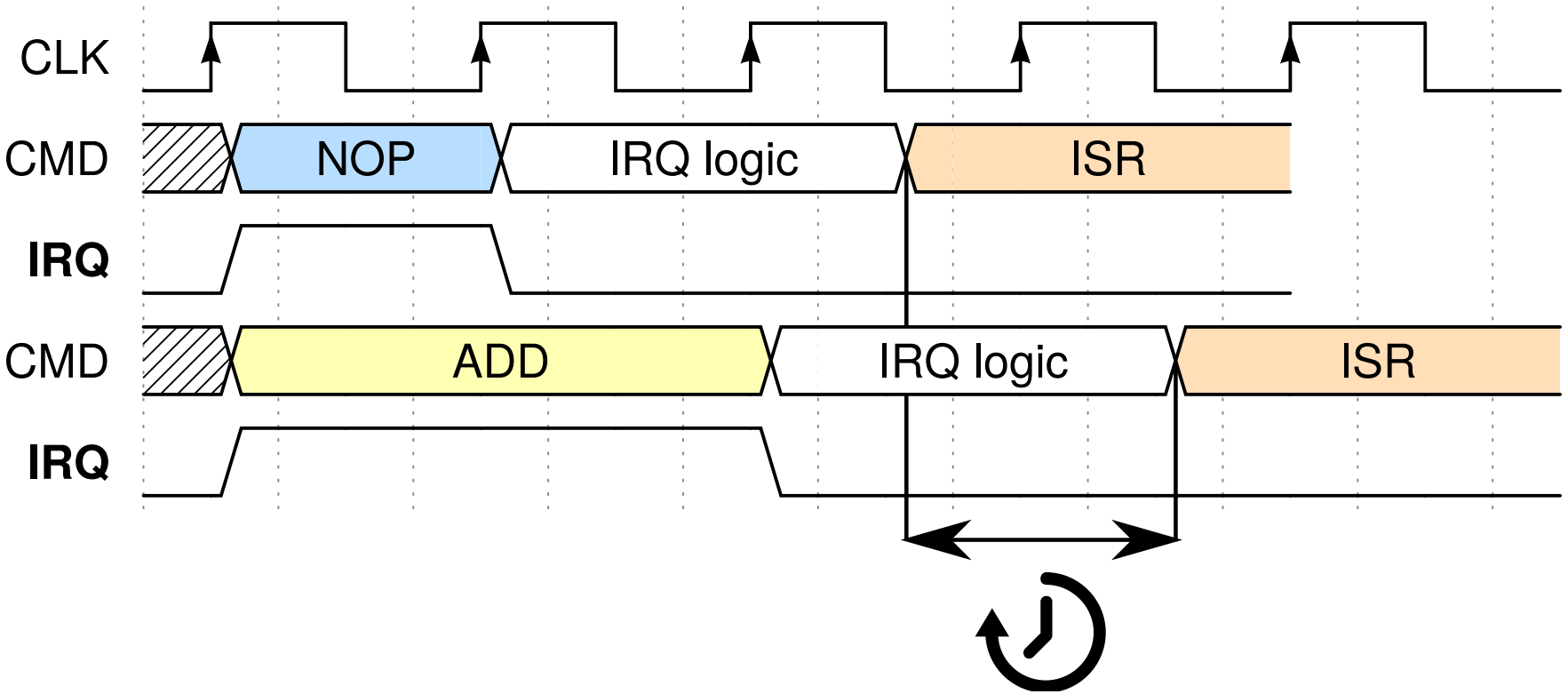
Nemesis [5]: Fetch-Decode-Execute Cycle



source: [5]

Interrupts only served on instruction retirement

Nemesis [5]: Interrupt Latency



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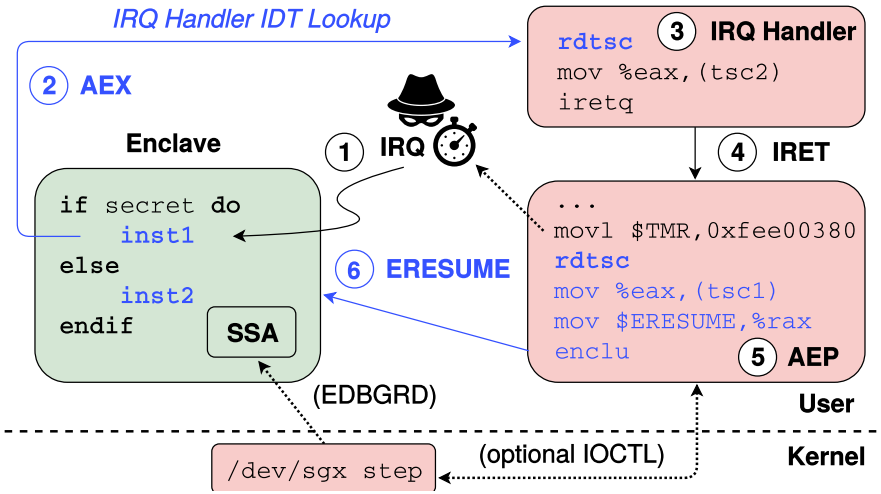
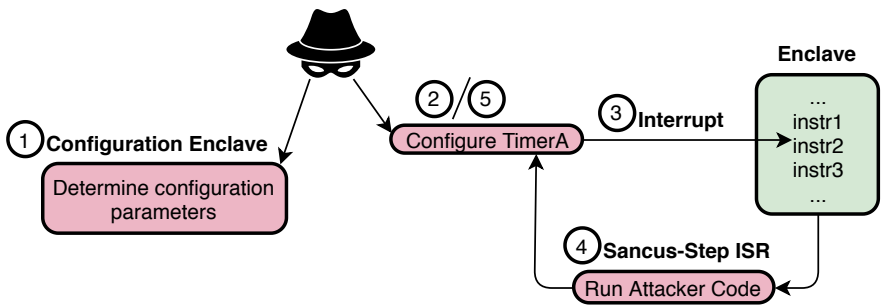
Attacker Frameworks

SGX-Step: Increase granularity and ease of use



source: [5]

Sancus-Step: Ease of use



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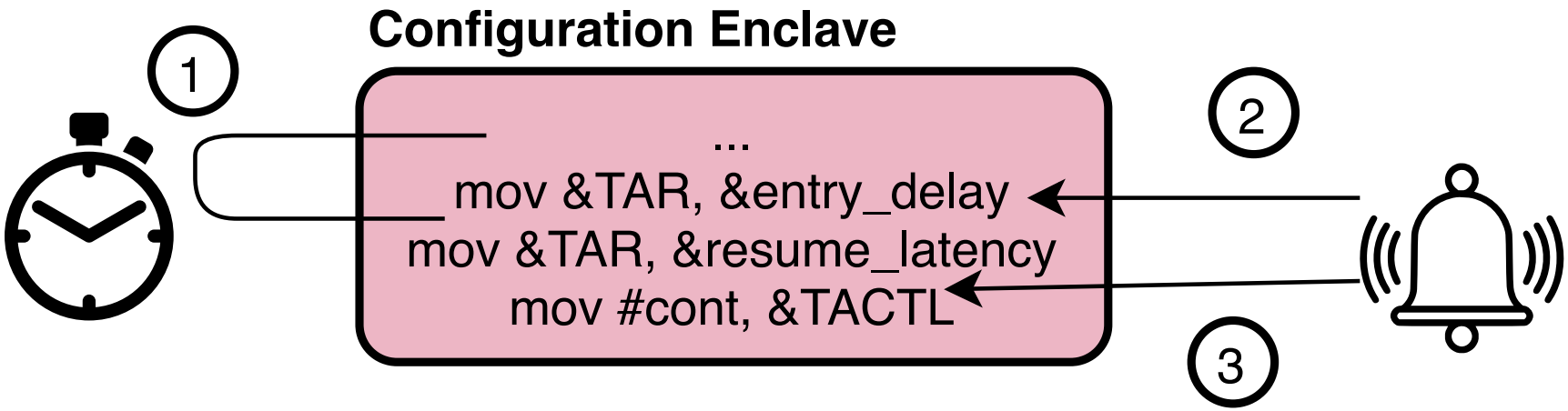
Sancus-Step Configuration



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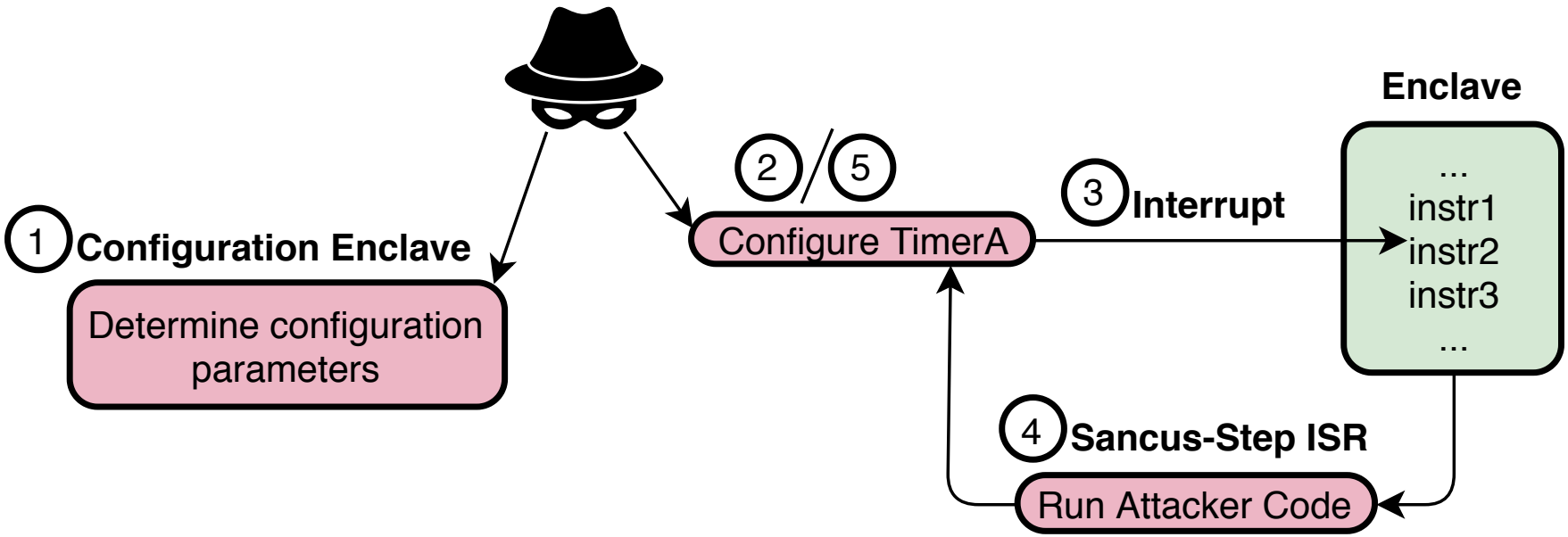
Sancus-Step Overview



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Verification TOCTOU

- Making enclaves interruptible $\rightarrow$ well known issues [2, 3, 4]

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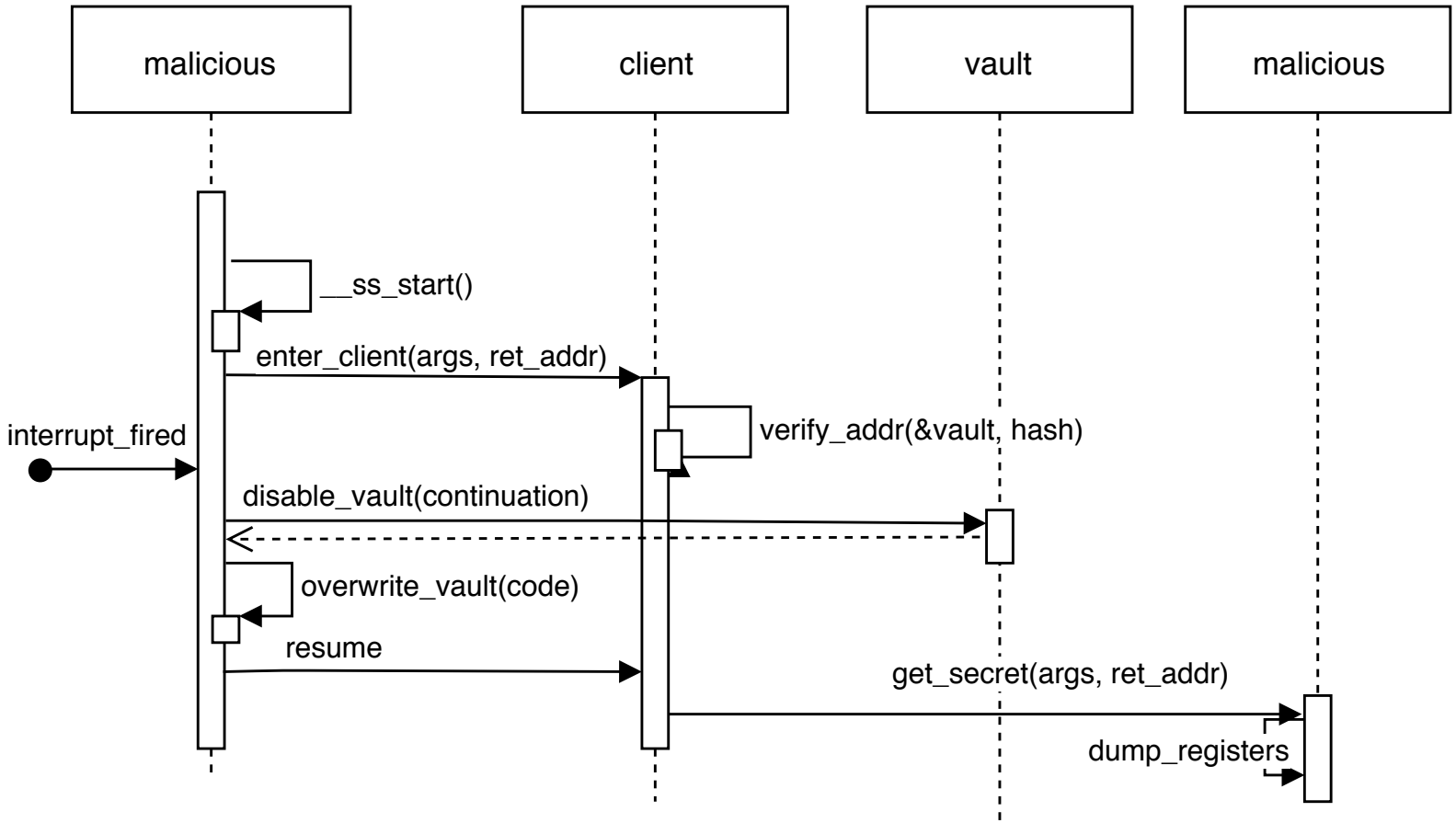

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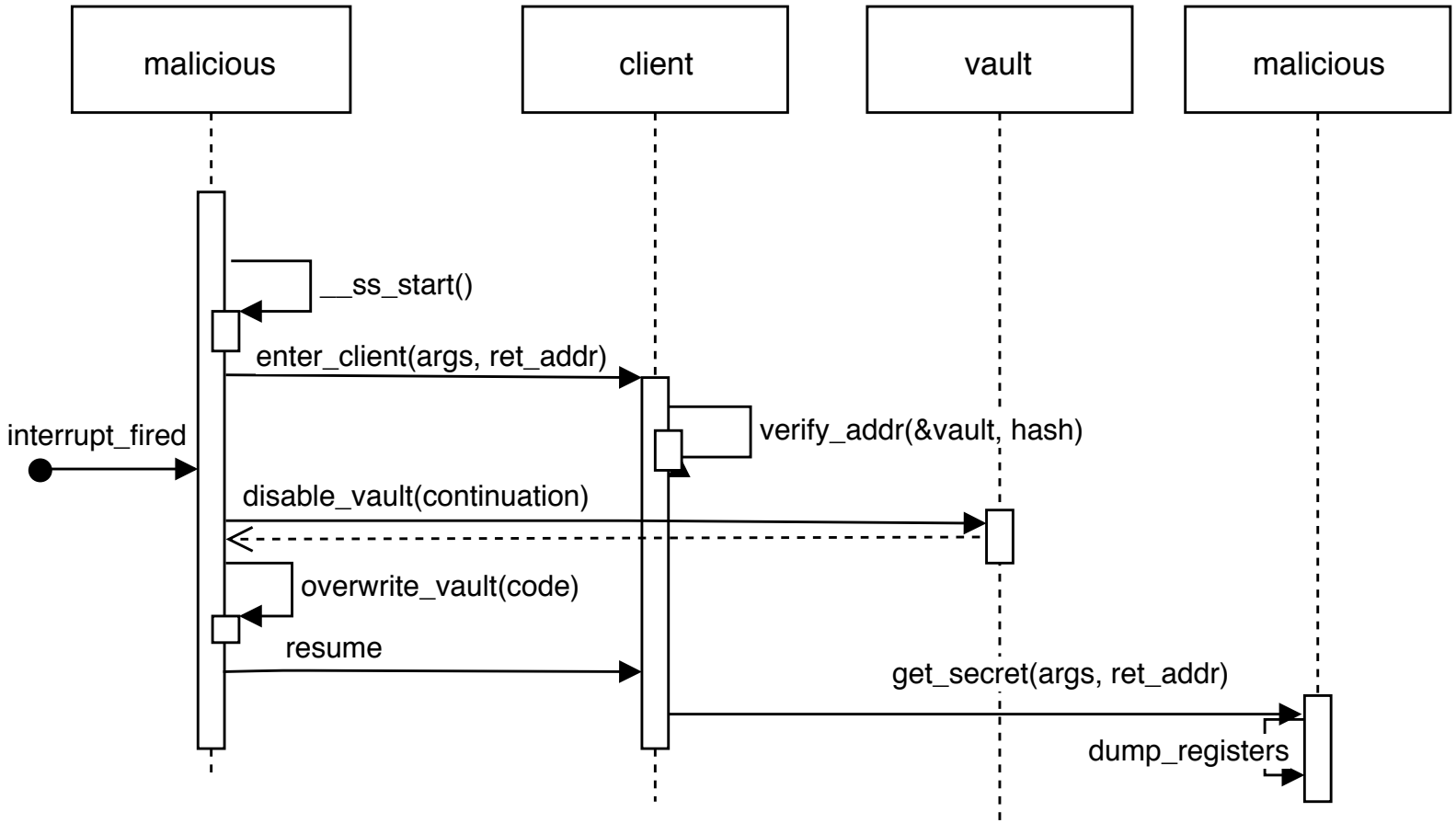

- Our ad-hoc implementation reveals vulnerabilities

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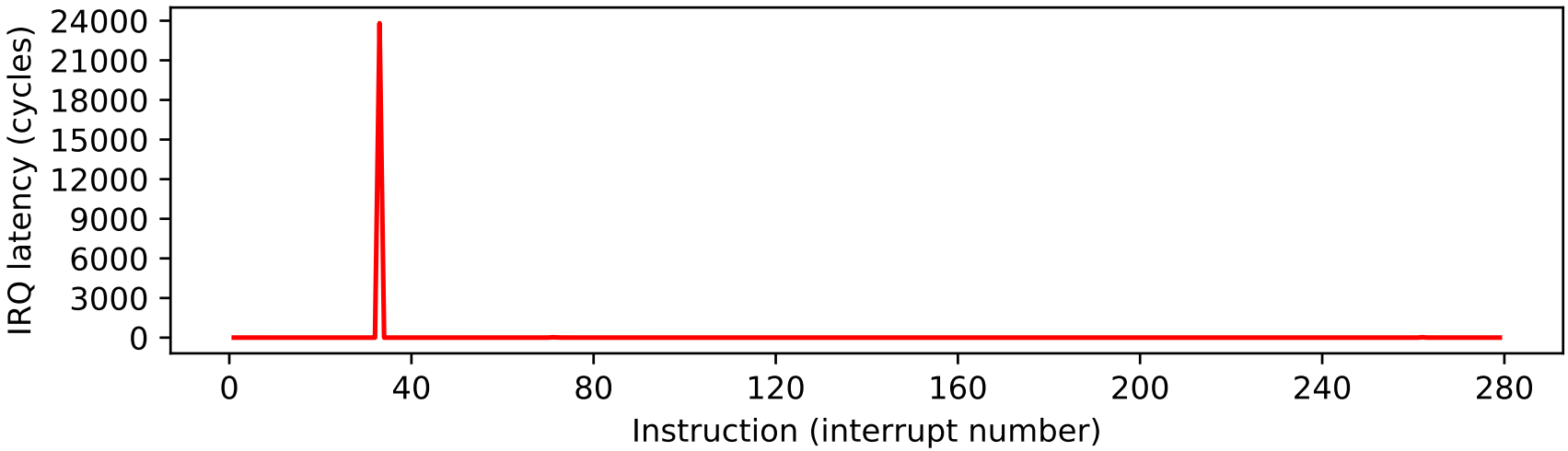
Verifcation TOCTOU: Automatic Exploit



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Side-Channel Analysis in Compiler Generated Code

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- Stubs:
  - Multiplication stub
  - Other arithmetic stubs
  - Entry and Exit stub

Side-Channel Analysis in Compiler Generated Code

- Stubs:
  - Multiplication stub
  - Other arithmetic stubs
  - Entry and Exit stub
- Both start-to-end and Nemesis

Reversing the Multiplication Stub

```
__sm_mulhi3:
    mov     r15, r13
    clr     r15
1:  tst     r14
    jz      3f
    clrc
    rrc     r13
    jnc     2f
    add     r14, r15
2:  rla     r14
    tst     r13
    jnz     1b
3:  ret
```

```
unsigned int mul(unsigned  int a,
                 unsigned int b)
{
    unsigned int rv = 0;
    while (a!=0)
    {
        if (b & 1)
            rv += a;
        b >>= 1;
        a <<= 1;
        if (b == 0)
            break;
    }
    return rv;
}
```

Intuition of the Multiplication Stub

```
unsigned int mul(unsigned  int a,
                 unsigned int b)
{
    unsigned int rv = 0;
    while (a!=0)
    {
        if (b & 1)
            rv += a;
        b >>= 1;
        a <<= 1;
        if (b == 0)
            break;
    }
    return rv;
}
```

```
   10(a)
x 101(b)
------
   10
  00
+10
------
 1010
```

Case Study: SM_mul

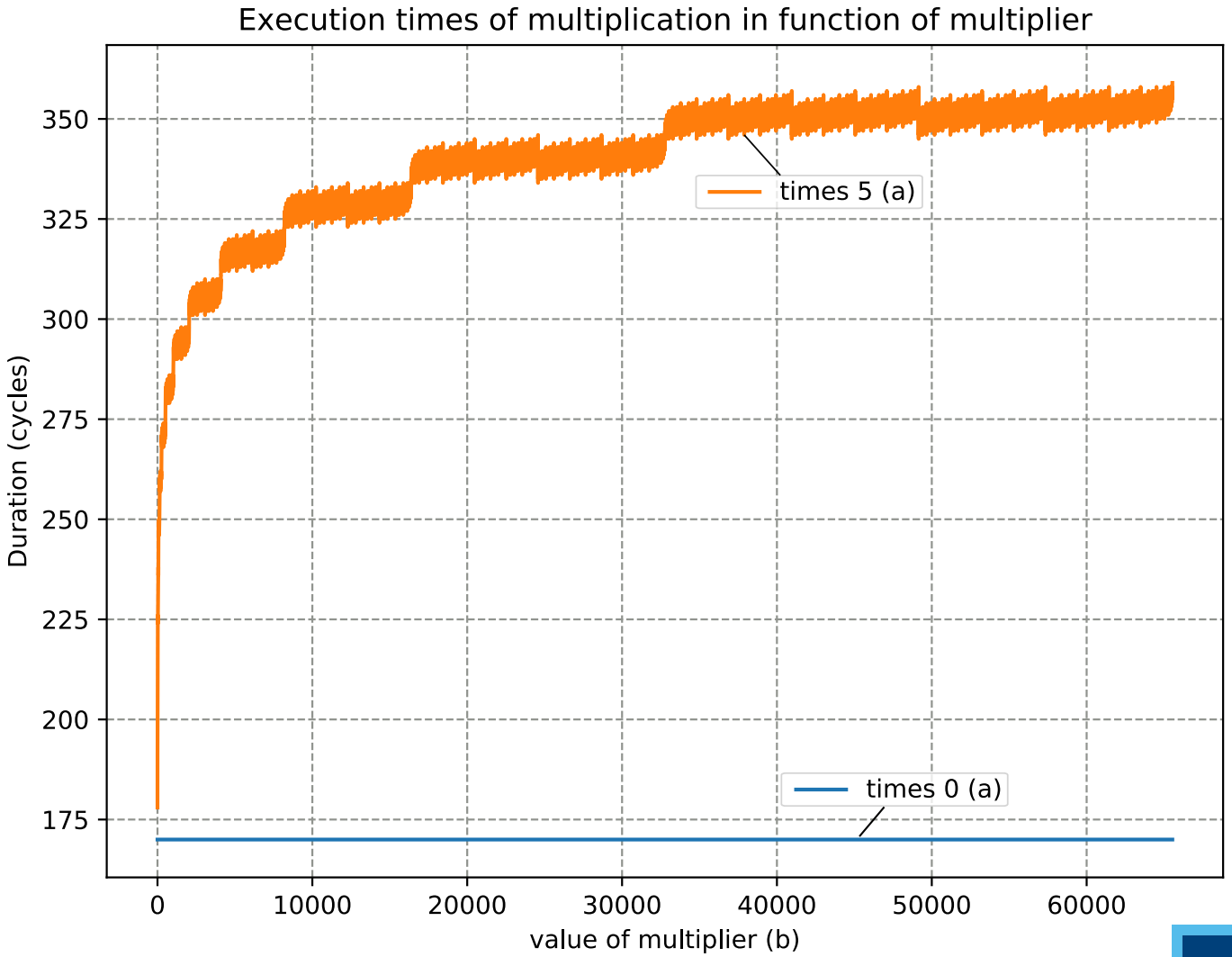
```
#include <sancus/sm_support.h>

DECLARE_SM(SM_mul, 0x1234);

int SM_DATA(SM_mul) a = -63;
int SM_DATA(SM_mul) b = 6;

int SM_ENTRY(SM_mul) sm_multiply(void)
{
    volatile int c = a * b;
    return 0;
}
```

Start-to-End Side-Channel in Multiplication



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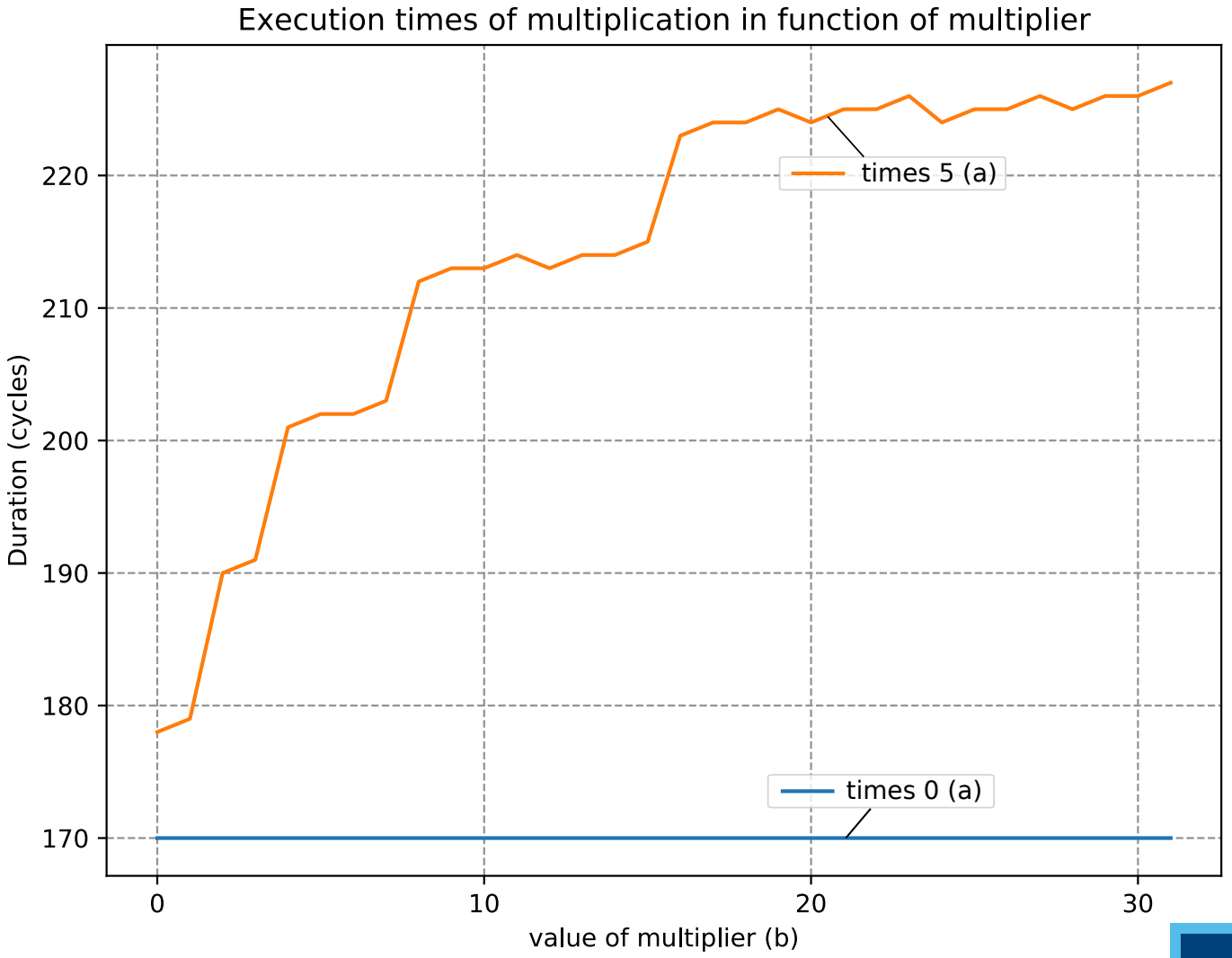
Start-to-End Side-Channel in Multiplication



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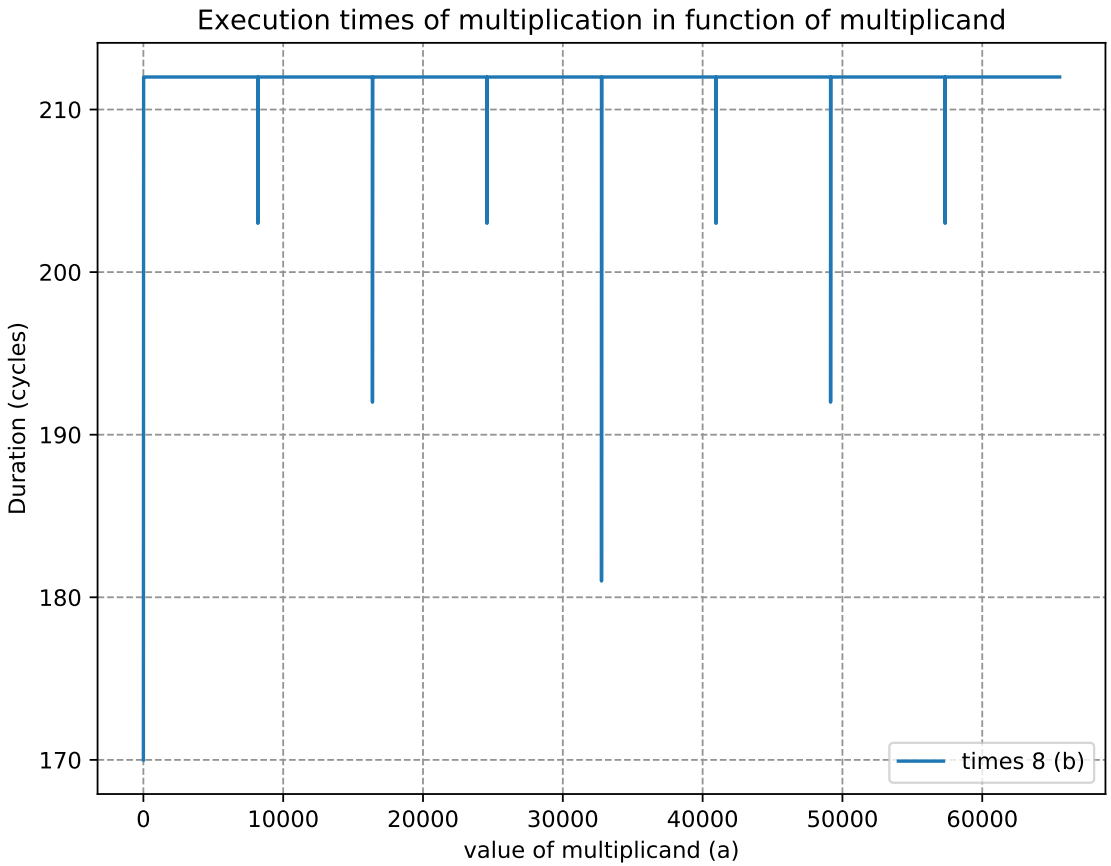
Start-to-End Side-Channel in Multiplication

a\b	...	14	15	...
...	...	...	...	...
120	...	213	214	...
121	...	213	214	...
...	...	...	...	...



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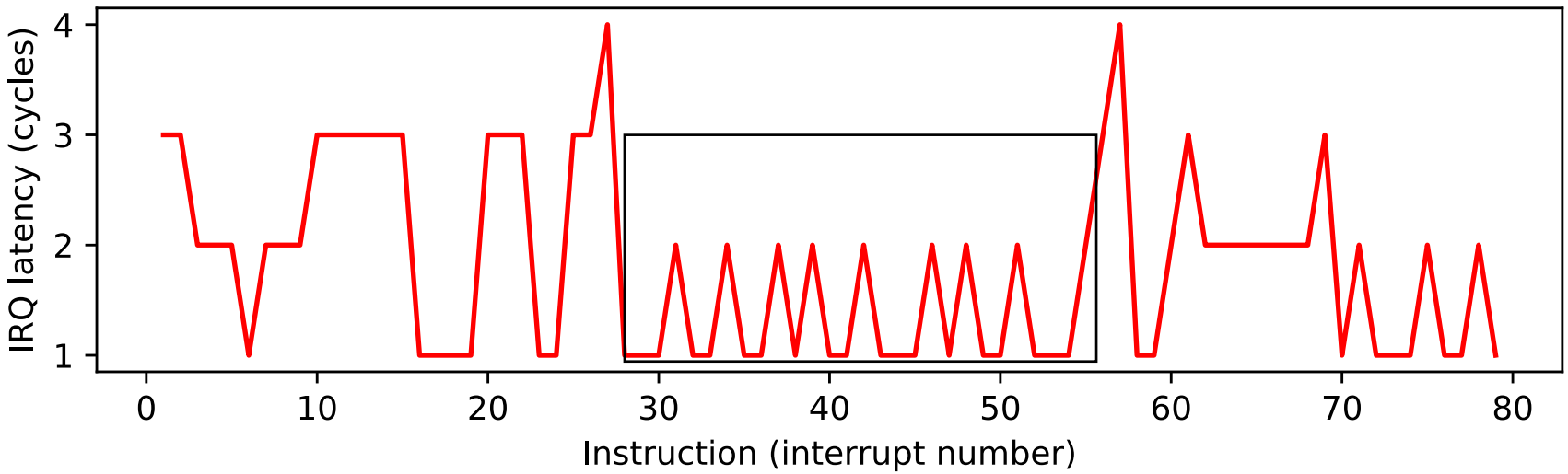
Nemesis Side-Channel in Multiplication



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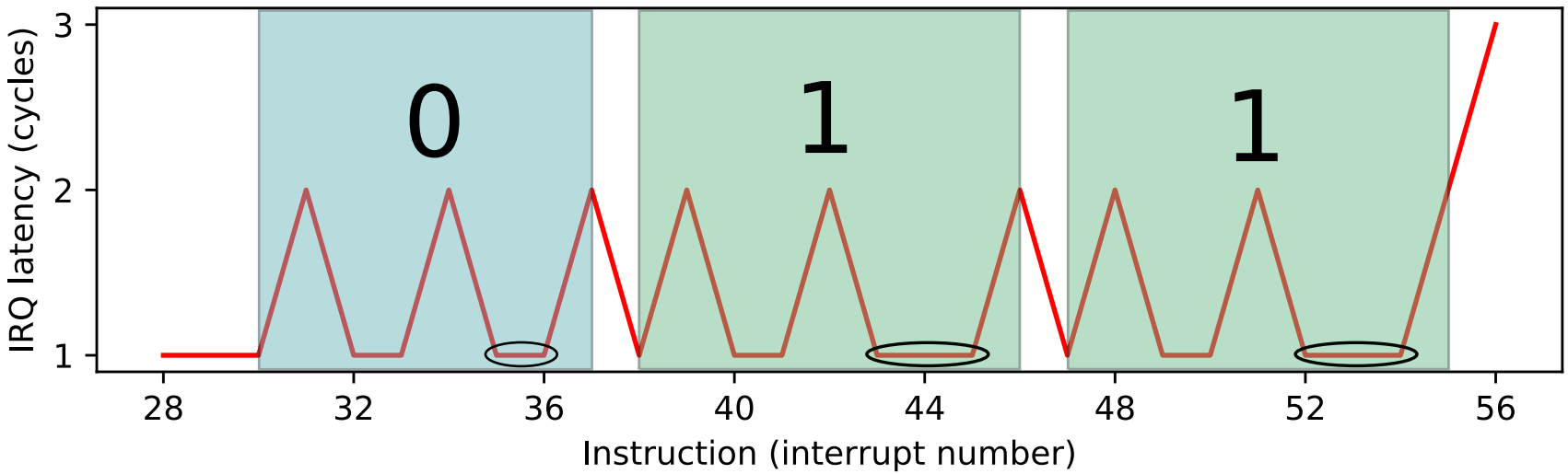
Leaking the Multiplier



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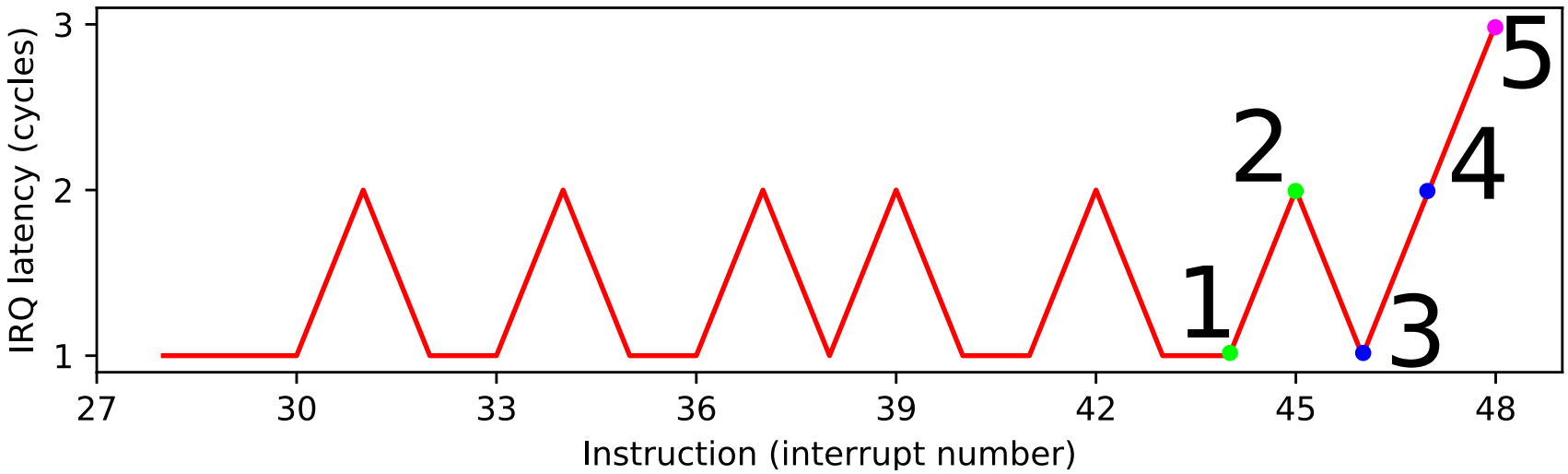
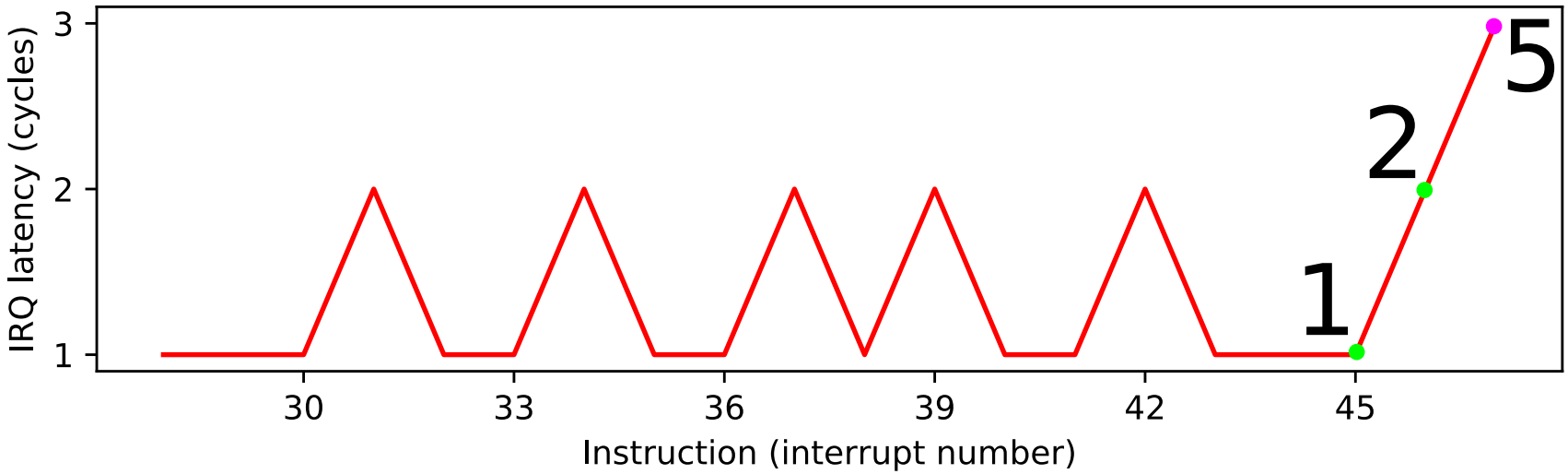
Determining the Stop Condition





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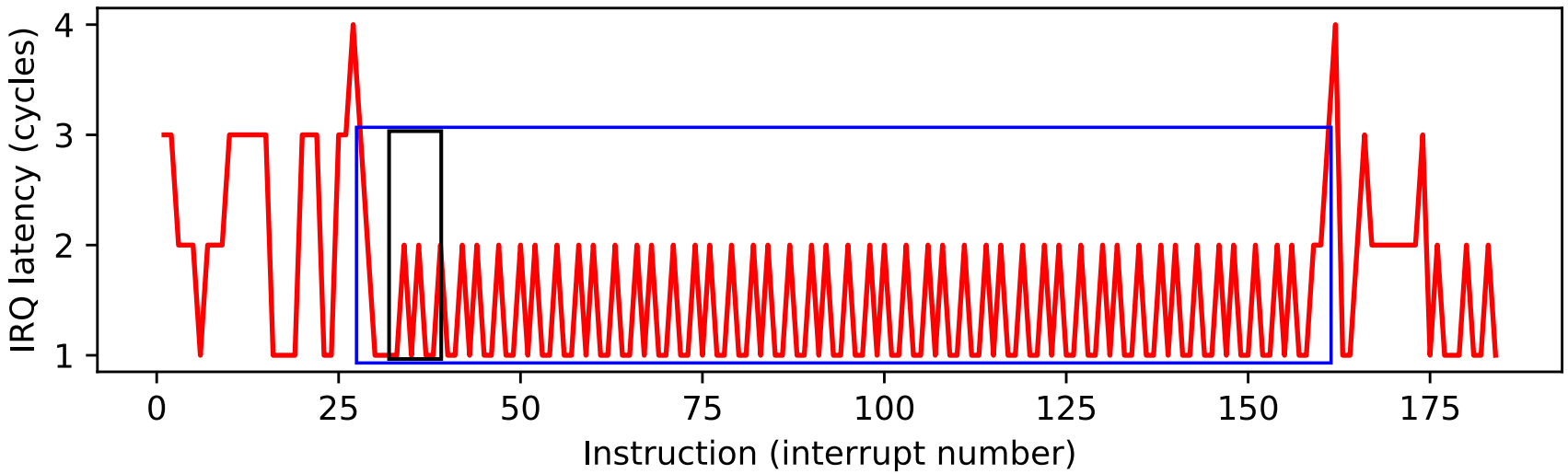
Hardening the Multiplication Stub

```
__sm_mulhi3:
    mov     #16, r12
    mov     r15, r13
    clr     r15
1:  clrc
    rrc     r13
    jnc     2f
    add     r14, r15
    jmp     4f
2:  nop
    jmp     4f
4:  rla     r14
    sub     #1, r12
    jnz     1b
3:  ret
```

```
unsigned int mul(unsigned  int a,
                 unsigned int b)
{
    unsigned int rv = 0;
    for (int i = 0; i < 16; i++)
    {
        if (b & 1)
            rv += a;
        else
            asm("nop");
        b >>= 1;
        a <<= 1;
    }
    return rv;
}
```

Closing Nemesis



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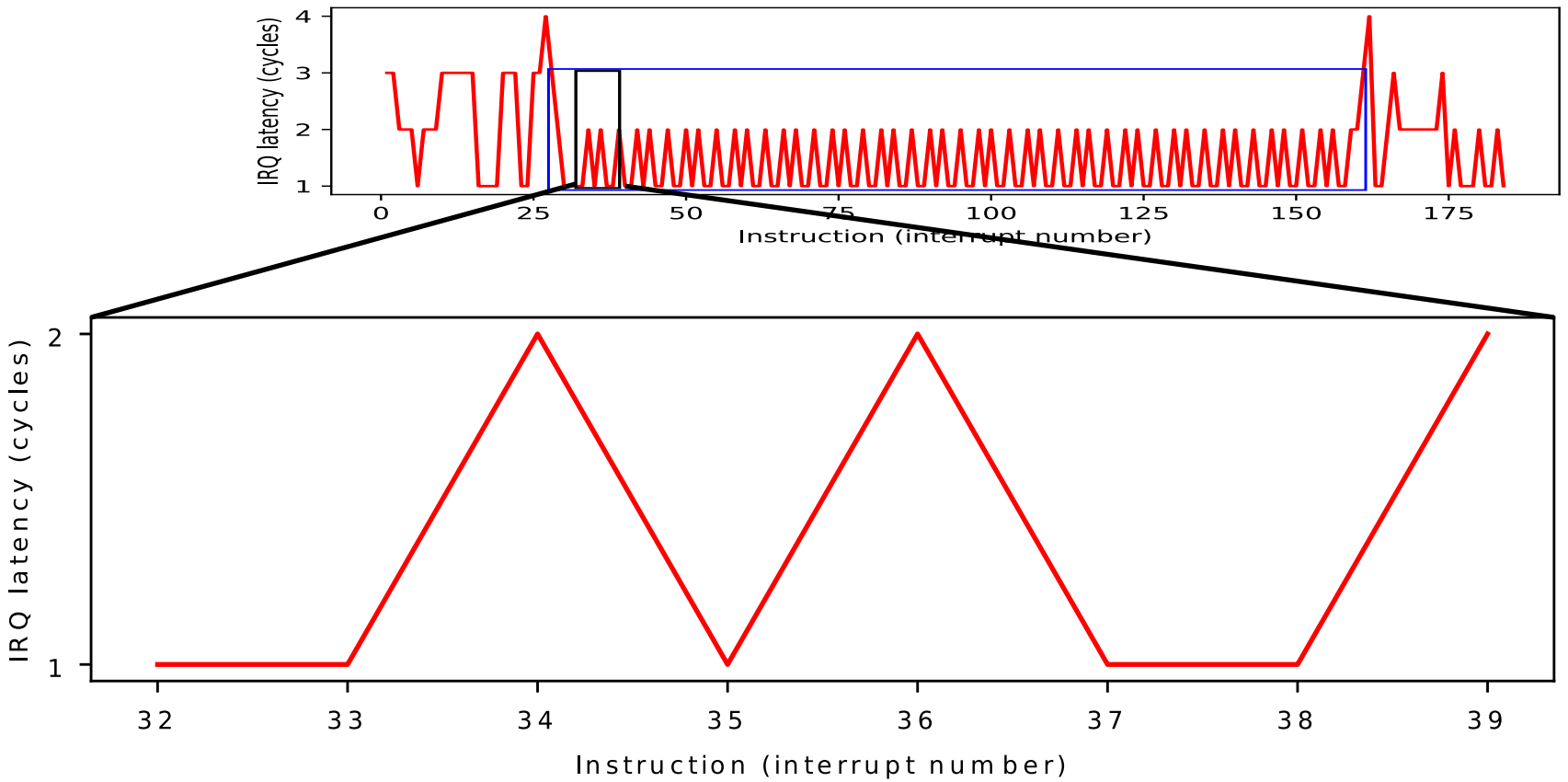
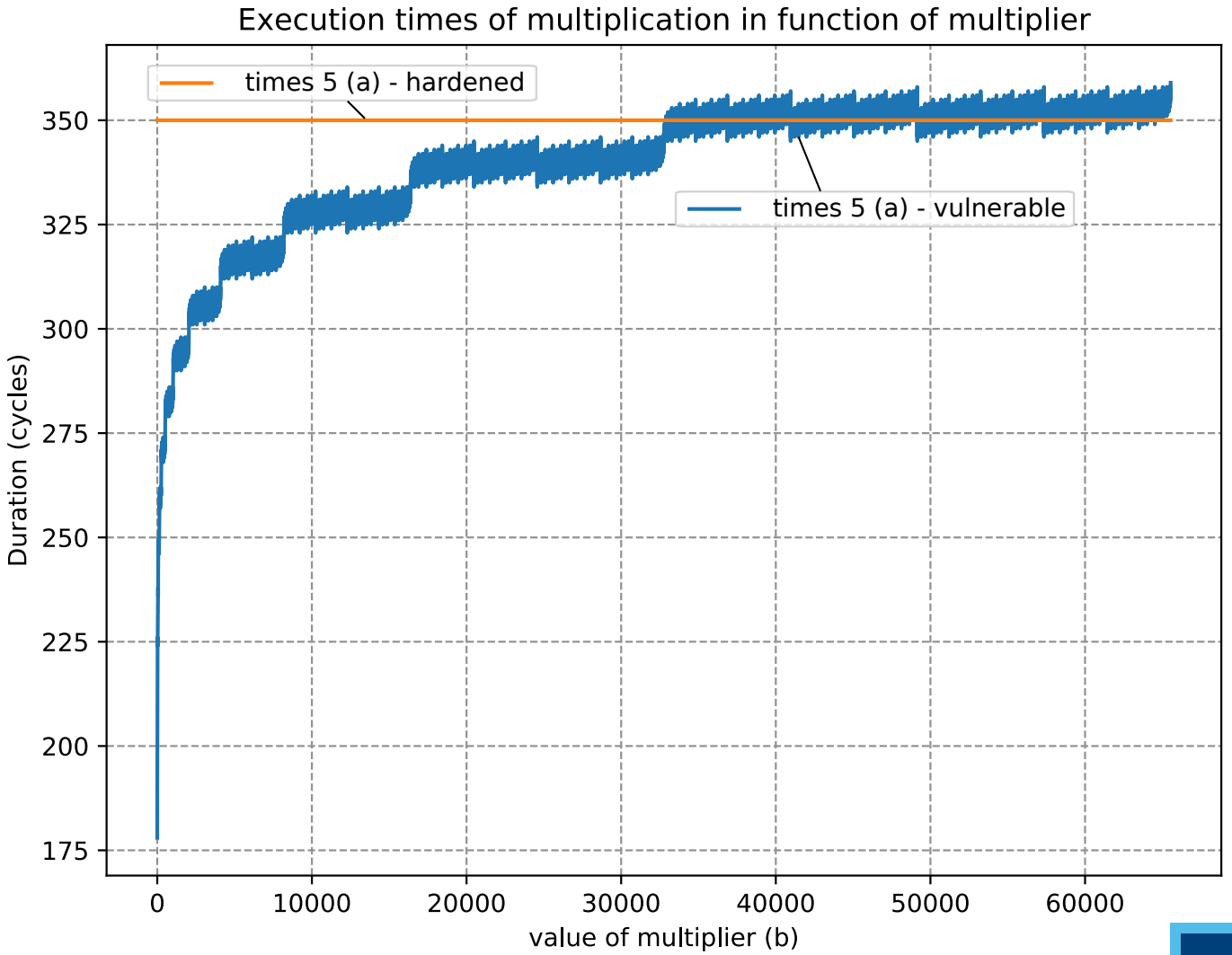
Closing Nemesis



Performance Comparison



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Future and Ongoing Work

- Analyse other stubs
  - Side-channel leakage
  - Atomicity issues
- Defense
  - Shortterm $\rightarrow$ software
  - Longterm $\rightarrow$ hardware (ongoing work [6])

Thank you!
Questions?

References I

Pieter Agten et al. "Secure Compilation to Modern Processors". In: *2012 IEEE 25th Computer Security Foundations Symposium*. IEEE, June 2012. DOI: 10.1109/csf.2012.12. URL: https://doi.org/10.1109/csf.2012.12.

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References II

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Raoul Strackx, Frank Piessens, and Bart Preneel. "Efficient Isolation of Trusted Subsystems in Embedded Systems". In: vol. 50. Sept. 2010, pp. 344–361. DOI: 10.1007/978-3-642-16161-2_20.

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References III

Jo Van Bulck, Frank Piessens, and Raoul Strackx. "Nemesis: Studying Microarchitectural Timing Leaks in Rudimentary CPU Interrupt Logic". In: *Proceedings of the 2018 ACM SIGSAC Conference on Computer and Communications Security*. CCS '18. Toronto, Canada: ACM, 2018, pp. 178–195. ISBN: 978-1-4503-5693-0. DOI: 10.1145/3243734.3243822. URL: http://doi.acm.org/10.1145/3243734.3243822.

Jo Van Bulck et al. "Towards Availability and Real-Time Guarantees for Protected Module Architectures". In: *Companion Proceedings of the 15th International Conference on Modularity (MASS'16)*. ACM, 2016, pp. 146–151.